Bus Arbitration

- Bus Arbitration refers to the process by which the current bus master accesses and then leaves the control of the bus and passes it to the another bus requesting processor unit. The controller that has access to a bus at an instance is known as **Bus master**.
- A conflict may arise if the number of DMA controllers or other controllers or processors try to access the common bus at the same time, but access can be given to only one of those.
- Only one processor or controller can be Bus master at the same point of time. To resolve these conflicts, **Bus Arbitration** procedure is implemented to coordinate the activities of all devices requesting memory transfers.
- Bus arbitration is the process by which the next device to become the bus master is selected and bus mastership is transferred to it.
- ☐ The selection of bus master must be based on fairness or priority basis.

☐ There are two approaches to bus arbitration: Centralized and distributed.

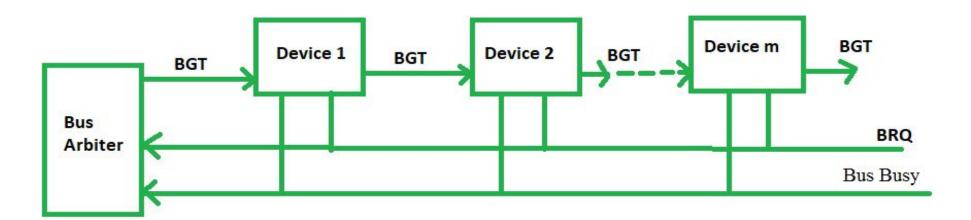
1. Centralized Arbitration

- In centralized bus arbitration, a single bus arbiter performs the required arbitration. The bus arbiter may be the processor or a separate controller connected to the bus.
- 2. Distributed bus arbitration All devices participate in the selection of the next bus master.
- Methods of Centralized BUS Arbitration There are three bus arbitration methods:

I. Daisy Chaining method

- It is simple and cheaper method. All masters make use of the same line for bus request.
- In response to the bus request the controller sends a bus grant if the bus is free.
- Bus Busy— this signal is to and from a bus master to enables all other units with the bus to note that presently bus access is not possible as one of the units is busy using the bus or has been granted control over the bus.
- The bus grant signal serially propagates through each master until it encounters the first one that is requesting access to the bus. This master blocks the propagation of the bus grant signal, activities the busy line and gains control of the bus.

- ☐ Therefore any other requesting module will not receive the grant signal and hence cannot get the bus access.
- ☐ During any bus cycle, the bus master may be any device the processor or any DMA controller unit, connected to the bus.



Daisy chained bus arbitration

■ Advantage

- Simplicity and Scalability.
- The user can add more devices anywhere along the chain, up to a certain maximum value.

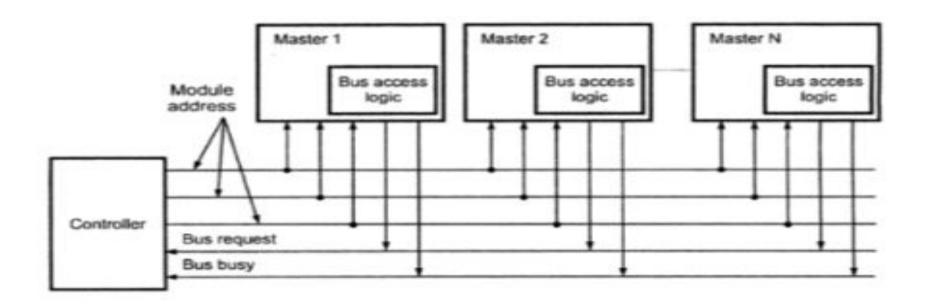
☐ Disadvantages –

- The value of priority assigned to a device is depends on the position of master bus.
- Propagation delay is arises in this method.
- If one device fails then entire system will stop working.

II. Polling or Rotating Priority method –

- In this the controller is used to generate the addresses for the master. Number of address line required depends on the number of master connected in the system.
- For example, if there are 8 masters connected in the system, at least three address lines are required.
- In response to the bus request controller generates a sequence of master address. When the requesting master recognizes its address, it activated the busy line and begins to use the bus.

• The system connections for polling method are shown in the below figure



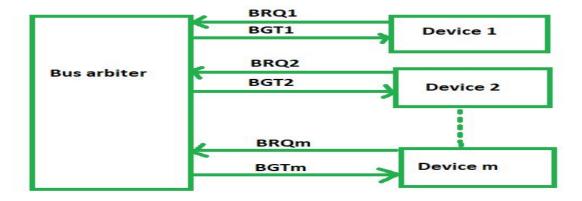
☐ Advantages –

- This method does not favor any particular device and processor.
- The method is also quite simple.
- If one device fails then entire system will not stop working.

- Disadvantages –
- Adding bus masters is difficult as increases the number of address lines of the circuit.

III. Fixed priority or Independent Request method –

- In this, each master has a separate pair of bus request and bus grant lines and each pair has a priority assigned to it.
- The built-in priority decoder within the controller selects the highest priority request and asserts the corresponding bus grant signal.
- The figure below shows the system connections for the independent request scheme



Fixed priority bus arbitration method

☐ Advantages –

• This method generates fast response.

☐ Disadvantage-

• Hardware cost is high as large no. of control lines are required.

2. Distributed Arbitration

- In distributed arbitration, all the devices participate in the selection of the next bus master.
- In this scheme each device on the bus is assigned a4-bit identification number.
- When one or more devices request for the control of bus, they assert the start-arbitration signal and place their 4-bit ID numbers on arbitration lines, ARB0 through ARB3.
- These four arbitration lines are all open-collector. Therefore, more than one device can place their 4-bit ID number to indicate that they need to control of bus.
- In this scheme the device having highest ID number has highest priority.