Janak Raj Srivastava

Software Engineer

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Summary

C++ Developer currently working as EDA Software Engineer at Synopsys, Noida. Currently working as a Compiler Performance Engineer for the VCS team at Synopsys. Previously worked for IR Drop Signoff tool Cadence Voltus.

Experience

Synopsys **Oct 2025 - Present**

Staff Software Engineer Noida, India

Working in the Functional Verification Solution VCS Product Team at Synopsys. Responsible for runtime performance improvement.

Cadence Design Systems **July 2024 - Oct 2025**

Lead Software Engineer Noida, India

https://www.cadence.com/

- Worked Closely with TSMC to develop Cell Libraries generation within Voltus for N2SPR and upcoming A16SPR. More than **1000 TSMC** big and small designs have been validated on new flow.
- Developed PGV Reuse feature for Qualcomm which allows reuse of physical or electrical design data while characterizing a cell library. Performance improved by more than **200% for Big Designs**.
- Developed JSON Dumping utility for Cell Libraries which allows information to be consumed by wide array of frontend applications.
- Worked with teammates to maintain and cleanup the Legacy codebase within Voltus. Modified the existing features to use Modern C++ and improve performance by utilising ASAN and Valgrind to remove/fix memory leaks. Developed unit tests and improved Code coverage **upto 85%**.

Cadence Design Systems **August 2022 - July 2024**

Software Engineer II Noida, India

- Developed features for Library Generation (LibGen) Tool component of Voltus. Providing custom solutions, developing specifications, debugging issues, providing workarounds, file & track code change requests, write & execute testing/validation plans. Coordinated with Voltus PEs to cater to Tier-1 customer needs across various geographies.
- Developed DC Simulation based Capacitance Computation which is upto **50% faster** than pre-exisiting AC Simulation Cap.
- Developed newer library Characterization method for Powergating Cells to bypass a legacy Plugin Call and directly integrate Cadence Spectre within Voltus. This reduced Fatal crashes and newer bugs by **more than 70%** on customer cases.
- Improved Liberty Files based Library generation to improved results during rush-current analysis etc. Flow skips simulations and improves performance by **more than 100%** over default flow.
- As part of learning process, worked on various Cadence tools like Virtuoso, Quantus etc. to get a better understanding of Chip Design Processes.

Computer Languages

C++, Python & Javascript

Skills

GDB debugging, Linux Environment, Bash Scripting, Multi Threading, Object Oriented Design, Data Structure and Algorithms, Computer Vision

Software Packages

C++20, Boost Library, ASAN, TSAN, LSAN, Valgrind, HSPICE, Flask Microframework, OpenCV, CMake, Verilog, SytemVerilog

Education

Indian Institute of Technology, Roorkee **July 2017 - June 2022**

Integrated Masters of Technology

Certifications

Algorithmic Toolbox **2020**

Coursera

Design And Analysis of Algorithms **2020**

IIT Madras

Minors in Quantum Computing **2019**

IIT Roorkee