Design of a CMOS Schmitt Trigger for 28nm process *

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ABSTRACT

The design of a CMOS Schmitt trigger implementation is proposed in this paper for the 28nm process. Design and implementation will be done using synopsys custom design compiler. A Schmitt trigger is a component that converts an analog input to a binary signal with a threshold that depends on the current output value. Its response has some hysterisis which helps reduce the impact of noise on signals.

REFERENCE CIRCUIT DETAILS

The Schmitt trigger circuit has been widely used in the input buffers to increase noise immunity. The conventional input buffer consists of a Schmitt trigger and a level-down converter. The circuit diagram for a CMOS schmitt trigger is shown in Fig 1. The Schmitt trigger circuit receives input signals from the I/O pad and rejects input noise. Then, the level-down converter can convert the signal swing from VCC to VDD.

When the output is a high, the threshold point to turn it low is V_H which is higher than the threshold point to turn a low into a high, V_L. This results in reduced impact of noise because noise will have to be of minimum magnitude $V_H - V_L$ to change the output.

The trigger conditions for long channel MOSFET approximation can be found to be as follows [1]

$$\frac{k_{N1}}{k_{N3}} = \left(\frac{V_{DD} - V_H}{V_H - V_{TN}}\right)^2 \tag{1}$$

$$\frac{k_{P1}}{k_{P3}} = \left(\frac{V_L}{V_{DD} - V_L - |V_{TP}|}\right)^2 \tag{2}$$

Here, k is the transconductance parameter of the MOSFET and is given by Eq. (3).

$$k = \mu_n C_{ox} \frac{W}{L} \tag{3}$$

Since μ_n and C_{ox} are technology parameters and are same for all p-MOSFETs and same for all n-MOSFETs, they can be replaced according to Eq.(4) and Eq.(5).

$$\frac{k_{P1}}{k_{P3}} = \frac{W_{P1} L_{P3}}{L_{P1} W_{P3}} \tag{4}$$

$$\frac{k_{N1}}{k_{N3}} = \frac{W_{P1} L_{P3}}{L_{P1} W_{P3}} \tag{5}$$

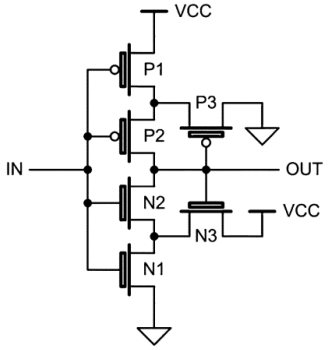

Fig. 1. Circuit for CMOS schmitt trigger [2]

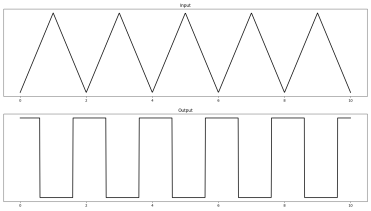

Fig. 2. Expected waveform

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