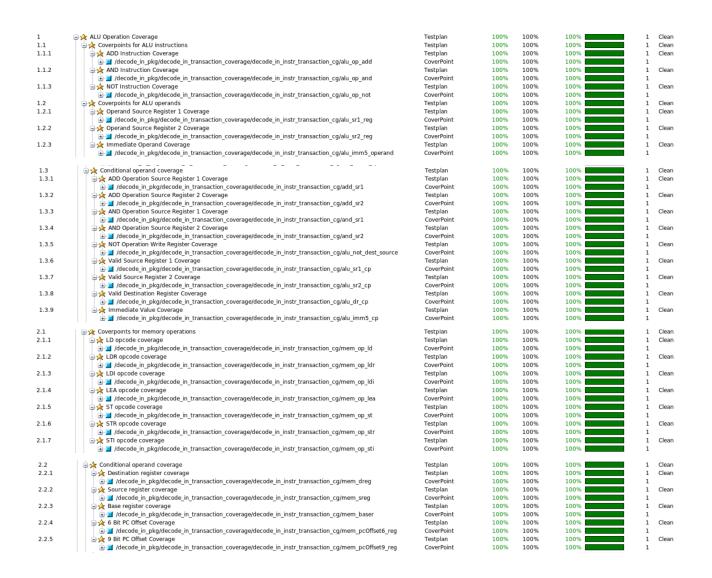
Tesplan

▼ Sec#Testplan Section / Coverage Link Type		Туре	Coverage	Goal	% of Goal	Status	Weight	Link Status
0		Testplan	100%	-	100%		1	Clean
1	🖃 🔆 ALU Operation Coverage	Testplan	100%	100%	100%		1	Clean
1.1		Testplan	100%	100%	100%		1	Clean
1.2		Testplan	100%	100%	100%		1	Clean
1.3	🕁 🔆 Conditional operand coverage	Testplan	100%	100%	100%		1	Clean
1.4	<u>→</u> ★ Cross Coverage	Testplan	100%	100%	100%		1	Clean
2	🖃 🔆 Memory Instructions	Testplan	100%	100%	100%		1	Clean
2.1		Testplan	100%	100%	100%		1	Clean
2.2	🗓 🔆 Conditional operand coverage	Testplan	100%	100%	100%		1	Clean
2.3	<u>→</u> ★ Cross Coverage	Testplan	100%	100%	100%		1	Clean
3	🖃 🔆 Control Instructions	Testplan	100%	100%	100%		1	Clean
3.1		Testplan	100%	100%	100%		1	Clean
3.2	🕁 🔆 Conditional operand coverage	Testplan	100%	100%	100%		1	Clean
3.3		Testplan	100%	100%	100%		1	Clean

Coverpoints



3.1	□☆ Coverpoints for control instructions	Testplan	100%	100%	100%	1	Clean
3.1.1	jMP Opcode Coverage	Testplan	100%	100%	100%	1	Clean
	i decode in pkg/decode in transaction coverage/decode in instr transaction g/ctrl op jmp	CoverPoint	100%	100%	100%	1	
3.1.2		Testplan	100%	100%	100%	1	Clean
	i decode_in_pkg/decode_in_transaction_coverage/decode_in_instr_transaction_cg/ctrl_op_br	CoverPoint	100%	100%	100%	1	
3.2	🛓 🏡 Conditional operand coverage	Testplan	100%	100%	100%	1	Clean
3.2.1	🚊 🔆 Branch Condition Flags Coverage	Testplan	100%	100%	100%	1	Clean
		CoverPoint	100%	100%	100%	1	
3.2.2		Testplan	100%	100%	100%	1	Clean
	i→ / decode_in_pkg/decode_in_transaction_coverage/decode_in_instr_transaction_cg/ctrl_pcoffset9	CoverPoint	100%	100%	100%	1	
3.2.3	🛓 🔆 Base Register Coverage for JMP	Testplan	100%	100%	100%	1	Clean
		CoverPoint	100%	100%	100%	1	

Cross

1.4	□☆ Cross Coverage	Testplan	100%	100%	100%	1	Clean
1.4.1	🖨 🔆 NOT Instruction Cross Coverage	Testplan	100%	100%	100%	1	Clean
	i / decode_in_pkg/decode_in_transaction_coverage/decode_in_instr_transaction_cg/not_x_sr1	Cross	100%	100%	100%	1	
1.4.2	□ 🔆 Cross Coverage for Source Register 1	Testplan	100%	100%	100%	1	Clean
	[i] /decode_in_pkg/decode_in_transaction_coverage/decode_in_instr_transaction_cg/alu_sr1_cross_cp	CoverPoint	100%	100%	100%	1	
1.4.3	☐ ☆ Cross Coverage for Source Register 2	Testplan	100%	100%	100%	1	Clean
	[i] /decode_in_pkg/decode_in_transaction_coverage/decode_in_instr_transaction_cg/alu_sr2_cross_cp	CoverPoint	100%	100%	100%	1	
1.4.4	☐ ☆ Cross Coverage for Destination Register	Testplan	100%	100%	100%	1	Clean
	<u>→ ■</u> /decode_in_pkg/decode_in_transaction_coverage/decode_in_instr_transaction_cg/alu_dr_cross_cp	CoverPoint	100%	100%	100%	1	
2.3	☐ 🔆 Cross Coverage	Testplan	100%	100%	100%	1	Clean
2.3.1	⇒ 🔆 LD Destination Register Cross	Testplan	100%	100%	100%	1	Clean
	// decode in pkg/decode in transaction coverage/decode in instr transaction cg/ld_x_dr	Cross	100%	100%	100%	1	
2.3.2	⇒ 🔆 LD PC Offset Cross	Testplan	100%	100%	100%	1	Clean
	Jdecode_in_pkg/decode_in_transaction_coverage/decode_in_instr_transaction_cg/ld_x_pcoffset9	Cross	100%	100%	100%	1	
2.3.3	⇒ 🔆 LDR Destination Register Cross	Testplan	100%	100%	100%	1	Clean
	Jdecode_in_pkg/decode_in_transaction_coverage/decode_in_instr_transaction_cg/ldr_x_dr	Cross	100%	100%	100%	1	
2.3.4	□ 🎪 LDR Base Register Cross	Testplan	100%	100%	100%	1	Clean
	Jecode in pkg/decode in transaction coverage/decode in instr transaction cg/ldr x baser	Cross	100%	100%	100%	1	
2.3.5	□ 🎪 LDR PC Offset Cross	Testplan	100%	100%	100%	1	Clean
	// decode in_pkg/decode in_transaction_coverage/decode in_instr_transaction_cg/ldr_x_pcoffset6	Cross	100%	100%	100%	1	
2.3.6	□ 🍁 LDI Destination Register Cross	Testplan	100%	100%	100%	1	Clean
	// decode in pkg/decode in transaction coverage/decode in instr transaction cg/ldi x dr	Cross	100%	100%	100%	1	
2.3.7	□ ½ LDI PC Offset Cross	Testplan	100%	100%	100%	1	Clean
	Jdecode in_pkg/decode in_transaction_coverage/decode in_instr_transaction_cg/ldi_x_pcoffset9	Cross	100%	100%	100%	1	
2.3.8	⇒ ★ ST Source Register Cross	Testplan	100%	100%	100%	1	Clean
	J /decode_in_pkg/decode_in_transaction_coverage/decode_in_instr_transaction_cg/st_x_sr	Cross	100%	100%	100%	1	
2.3.9	□ 🎪 ST PC Offset Cross	Testplan	100%	100%	100%	1	Clean
	Jdecode in_pkg/decode in_transaction_coverage/decode in_instr_transaction_cg/st_x_pcoffset9	Cross	100%	100%	100%	1	
2.3.10	⇒ ★ STR Source Register Cros	Testplan	100%	100%	100%	1	Clean
	decode_in_pkg/decode_in_transaction_coverage/decode_in_instr_transaction_cg/str_x_sr	Cross	100%	100%	100%	1	
2.3.11	→ STR Base Register Cross	Testplan	100%	100%	100%	1	Clean
	Jdecode in_pkg/decode in_transaction_coverage/decode in_instr_transaction_cg/str_x_baser	Cross	100%	100%	100%	1	
2.3.12	□ 🎪 STR PC Offset Cross	Testplan	100%	100%	100%	1	Clean
	Jecode in_pkg/decode in_transaction_coverage/decode in_instr_transaction_cg/str_x_pcoffset6	Cross	100%	100%	100%	1	
2.3.13	□ 🎪 STI Source Register Cross	Testplan	100%	100%	100%	1	Clean
	Jecode in pkg/decode in transaction coverage/decode in instr transaction cg/sti x sr	Cross	100%	100%	100%	1	
2.3.14	→ STI PC Offset Cross	Testplan	100%	100%	100%	1	Clean
	J /decode_in_pkg/decode_in_transaction_coverage/decode_in_instr_transaction_cg/sti_x_pcoffset9	Cross	100%	100%	100%	1	
2.3.15	□ ½ LEA Destination Register Cross	Testplan	100%	100%	100%	1	Clean
	Jacobe_in_pkg/decode_in_transaction_coverage/decode_in_instr_transaction_cg/lea_x_dr	Cross	100%	100%	100%	1	
2.3.16	□ 🎪 LEA PC Offset Cross	Testplan	100%	100%	100%	1	Clean
		Cross	100%	100%	100%	1	
3.3	□ ★ Cross Coverage	Testplan	100%	100%	100%	1	Clean
3.3.1	☐ ★ JMP Base Register Cross	Testplan	100%	100%	100%	1	Clean
3.3.1	decode in_pkg/decode in_transaction_coverage/decode in_instr_transaction_cg/baser_x_imp	Cross	100%	100%	100%	1	Cicali
3.3.2	□ ★ BR PC Offset Cross	Testplan	100%	100%	100%	1	Clean
3.3.2	decode_in_pkg/decode_in_transaction_coverage/decode_in_instr_transaction_cg/pcoffset9_x_br	Cross	100%	100%	100%	1	Ciedii
3.3.3	BR Condition Flags Cross		100%	100%	100%	1	Clean
3.3.3		Testplan	100%	100%	100%	1	Ciedii
	→	Cross	100%	100%	10070	1	