Abstract

- Amplification of small voltage swing to recognizable logic level in 4X4 SRAM using Sense Amplifier.
- Demonstration of Sense Amplifier offset voltage in a 180nm CMOS fully functional SRAM.

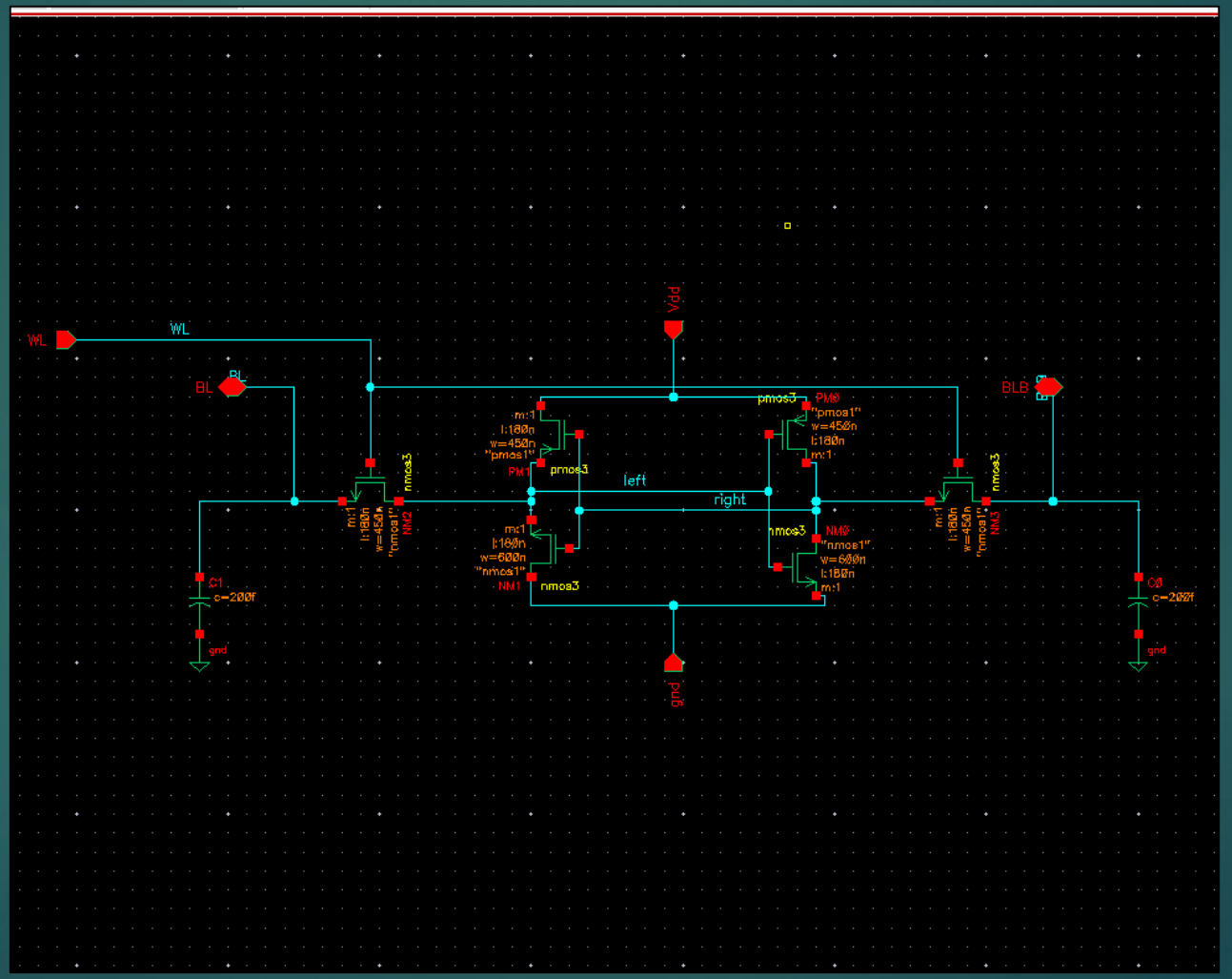
SRAM

Static random-access memory (**static RAM** or **SRAM**) is a type of semiconductor memory that uses flip-flop to store each bit.

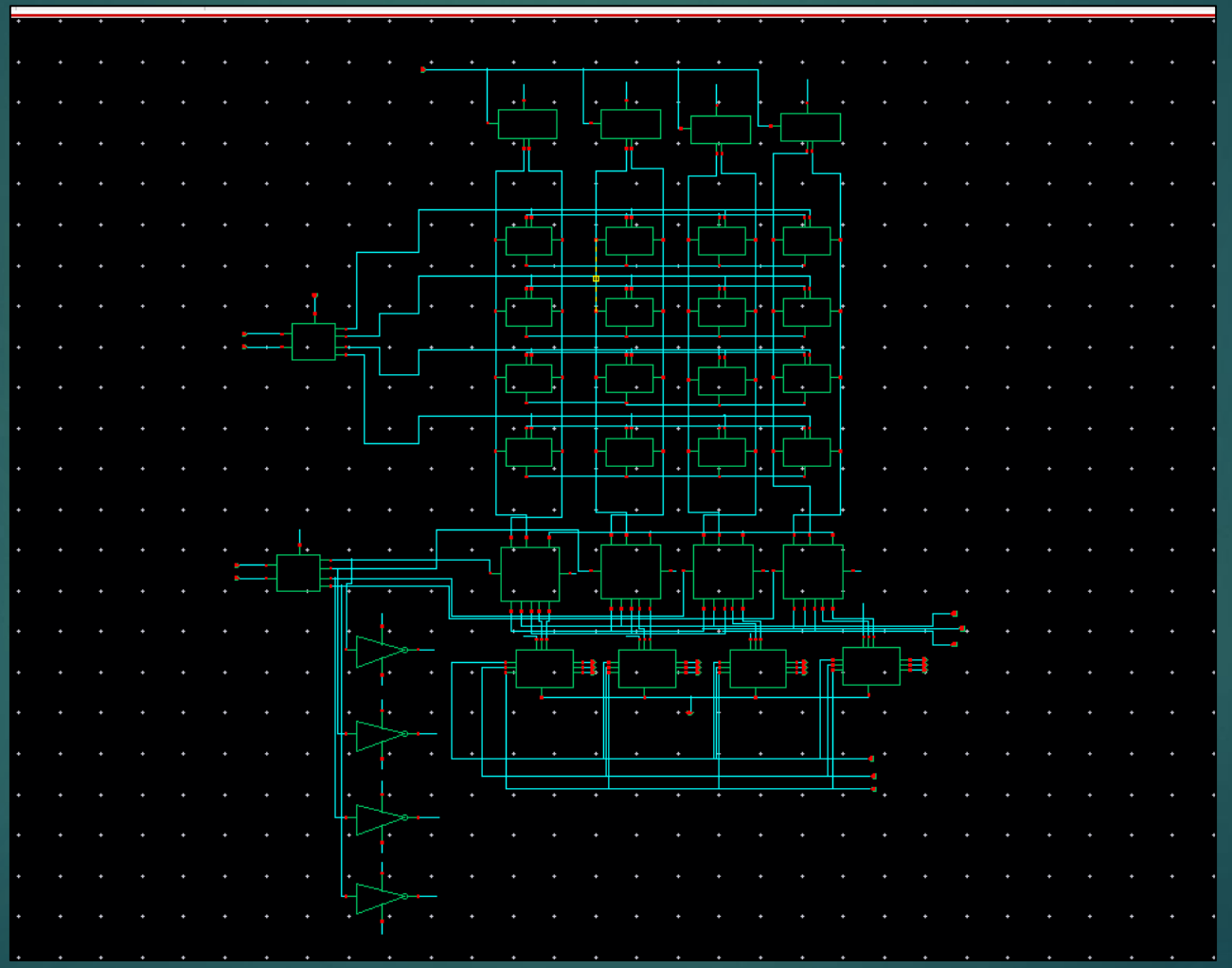
SRAM of Static Random Access Memory is a memory device with two key features:

1. SRAM is a form of random access memory
2. The data is held statically

Structure of 1-bit SRAM



Structure of 4X4 SRAM with Sense Amplifier



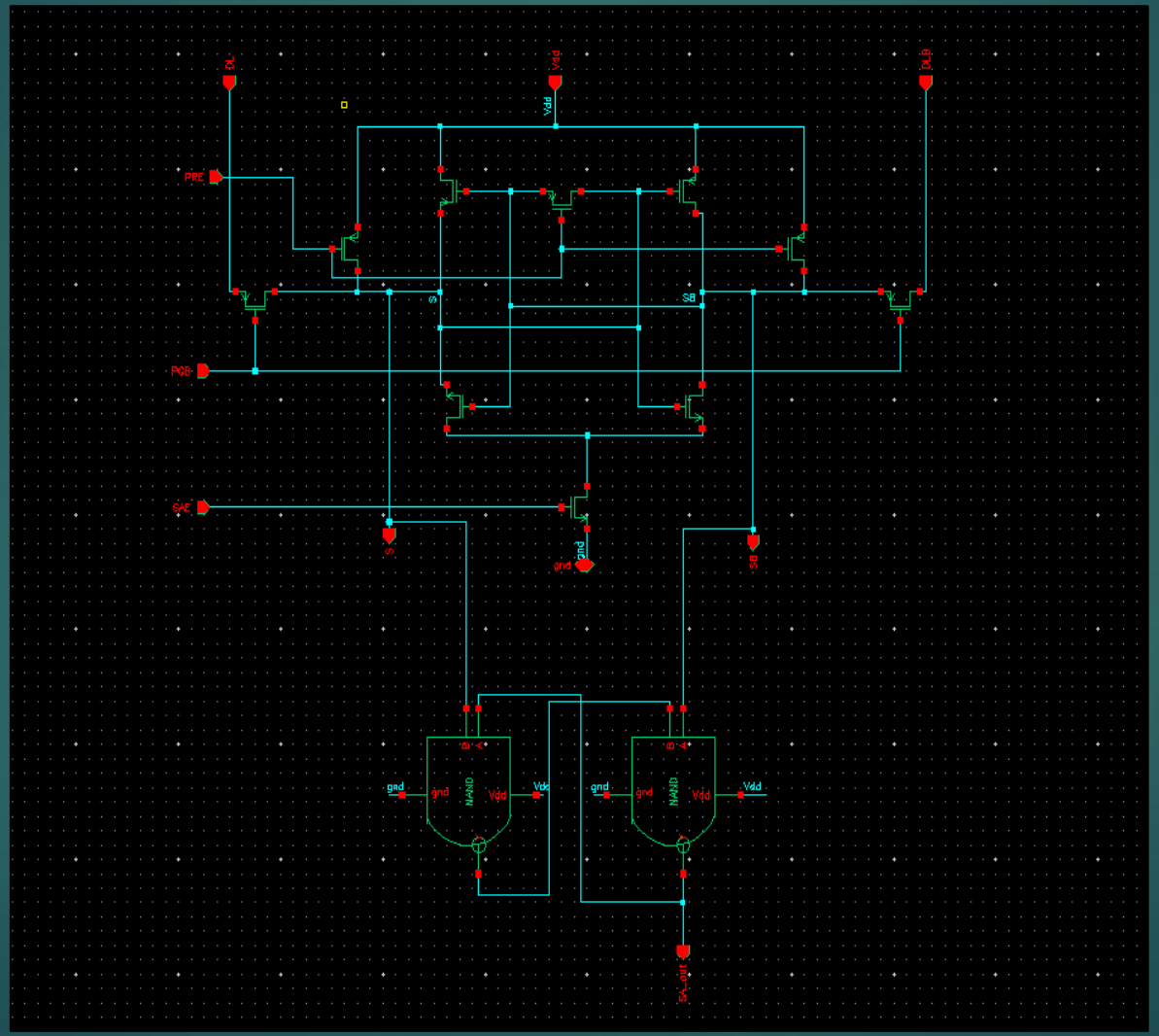
SENSE AMPLIFIER

- A sense amplifier is part of the read circuitry that is used when data is read from the memory; its role is to sense the low power signals from a *bit-line* that represents a data bit (1 or 0) stored in a memory cell, and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly by logic outside the memory.

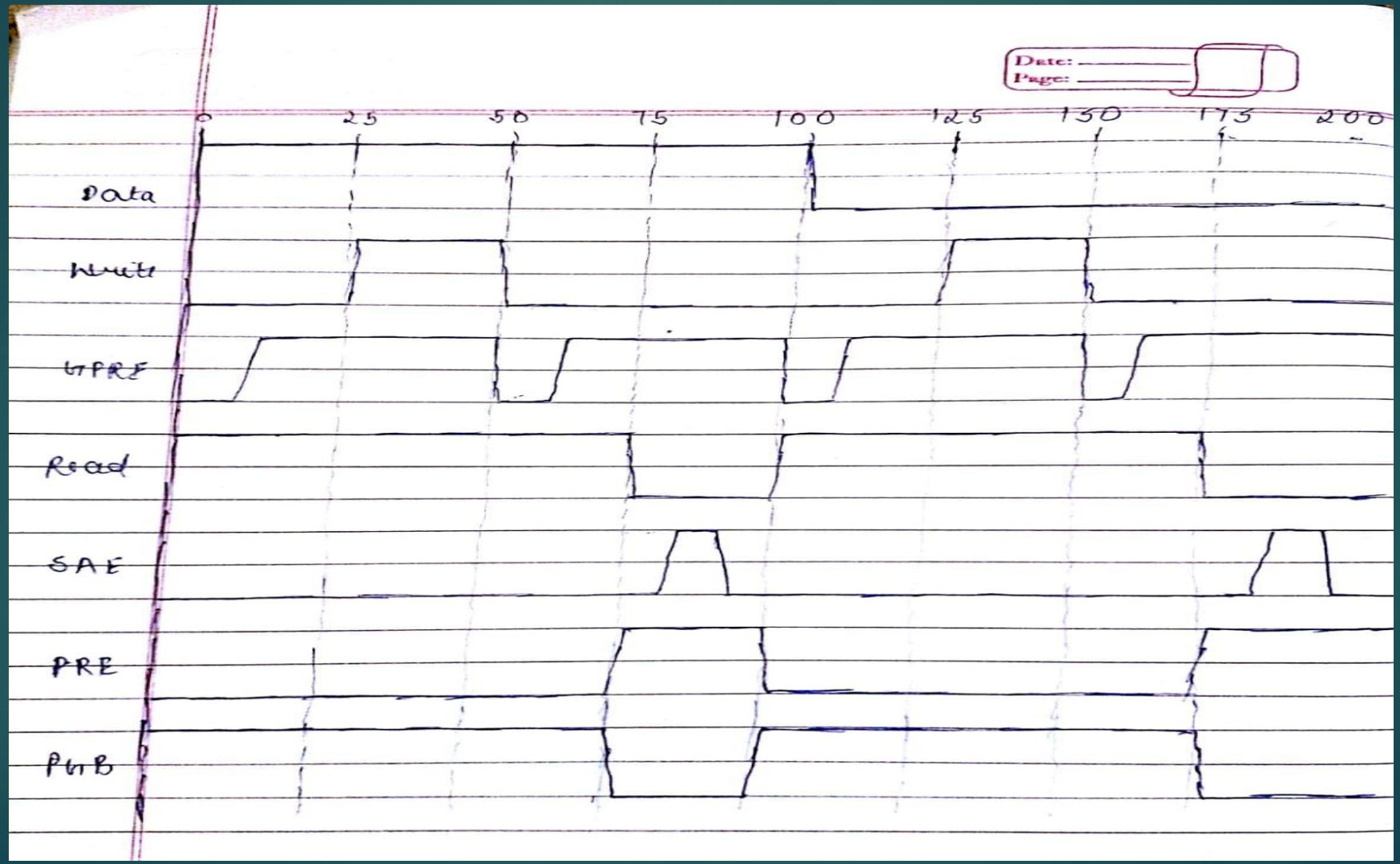
- There is one sense amplifier for each column of memory cells so there are four identical sense amplifiers in the 4X4 SRAM used in our demonstration.

- Sense Amplifier is required during the data read and refresh operation from the memory concerned.

Structure of Sense Amplifier



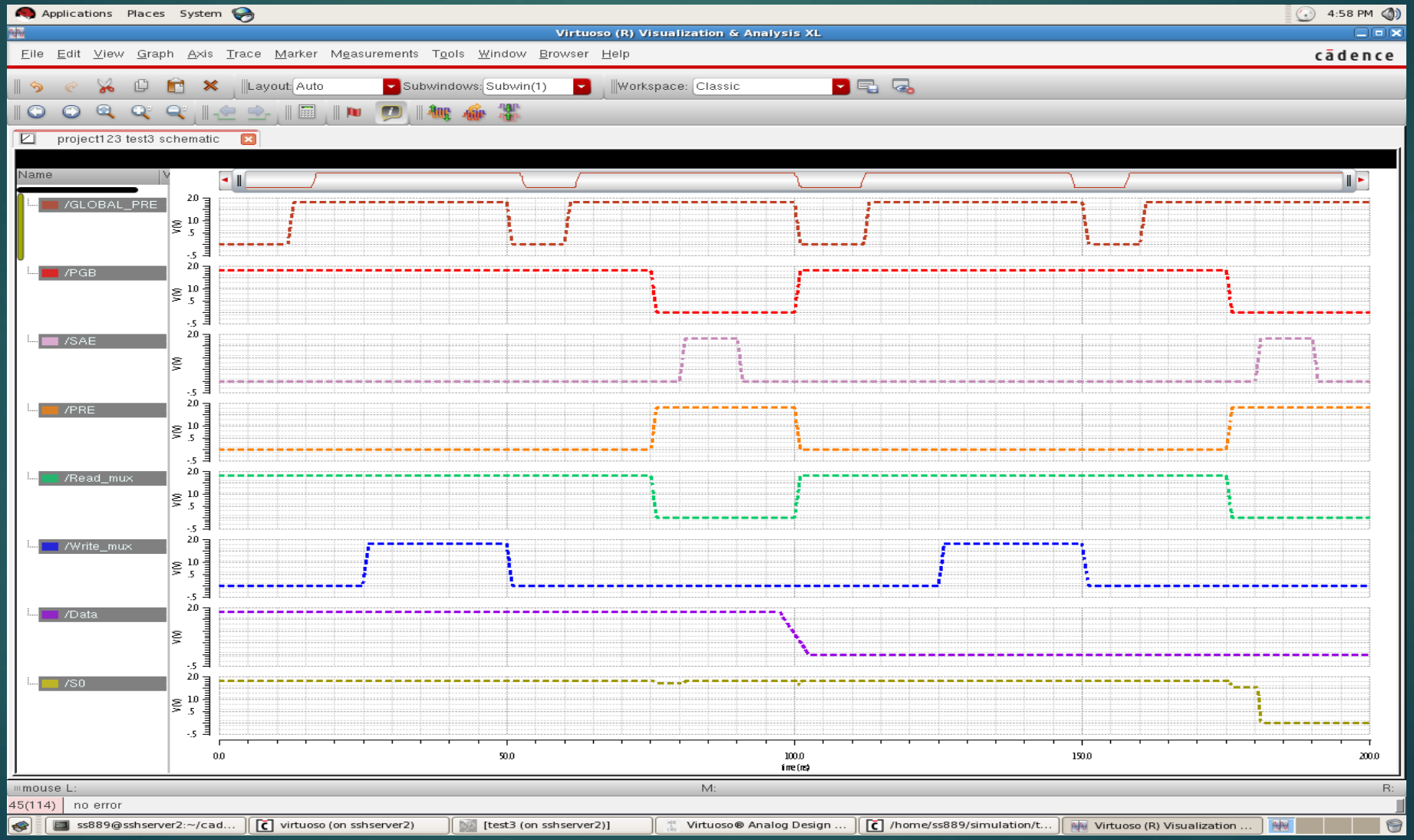
Input to Sense Amplifier



Functioning of the Sense Amplifier

- To read a bit from a particular memory cell, the word line along the cell's row is turned on, activating all the cells in the row. The stored value (Logic 0 or 1) from the cell then comes to the Bit-lines associated with it. The sense amplifier at the end of the two complimentary bit-lines amplify the small voltages to a normal logic level.
- Adjusting the external voltage source creates a differential voltage on the DL & DLB signal nodes capable of being transferred to the sense amplifier using a PMOS pair. This enables differential data to be read out to a read-output latch.

Output of sense amplifier in read and write cycle



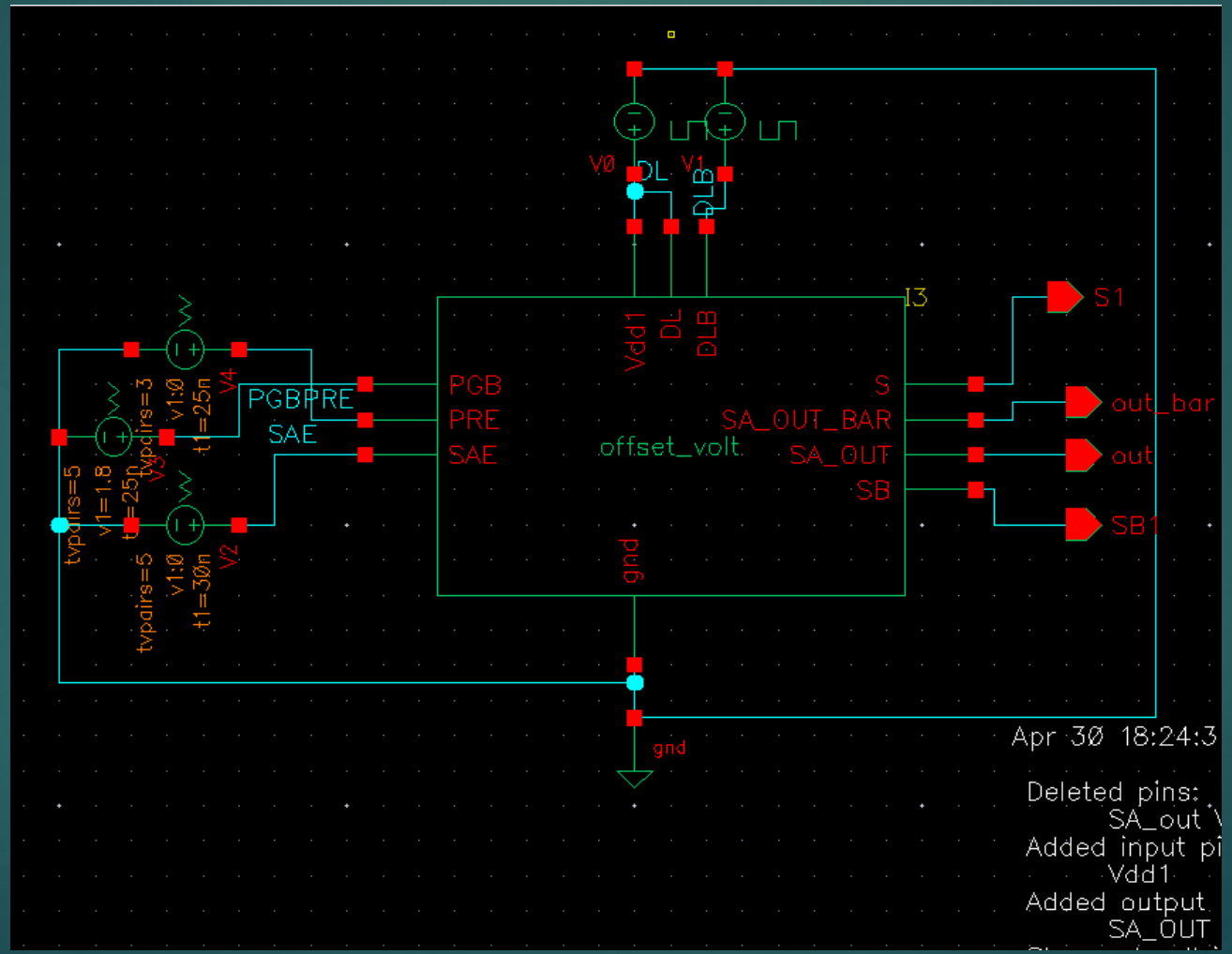
Offset Voltage

- Adjusting the external voltage input of sense amplifier creates a differential voltage on the DL & DLB signal nodes. If This differential input to the sense amplifier is greater than Vsa(offset voltage),a correct read ‘1’ operation is performed.
- As soon as the differential voltage goes below the offset voltage (Vsa) ,the sense amplifier flips to the read ’0’ operation.
- The point where output gets flipped i.e. from 1 to 0 is known as offset voltage.

Procedure to find Offset Voltage

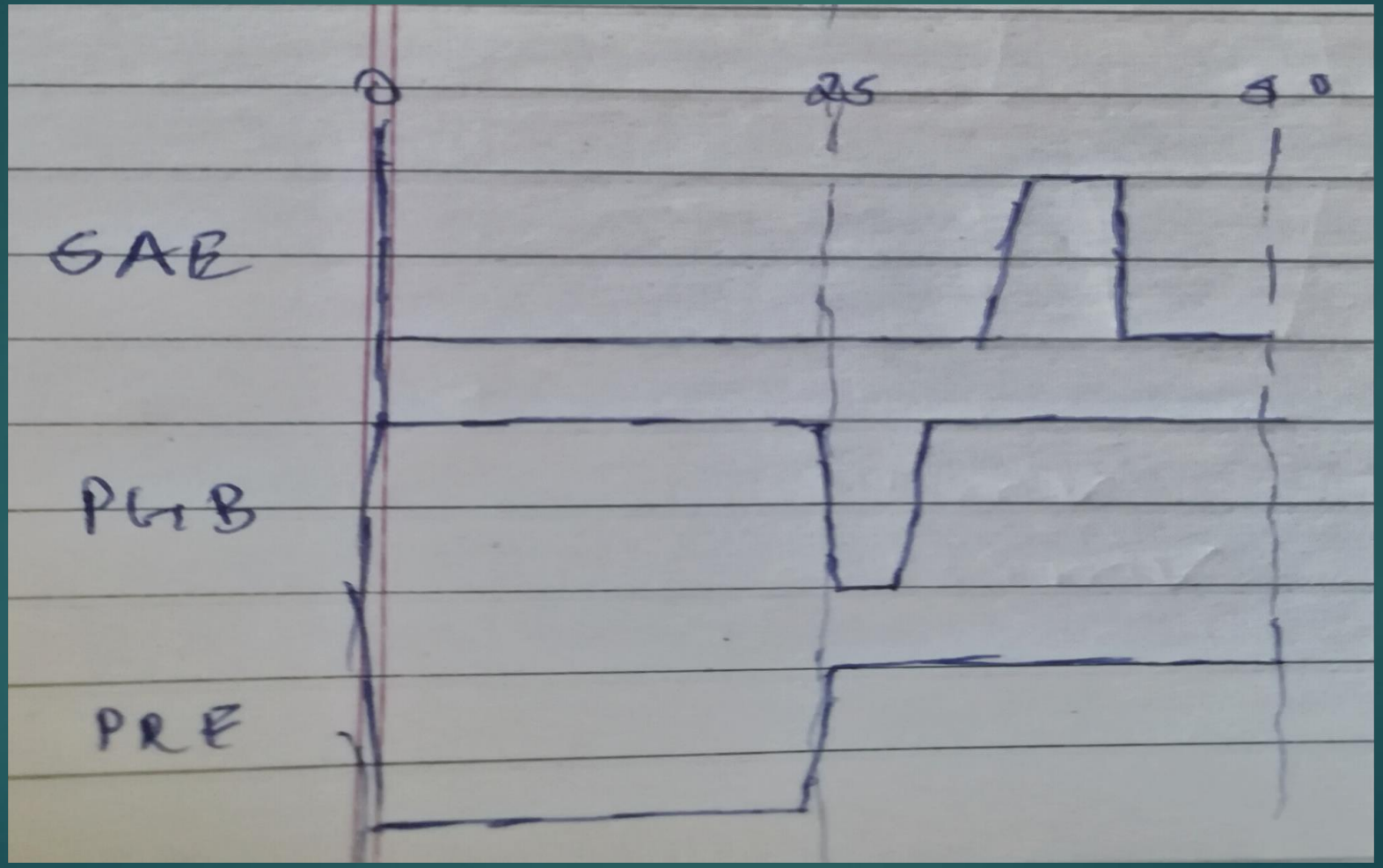
- Create a voltage differential Vsa (Vdl – Vdlb) on the input pair of sense amplifier i.e. DL and DLB.
- Enable the sense amplifier by giving appropriate input to PRE, PGB, and SAE and read out the voltage differential (Vsa) on DL and DLB.
- Continue reducing Vsa by adjusting the external Dc voltage source until the output of sense amplifier flips.

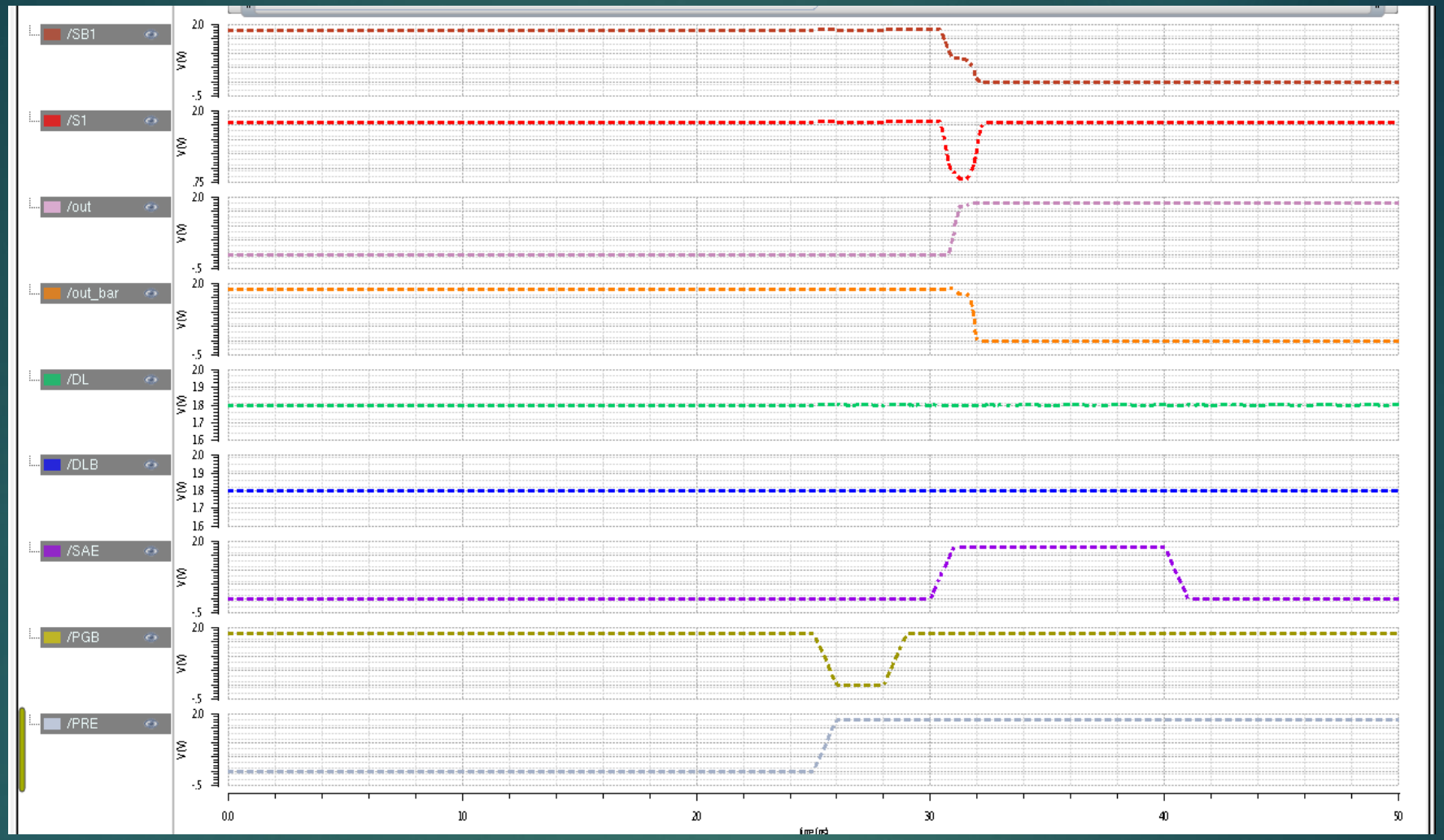
Circuit for calculating Offset Voltage



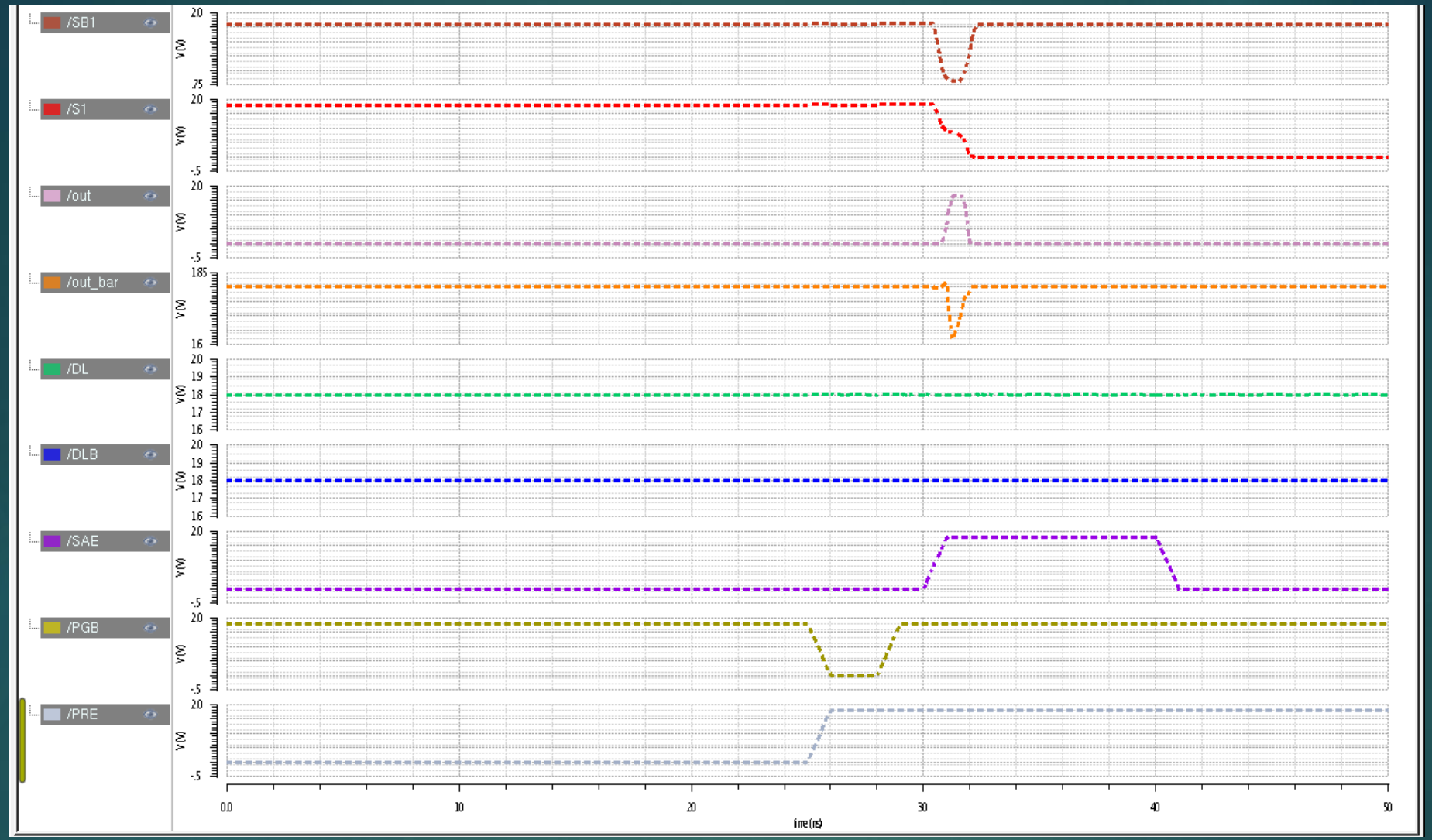
Observations & Conclusions

Input for calculating Offset Voltage





When Differential Voltage(Vdl-Vdlb)=0.14 mv , Correct Read operation was performed.



When Differential Voltage(Vdl-Vdlb)<0.14 mv ， Output gets flipped.

Conclusions:

- From the previous two observations, we conclude that offset voltage is 0.14 mv.
- We also observed that as mismatching is done between the n-mos connected to DL and DLB , offset voltage increases.

N-Mos connected to DL	N-Mos connected to DLB	Offset Voltage
Wn=2u	Wn=2u	0.14mV
Wn=2.3u	Wn=2u	14.60mV