Experiment - 9.

Aim:- Write test bench for full adder circuit with VHDL code.

Software:- Model Sim.

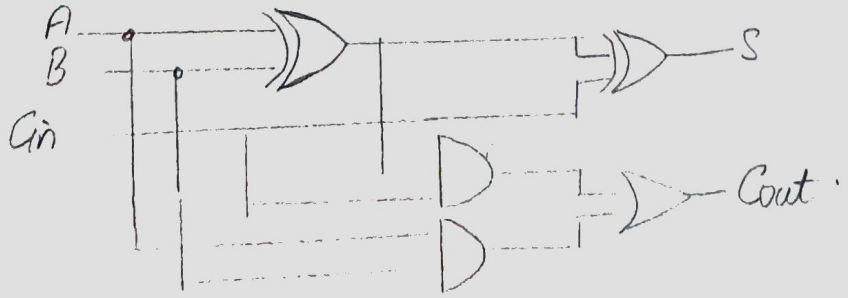
Theory:- A test bench is a model that is used to excersice and verify the correctness of a hardware model. A test bench is needed for three main purposes.

a) To generate stimulus for simulation (waveforms)
b) To apply this stimulus to the entity under test and to monitor the output responses.
c) To compose output responses with expected known values.

Steps to write a test bench:

1) The entity port list is always empty.
2) Under the architecture, all the components are declared for the under unit test (uut)
3) Inputs are declared & intialized to zero alongs with o/ps.
4) For sequential circuits, clock period is defined too.
5) UUT is initialized and process for stimulus is written for sequential designs, process for clock is coullen

Circuit Diagram:



Full adder.

BOOLEAN EXPRESSIONS:

C_{IN}	B	A	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = A \oplus B \oplus C$

$Cout = AB + BCin + ACin$

Result:- Test bench for full adder circuit was written and implemented in VHDL.