Experiment - 1

Aim: To study features of 8085 microprocessor. Study the architecture and pin diagram of 8085 microprocessor. Write a brief description of 8085 simulator.

INTEL 8085 MICROPROCESSOR :-

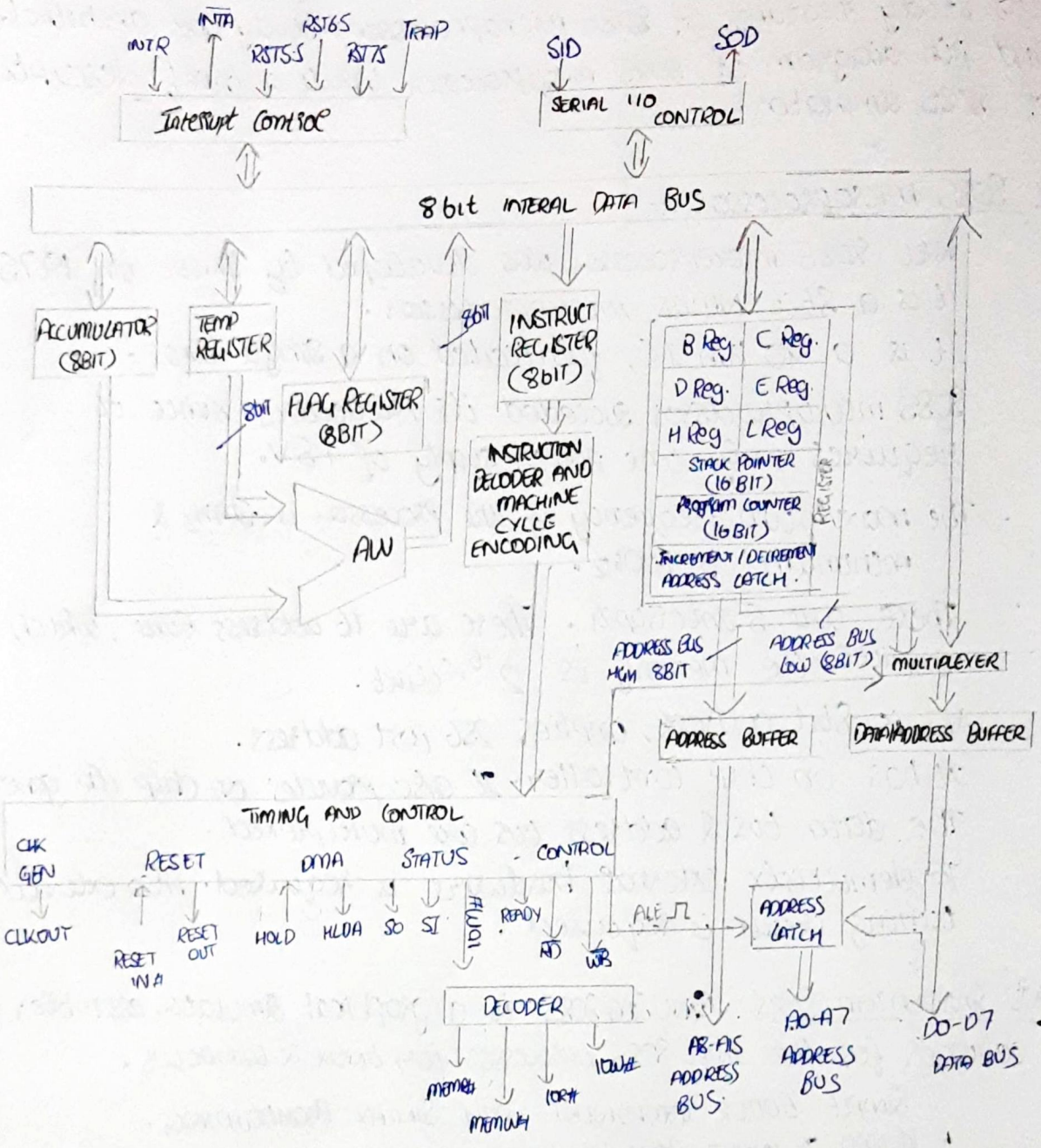
INTEL 8085 microprocessor was developed by INTEL in 1975.
It is a 8bit NMOS microprocessor.
It is a 40 Pin IC, fabricated on a single line.
8085 microprocessor succeded its predecessors since it requires only one power supply of +5V.
The maximum frequency of the processor is 3MHz & minimum is 500Hz.
There are 5 interrupts. There are 16 address line, which implies the memory is $2^{16} = 64kb$.
I/O is 8bit address, implies 256 port address.
It has on chip controller. It also provides on chip clk generat
The data bus & address bus are multiplexed.
To demultiplex external hardware is required. Also external tuning circuit is required.

GNU SIMULATOR 8085: GNUSim8085 is a graphical simulator, assembler & debugger for the INTEL 8085 µprocessor for LINUX & WINDOWS.

- SIMPLE EDITOR COMPONENT WITH SYNTAX HIGHLIGHTING.
- KEYPAD TO INPUT Assembly language instructions
- easy view of registers contents
- easy view of flag contents.
- hexadecimal to decimal converter.
- view of stack, memory & I/O contents.

nbyte instruction is the number of n memory location required to store the instruction.
- MOV is 1byte ins - MVI is 2byte inst - LDA is 3byte Inst

Architecture of 8085 microprocessor:



Can be divided into 5 groups:

1. Arithematic Logical unit Group:
    1. Accumulator:
        1. 8bit register
        2. General Purpose
    2. Temp Reg:
        1. not available for the user
        2. used internally by microprocessor
        3. Example are W, and Z
    3. Flag flip-flops
    4. Instruction Register
    5. ALU:
        1. Inputs are Accumulator and Temp reg
        2. It performs arithematic operations
2. Register Group
3. Interrupt Control Group:
    1. 5 interrupts are there and one acknowledgement
4. Serial I/O Control Group:
    1. SOD
    2. SID
5. Timing and Control Group:
    1. Instruction register:
        - used for internally usage
        - instruction are stored here
    2. Instruction decoder and machine cycle encoding:
        - when opcode is availabe for instruction
        - operands are not accepted
        - non programmable register
        - bit pattern is accepeted from IR
        - and sends it to Timing and Control
    3. Timing and Control:
        - Control Section
        - generates “microsteps” to perform the instruction
        - Clock input and sychronizing
        - communication between peripheral and 8085

Flag Register

- 8bit register
- Sign Flag, Zero Flag, Auxillary Carry Flag, Parity Flag, Carry Flag

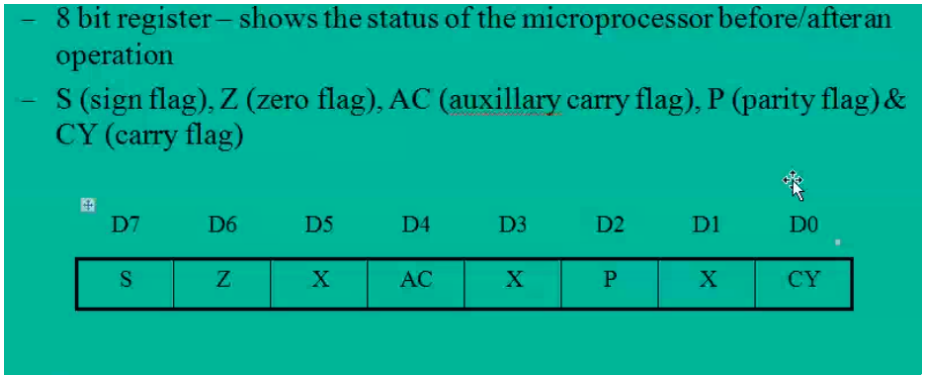


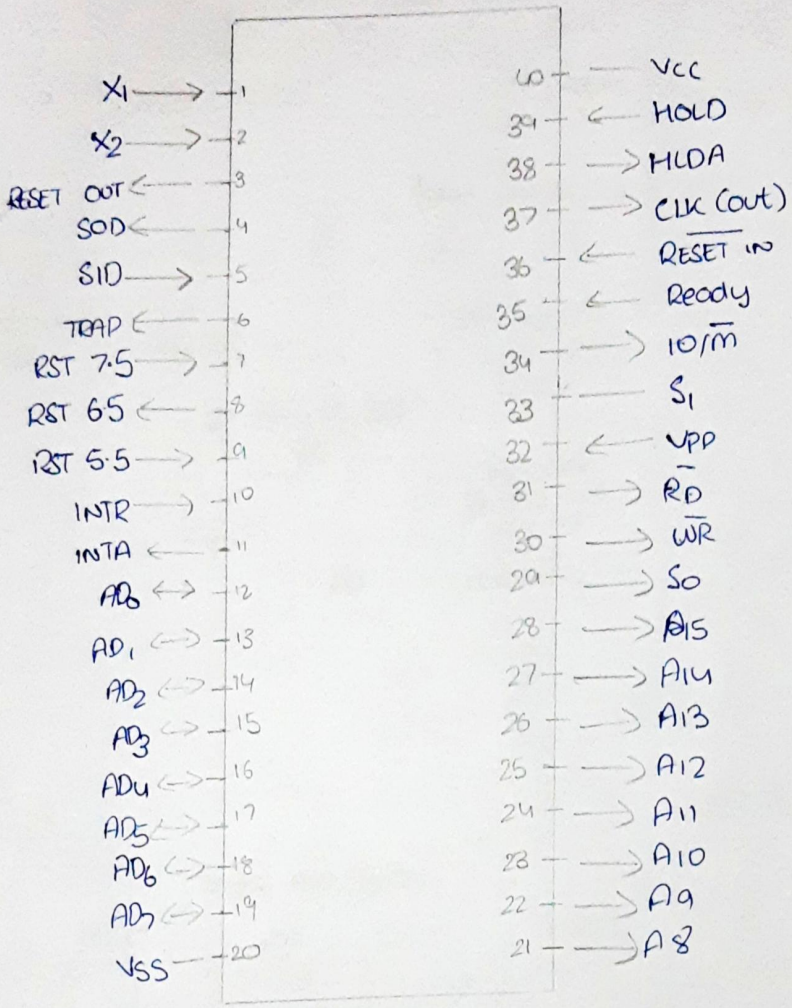
Figure 2: Flag Register

- Carry Flag:
  - used when carry is generated
  - acts as 9th bit
  - borrow bit in difference
- Auxillary Flag:
  - Carry is genereted at lower nibble, to upper nibble then this flag is set
  - used internally only
  - binary to binary conversion
  -
- Zero Flag:
  - if operation result is zero, this flag is set
- Sign Flag:
  - set if negative, reset if positive, that is for MSB bit
  - used to indicate the sign of data in accumulator
- Parity Flag:
  - used to indicate the parity of result, if the result contains even no. of "1" then the flag is set, if odd the reset

Types of register

- temp: W and z:
  - used internally
  - for calculation purposes
- General Purpose: B, C, D, E, H, L:
  - to form register pair of 16bit
  - 8bit register
  - programmable by user
- Special purpose:
  - Stack Pointer:
    - used for execution of programs
    - points to memory address to fetch next instruction
    - store the information cpu
    - works in lifo
    - 16bit address used to define starting point
    - tracks the data stored
  - Program Counter:
    - increments by one when fetching next instruction
    - at start, it set at 0
    - it is of 16bit, since 8085 contains 16 address line using which any memory location can be accessed. Hence 16bit are sufficient
  - Incremental/ Decrementer address latch:
    - used in co-ordination with above two
    - to increment and decrement infro
  - 16bit registers

PIN DIAGRAM:-


X1
X2
RESET OUT
SOD
SID
TRAP
RST 7.5
RST 6.5
RST 5.5
INTR
INTA
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
VSS
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
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40
39
38
37
36
35
34
33
32
31
30
29
28
27
26
25
24
23
22
21
VCC
HOLD
HLDA
CLK (out)
RESET IN
Ready
IO/M
S1
VPP
RD
WR
SO
A15
A14
A13
A12
A11
A10
A9
A8

- 40 pin IC
- can be divided into 10 types:
  - Address Data bus 21 to 28:
    - ouptut tristate signal used as higher order 16bit signal
    - unidirection signals, only address is given by 8085 to peripheral devices
    - Reset, hold, halt
  - Multiplexed Address data Bus 12 to 19:
    - input/output tristate signal, address in data
    - lower order 8bit signal
    - used as data bus later on
    - less pins are required because of multiplexing
    - demultiplexing is required which is disadvantage, hence more time and circuit is required.
  - Control Signals :
    - 30th (ALE) demultiplexing of lower order data bus
    - 34 (IO/$\overline{M}$) Input/Output Memory, gives status of operation mode
    - 32 ($\overline{RD}$) READ
    - 31 ($\overline{WR}$) WRITE
    - 35 (READY) input to microprocessor from lower peripheral to faster microprocessor and synchronizes it and check if data transfer is ready
  - Status Pins : Gives Stauts of what operation is performed
    - 29 (S_0)
    - 33 (S_1)

S1	S0	Operation
0	0	Hatl
0	1	Write
1	0	Read
1	1	Fetch

  - Clock Signal:
    - 37 Clock out input signal used as internal clock
    - 1 : connected to crystal
    - 2 :
  - Interupt Signal:
    - 6 Trap: level high signal, edge triggered, level triggered, highest priority, non maskable interrupt
    - 7 RST 7.5: Restart interuptts, active high,edge or level triggered, maskable interrupt
    - 8 RST 6.5
    - 9 RST 5.5
    - 10 INTR: Interrupt request
    - 11 $\overline{INTA}$

- Serial Signal :
  - 5 SID: input signal for software contro
  - 4 SOD: output signal
- DMA Request Signal: Direct memory access
  - 39 HOLD: active high, used by other control to access data signals and address signals, input signal
  - 38 HLDA: acknowledgment signal to HOLD
- RESET Singal:
  - 3 RESET OUT:
  - 35 RESET IN: used to clear program counter to 00000
- Power Supply:
  - VCC: 5v
  - VSS: Ground