Experiment-4

Aim:- To design and implement following:

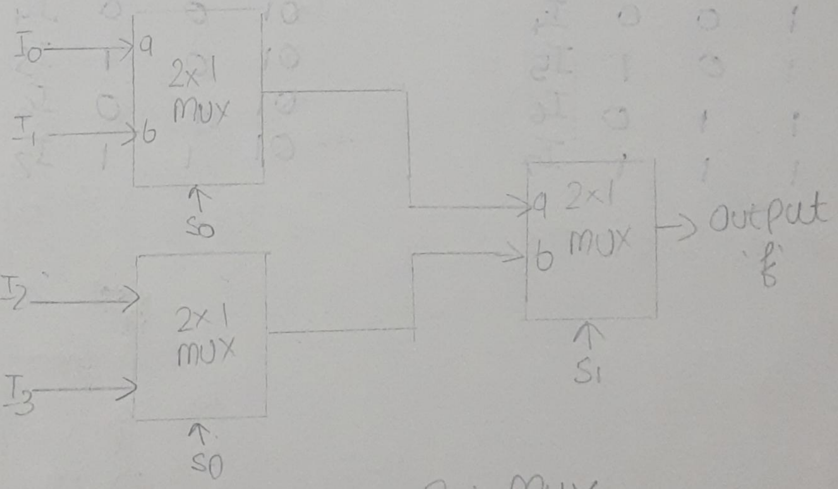
1. 4:1 mux using 2:1 mux
2. 8:1 mux using 4:1 mux
3. 16:1 mux using 4:1 mux
4. Full adder using HA
5. Full subtractor using HS.

Software Used:- ModelSim

Theory:- 4:1 Mux Using 2:1 Mux:

A 4:1 mux consists of four data inputs lines as D0 to D3, 2 select lins as S0 and S1. And single output Y0. When S0 & S1=0 then Y is D0, 11ly Y is D1 if $S_0=1$, & $S_1=0$ & so on.

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3



4x1 MUX using 2x1 MUX

The truth table for 2:1 mux using 4:1 mux is.

S_1	S_0	f
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

2· 8:1 mux using 4:1 mux·

In this configuraton, 2 4x1 Mux & 1 2x1 Mux is required. The two multiplexer in first stage in order to get 8data inputs and 2:1 Mux is second stage·

II Using Or gate & 4:1 Mux

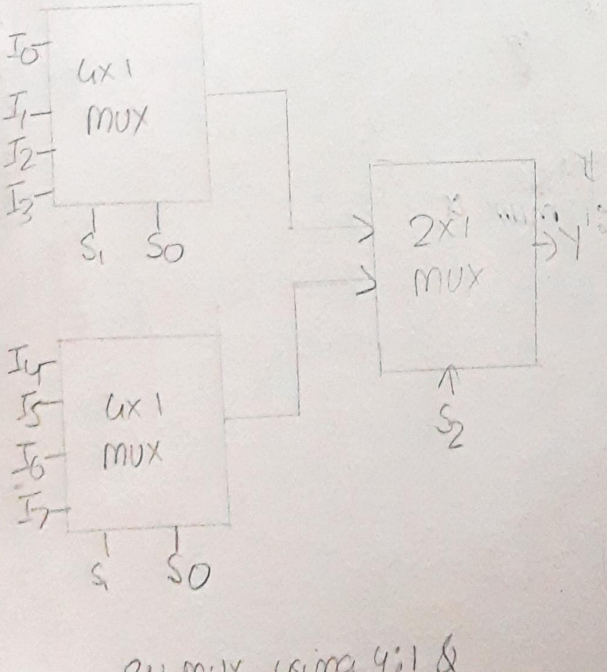
It contains 2 4x1 mux which will take 8 inputs & the outputs of first stage is passed through the or gate to OR gate to get the output

S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

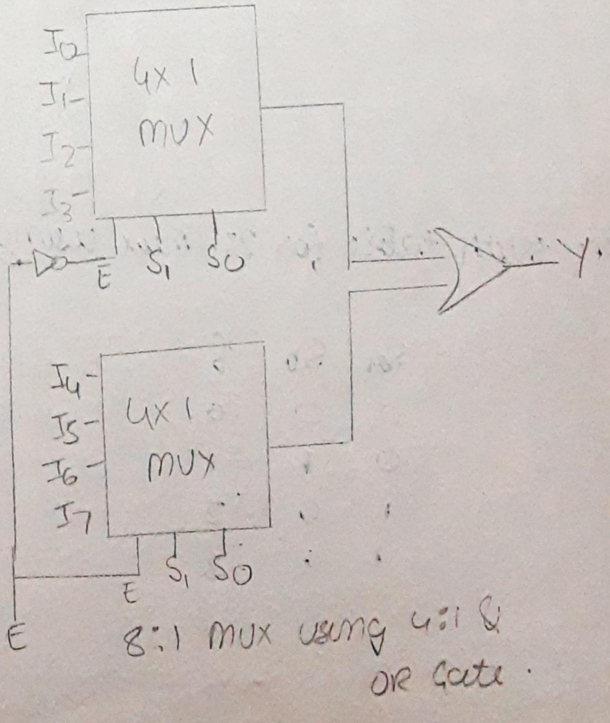
2 4:1 mux & 1 2:1 MUX

E	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
01	0	0	I_4
01	0	1	I_5
01	1	0	I_6
01	1	1	I_7

2 4:1 Mux & OR Gate



8:1 MUX using 4:1 & 2:1 MUX

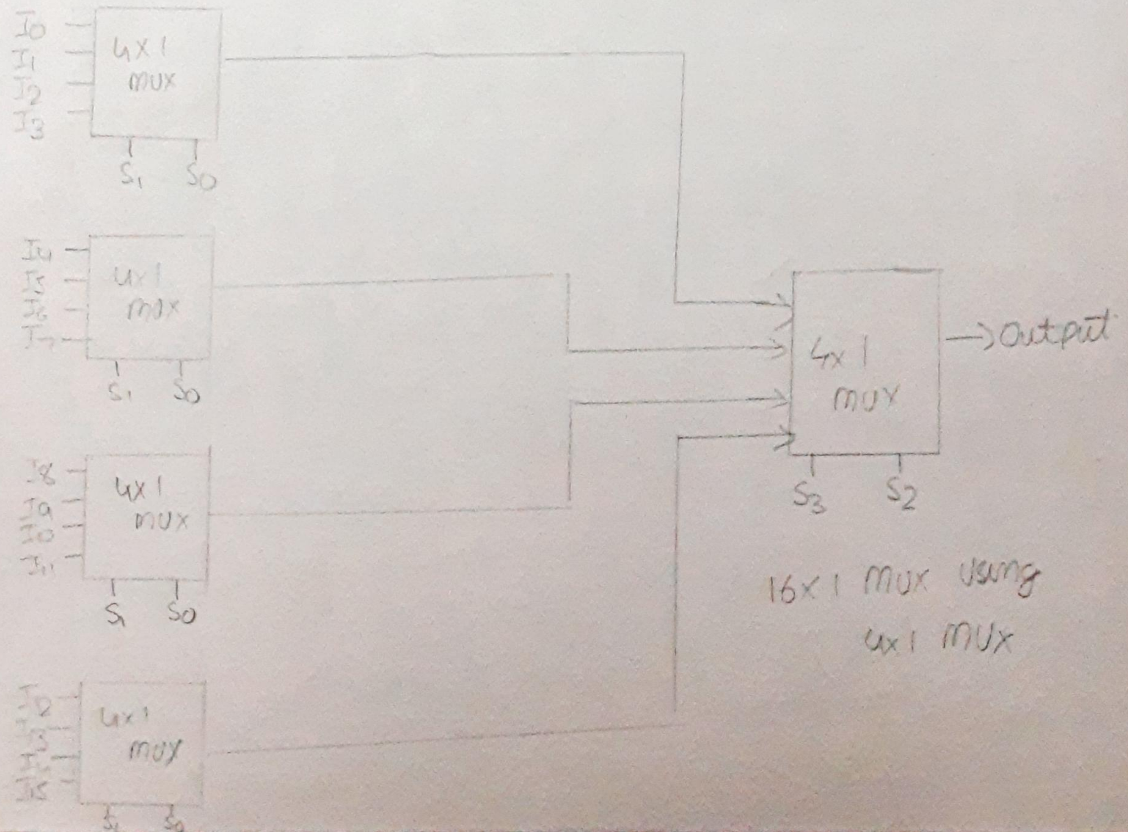


8:1 MUX using 4:1 & OR Gate·

3. 16:1 Mux Using 4:1 Mux:-

It contains 16 inputs lines & 4 select lines. 5 '4x1' MUX are used out of which 4 '4x1' mux are used to get 16 input lines and the output of the mux & fed to another 4x1 mux to get desired out output.

S_0	S_1	S_2	S_3	Y
0	0	0	0	I_0
0	0	0	1	I_1
0	0	1	0	I_2
0	0	1	1	I_3
0	1	0	0	I_4
0	1	0	1	I_5
0	1	1	0	I_6
0	1	1	1	I_7
1	0	0	0	I_8
1	0	0	1	I_9
1	0	1	0	I_{10}
1	0	1	1	I_{11}
1	1	0	0	I_{12}
1	1	0	1	I_{13}
1	1	1	0	I_{14}
1	1	1	1	I_{15}



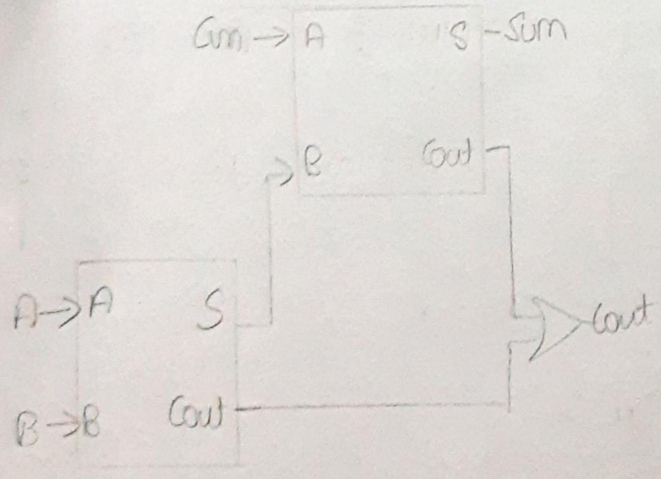
16×1 Mux Using 4x1 MUX

4. **Full Adder Using Half Adder** :; Full adder is adder which adds 3 input and produces two output. The first two inputs are A and B & third input carry C_{in}. The output is Sum & Cout. To implement full adder 2 half adder & 2 orgate is required.

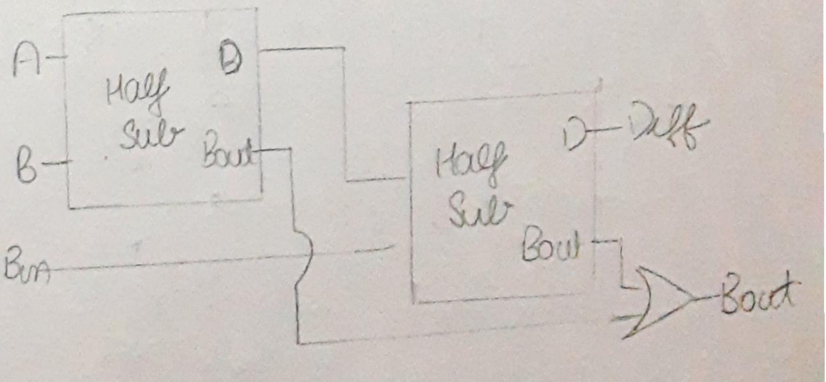
Full Sultractor using Half Subtractor :- Full subtractor is subtracto which subtracts 3 inputs and produces two output. The first two inputs are A and B and third input borrow as input. The output is B out & difference. To implement full sub 2 half sub & or gate is required

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

A	B	Bin	Diff(D)	Bout
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1



Full adder using Half adder.



Full Subtractor using Half Subtractor.