Experiment 5.

Aim: To study the architecture & pin diagrams of 8085 microprocessor.

Theory: 8086 is a 16 bit integer processor in a 40 pin, Dual Inline Packaged IC. The internal architecture of Intel 8086 is divided into 2 units:

a) Bus Interface Unit (BIU)
b) Execution Unit (EU)

I. **The Bus Interface Unit:** It provides the interface of 8086 to external memory & I/O devices via the system Bus. It performs the following functions:

- Generates the 20 bit physical address for memory access
- It fetches instructions from the memory.
- It transfers data to & from the memory & I/O.
- Maintains the 6 byte prefetch instruction queue.

BIU mainly consists of:

1. 4 segment registers
2. Instruction Pointer.
3. Prefetch queue.
4. Address Generation circuit.

a. **Code segment register (CRS):** It holds the Bus address for the code segment. All programs are sorted in CS & accused via IP.

b. **Data Segment register (DS):** It holds the Base address for the Data Segment.

c. **Stack Segment register (SS):** It hold the Base address for the Stack Segment

d. **Extra Segment Register (ES):** It holds the Base address for the Extra Segment.

Instruction Pointer :
- It is a 16 bit register. It holds offset of the next instruction in the code segment.
- It is incremented after every instruction byte is fetched.
- CS is multiplied by 10H to give 20 bit physical address of code segment
- Address of next Instruction is calculated as : CS x 10H + IP

6 Byte Pre-Fetched Queue :
- It is a 6 byte queue (FIFO)
- Gets flushed whenever a branch instruction occurs
- Fetching the next instruction (by BIU from CS) while executing the instruction is called Pipelining

Address Generation Circuit :-
Generates 20 bit physical address using segmented and offset address using the formula -

PA = SA x 10H + OA.

II. The Execution Unit (EU)
Main components of EU are General Purpose registers, ALU, Special purpose registers, Instruction Registers and Instruction Decoders. Flag / Status registers.

a. General Purpose Registers :- 8086 has 4 16 bit GPRs - Ax, Bx, Cx, Dx. These store intermediate value during execution. Each of this have two 8 bit parts (higher & lower).

1. AX Register : It holds the op & results during multiplication & division op. Also an accumulator for string
2. Bx register : It holds the memory address in Indexed Add mode
3. Cx register : It holds the count for instruction like loop, rotate, shift & string operation.
4. Dx register : Used with AX to hold 32 bit values during multiplication & division

b. Arithmetic Logic Unit (ALU) 16 bit:
It performs 8 & 16 bit arithmetic & logic operations

c. Special Purpose Registers (16 bit)

1. Stack Pointer:- Points to stack top. Stack is in stack segment, used during inst like PUSH, POP, CALL, RET, etc.

2. Base Pointer:- It holds the offset address of any location in the stack segment. Used to access random locations of stack.

3. Source Index:- It holds the offset address in Data segment during string operations.

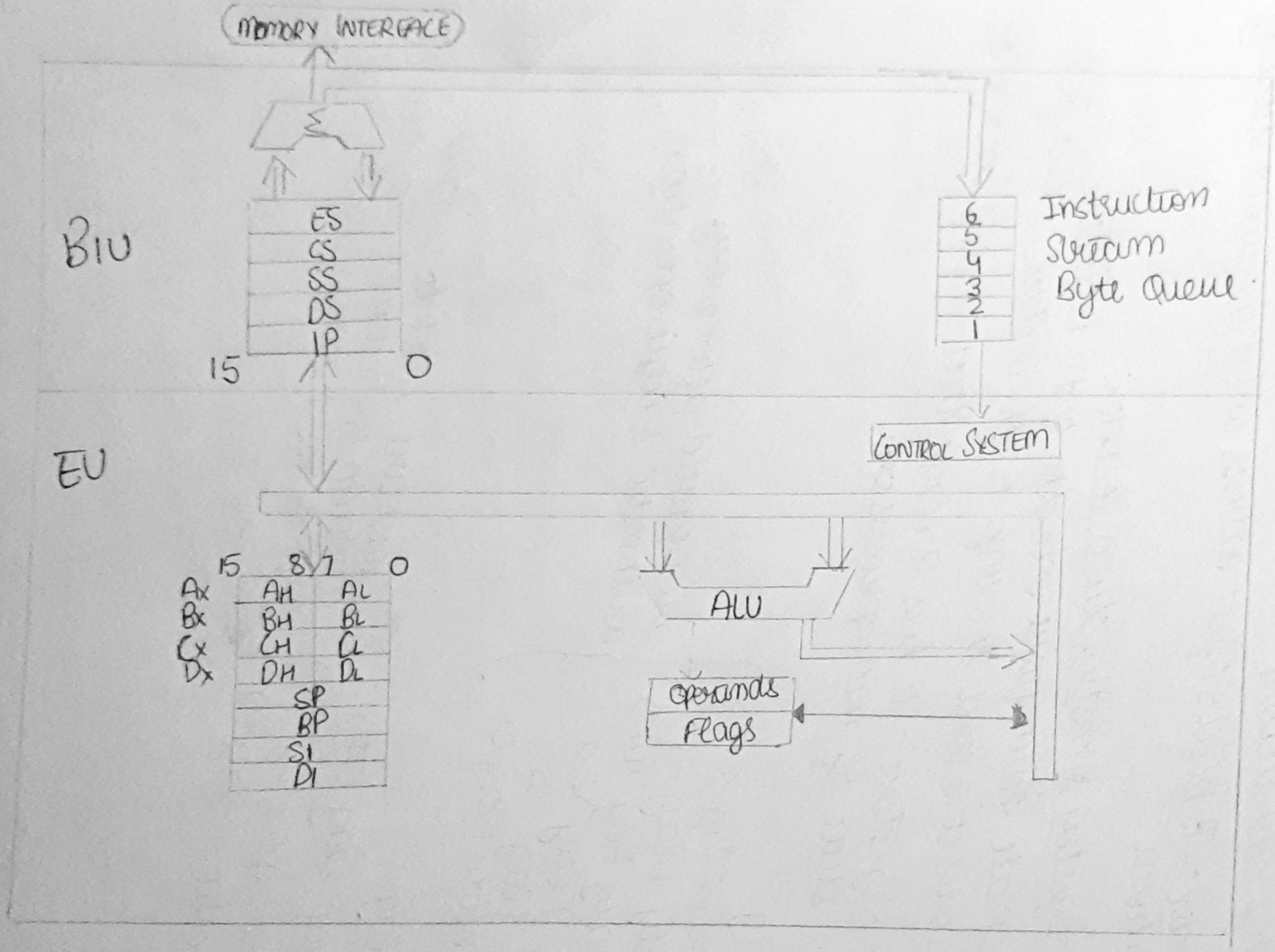
4. Destination Index:- It holds offset address in Extra segment during string operations.

d. Instruction Register & Instruction Decoder:
- EU fetches an opcode from queue into the Instr. Register.
- The decoder decodes it & sends the info to the control circuit for ex.

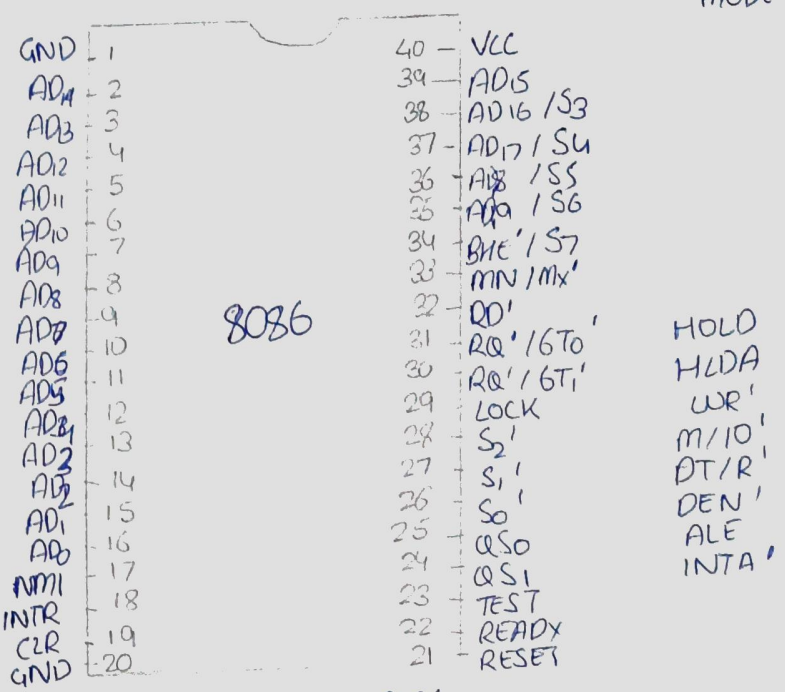
e. Flag/Status Registers:- It has 9 flags that helps change or recognise the state of microprocessor.

6 Status Flag:
a. Carry Flag (CF)
b. Parity Flag (PF)
c. Auxillary Flag (AF)
d. Zero Flag (Z)
e. Sign Flag (S)
f. Overflow Flag O
} are updated after every arithmetic & logic operation

3 Control Flag:
a. Trap flag (TF)
b. Interrupt flag (IF)
c. Direction flag (DF)
} These are used to control certain operations. They can be set or reset using control Inst.


MEMORY INTERFACE
BIU
ES
CS
SS
DS
IP
15
0
6
5
4
3
2
1
Instruction Stream Byte Queue
EU
CONTROL SYSTEM
15
8
7
0
AX
BX
CX
DX
AH
AL
BH
BL
CH
CL
DH
DL
SP
BP
SI
DI
ALU
Operands
Flags

PIN DIAGRAM



PIN DIAGRAM FOR 8086.

8086 uses a 5V DC supply for its operation. It uses 20 line address bus, 16 line data bus.

$AD_0 - AD_{15}$:- Address/Data Bus. These are low order address bus which are multiplexed with data. When transmitting memory address, AD is replaced with A and when data, then AD with D.

$A_{16} - A_{19}$:- High order address bus. These are multiplexed with status signals.

S_2, S_1, S_0 :- Status pins. These pins are active during T_4, T_1 & T_2 states and is returned to passive state access control signals.

S_2	S_1	S_0	Characteristics
0	0	0	Interrupt Acknowledge
0	0	1	Read I/O Port
0	1	0	Write I/O Port
0	1	1	Halt
1	0	0	Code Access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive State

A_{16}/S_3, A_{17}/S_4, A_{18}/S_5, A_{19}/S_6 : Specified address lines code are multiplexed with corresponding status signals.

A_{17}/S_4	A_{18}/S_5	Function
0	0	Extra Segment Access
0	1	Stack Segment Access
1	0	code Segment Access
1	1	Data Segment Access

BHE'/S7 ; Bus High Enable/Status. When T_1 is low, it is used to enable data onto the most significant half of data bus, D_8-D_{15}. 8 bit device connected to upper half of data bus use BHE (active low) signal. It is multiplexed with status signal S_7. S_7 signal is available during T_2, T_3 & T_4

RD' ; This is used for read operation. It is an active low output signal.

READY ; This is the acknowledgement from the memory or slow device that they have completed data than. It is an active high signal

INTR : Interrupt Request. This is triggered input. This is an active high signal & is synchronized internally.

NMI : Non Maskable Interrupt. This is edge triggered input which results in a type II interrupt

INTA : Interrupt Acknowledge. It is active low during T_2, T_3 & T_W of each interrupt acknowledge cycle.

MN/MX' ; Minimum/Maximum. This pin signal indicates what mode the process will operate in.

RQ'/GT1', RQ'/GT0' : Request/Grant. These pins are used by local bus masters used to force the microprocessor to release the local bus at the end of μprocessor's current bus cycle.

LOCK' ; Active low pin. It indicates that other system bus masters have not been allowed to gain control of the system bus while active

TEST' ; This is examined by a 'WAIT' instruction. If this pin goes low, execution will continue, else the processor remain idle state.

CLK ; Clock input. It provides the basic timing for the processing operations & bus control activity.

RESET ; This pin requires the μprocessor to terminate its present activity immediately.

Vcc : Power Supply (+5V DC)

GND: GROUND PIN

QS1, QS0 Queue Status. These signals indicate the status of the internal 8086 instruction queue according to the table.

QS_1	QS_0	STATUS
0	0	No operation
0	1	First byte of opcode from queue
1	0	Empty the queue
1	1	Subsequent byte from queue

DT/R: Data Transmit/Receive. It is required in minimum system that want to use an 8286 or 8287 data bus transceiver.

DEN: Data Enable: This pin provides as an output enable for 8286/8287. This pin in a min system which uses transceiver. It is active low during each memory & I/O access & for INTA cycles.

HOLD/HLDA: It indicates that another master has requested a local bus. It is an active high signal. The μprocessor receiving the HOLD request will issue HLDA (high) as an acknowledgment in middle of a T_4 or T_1 clock.

ALE: Address latch enable. ALE is provided by the μprocessor to latch the address into 8282 or 8283 address latch. It is an active high pulse during T_1 of any bus cycle. It is never floated, is always integer.

Result: The architecture & pin diagram of 8086 μprocessor was studied.