Digital System Design Quiz-1.

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1. VHDL is an acronym for Very High Speed Integrated (VHSIC) Hardware description language.

Capabilities: - It can be utilized as an exchange medium b/w chip & CAD tool users.
- Used to communicate b/w CAD & CAE tools.
- It support hierarchy; i.e interconnected component sets
- Generics and attributes are used in describing parameterized designs.
- Can be used for simulation purpose as well, no need for another language.
- Supports both synchronous & asynchronous timing models.

2. Design Units: These are the primary constructs that VHDL provides to describe an entity. There are 5 design units in VHDL:

A. Entity declaration: It specifies the name of the entity being modeled & list the set of interface ports.

Eg of Entity declaration of half adder circuit

```
entity Half_Adder is
    port (A,B : in Bit;
          Sum, Carry : out Bit);
end Half_Adder;
```

B. Architecture Body :- It specifies the details of an entity based on modelling styles such as:
i) Structural Style
ii) Dataflow style
iii) Behavorial Style
iv) Mixed Style.

Eg of architecture body using dataflow Style of modelling for Half adder circuit

```
architecture HA_df of Half_Adder is
begin
    Sum <= A xor B;
    CARRY <= A and B;
end HA_df;
```

C. Configuration Declaration: It used to select one of the possibly many architecture bodies that an entity may have, & to bind components, used to represent structure in that architecture body, to entities represented by an entity-architecture pairs.

Eg of HALF-Adder entity configuration

```
library CMOS_LIB, MY_LIB;
  configuration HA_Binding of HALF_Adder is
   for HA_Structure
      for X1 : XOR2
         use entity CMOS_LIB.XOR_GATE(DATAFLOW);
      end for;
      for A1 : AND2
           use configuration MY_LIB_AND_CONFIG;
       end for;
    end for;
  end HA_Binding;
```

D. Package Declaration: It stores the set of common declarations, such as components, types, procedures & functions.

Example: STD_LOGIC_1164, is a package that is IEEE std.

Example Declaration:

```
package Example_pack is
   type SUMMER is (MAY, JUN, AUG, SEP);
   component D_Flip-flop
       port (D, Clk : in BIT; Q, Q_bar : out bit);
   end component;
   constant Min 2 Pin_Delay : Time := 125 ns;
   function INT2bit_VEC (Int_Value : Integer)
       return bit_vector;
end example_pack;
```

E. Package body :- It is used to store the definitions of functions & procedures that were declared in corresponding package declaration.

Eg: For Example-Pack;

```
package body Example-Pack is
    function INT2BIT_VEC (Int_VALUE: INTEGER)
        return BIT_VECTOR is
    begin
        -- Behaviour
    end INT2BIT_VEC;
end Example Pack.
```

8. Different Style of Modelling in VHDL.

A. Structureal Style of modelling;

i) Interconnected components are use to specify the architecture of entity.

ii) The components are instantiated at the beging of body, and connected later using port mapping statement to the signals.

B. Dataflow Style of Modelling:

1) Concurrent assignment statement to specify the architecture of the the entity

2) Dataflow description directly implies a corresponding gate-level implementation.

C. Behavioral Style of Modelling:

i) Sequential statements are executed sequentially by a simulator.

ii) Consists of Process statements. Each process statement is a single concurrent statement that itself contains one or more sequential statements.

D. Mixed Style of modelling:-

Combination of above 3

4. Package Declaration:

A package declaration is used to store a set of common declaration like components types, Procedure & functions.

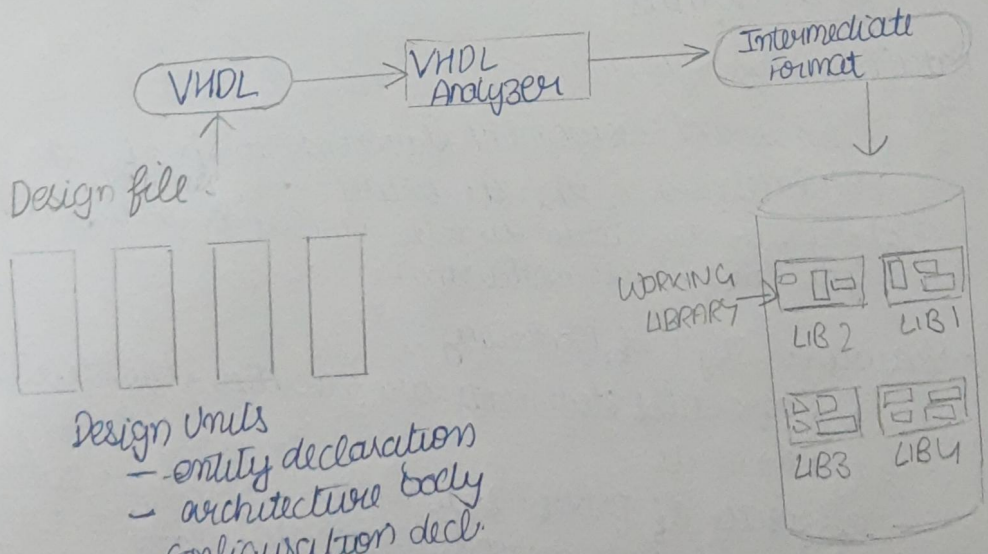
Entity Declaration:

The entity declaration specifies the name of the entity being modelled & lists the set of interface ports. Ports are signals through which the entity communications with other models in its external environment.

5. Elaboration Phase:- In this phase, the hierarchy of the entity is expanded & linked, components are bound to entities in a library, & the top level entity is built as a network of behavioral models that is ready to be simulated.

Initialization Phase:- Driving & effective values for all explicitly declared signals are computed, implicit signals are assigned values, process are executed once until they suspend & simulation time is set to 0ns.

6.



Design Units
- entity declaration
- architecture body
- configuration decl.
- package declaration
- package body

Compilation Process:

7. Variables: Temporary location; they are used to store intermediate values within 'process'.
- Locally declared; no delays; declared within process.

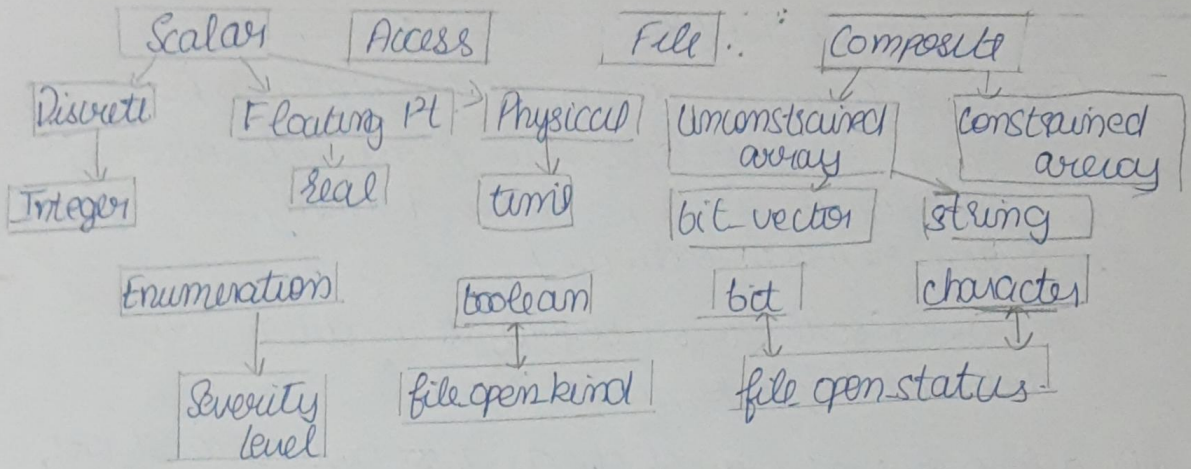
Signals: Update signal values. Run process activated by change on signal. While process is running all signals in system remain unchanged.
- They are global (before begin); delay due to wire; declared before key word begin.

8. VHDL defines several types of objects. These include constants, variables, signals & files
The types of value which can be assigned to these objects are called data types.
Same data type may be assigned to different object types. For example, a constant, a variable, & a signal can all have values which are of datatypes BIT.

Declaration of object include their object as well as the datatype of values that they can acquire.
Eg. signal Enable: BIT;

4 major categories :-

1. Scalar types :- Values belonging to these type appear in sequential order.
2. Composite types: These are composed of elements of a single type (an array type) or elements of different types.
3. Access types: These provide access to objects of a given type.
4. File-types :- These provide access to objects that contain a sequence of values of a given type.



Data types in VHDL:

Q. Subtype: A type together with a constraint. A value belongs to a subtype of a given type if it belongs to the type & satisfies the constraint; the given type is called subtype.

Example:
```
function Resolv_value (anonymous: BIT_vector) return BIT;
subtype BIT_NEW is Resolv_value BIT;
```

Constant: Constant is an object whose value can't be changed once defined for the design.

Example:
```
type weekday is (Mon, Tue, Wed, Thur, Fri);
constant StartDay : weekday := Mon;
```

10. Operators:

- NAND, NOT: These are logical operators in VHDL, NOT has the highest priority whereas NAND has the lowest priority.

NOT.

A	not A
0	1
1	0

NAND

A	B	A nand B
0	0	1
0	1	1
1	0	1
1	1	0

These work on BIT & BOOLEAN Types & arrays of these types

Syntax

```
begin
  o0 <= not i0;
end notgate
```

- <=, /= : Relational Operator

<=:- It is a relational operator indicating less than or equal to. (Operator overloading as Assignment operator).

/=:- Relational operator of inequality

- & : It is an adding operator used for concatenation of 1 dimensional array or an element type

Eg: 'C' & 'A' & 'T'

Result "CAT"

- MOD: Multiplying operator

A mod B = A - B*n for some integer N

The result is same sign as of second operand

- REM: Multiplying operation type.
  A rem B = A − (A/B)*B
  Sign of first operand.
- Abs: Gives absolute value of operand.
- **: Gives exponential value of left operand to power of right operand.