Rules:

1. See the sample solution at last page
2. Draw the circuit using pencil
3. All the lab must be handwritten
4. A margin of 1.25 inch to left and 1 inch to top, right and bottom should be given
5. The lab report must be in the same format as the given sample solution,
6. After Deadline no report should be considered as done

Failed to achieve the above mentioned rules result in the rejection of report and have to redo the report

Deadline: 4th Asoj 2080/ 21 September 2023

BIM Digital Logic Lab

1. Introduction to gates
    a. Basic gates
    b. Universal gates
        i. NOR as all possible gates
        ii. NAND as all possible gates
    c. Derived gates
    d. If F= x'(y+z)+(yz+x'y).(y+z)+xy'. Design a circuit using only NAND and NOR gates
    e. Verify De-Morgan's law using basic gates using truth table
    f. Verify Distributive law using gates with Truth table
2. K-Map Simplification
    a. Simplify the following using K-Map
    F= ABCD'+A'B'CD+ABC+A'B'C'D'+ACD+AB'C'D using NOR only
    b. Minimize the given expression using K-MAP and draw the circuit diagram using minimum number of NAND gate only
    Y=AABC+BC'D+CD'+AB'D+A'BCD+A''B'C'D
3. Combinational Circuit
    a. Using Truth table draw the circuit of Half adder, Half Subtractor
    b. Using HA construct FA with Truth table
    c. Using HS construct FS with Truth table
    d. If A= 1100 and B = 0101. Design Parallel Adder to add A and B
    e. Draw a combinational circuit that accepts 3 bit binary number and output is generated as the square of the input number

f. Draw a combinational circuit that takes 4 bit binary number as input and output is generated as gray code of the binary number
g. Design a combinational circuit for :
    i. BCD to excess 3- code converter
    ii. 4 bit odd and even parity checker
    iii. 3 bit even parity

4. Multiplexer and DeMultiplexer
    a. Design 2x1 MUX
    b. Design 4x1, 8x1 and 16x1 MUX along with block diagram and circuit diagram with truth tables
    c. Implement 8:1 MUX using 4:1 MUX
    d. Implement the following Boolean function using 8:1 MUX
    $F(A,B,C,D) = \sum(0,2,4,6,8,13,15)$
    e. Design 1x8 DeMUX using NOR gates only

5. Encoder and Decoder
    a. Draw Octal to Binary encoder
    b. Draw Hexadecimal to binary encoder
    c. Design 3:8 decoder
    d. Design 4*16 decoder using 3*8 decoder
6. SSD
    a. BCD to SSD
    b. HEX to SSD
    c. Implement (2,5,8,E) in SSD
7. Flip-Flop and Latch
    a. Draw S-R Latch with truth table and cases
    b. Draw S-R FF, D FF, JK FF, T FF along with function table, characteristic table and Excitation table
    c. Draw MS- JK FF with timing diagram
8. Counter
    a. Design 4 bit asynchronous up/down counter using T FF along with timing diagram
    b. Design MOD-13 asynchronous counter using JK FF along with timing diagram
    c. Design Decade asynchronous counter along with timing diagram
    d. Design MOD-11 synchronous counter using JK FF along with timing diagram
    e. Design 3 – Bit Synchronous up/down counter using T FF with timing diagram
    f. Design a synchronous counter which counts odd numbers from 0-7
    g. Design asynchronous and synchronous counter which counts prime number from 0 to 15.
9. Registers

a. Show the process of shifting right 10010 using with timing diagrams:
    i. PISO
    ii. SISO
b. Show the process of shifting 1011 using with timing diagrams
    i. PIPO
    ii. SIPO
c. You are provided with data bits 101101 to operate in a register which support I/O (Single bit per clock Pulse) from either side of it. Also draw timing diagram to illustrate store/retrieve operation
d. Ring and Johnson Counter with diagram and Timing diagram

10. Implement the following Combinational logic function using ROM

A1	A0	F1	F2
0	1	1	0
0	1	0	1
1	0	1	1
1	1	1	0

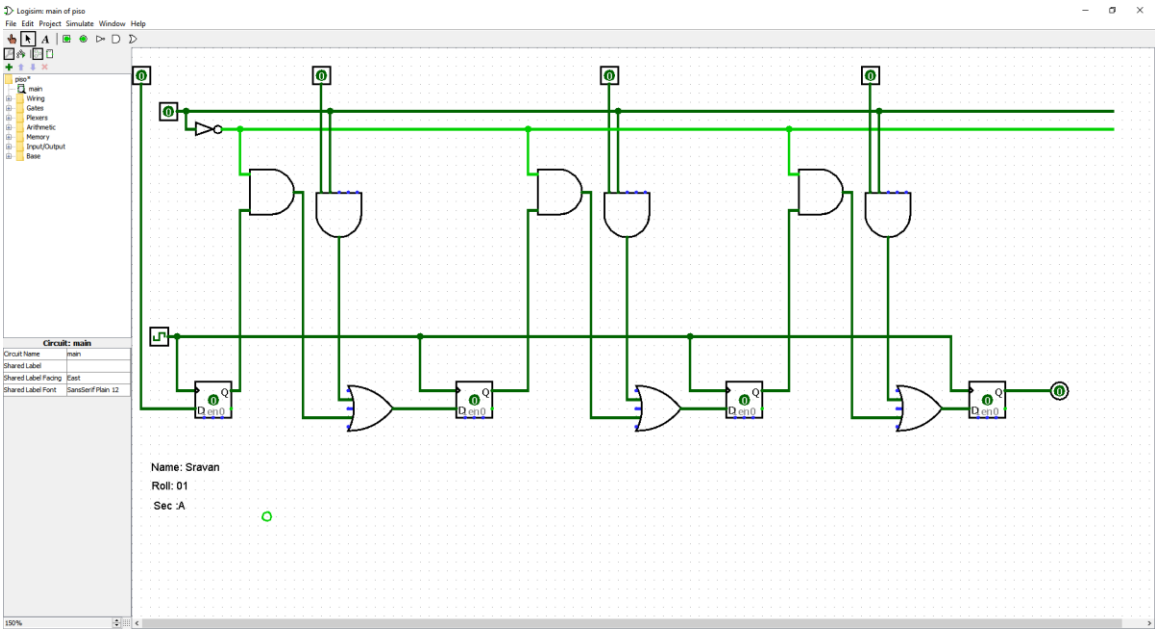
11. Design PLA circuit with given functions
    F1(A,B,C)= $\sum(3,5,6,7)$
    F2(A,B,C) =$\sum(0,2,4,7)$
    Design PLA program table also

Sample solution:

Question no: write the question here
description: write the description or related theories here

Draw the circuit diagram and truth table if there is timing diagram draw that too (by pencil)

Output from simulator



The simulator output must contain your name roll and sec

Similar for other question also