



## 1. Description

### 1.1. Project

Project Name	Casper2
Board Name	custom
Generated with:	STM32CubeMX 6.16.1
Date	02/07/2026

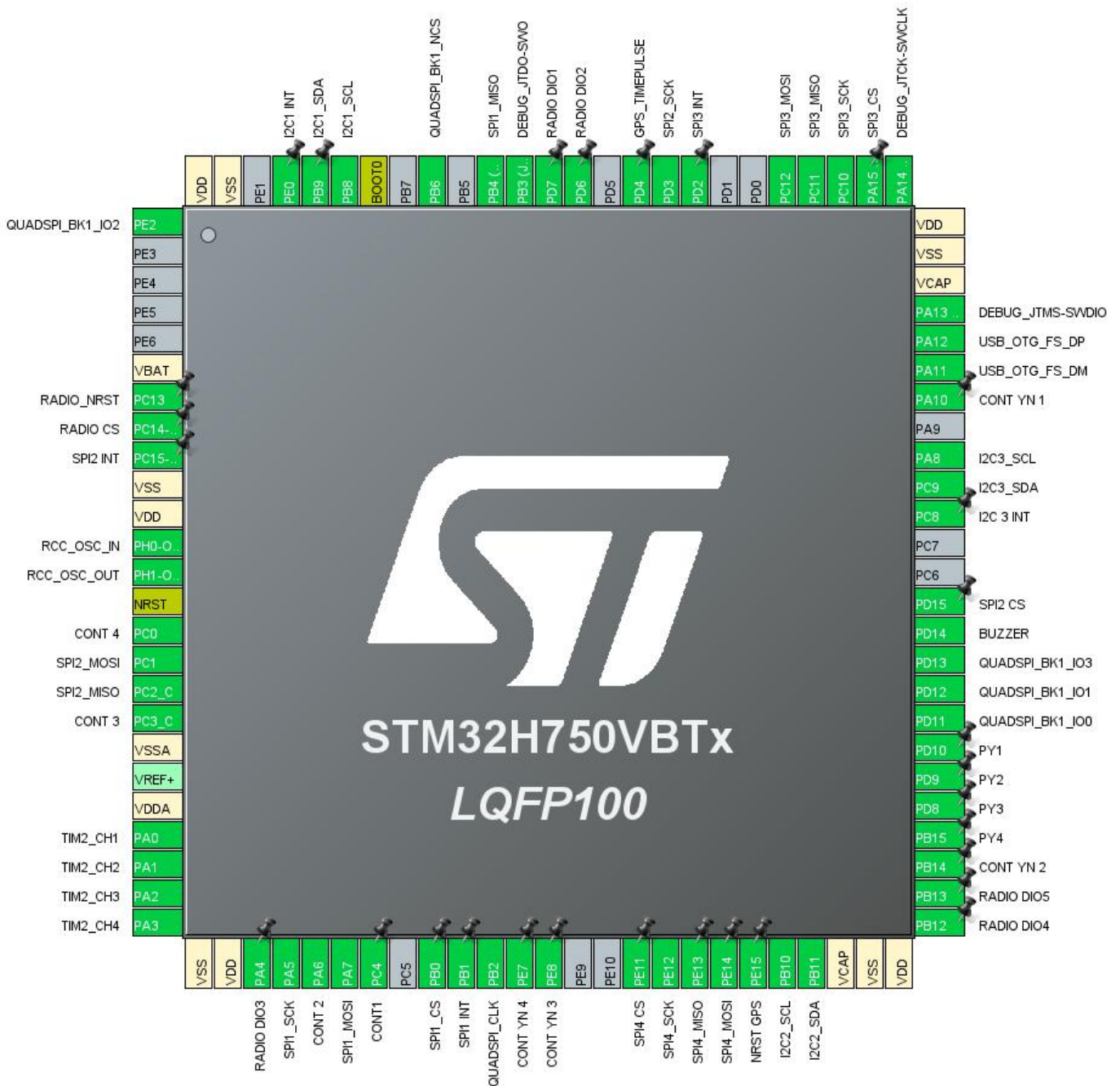
### 1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H750 Value line
MCU name	STM32H750VBTx
MCU Package	LQFP100
MCU Pin number	100

### 1.3. Core(s) information

Core(s)	ARM Cortex-M7
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## 2. Pinout Configuration



### 3. Pins Configuration

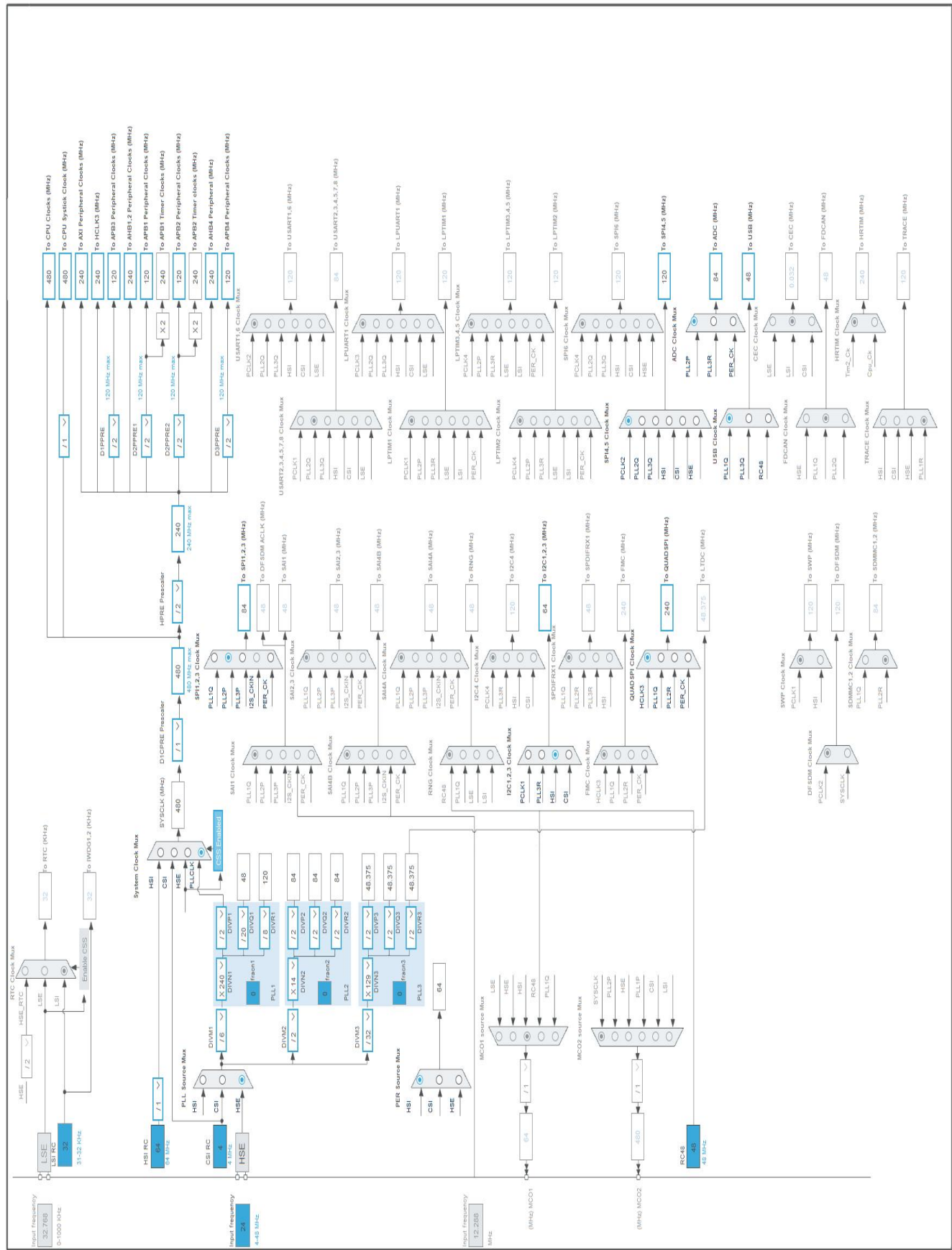
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	QUADSPI_BK1_IO2	
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Output	RADIO_NRST
8	PC14-OSC32_IN (OSC32_IN) *	I/O	GPIO_Output	RADIO CS
9	PC15-OSC32_OUT (OSC32_OUT)	I/O	GPIO_EXTI15	SPI2 INT
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0	I/O	ADC2_INP10	CONT 4
16	PC1	I/O	SPI2_MOSI	
17	PC2_C	I/O	SPI2_MISO	
18	PC3_C	I/O	ADC3_INP1	CONT 3
19	VSSA	Power		
21	VDDA	Power		
22	PA0	I/O	TIM2_CH1	
23	PA1	I/O	TIM2_CH2	
24	PA2	I/O	TIM2_CH3	
25	PA3	I/O	TIM2_CH4	
26	VSS	Power		
27	VDD	Power		
28	PA4	I/O	GPIO_EXTI4	RADIO DIO3
29	PA5	I/O	SPI1_SCK	
30	PA6	I/O	ADC1_INP3	CONT 2
31	PA7	I/O	SPI1_MOSI	
32	PC4	I/O	ADC1_INP4	CONT1
34	PB0 *	I/O	GPIO_Output	SPI1_CS
35	PB1	I/O	GPIO_EXTI1	SPI1 INT
36	PB2	I/O	QUADSPI_CLK	
37	PE7 *	I/O	GPIO_Output	CONT YN 4
38	PE8 *	I/O	GPIO_Output	CONT YN 3
41	PE11 *	I/O	GPIO_Output	SPI4 CS
42	PE12	I/O	SPI4_SCK	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
43	PE13	I/O	SPI4_MISO	
44	PE14	I/O	SPI4_MOSI	
45	PE15 *	I/O	GPIO_Output	NRST GPS
46	PB10	I/O	I2C2_SCL	
47	PB11	I/O	I2C2_SDA	
48	VCAP	Power		
49	VSS	Power		
50	VDD	Power		
51	PB12	I/O	GPIO_EXTI12	RADIO DIO4
52	PB13	I/O	GPIO_EXTI13	RADIO DIO5
53	PB14 *	I/O	GPIO_Output	CONT YN 2
54	PB15 *	I/O	GPIO_Output	PY4
55	PD8 *	I/O	GPIO_Output	PY3
56	PD9 *	I/O	GPIO_Output	PY2
57	PD10 *	I/O	GPIO_Output	PY1
58	PD11	I/O	QUADSPI_BK1_IO0	
59	PD12	I/O	QUADSPI_BK1_IO1	
60	PD13	I/O	QUADSPI_BK1_IO3	
61	PD14	I/O	TIM4_CH3	BUZZER
62	PD15 *	I/O	GPIO_Output	SPI2 CS
65	PC8 *	I/O	GPIO_Output	I2C 3 INT
66	PC9	I/O	I2C3_SDA	
67	PA8	I/O	I2C3_SCL	
69	PA10 *	I/O	GPIO_Output	CONT YN 1
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
72	PA13 (JTMS/SWDIO)	I/O	DEBUG_JTMS-SWDIO	
73	VCAP	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14 (JTCK/SWCLK)	I/O	DEBUG_JTCK-SWCLK	
77	PA15 (JTDI) *	I/O	GPIO_Output	SPI3_CS
78	PC10	I/O	SPI3_SCK	
79	PC11	I/O	SPI3_MISO	
80	PC12	I/O	SPI3_MOSI	
83	PD2	I/O	GPIO_EXTI2	SPI3 INT
84	PD3	I/O	SPI2_SCK	
85	PD4 *	I/O	GPIO_Input	GPS_TIMEPULSE
87	PD6	I/O	GPIO_EXTI6	RADIO DIO2

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
88	PD7	I/O	GPIO_EXTI7	RADIO DIO1
89	PB3 (JTDO/TRACESWO)	I/O	DEBUG_JTDO-SWO	
90	PB4 (NJTRST)	I/O	SPI1_MISO	
92	PB6	I/O	QUADSPI_BK1_NCS	
94	BOOT0	Boot		
95	PB8	I/O	I2C1_SCL	
96	PB9	I/O	I2C1_SDA	
97	PE0	I/O	GPIO_EXTI0	I2C1 INT
99	VSS	Power		
100	VDD	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H750 Value line
MCU	STM32H750VBTx
Datasheet	DS12556_Rev6

### 1.2. Parameter Selection

Temperature	25
Vdd	3.0

### 1.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1



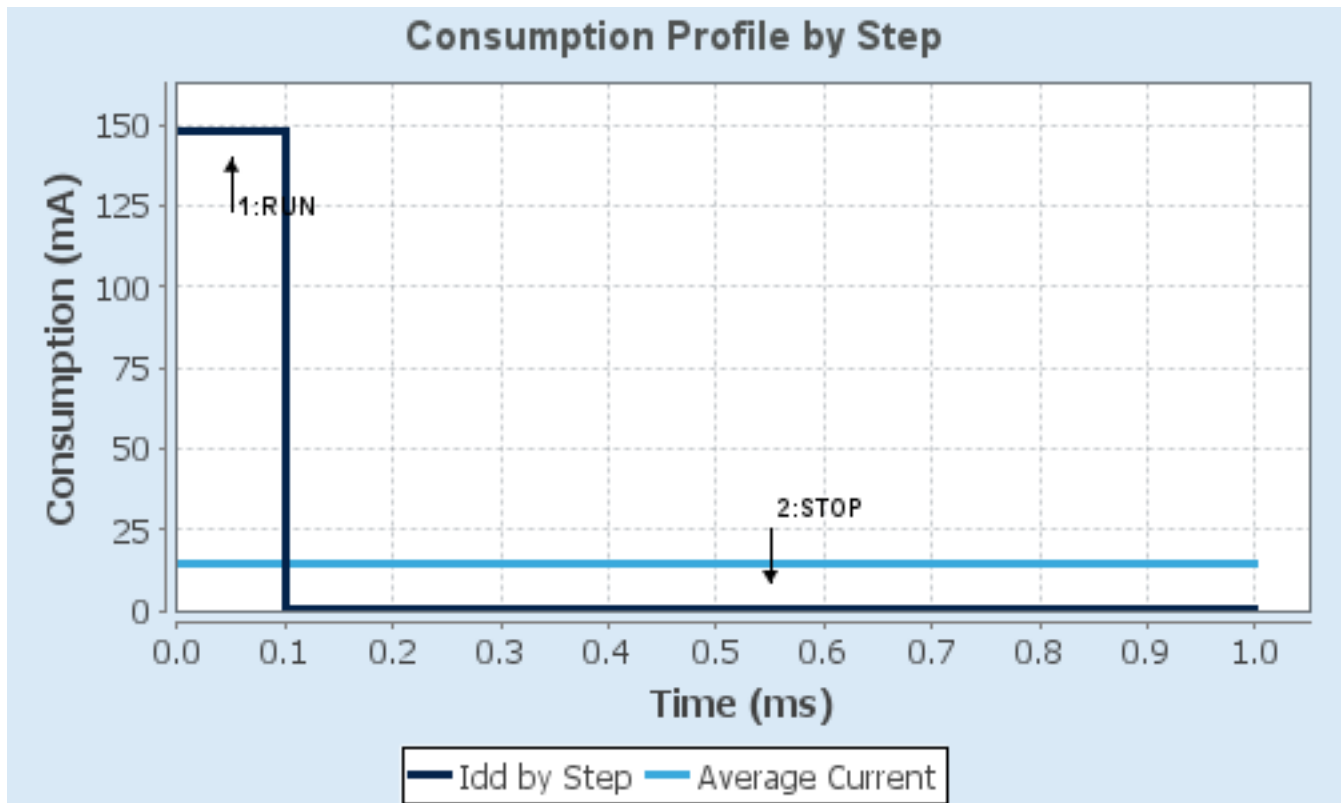
#### 1.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.0	3.0
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	VOS0: Scale0-High	SVOS5: System-Scale5
<b>D1 Mode</b>	DRUN/CRUN	DSTANDBY
<b>D2 Mode</b>	DRUN	DSTANDBY
<b>D3 Mode</b>	DRUN	DSTOP
<b>Fetch Type</b>	ITCM	NA
<b>CPU Frequency</b>	480 MHz	0 Hz
<b>Clock Configuration</b>	HSE BYP PLL	Flash-OFF
<b>Clock Source Frequency</b>	24 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	148 mA	150 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	1027.0	0.0
<b>Ta Max</b>	105.02	124.98
<b>Category</b>	In DS Table	In DS Table

#### 1.5. Results

Sequence Time	1 ms	Average Current	14.94 mA
Battery Life	1 day, 17 hours	Average DMIPS	1027.2001 DMIPS

#### 1.6. Chart



## 2. Software Project

### 2.1. Project Settings

Name	Value
Project Name	Casper2
Project Folder	E:\C.A.S.P.E.R\C.A.S.P.E.R Flight Software V2\Casper 2 flight
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_H7 V1.12.1
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_ADC1_Init	ADC1
4	MX_ADC2_Init	ADC2
5	MX_ADC3_Init	ADC3
6	MX_I2C1_Init	I2C1
7	MX_I2C2_Init	I2C2
8	MX_QUADSPI_Init	QUADSPI
9	MX_SPI1_Init	SPI1
10	MX_SPI2_Init	SPI2
11	MX_SPI4_Init	SPI4

Rank	Function Name	Peripheral Instance Name
12	MX_TIM2_Init	TIM2
13	MX_CRC_Init	CRC
14	MX_TIM4_Init	TIM4
15	MX_I2C3_Init	I2C3
16	MX_SPI3_Init	SPI3
17	MX_USB_DEVICE_Init	USB_DEVICE

### 3. Peripherals and Middlewares Configuration

#### 3.1. ADC1

**IN3: IN3 Single-ended**

**IN4: IN4 Single-ended**

##### 3.1.1. Parameter Settings:

##### **ADCs\_Common\_Settings:**

Mode Independent mode

##### **ADC\_Settings:**

Clock Prescaler

**Asynchronous clock mode divided by 2 \***

Resolution

ADC 16-bit resolution

Scan Conversion Mode

Disabled

Continuous Conversion Mode

Disabled

Discontinuous Conversion Mode

Disabled

End Of Conversion Selection

End of single conversion

Overrun behaviour

Overrun data preserved

Left Bit Shift

No bit shift

Conversion Data Management Mode

Regular Conversion data stored in DR register only

Low Power Auto Wait

Disabled

##### **ADC\_Regular\_ConversionMode:**

Enable Regular Conversions

Enable

Enable Regular Oversampling

Disable

Oversampling Ratio

1

Number Of Conversion

1

External Trigger Conversion Source

Regular Conversion launched by software

External Trigger Conversion Edge

None

Rank

1

Channel

Channel 3

Sampling Time

1.5 Cycles

Offset Number

No offset

Offset Signed Saturation

Disable

##### **ADC\_Injected\_ConversionMode:**

Enable Injected Conversions

Disable

##### **Analog Watchdog 1:**

Enable Analog WatchDog1 Mode

false

##### **Analog Watchdog 2:**

Enable Analog WatchDog2 Mode

false

##### **Analog Watchdog 3:**

Enable Analog WatchDog3 Mode

false

## 3.2. ADC2

### IN10: IN10 Single-ended

#### 3.2.1. Parameter Settings:

##### ADCs\_Common\_Settings:

Mode Independent mode

##### ADC\_Settings:

Clock Prescaler

**Asynchronous clock mode divided by 2 \***

Resolution

ADC 16-bit resolution

Scan Conversion Mode

Disabled

Continuous Conversion Mode

Disabled

Discontinuous Conversion Mode

Disabled

End Of Conversion Selection

End of single conversion

Overrun behaviour

Overrun data preserved

Left Bit Shift

No bit shift

Conversion Data Management Mode

Regular Conversion data stored in DR register only

Low Power Auto Wait

Disabled

##### ADC\_Regular\_ConversionMode:

Enable Regular Conversions

Enable

Enable Regular Oversampling

Disable

Oversampling Ratio

1

Number Of Conversion

1

External Trigger Conversion Source

Regular Conversion launched by software

External Trigger Conversion Edge

None

Rank

1

Channel

Channel 10

Sampling Time

1.5 Cycles

Offset Number

No offset

Offset Signed Saturation

Disable

##### ADC\_Injected\_ConversionMode:

Enable Injected Conversions

Disable

##### Analog Watchdog 1:

Enable Analog WatchDog1 Mode

false

##### Analog Watchdog 2:

Enable Analog WatchDog2 Mode

false

##### Analog Watchdog 3:

Enable Analog WatchDog3 Mode

false

### 3.3. ADC3

#### IN1: IN1 Single-ended

##### 3.3.1. Parameter Settings:

###### **ADC\_Settings:**

Resolution	ADC 16-bit resolution
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
End Of Conversion Selection	End of single conversion
Overrun behaviour	Overrun data preserved
Left Bit Shift	No bit shift
Conversion Data Management Mode	Regular Conversion data stored in DR register only
Low Power Auto Wait	Disabled

###### **ADC\_Regular\_ConversionMode:**

Enable Regular Conversions	Enable
Enable Regular Oversampling	Disable
Oversampling Ratio	1
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
<u>Rank</u>	1
Channel	Channel 1
Sampling Time	1.5 Cycles
Offset Number	No offset
Offset Signed Saturation	Disable

###### **ADC\_Injected\_ConversionMode:**

Enable Injected Conversions	Disable
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###### **Analog Watchdog 1:**

Enable Analog WatchDog1 Mode	false
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###### **Analog Watchdog 2:**

Enable Analog WatchDog2 Mode	false
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###### **Analog Watchdog 3:**

Enable Analog WatchDog3 Mode	false
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### 3.4. CORTEX\_M7

### 3.4.1. Parameter Settings:

#### Speculation default mode Settings:

Speculation default mode **Enabled \***

#### Cortex Interface Settings:

CPU ICache Disabled

CPU DCache Disabled

#### Cortex Memory Protection Unit Control Settings:

MPU Control Mode Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers

#### Cortex Memory Protection Unit Region 0 Settings:

MPU Region Enabled

MPU Region Base Address **0x0 \***

MPU Region Size 4GB

MPU SubRegion Disable **0x87 \***

MPU TEX field level level 0

MPU Access Permission ALL ACCESS NOT PERMITTED

MPU Instruction Access DISABLE

MPU Shareability Permission ENABLE

MPU Cacheable Permission DISABLE

MPU Bufferable Permission DISABLE

#### Cortex Memory Protection Unit Region 1 Settings:

MPU Region Disabled

#### Cortex Memory Protection Unit Region 2 Settings:

MPU Region Disabled

#### Cortex Memory Protection Unit Region 3 Settings:

MPU Region Disabled

#### Cortex Memory Protection Unit Region 4 Settings:

MPU Region Disabled

#### Cortex Memory Protection Unit Region 5 Settings:

MPU Region Disabled

#### Cortex Memory Protection Unit Region 6 Settings:

MPU Region Disabled

#### Cortex Memory Protection Unit Region 7 Settings:

MPU Region Disabled

#### Cortex Memory Protection Unit Region 8 Settings:

MPU Region Disabled

#### Cortex Memory Protection Unit Region 9 Settings:

MPU Region Disabled



#### **Cortex Memory Protection Unit Region 10 Settings:**

MPU Region Disabled

#### **Cortex Memory Protection Unit Region 11 Settings:**

MPU Region Disabled

#### **Cortex Memory Protection Unit Region 12 Settings:**

MPU Region Disabled

#### **Cortex Memory Protection Unit Region 13 Settings:**

MPU Region Disabled

#### **Cortex Memory Protection Unit Region 14 Settings:**

MPU Region Disabled

#### **Cortex Memory Protection Unit Region 15 Settings:**

MPU Region Disabled

### **3.5. CRC**

**mode: Activated**

#### **3.5.1. Parameter Settings:**

##### **Basic Parameters:**

Default Polynomial State Enable

Default Init Value State Enable

##### **Advanced Parameters:**

Input Data Inversion Mode None

Output Data Inversion Mode Disable

Input Data Format Bytes

### **3.6. DEBUG**

**Debug: Trace Asynchronous Sw**

### **3.7. I2C1**

**I2C: I2C**

#### **3.7.1. Parameter Settings:**

##### **Timing configuration:**

Custom Timing Disabled

I2C Speed Mode Standard Mode

I2C Speed Frequency (KHz) 100

Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

**Slave Features:**

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

### 3.8. I2C2

#### I2C: I2C

##### 3.8.1. Parameter Settings:

**Timing configuration:**

Custom Timing	Disabled
I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

**Slave Features:**

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

### 3.9. I2C3

#### I2C: I2C

##### 3.9.1. Parameter Settings:

**Timing configuration:**

Custom Timing	Disabled
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I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10707DBC

#### **Slave Features:**

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

### **3.10. MEMORYMAP**

**mode: Activated**

### **3.11. PWR**

**Power Voltage Detector In: Power Voltage Detector In (Internal analog voltage)**

#### **3.11.1. Parameter Settings:**

##### **Programmable\_Voltage\_Detector\_Settings:**

PVD detection Level	<b>PWR PVD LEVEL 6 (2.85 V) *</b>
PWR PVD Mode	<b>External Interrupt Mode with Rising/Falling edge trigger detection *</b>

### **3.12. QUADSPI**

**QuadSPI Mode: Bank1 with Quad SPI Lines**

#### **3.12.1. Parameter Settings:**

##### **General Parameters:**

Clock Prescaler	255
Fifo Threshold	1
Sample Shifting	No Sample Shifting
Flash Size	1
Chip Select High Time	1 Cycle
Clock Mode	Low

Flash ID	Flash ID 1
Dual Flash	Disabled

### 3.13. RCC

#### High Speed Clock (HSE): Crystal/Ceramic Resonator

##### 3.13.1. Parameter Settings:

###### Power Parameters:

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

###### RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
CSI Calibration Value	32
HSI Calibration Value	64

###### System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	4 WS (5 CPU cycle)
Product revision	rev.V

###### PLL range Parameters:

PLL1 clock Input range	Between 4 and 8 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	MEDIUM VCO range

### 3.14. SPI1

#### Mode: Full-Duplex Master

##### 3.14.1. Parameter Settings:

###### Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

###### Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	<b>42.0 MBits/s *</b>

Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge
<b>Advanced Parameters:</b>	
CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

### 3.15. SPI2

#### Mode: Full-Duplex Master

##### 3.15.1. Parameter Settings:

###### Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

###### Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	<b>42.0 Mbits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

###### Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable

Master Keep Io State  
IO Swap

Master Keep Io State Disable  
Disabled

### 3.16. SPI3

#### Mode: Full-Duplex Master

##### 3.16.1. Parameter Settings:

###### Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

###### Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	<b>42.0 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

###### Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

### 3.17. SPI4

#### Mode: Full-Duplex Master

##### 3.17.1. Parameter Settings:

###### Basic Parameters:

Frame Format	Motorola
Data Size	4 Bits
First Bit	MSB First

**Clock Parameters:**

Prescaler (for Baud Rate)	2
Baud Rate	<b>60.0 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

**Advanced Parameters:**

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 01 Data
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

### 3.18. SYS

**Timebase Source: SysTick**

### 3.19. TIM2

**Channel1: PWM Generation CH1**

**Channel2: PWM Generation CH2**

**Channel3: PWM Generation CH3**

**Channel4: PWM Generation CH4**

#### 3.19.1. Parameter Settings:

**Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

**Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

**Clear Input:**

Clear Input Source	Disable
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### PWM Generation Channel 1:

Mode PWM mode 1

Pulse (32 bits value)	0
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Output compare preload	Enable
------------------------	--------

Fast Mode Disable

CH Polarity High

### PWM Generation Channel 2:

Mode PWM mode 1

Pulse (32 bits value)	0
-----------------------	---

Output compare preload	Enable
------------------------	--------

Fast Mode Disable

CH Polarity High

### PWM Generation Channel 3:

Mode PWM mode 1

Pulse (32 bits value)	0
-----------------------	---

Output compare preload	Enable
------------------------	--------

Fast Mode Disable

CH Polarity High

### PWM Generation Channel 4:

Mode PWM mode 1

Pulse (32 bits value)	0
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Output compare preload	Enable
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Fast Mode Disable

CH Polarity High

### 3.20. TIM4

### Channel3: PWM Generation CH3

### 3.20.1. Parameter Settings:

### Counter Settings:

Prescaler (PSC - 16 bits value)	0
---------------------------------	---

Counter Mode Up

Counter Period (AutoReload Register - 16 bits value ) 65535

Internal Clock Division (CKD) No Division

auto-reload preload	Disable
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### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
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Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
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**Clear Input:**

Clear Input Source	Disable
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**PWM Generation Channel 3:**

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

### 3.21. USB\_OTG\_FS

**Mode: Device\_Only**

3.21.1. Parameter Settings:

Speed	Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Low power	Disabled
Battery charging	Disabled
Link Power Management	Disabled
Use dedicated end point 1 interrupt	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

### 3.22. USB\_DEVICE

**Class For FS IP: Communication Device Class (Virtual Port Com)**

3.22.1. Parameter Settings:

**Basic Parameters:**

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message
USBD_LPM_ENABLED (Link Power Management)	1: Link Power Management supported

**Class Parameters:**

USB CDC Rx Buffer Size	2048
USB CDC Tx Buffer Size	2048

### 3.22.2. Device Descriptor:

#### **Device Descriptor:**

VID (Vendor Identifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

#### **Device Descriptor FS:**

PID (Product Identifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

\* User modified value

## 4. System Configuration

### 4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA6	ADC1_INP3	Analog mode	No pull-up and no pull-down	n/a	CONT 2
	PC4	ADC1_INP4	Analog mode	No pull-up and no pull-down	n/a	CONT1
ADC2	PC0	ADC2_INP10	Analog mode	No pull-up and no pull-down	n/a	CONT 4
ADC3	PC3_C	ADC3_INP1	Analog mode	No pull-up and no pull-down	n/a	CONT 3
DEBUG	PA13 (JTMS/SWDIO)	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	
	PB3 (JTDO/TRACESWO)	DEBUG_JTDO-SWO	n/a	n/a	n/a	
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB9	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PB11	I2C2_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
I2C3	PC9	I2C3_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Low	
	PA8	I2C3_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Low	
QUADSPI	PE2	QUADSPI_BK1_IO2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB2	QUADSPI_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD11	QUADSPI_BK1_IO0	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD12	QUADSPI_BK1_IO1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	QUADSPI_BK1_IO3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB6	QUADSPI_BK1_NCS	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-	RCC_OSC_OUT	n/a	n/a	n/a	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	OSC_OUT (PH1)					
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB4 (NJTRST)	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI2	PC1	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC2_C	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD3	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI3	PC10	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC11	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PC12	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
SPI4	PE12	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE13	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE14	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA2	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	TIM2_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	BUZZER
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RADIO_NRST
	PC14-OSC32_IN (OSC32_IN)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	RADIO CS
	PC15-OSC32_OUT	GPIO_EXTI15	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	SPI2 INT
	PA4	GPIO_EXTI4	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	RADIO DIO3
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI1_CS
	PB1	GPIO_EXTI1	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	SPI1 INT
	PE7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CONT YN 4
	PE8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CONT YN 3
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI4 CS
	PE15	GPIO_Output	Output Push Pull	<b>Pull-up *</b>	Low	NRST GPS
	PB12	GPIO_EXTI12	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	RADIO DIO4

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	RADIO DIO5
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CONT YN 2
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PY4
	PD8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PY3
	PD9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PY2
	PD10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	PY1
	PD15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI2 CS
	PC8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	I2C 3 INT
	PA10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	CONT YN 1
	PA15 (JTDI)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SPI3_CS
	PD2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	SPI3 INT
	PD4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPS_TIMEPULSE
	PD6	GPIO_EXTI6	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	RADIO DIO2
	PD7	GPIO_EXTI7	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	RADIO DIO1
	PE0	GPIO_EXTI0	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	I2C1 INT

#### 4.2. DMA configuration

nothing configured in DMA service

#### 4.3. BDMA configuration

nothing configured in DMA service

#### 4.4. MDMA configuration

nothing configured in DMA service

## 4.5. NVIC configuration

### 4.5.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
USB On The Go FS End Point 1 Out global interrupt	true	0	0
USB On The Go FS End Point 1 In global interrupt	true	0	0
USB On The Go FS global interrupt	true	0	0
PVD and AVD interrupts through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
EXTI line0 interrupt	unused		
EXTI line1 interrupt	unused		
EXTI line2 interrupt	unused		
EXTI line4 interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
EXTI line[9:5] interrupts	unused		
TIM2 global interrupt	unused		
TIM4 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
SPI2 global interrupt	unused		
EXTI line[15:10] interrupts	unused		
SPI3 global interrupt	unused		
I2C3 event interrupt	unused		
I2C3 error interrupt	unused		
FPU global interrupt	unused		
SPI4 global interrupt	unused		
QUADSPI global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
HSEM1 global interrupt		unused	
ADC3 global interrupt		unused	

#### 4.5.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	true
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
USB On The Go FS End Point 1 Out global interrupt	false	true	true
USB On The Go FS End Point 1 In global interrupt	false	true	true
USB On The Go FS global interrupt	false	true	true

\* User modified value

## 5. System Views

### 5.1. Category view

#### 5.1.1. Current

Category view

Power Domain view

Choose filters ...

... by Power Domain

☐ D1

☐ D2

☐ D3

☒ None

Middleware




USB\_DEVICE ✓

System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Trace and Debug	Power and Thermal	Other
BDMA	ADC1 ✓	TIM2 ✓	I2C1 ✓			CRC ✓	DEBUG ✓	PWR ✓	
CORTEX_M7 ✓	ADC2 ✓	TIM4 ✓	I2C2 ✓						
DMA	ADC3 ✓		I2C3 ✓						
GPIO ✓			QUADSPI ✓						
MDMA			SP1 ✓						
IVIC ✓			SPI2 ✓						
RCC ✓			SPI3 ✓						
SYS ✓			SPI4 ✓						
			USB_FS ✓						



### 5.1.2. Without filters

Category view   Power Domain view

   Choose filters ...

... by Power Domain

☐ D1   ☐ D2   ☐ D3   ☒ None

#### Middleware

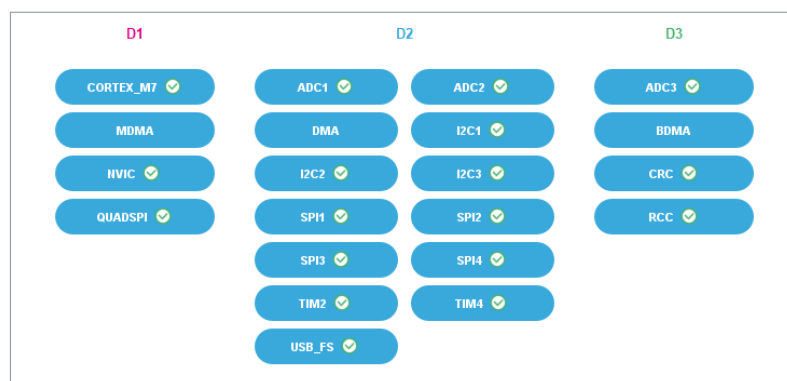
USB\_DEVICE ✓

System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing	Trace and Debug	Power and Thermal	Other
BDMA	ADC1 ✓	TIM2 ✓	I2C1 ✓			CRC ✓	DEBUG ✓	PWR ✓	
CORTEX_M7 ✓	ADC2 ✓	TIM4 ✓	I2C2 ✓						
DMA	ADC3 ✓		I2C3 ✓						
GPIO ✓			QUADSPI ✓						
MDMA			SP1 ✓						
IVIC ✓			SPI2 ✓						
RCC ✓			SPI3 ✓						
SYS ✓			SPI4 ✓						
			USB_FS ✓						

## 5.2. Power Domain view

Category view

Power Domain view



## 6. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32h7_bsd1.zip">https://www.st.com/resource/en/bsdl_model/stm32h7_bsd1.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip">https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip</a>
System View Description	<a href="https://www.st.com/resource/en/svd/stm32h7-svd.zip">https://www.st.com/resource/en/svd/stm32h7-svd.zip</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf</a>
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Brochures	<a href="https://www.st.com/resource/en/brochure/brstm32h7.pdf">https://www.st.com/resource/en/brochure/brstm32h7.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32nucleo.pdf">https://www.st.com/resource/en/flyer/flstm32nucleo.pdf</a>
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Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32h7rs.pdf">https://www.st.com/resource/en/flyer/flstm32h7rs.pdf</a>
Security Bulletin	<a href="https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf">https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-tn1489stpsirt-physical-attacks-on-stm32-and-stm32cube-firmware-stmicroelectronics.pdf</a>
Security Bulletin	<a href="https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-protection-statement-for-stmicroelectronics-certified-products-">https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-protection-statement-for-stmicroelectronics-certified-products-</a>

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