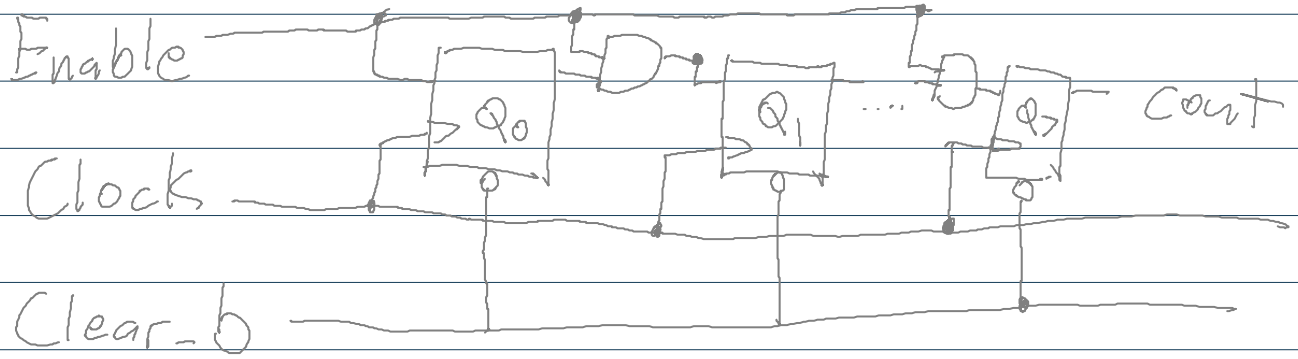
Lab 5

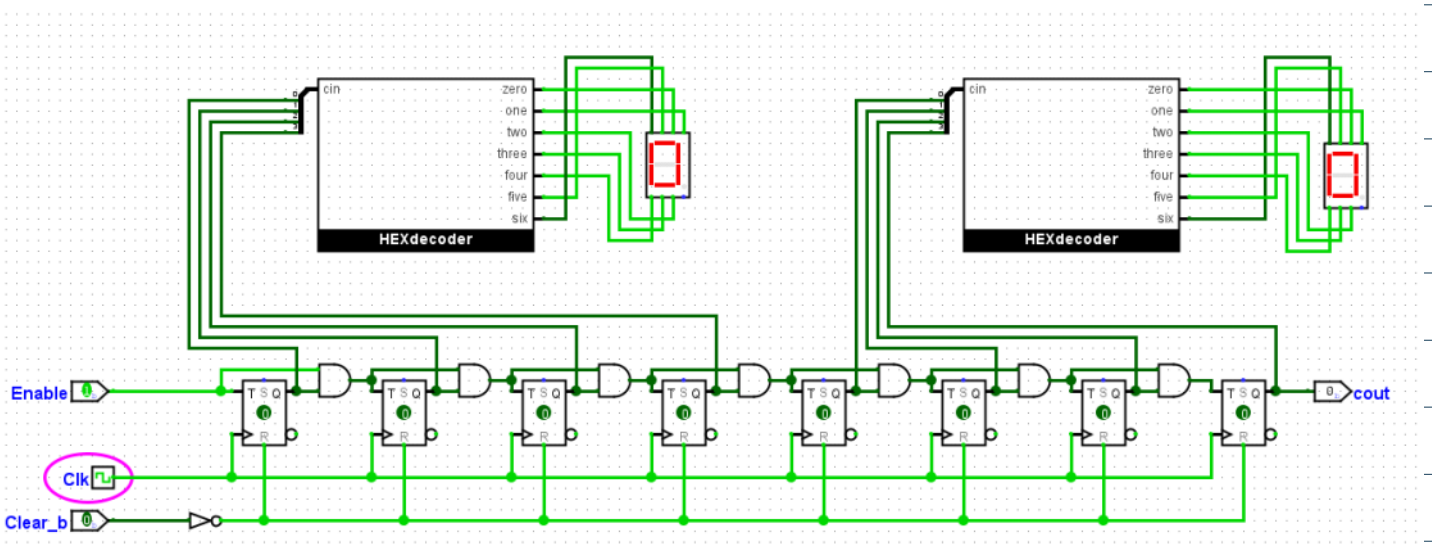
June 14, 2021 8:12 PM

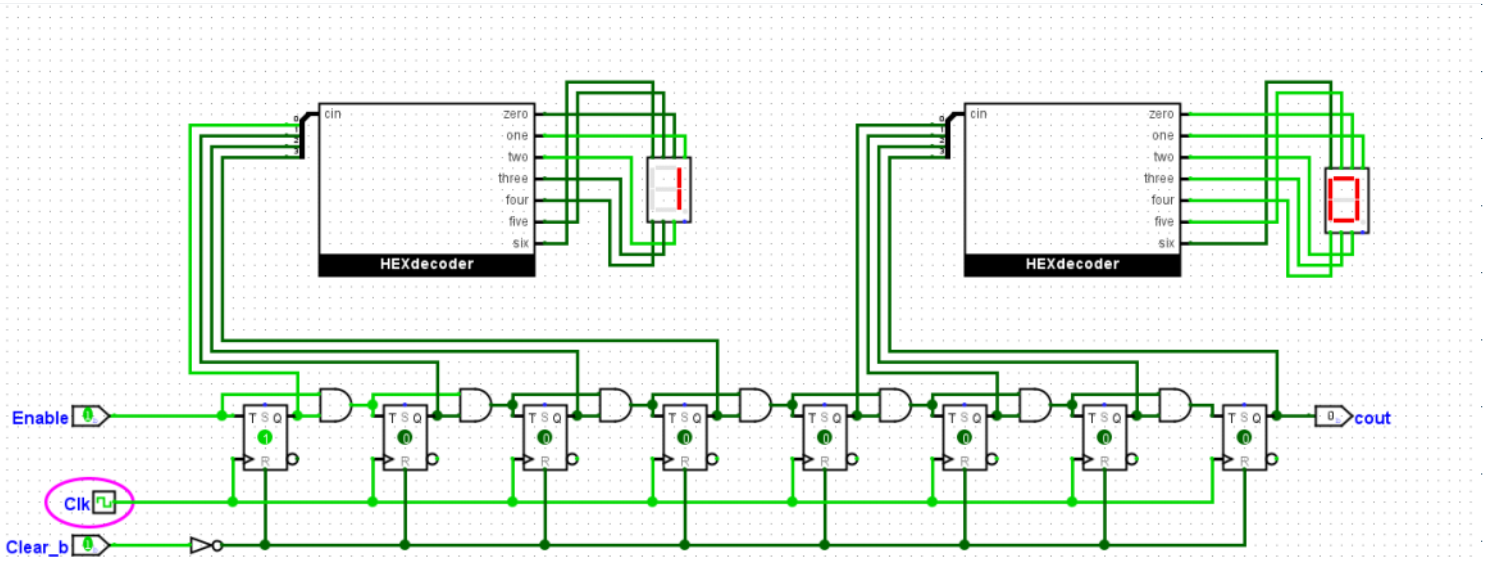
Part I

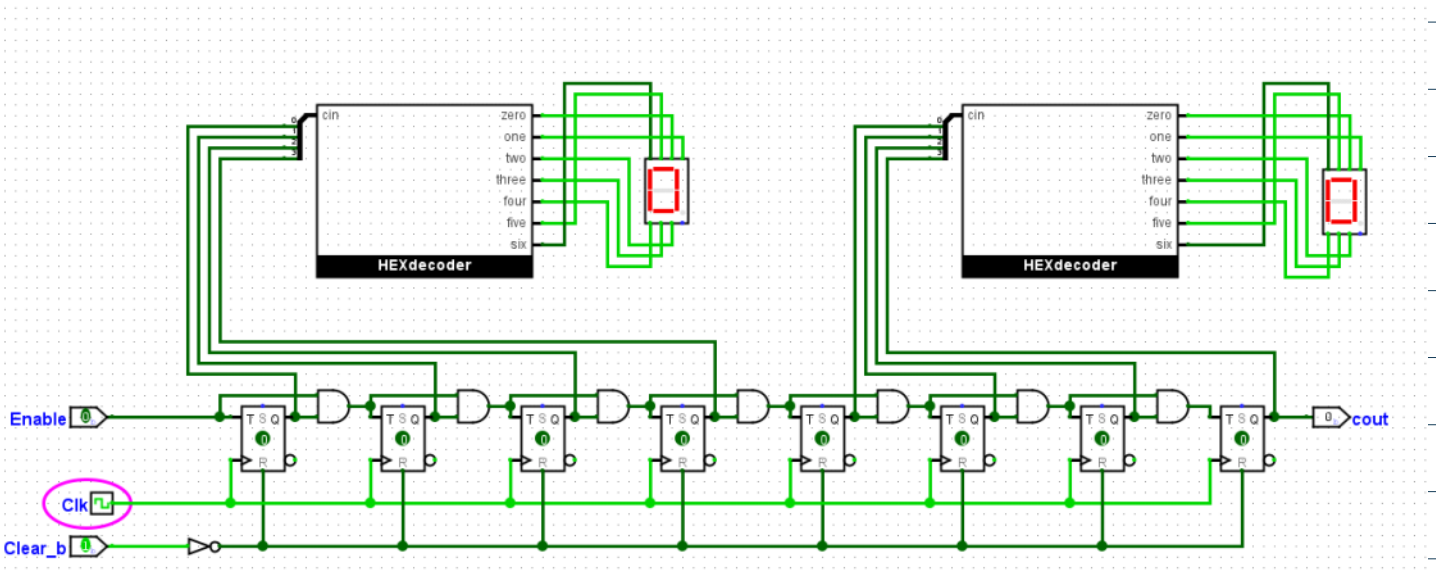
1. Schematic



5. Tests







Part II

1. Max value check

We know the "On Action Overflow" is either wrap around or continue counting, so whenever you try to count up from 1111 (or down from 0000) the register will automatically restart the counter to 0000 (or 1111 with the opposite scenario)

2. Count 0-9

Change the inputs into the AND gate at the end such that it only outputs 1 when the 4 bits order from most to least significant are: 1001 (decimal 9 in binary)

3. Action on Overflow

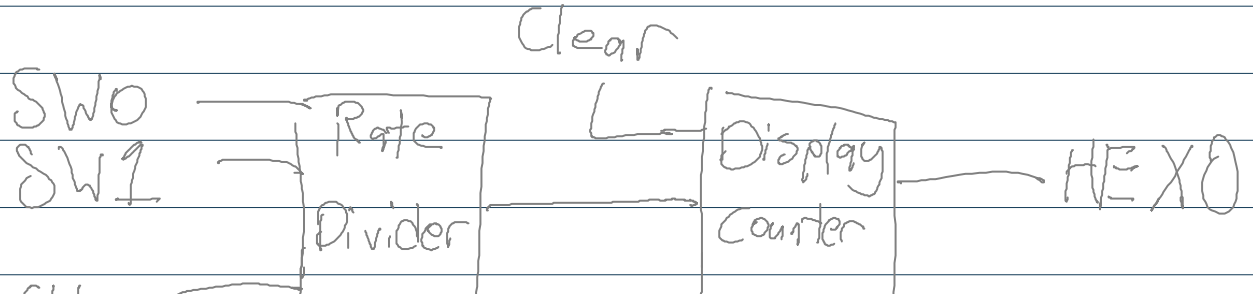
As far as I see "Wrap Around" and "Continue Counting" do the same thing, if the stored value is 1111 and you count up it will restart to 0, and if the value is 0000 and you count down, it will wrap to 0000.

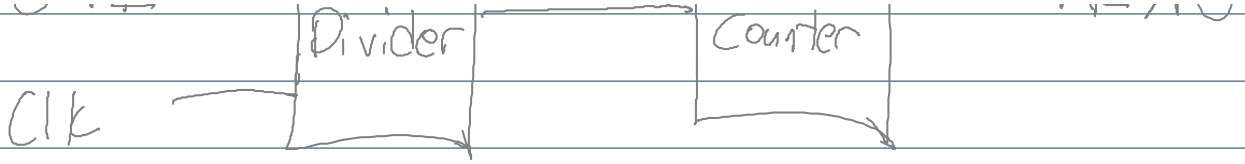
"Stay at Value" is self-explanatory, if you count down from 0000 it won't change and similarly with 1111
"~~Load next value" also makes sense: Upon the next high clock edge on overflowing, the next value will~~ be loaded into the register.

50 million clock cycles

Using basic math, we know $\lceil \log_2(x) \rceil$ = number of bits to represent x, in the case of 50 000 000, the answer is 26 bits.

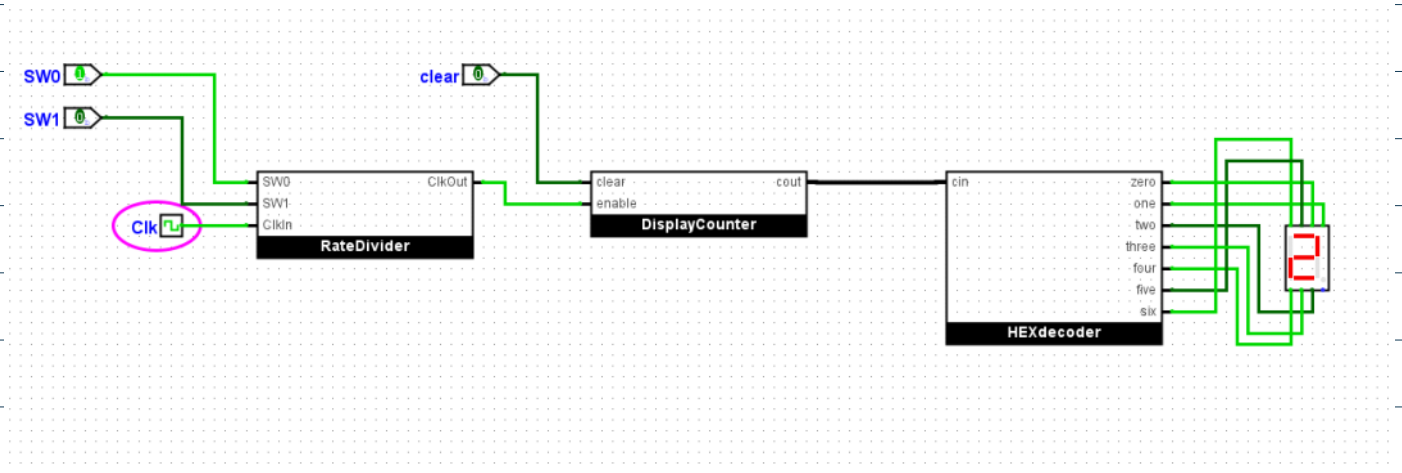
1. Schematic



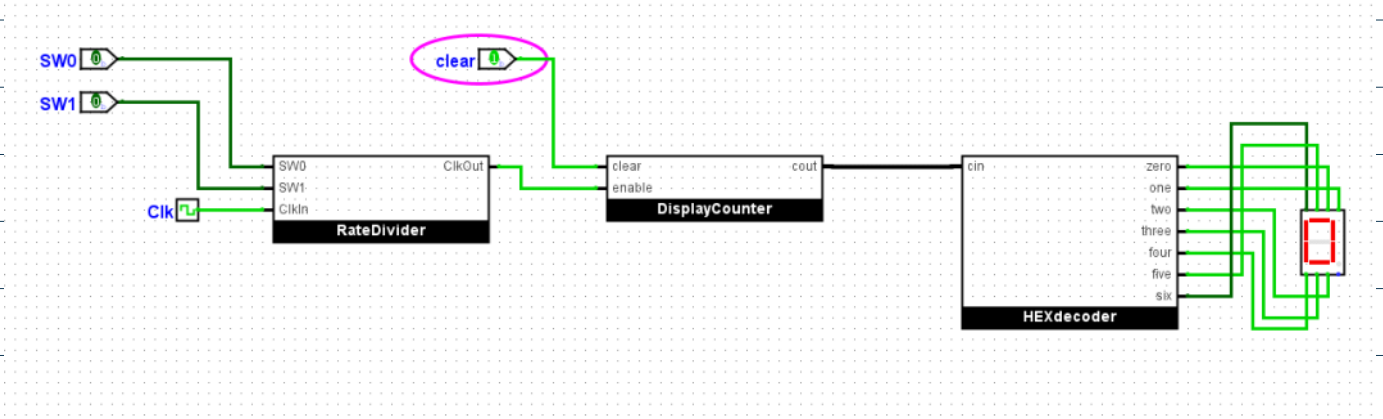


2. Tests

Counter seems to go up every clock cycle and the divider looks like it works with every input of SW



Clear also works

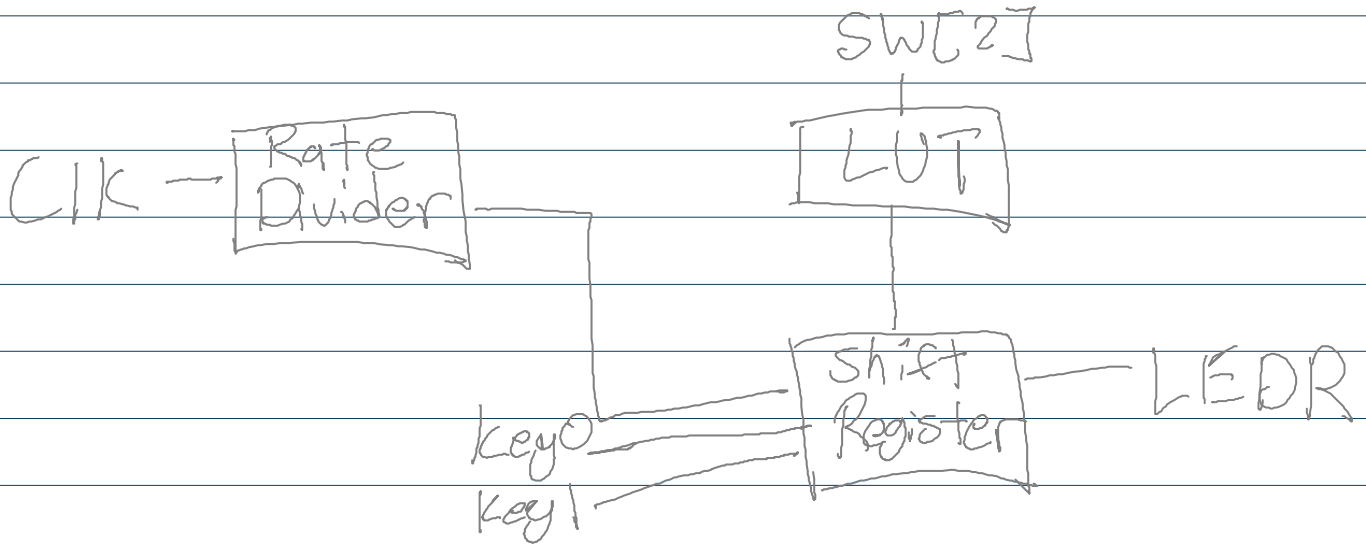


Part III

LUT

Letter	Morse Code	Patter Rep (16 bits)
S	...	1010100000000000
T	_	1110000000000000
U	.._	1010111000000000
V	..._	1010101110000000
W	.__ _	1011101110000000
X	_.._	1110101011100000
Y	_._ _	1110101110111000
Z	_ _..	1110111010100000

2. Schematic



4. Tests

Base case test