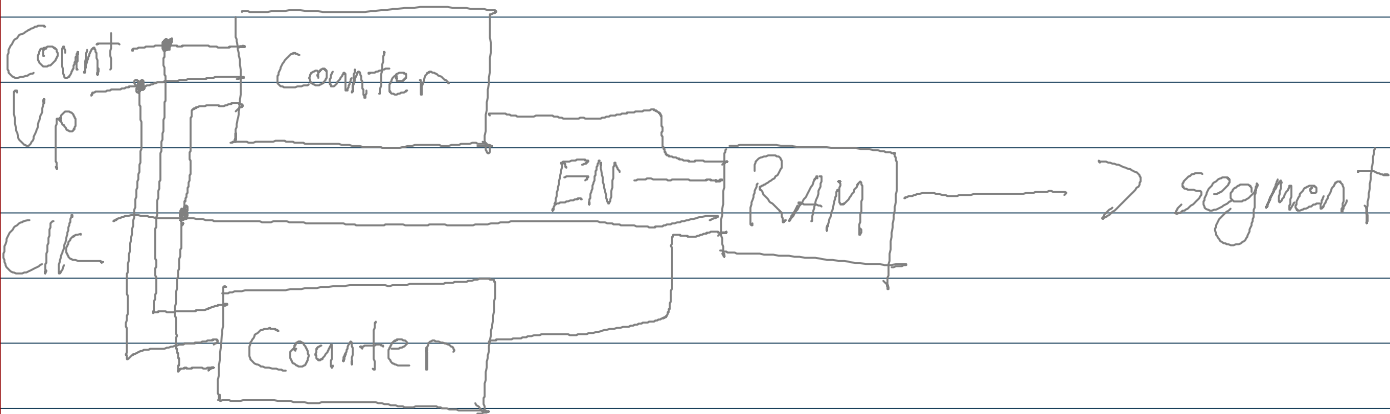Lab 7

July 14, 2021   1:41 PM

Part I

2. Both Signals

When both signals are low, there is no change to the RAM module or output when the clock goes high.
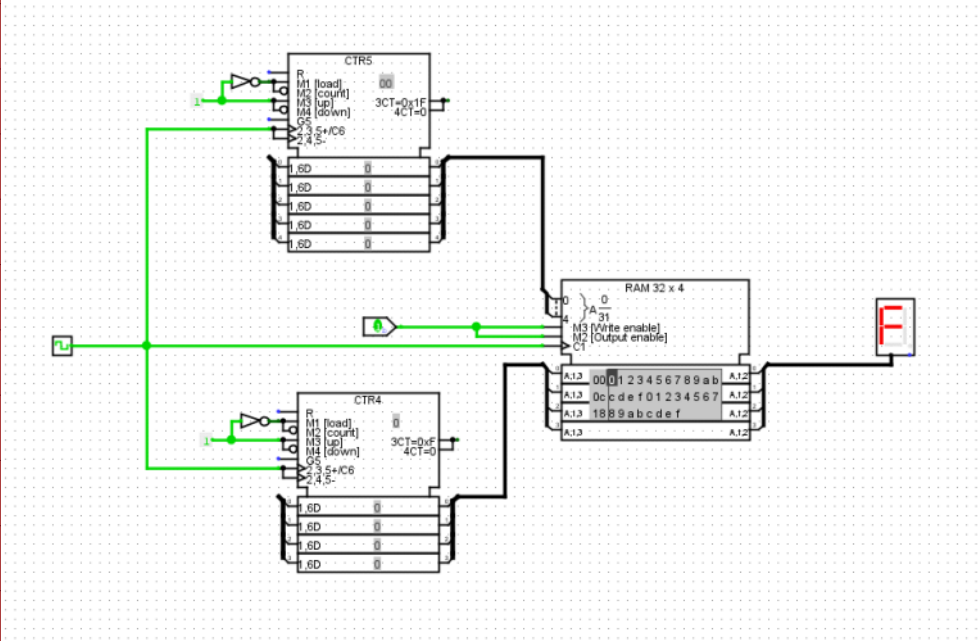
When both signals are high, the input is written in the correct memory address and output when the clock goes high.

5. Schematic

6. Testing

After full 32 clock cycles

Part II

Questions

1. What happens if you don't turn Enable off before updating X and Y?

Depending on the implementation, it could create a trail of the old square colour whilst the cursor goes to the new location
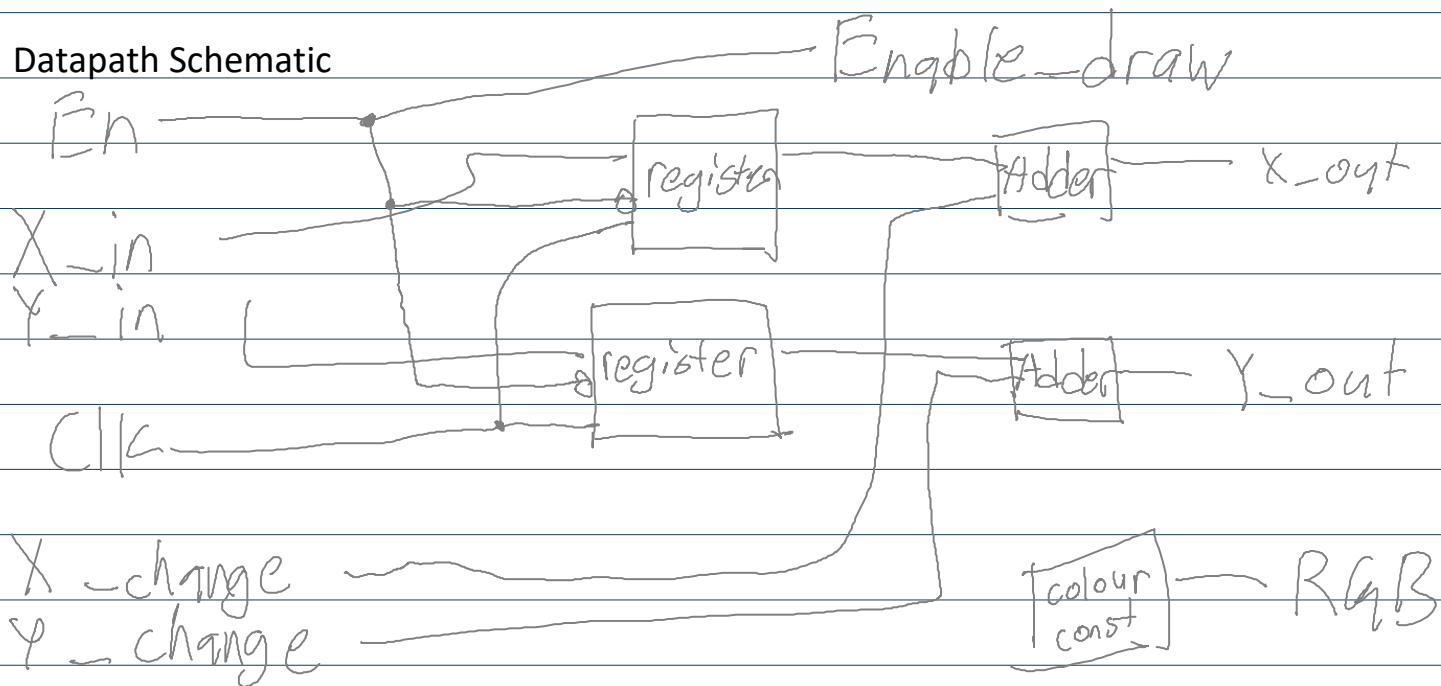
2. What happens if you turn Enable off before 256 clock cycles have passed?

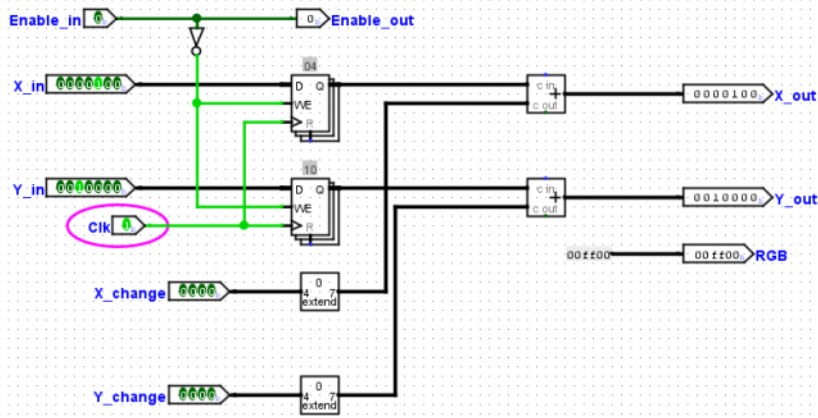The square would just be incomplete as no more pixel inputs are accepted after enable is off

3. What happens if you turn Reset on while Enable is on?
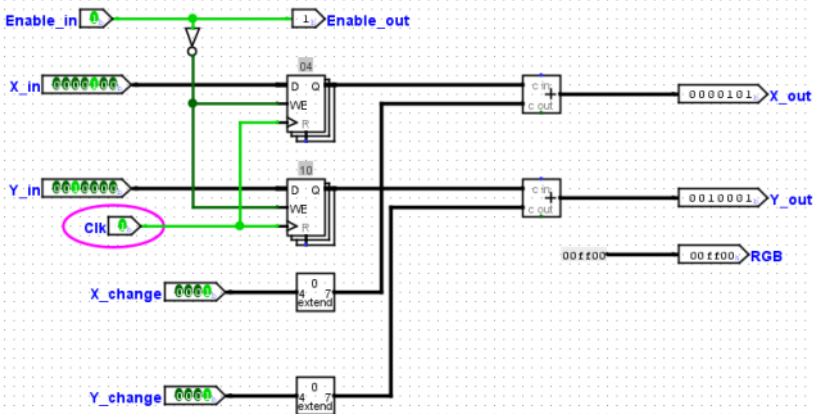
The screen would stay black because of reset

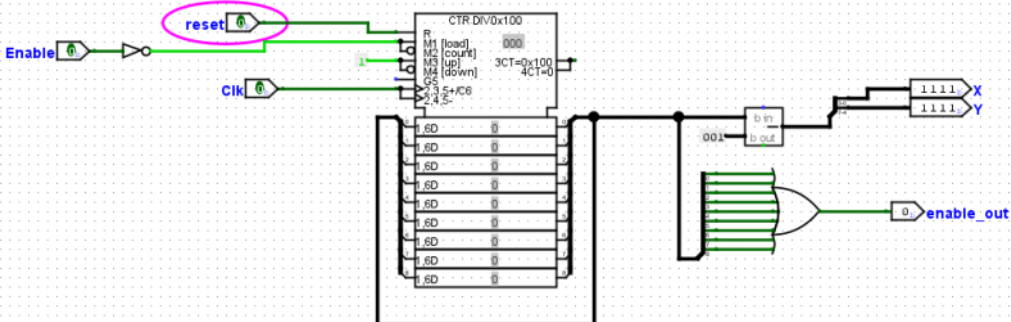## 1. Datapath Schematic

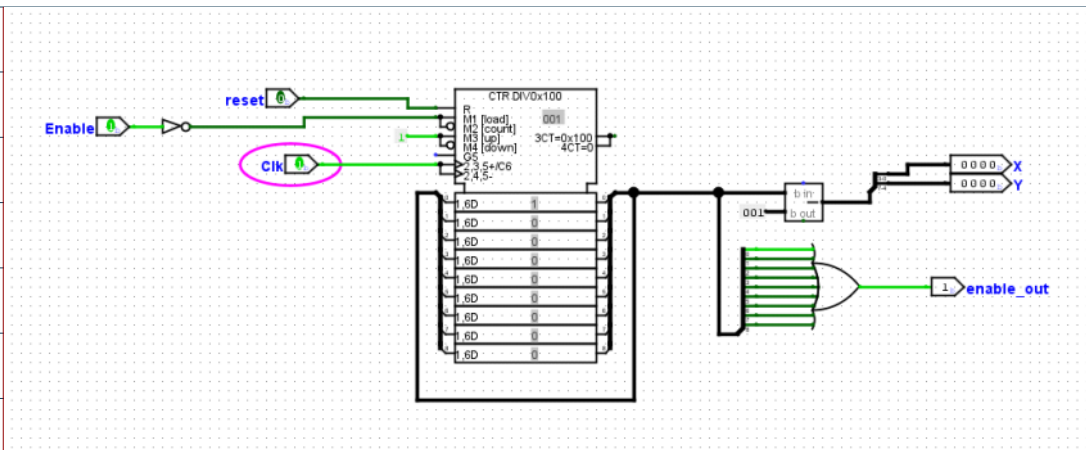Load X and Y in when enable is low

Do arithmetic when enable is high

2. FSM Tests

First state is loading X and Y state

All other states up to 1 0000 0000 give correct X and Y displacement and enable signal

3. FSM Tests

Starts drawing in correct place