Lab 6

June 29, 2021 7:23 PM

Part I

1. Questions

Given the starter circuit, is the Reset signal a synchronous or asynchronous reset?
ANS: Asynchronous

Is it active high, or active low signal?
ANS: Active high

How should the Reset signal feature in the tests that you run on your FSM?
ANS: It should set the FSM back to the first (A) state

2. Tables

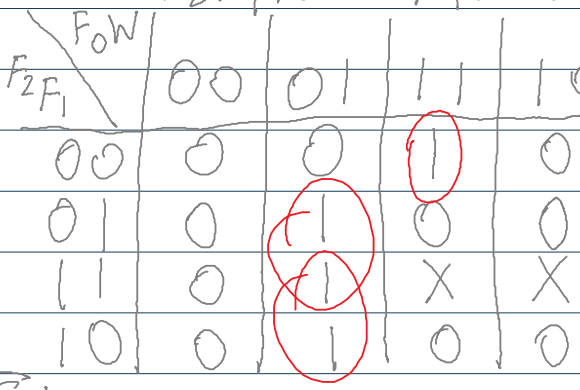
Flip-flop values

	F2	F1	F0
A	0	0	0
B	0	0	1
C	0	1	0
D	0	1	1
E	1	0	0
F	1	0	1
G	1	1	0

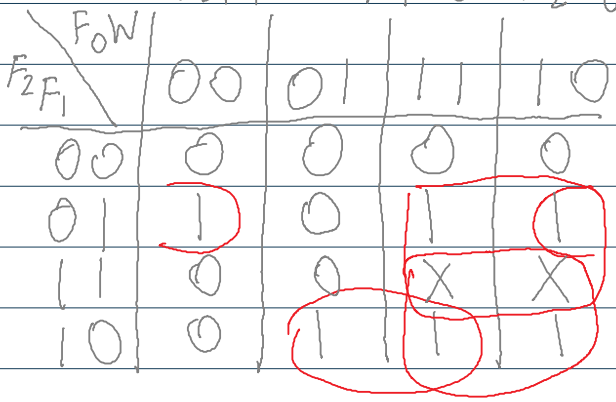
State table

F2	F1	F0	W	F2*	F1*	F0*
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	0	1	1
0	1	1	0	1	0	0
0	1	1	1	1	0	1
1	0	0	0	0	0	0
1	0	0	1	1	1	0
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	0	0
1	1	0	1	0	1	0

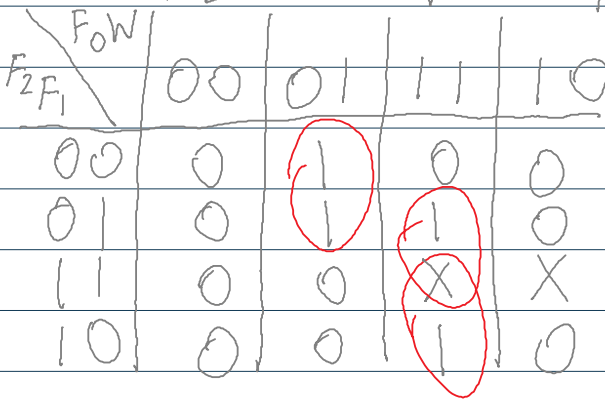
$F_1^* = \bar{F}_2\bar{F}_1F_0W + F_1\bar{F}_0W + F_2\bar{F}_0W$



$F_2^* = \bar{F}_2F_1W + F_1F_0 + F_2F_0 + F_2\bar{F}_1W$

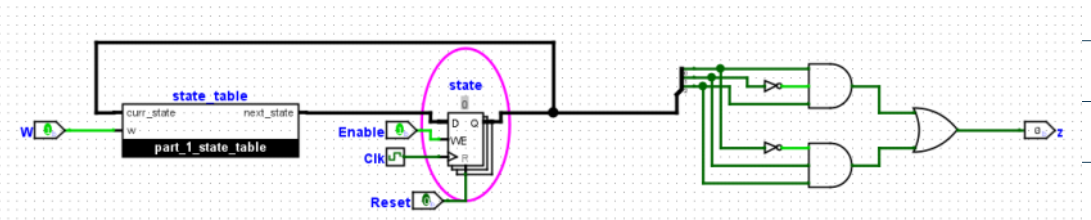


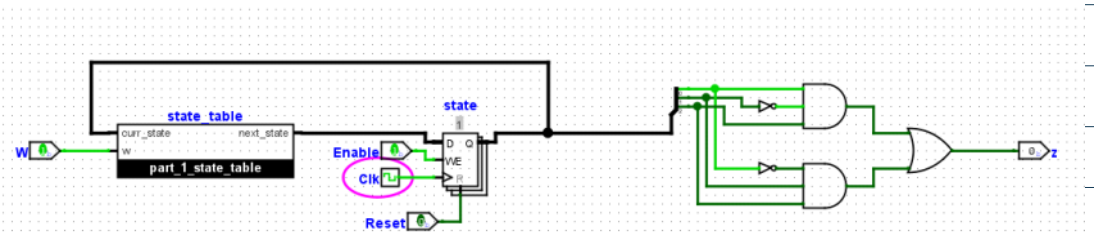
$F_0^* = \bar{F}_2\bar{F}_0W + F_1\bar{F}_0W + F_2\bar{F}_0W$



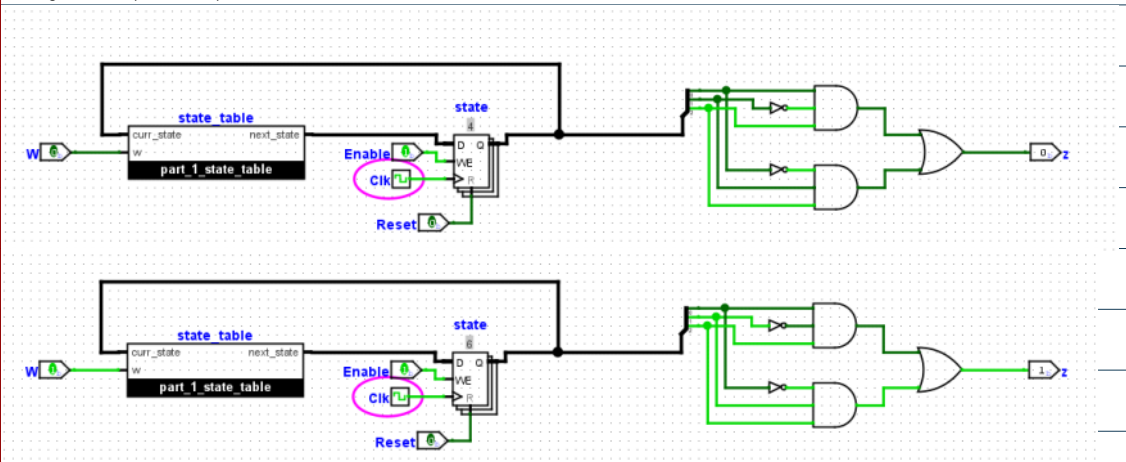
5. Tests

Basic test case, going from A to B using W=1, 1 clock cycle





Going from z=0 output to z=1 output



Part II

2. Register Table

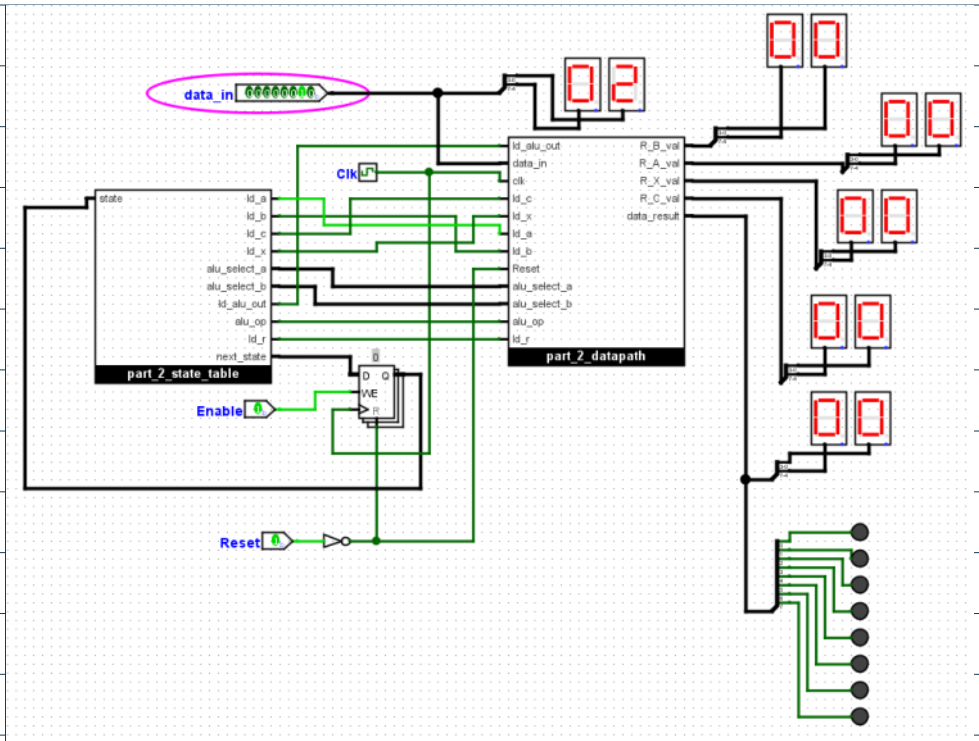
Clk Cycle	Id_a	Id_b	Id_c	Id_x	alu_select_a	alu_select_b	Id_alu_out	alu_op	Id_r	R_A	R_B	R_C	R_X	R_R	Flip-flop State
1	1	0	0	0	00	00	0	0	0	A	0	0	0	0	0000
2	0	1	0	0	00	00	0	0	0	A	B	0	0	0	0001
3	0	0	1	0	00	00	0	0	0	A	B	C	0	0	0010
4	0	0	0	1	00	00	0	0	0	A	B	C	x	0	0011
5	0	1	0	0	01	11	1	1	0	A	Bx	C	x	0	0100
6	1	0	0	0	00	01	1	0	0	A+Bx	Bx	C	x	0	0101
7	0	1	0	0	11	11	1	1	0	A+Bx	x^2	C	x	0	0110
8	0	1	0	0	10	01	1	1	0	A+Bx	Cx^2	C	x	0	0111
9	0	0	0	0	00	01	0	0	1	A+Bx	Cx^2	C	x	Cx^2+Bx+A	1000

3. State diagram

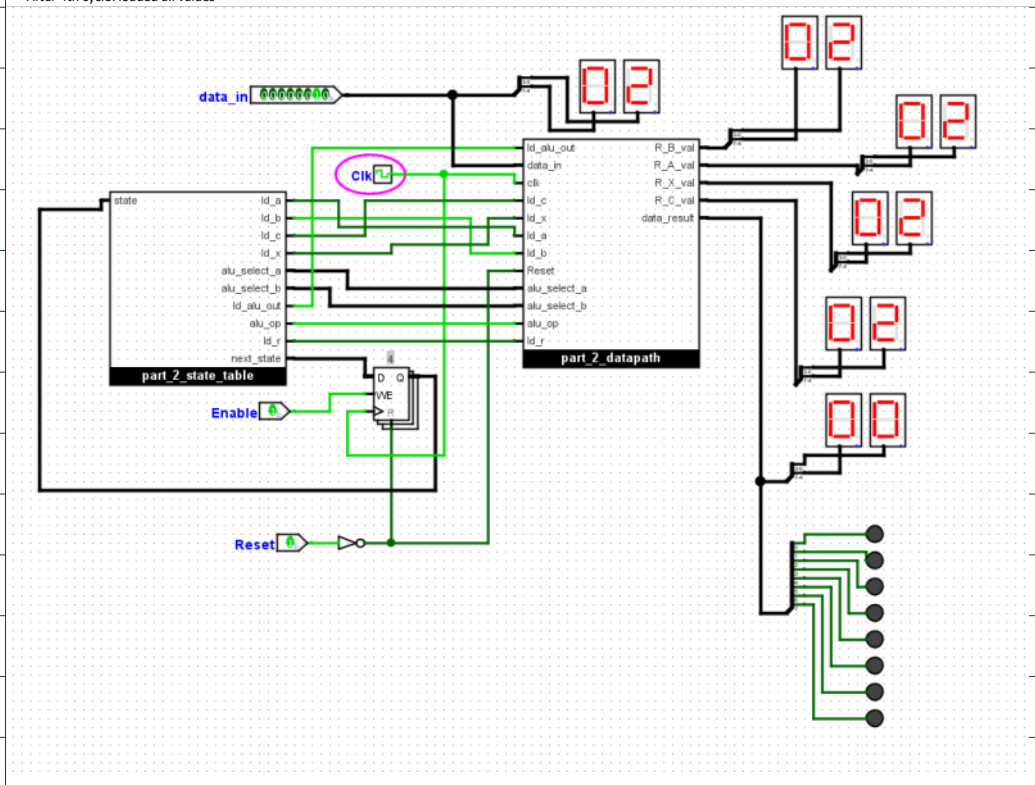
Goes from 0000 incrementing by 1 until 1000 and repeat

5. Testing

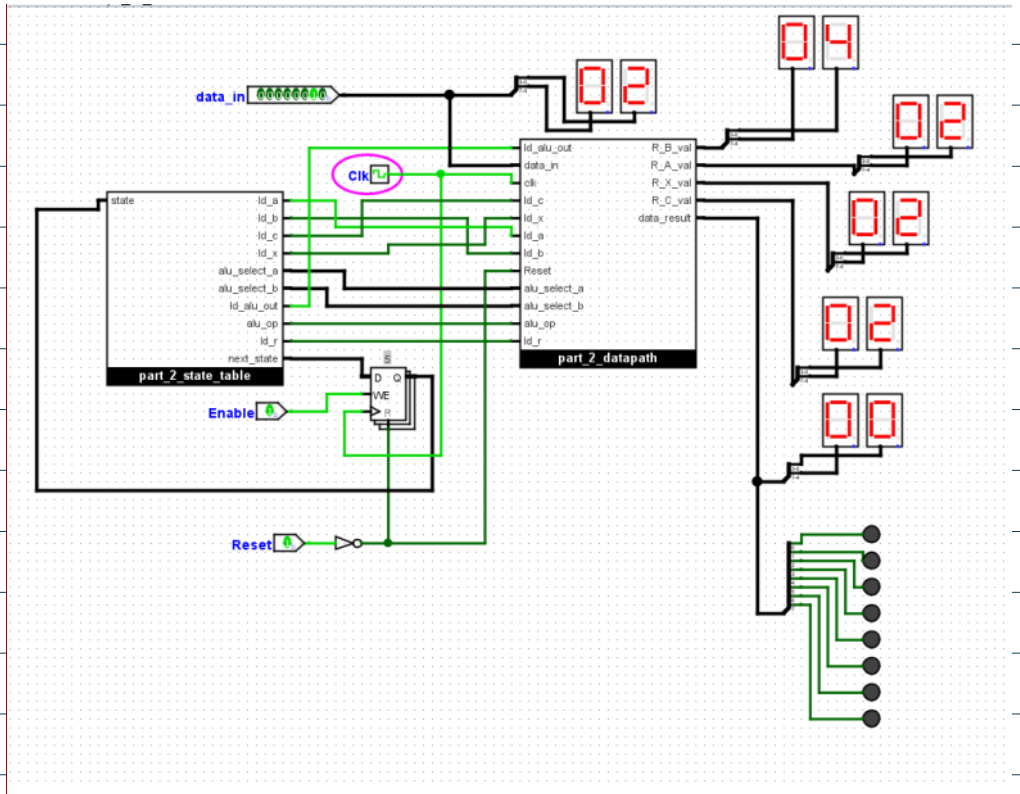
Simple test with A,B,C,x = 2, so Cx^2+Bx+A = 14, starting with the 0th cycle:



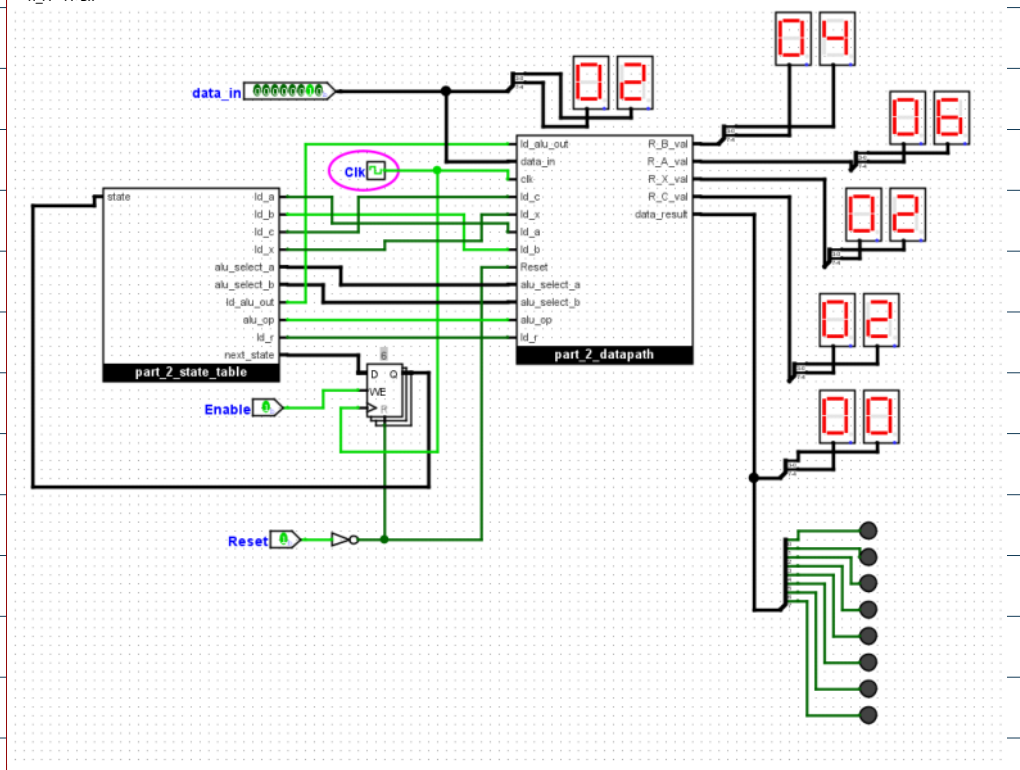
After 4th cycle: loaded all values



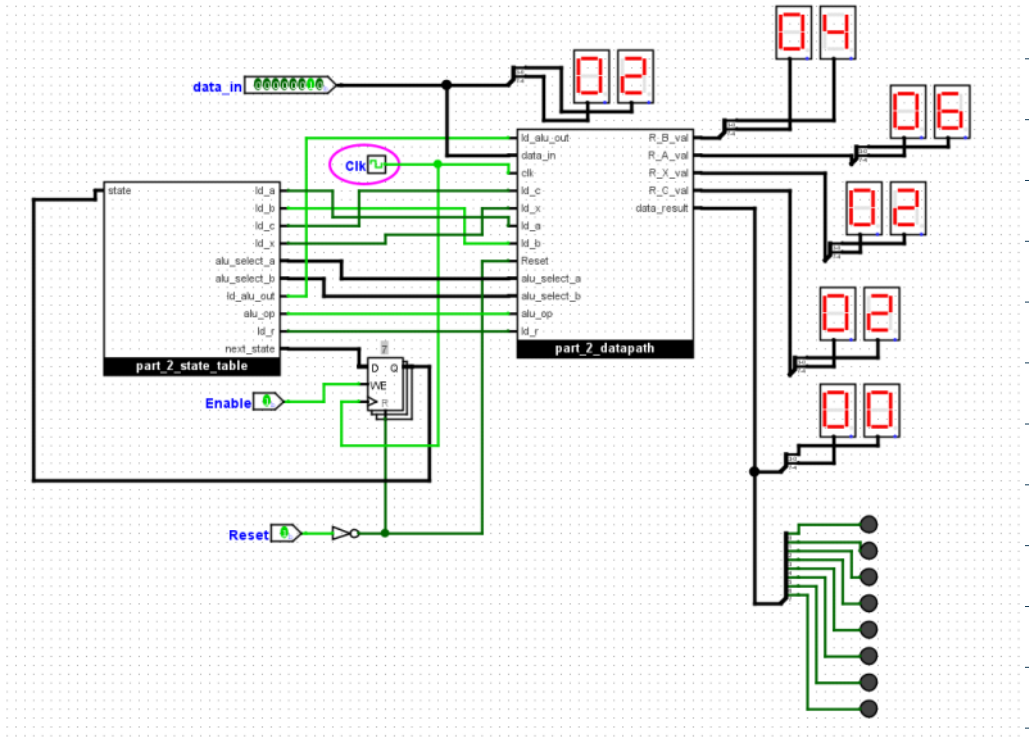
R_B = Bx


data_in
Clk
Reset
Enable
state
ld_a
ld_b
ld_c
ld_x
alu_select_a
alu_select_b
ld_alu_out
alu_op
ld_r
next_state
part_2_state_table
D Q
WE
R
ld_alu_out
data_in
clk
ld_c
ld_x
ld_a
ld_b
Reset
alu_select_a
alu_select_b
alu_op
ld_r
R_B_val
R_A_val
R_X_val
R_C_val
data_result
part_2_datapath
04
02
02
02
02
00

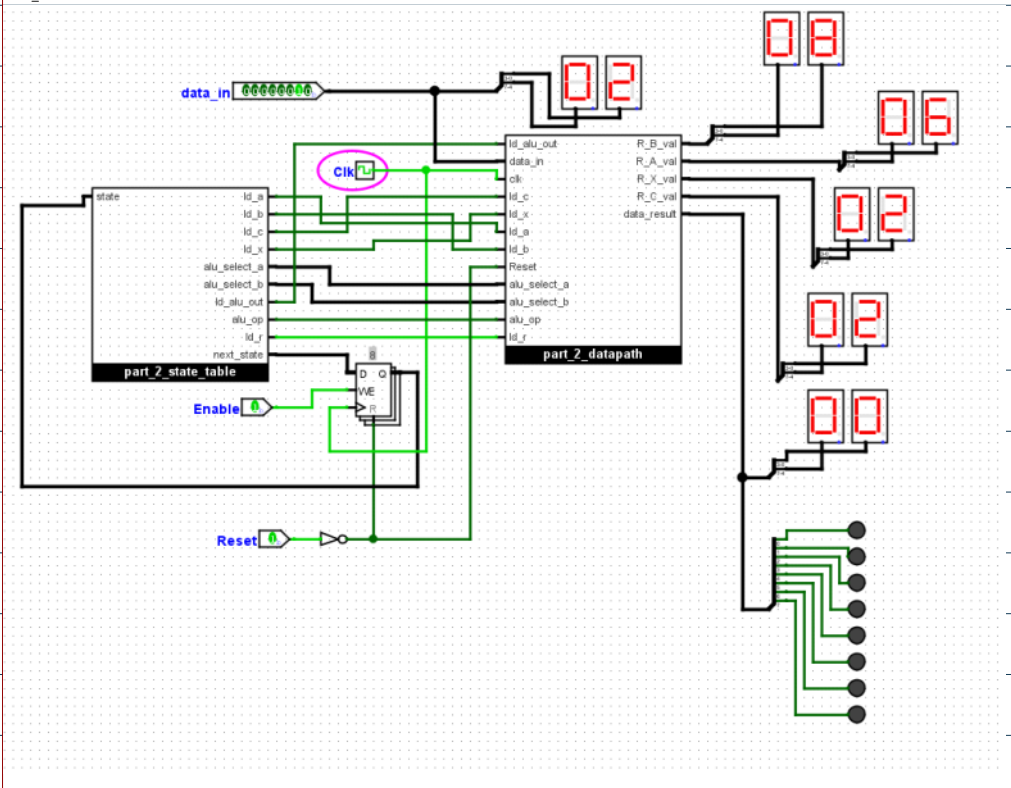
R_A = A+Bx


data_in
Clk
Reset
Enable
state
ld_a
ld_b
ld_c
ld_x
alu_select_a
alu_select_b
ld_alu_out
alu_op
ld_r
next_state
part_2_state_table
D Q
WE
R
ld_alu_out
data_in
clk
ld_c
ld_x
ld_a
ld_b
Reset
alu_select_a
alu_select_b
alu_op
ld_r
R_B_val
R_A_val
R_X_val
R_C_val
data_result
part_2_datapath
04
02
06
02
02
00

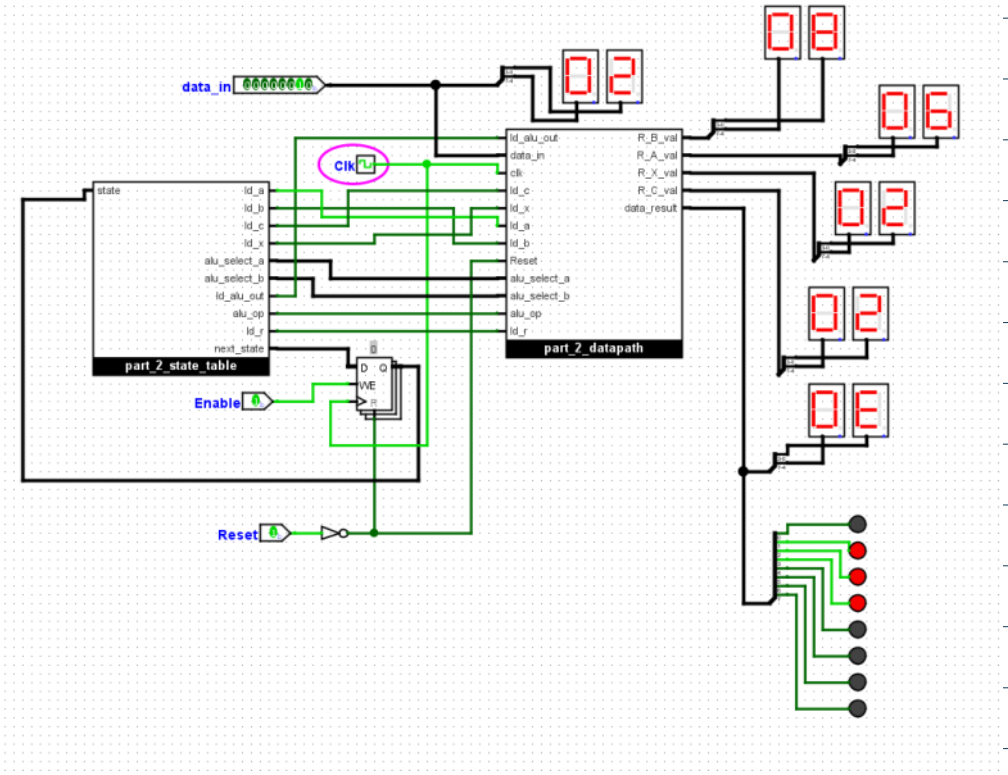
R_B = x^2



R_B = Cx^2



Data_result = 14 (E in hex)


data_in
Clk
state
ld_a
ld_b
ld_c
ld_x
alu_select_a
alu_select_b
ld_alu_out
alu_op
ld_r
next_state
part_2_state_table
Enable
Reset
D
Q
WE
R
ld_alu_out
data_in
clk
ld_c
ld_x
ld_a
ld_b
Reset
alu_select_a
alu_select_b
alu_op
ld_r
R_B_val
R_A_val
R_X_val
R_C_val
data_result
part_2_datapath
02
08
06
02
02
0E