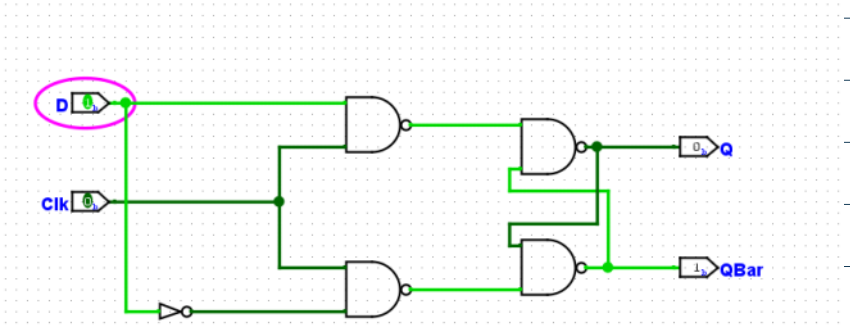
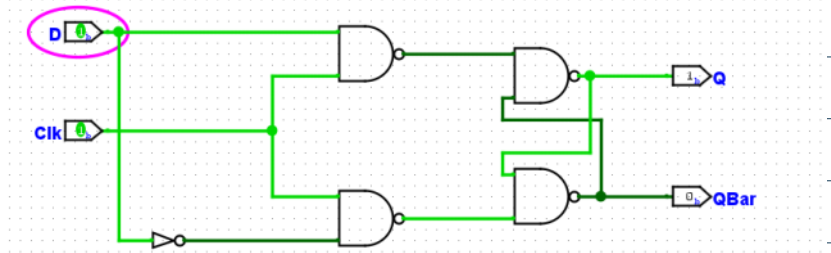
Lab 4

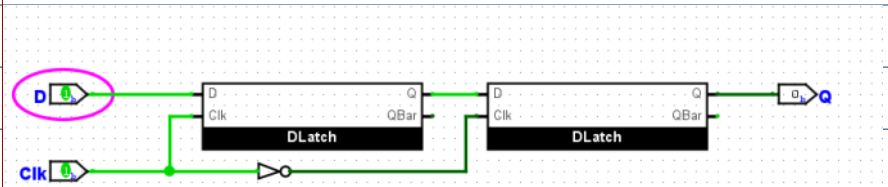
June 7, 2021 2:40 PM

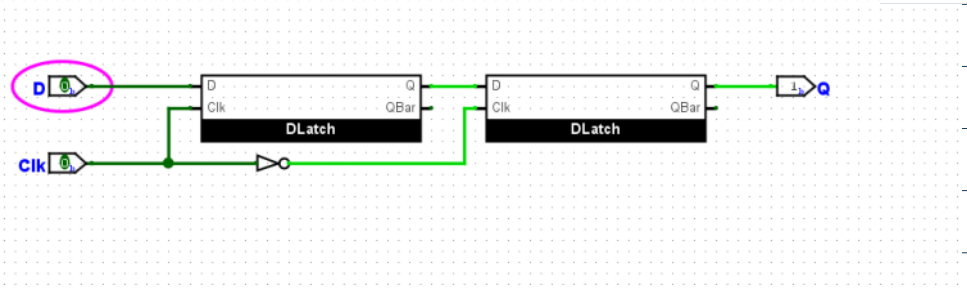
Part I

2. Behaviour









3. Invalid input

There is no indeterminate input for the latch and flip-flop, but any starting with the Clk at 0 won't change the state of the circuit at all, and with the 2nd d-latch in the master slave, there won't be any input coming from the previous d-latch.

Part II

a) What would happen if you didn't include the register in your diagram?

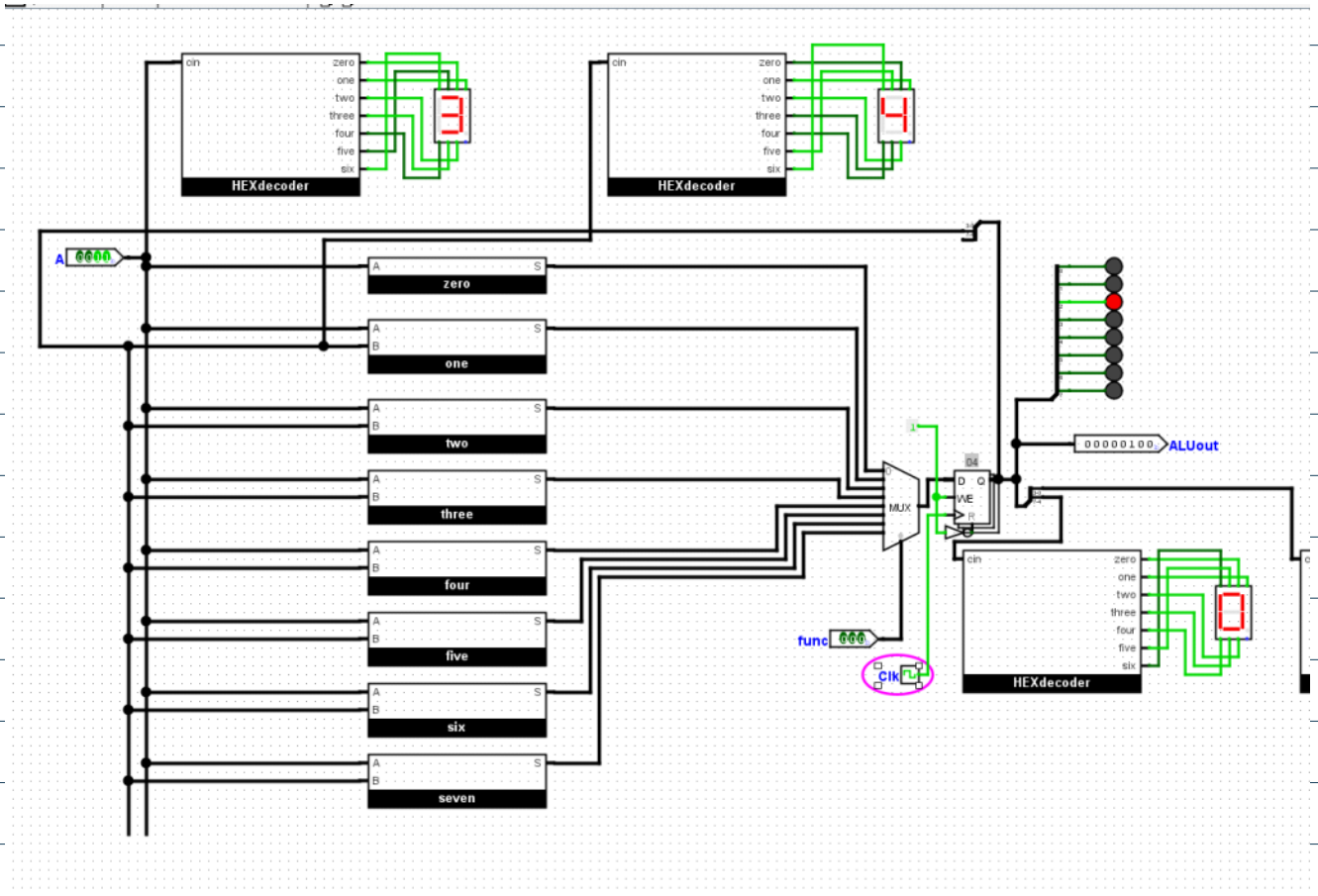
The output of the circuit would immediately be routed to the B input, whilst with a register, the register will only let the output through when the clock is high.

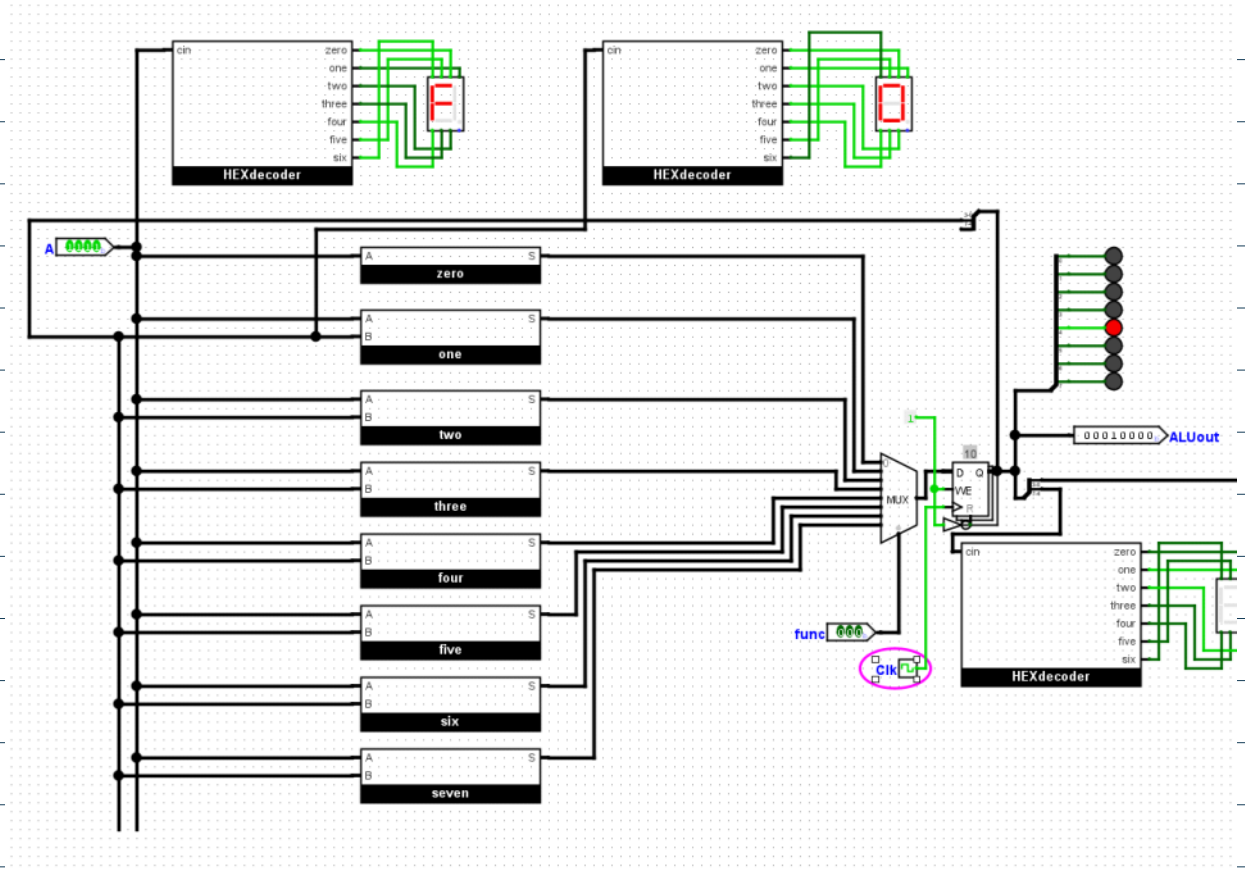
a) When multiplying two n-bit binary numbers, how many bits will you need to store the result?

You would need 2n bits as an upper bound of the number of bits to store the product of a n-bit multiplication

2. Testing

Function 0

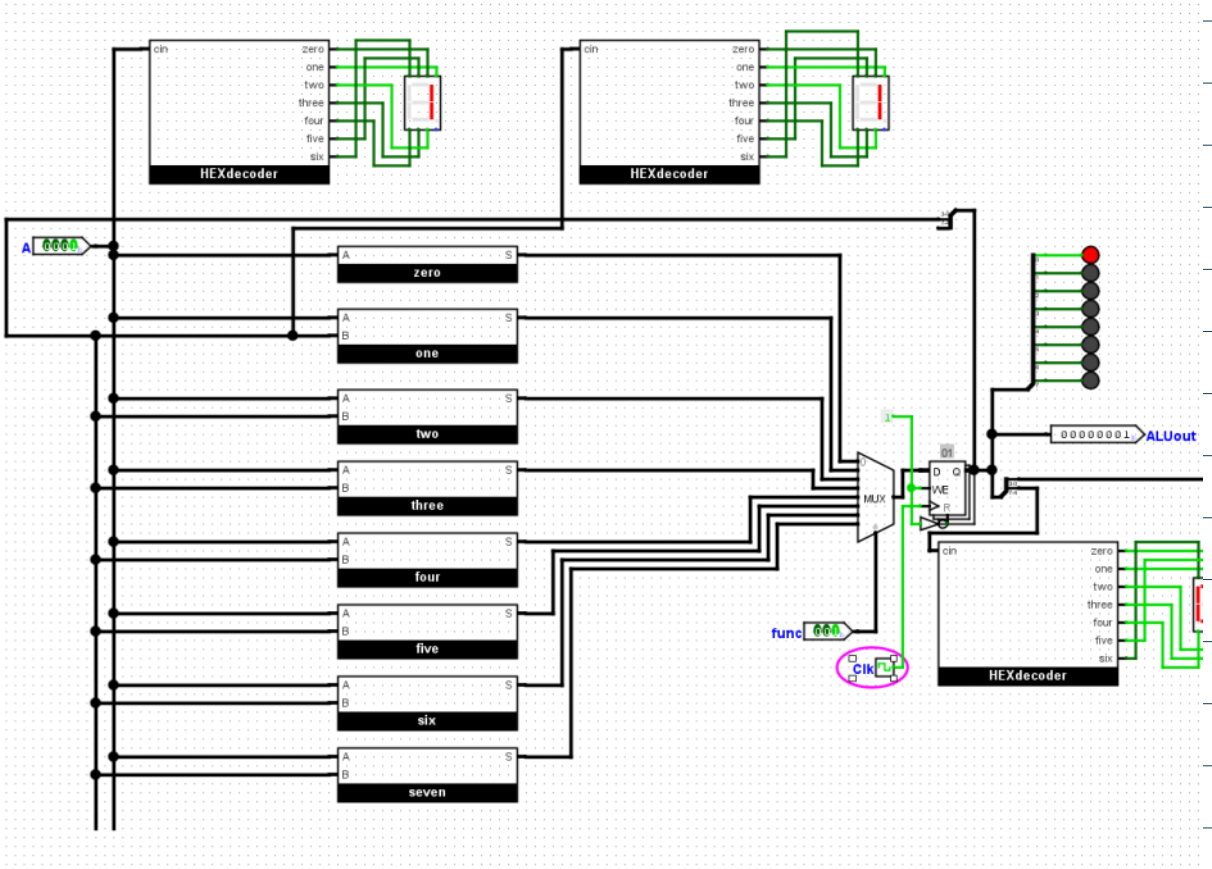




The output to the register is always A + 1 no matter what is stored in the register

Function 1

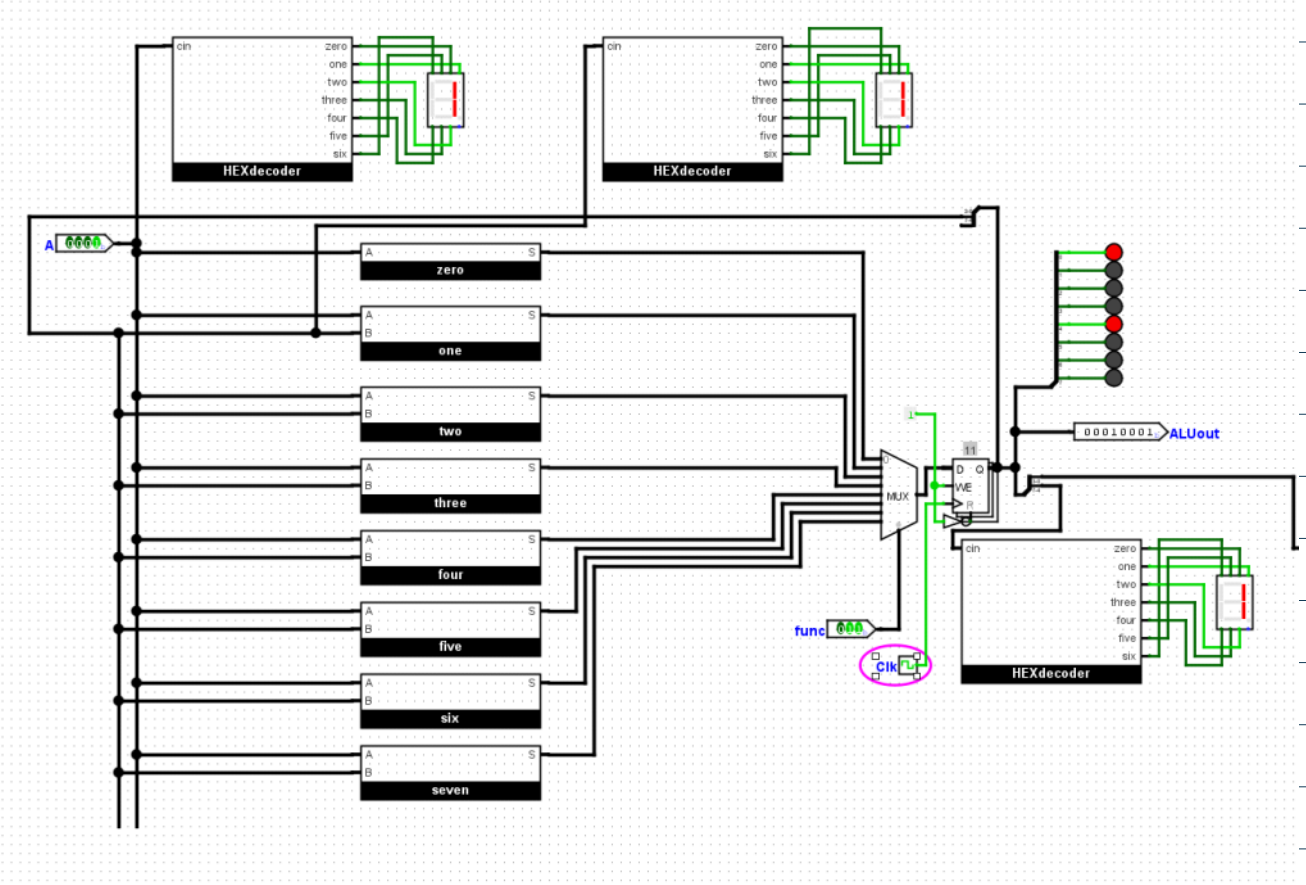
By constantly changing the state of the clock, the value of the register should keep increasing with the formula of Ans = A + PrevAns

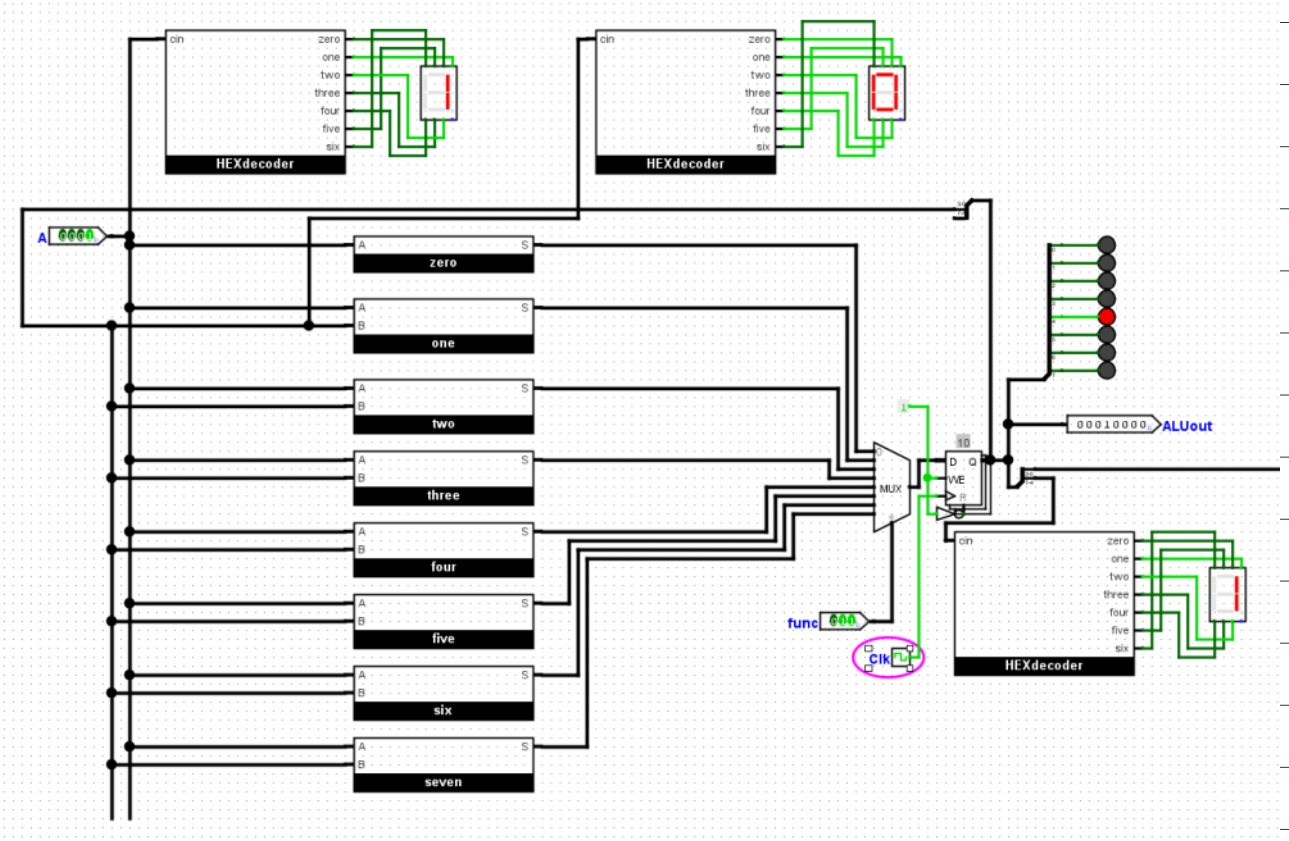


Function 2

Same as function 1

Function 3





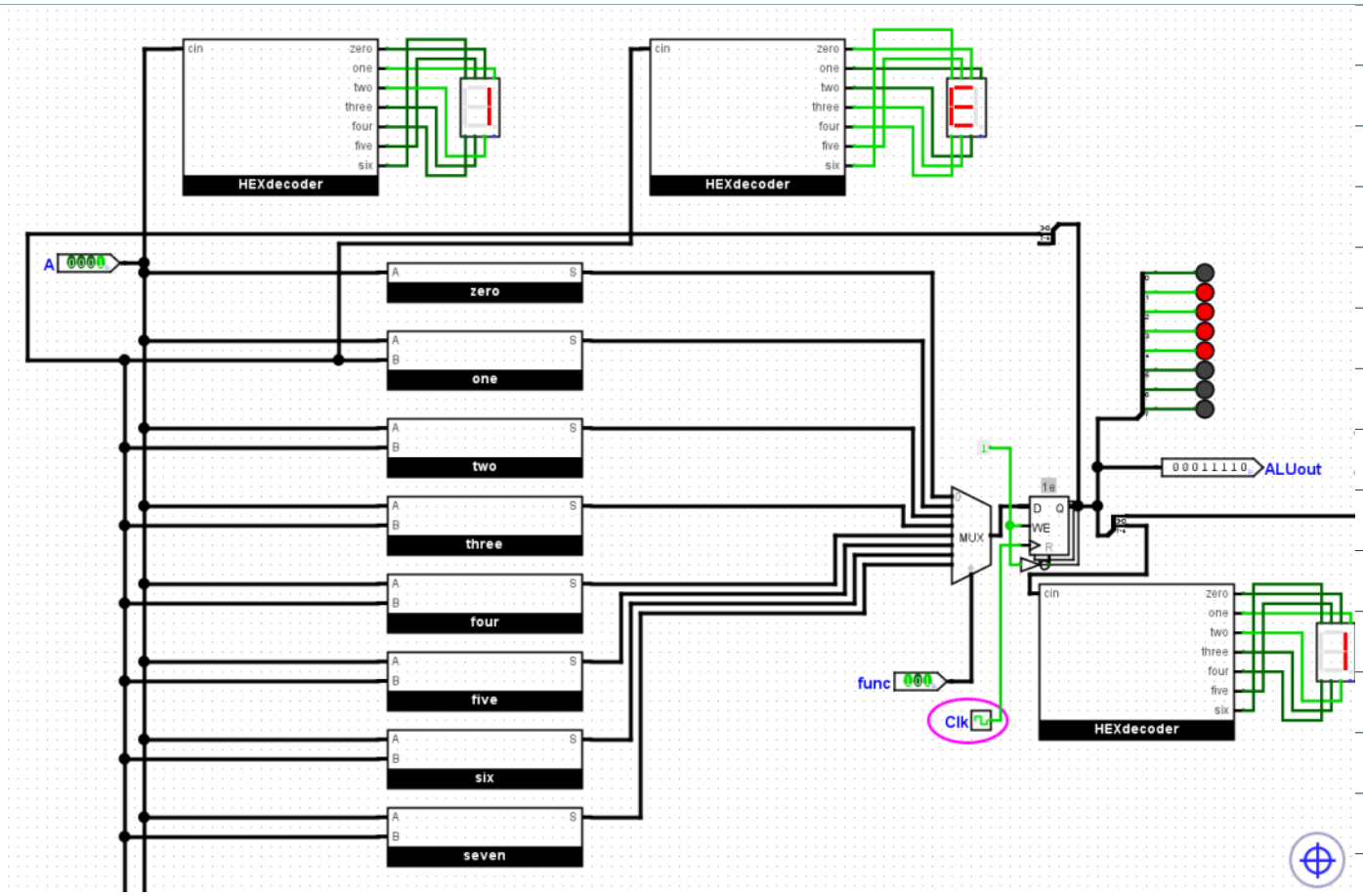
Using A = 0001, the register will store 0001 0000 on the first clock cycle, and repeat between that and 0001 0001 since only the least significant 4 bits are fed back as input B, and the first 4 bits = A XOR B. It will continuously do 0001 XOR 0000 then 0001 XOR 0001, causing the first bit to change on each cycle.

Function 4

As expected, if the register starts with 0, it will always stay 0 if A = 0000
If A is anything but 0, register stores 1 and then since there's a 1 in the input now, the output will stay as 1

Function 5

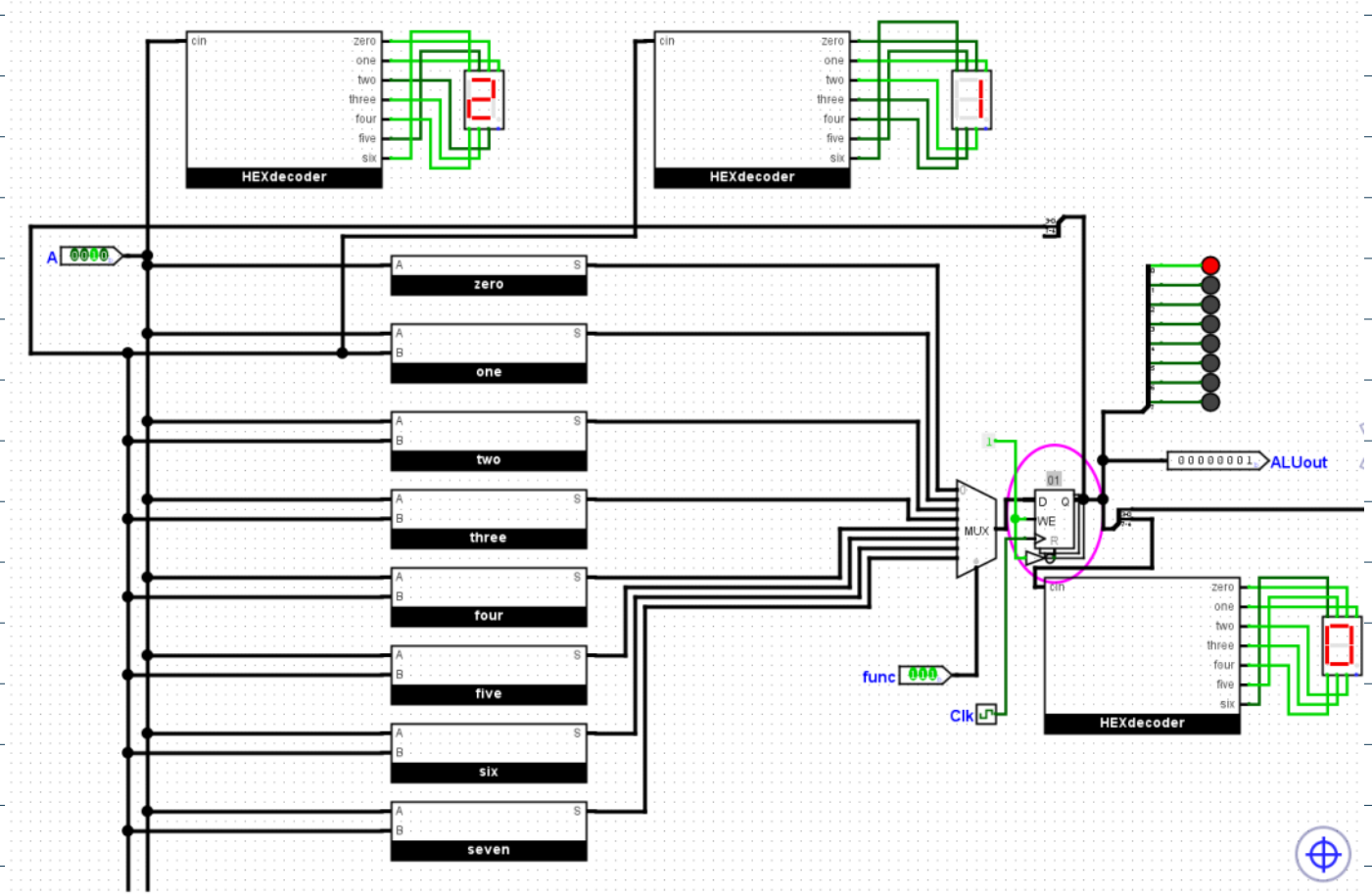
Set the initial value in the register to 0000 1111, then test the shifting with A = 0001, next clock cycle register should be0001 1110

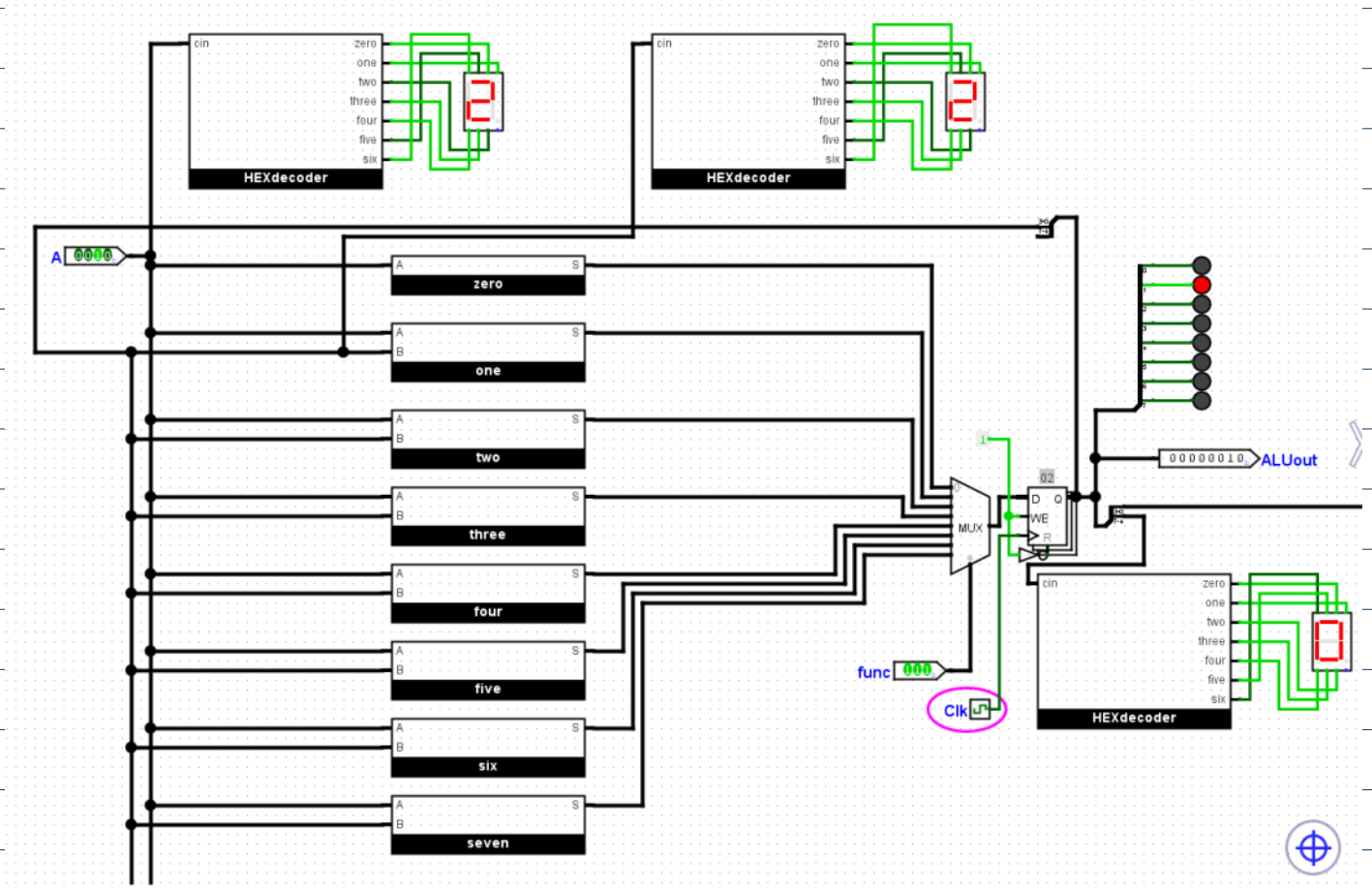


Function 6

Same as function 5, just shifting right instead

Function 7





Setting the register to 0000 0001 to start and A = 0010, every clock cycle will shift the 1 down a bit (because of multiplying by 2) up to 0001 0000 because it only routes the first 4 bits back as input B.

Part III

1. Behaviour:

What is the behaviour of the 8-bit shift register shown in Figure 5 when Load n = 1 and ShiftRight = 0 ?

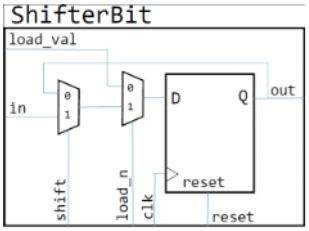
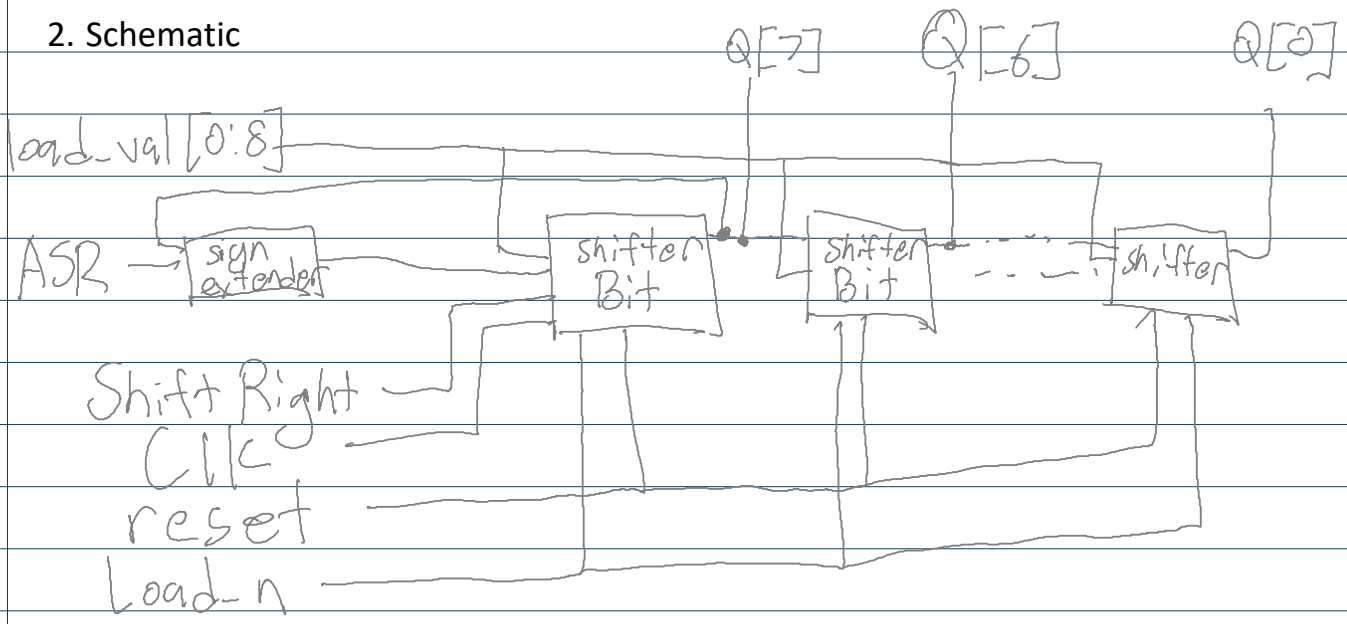


Figure 4: Single-bit shift-register

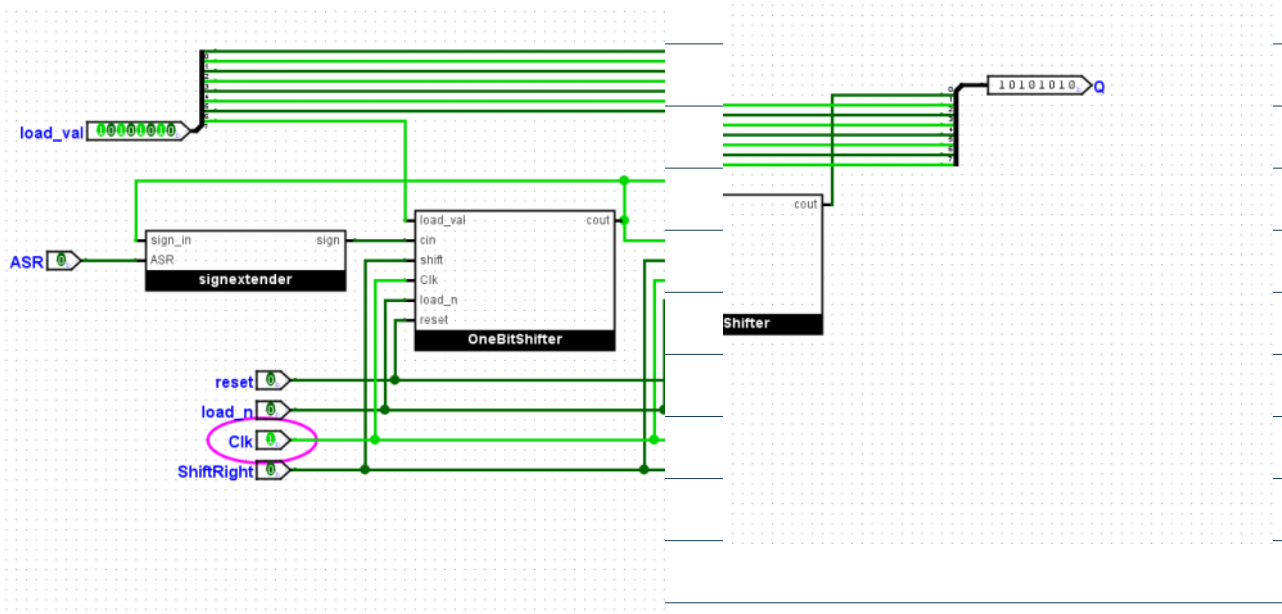
As shown in figure 4, if shift = 0 and load_n = 1, the flip=flop will keep its current output as the same. So on the scale of the 8-bit shift register, all 8 ShifterBits will keep their current value.

2. Schematic

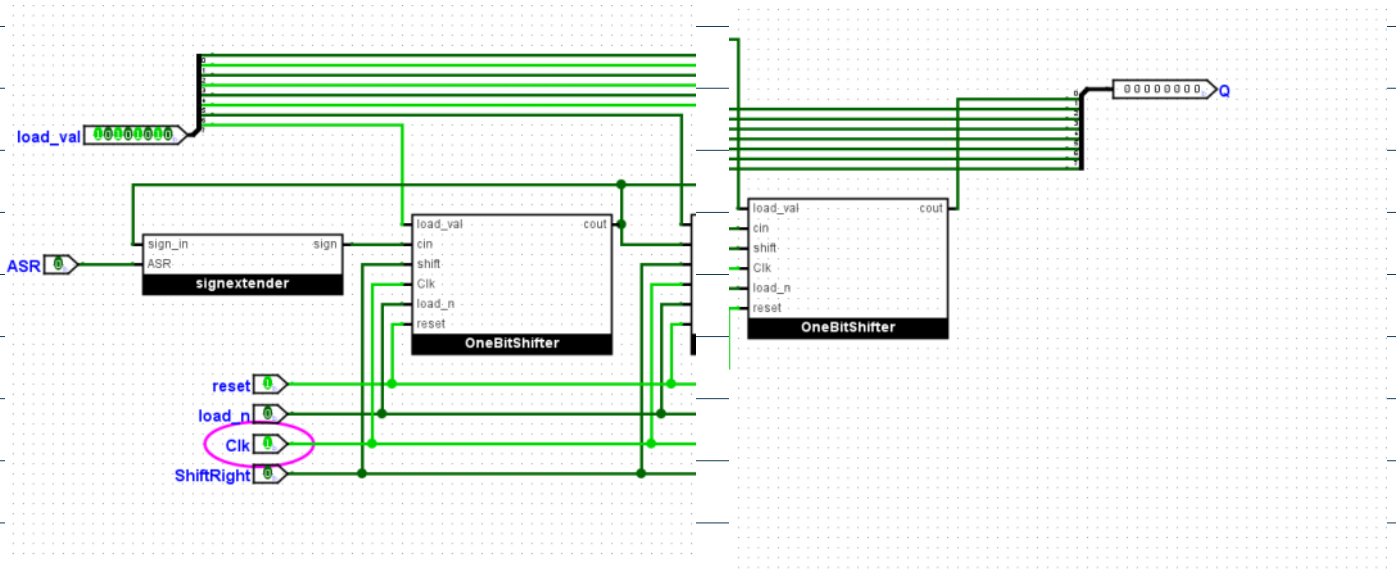


5. Simulations

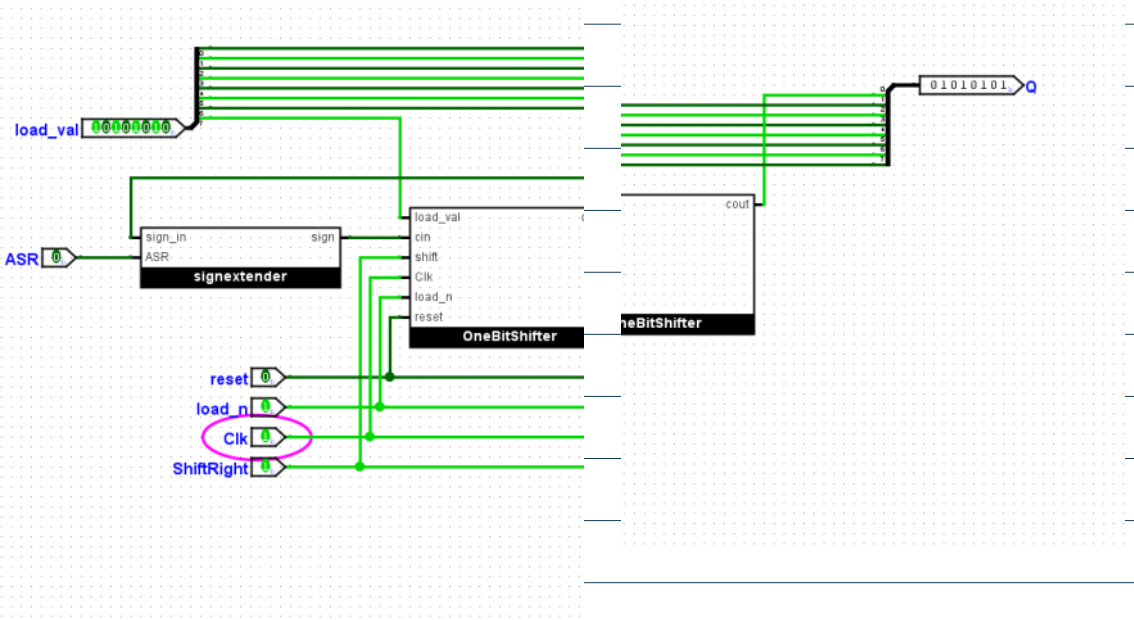
Test 1: Normal loading of load_val



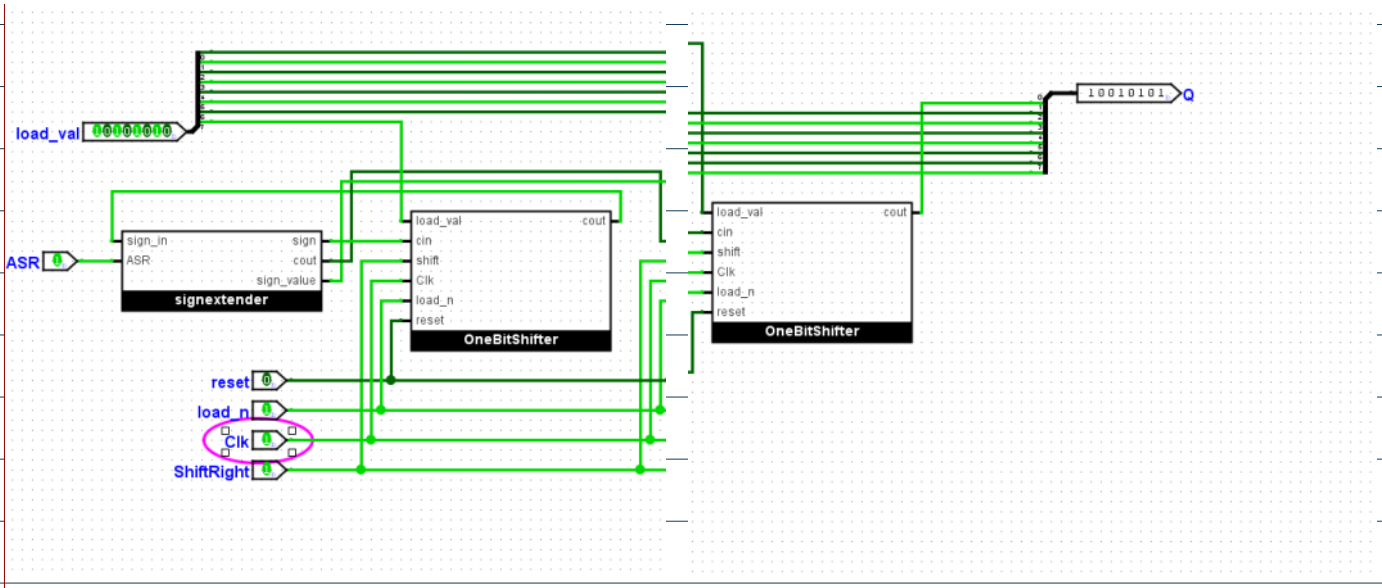
Test 2: Reset all to 0



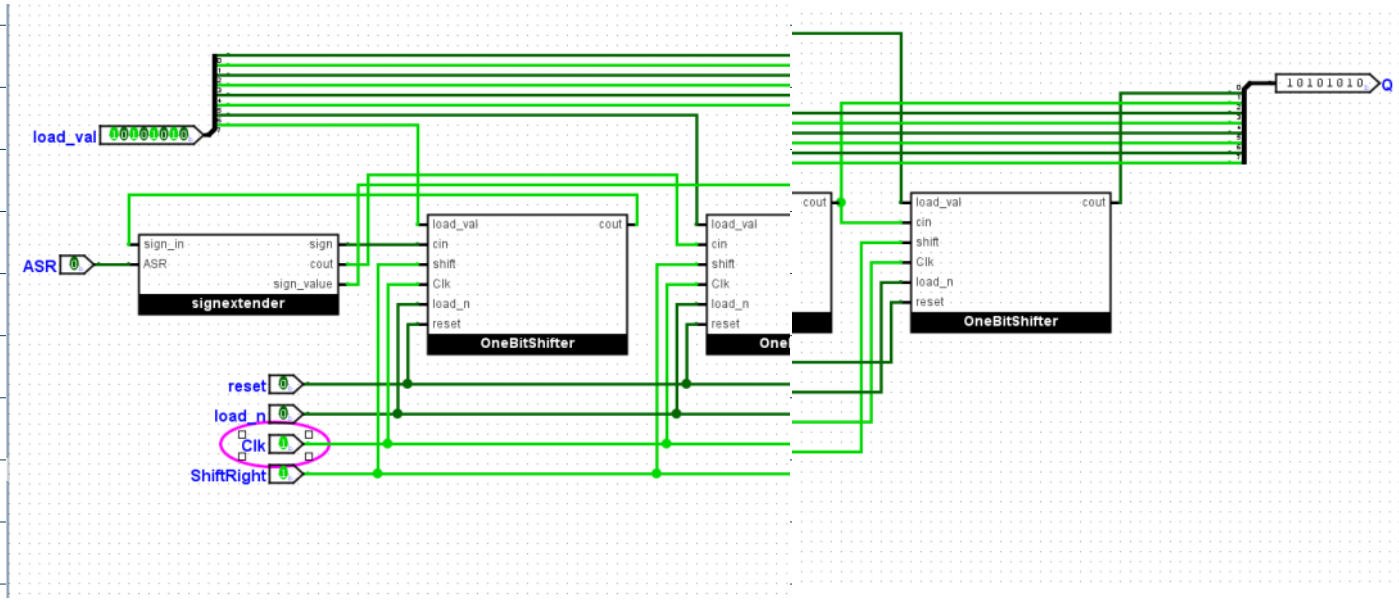
Test 3: Shift right 1 clock cycle



Test 4: Shift right 1 clock cycle with ASR



Test 5: ShiftRight without load_n



Test 6: Try loading load_vals with load_n = 1