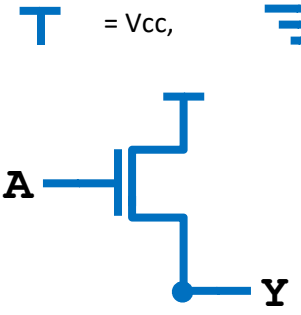
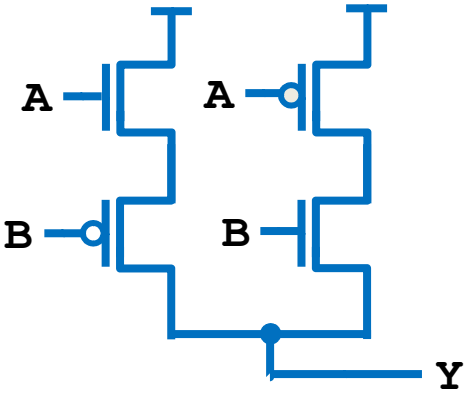
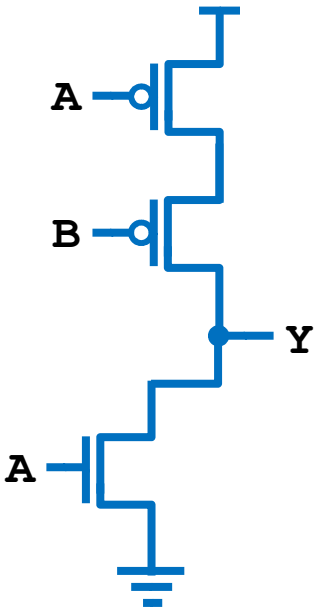
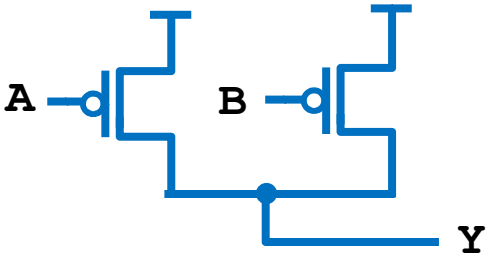
Quiz C

1) The following transistor diagrams are attempting to implement logic gates, but part of each transistor circuit is missing. In the diagrams below, complete the missing parts of each circuit and fill in the name of the completed gate in the space provided below the circuit.

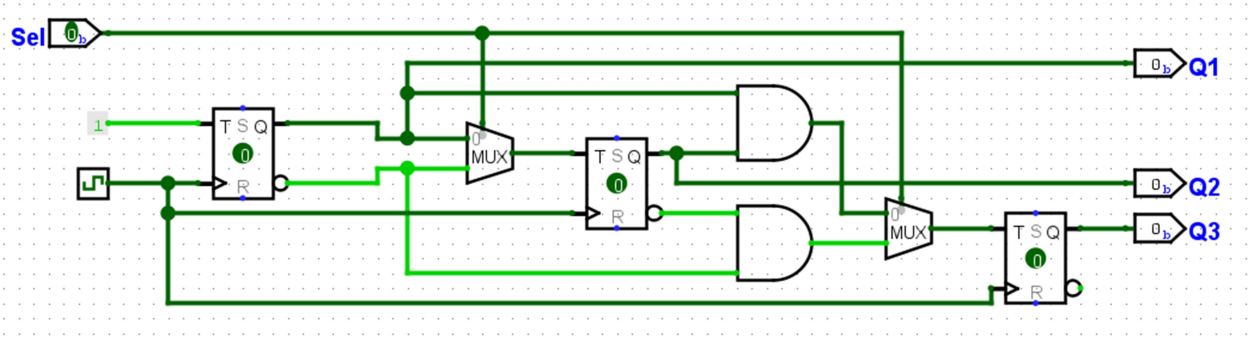




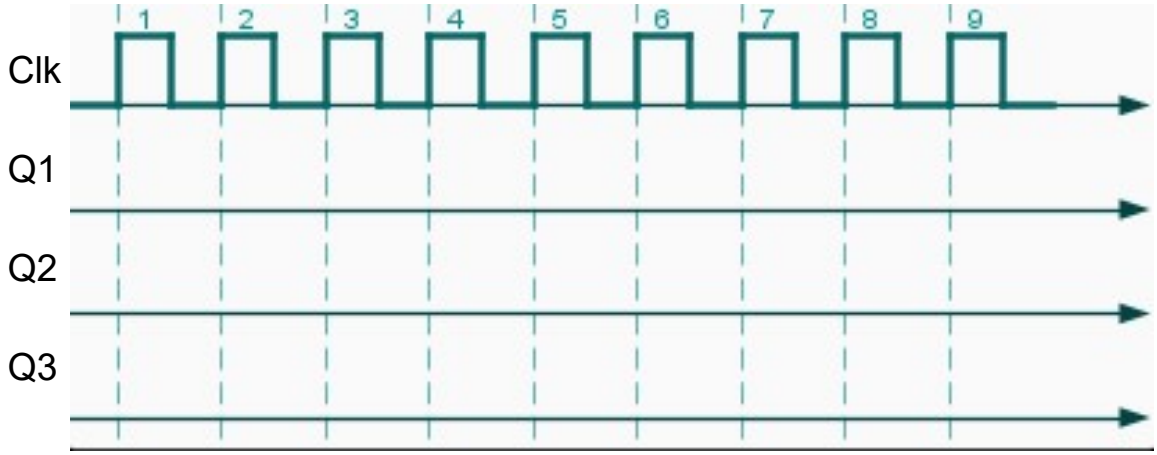




2) Complete the following timing diagrams based on the T Flip flop circuit shown below. Assume that the flip-flop output values are all low before the first positive clock edge, and that delays should be factored in your answer.



a) When 'Sel' is high (Logic '1').



b) Name or describe the circuit based on the timing diagram created in part (a).

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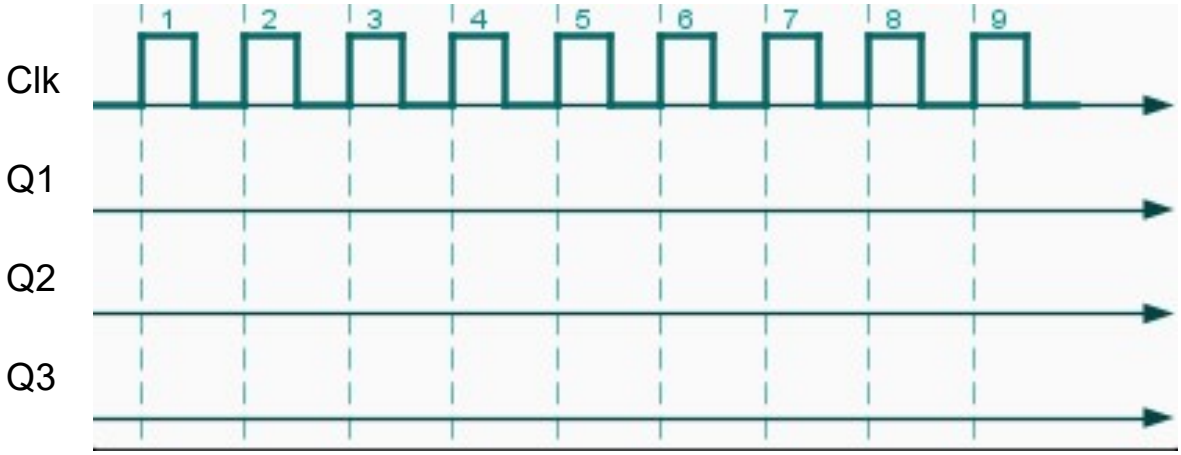
c) When 'Sel' is low (Logic '0').



d) Name or describe the circuit based on the timing diagram created in part (c). **(2**

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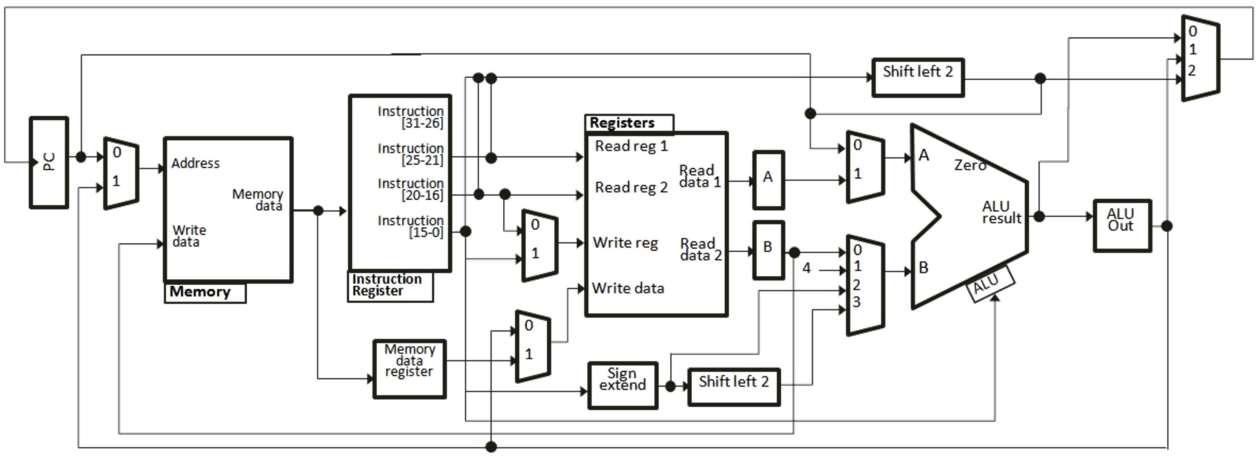
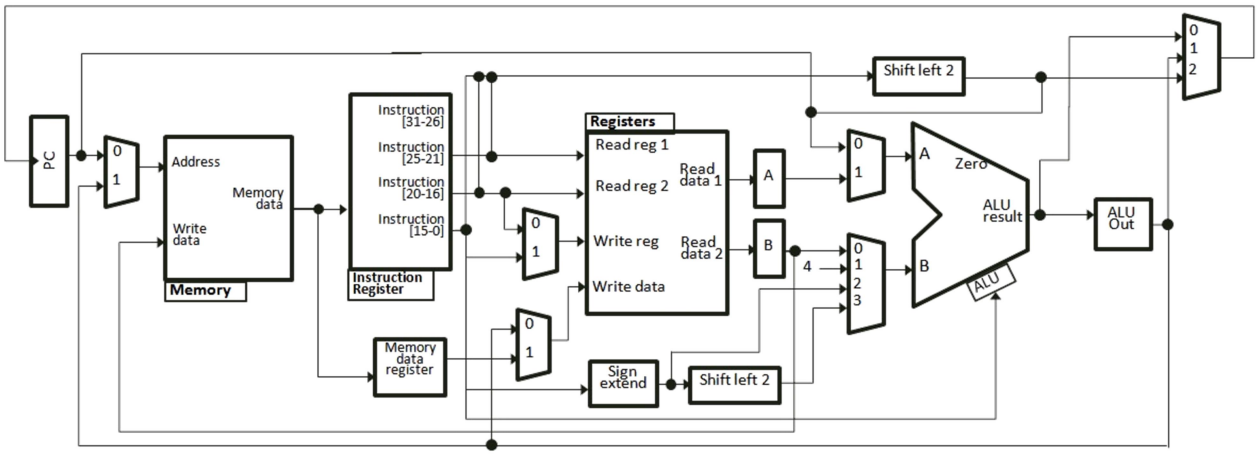
3) Consider the datapath diagrams below. For each of the following steps in an operation, highlight the path (wires) that the data needs to take, from start to finish. Please use a color or marking that will scan properly onto your submission PDF.

a) Branch back to the beginning of Loop which is 4 instructions before the current one.



b) Calculate address of 12($sp) and send to Memory to prepare for loading the value.



c) Store the address of the next instruction into $ra.