Sommaire

I) Convertisseur analogique/numérique AD7822

ANALOG DEVICES

3 V/5 V, 2 MSPS, 8-Bit, 1-, 4-, 8-Channel Sampling ADCs

AD7822/AD7825/AD7829

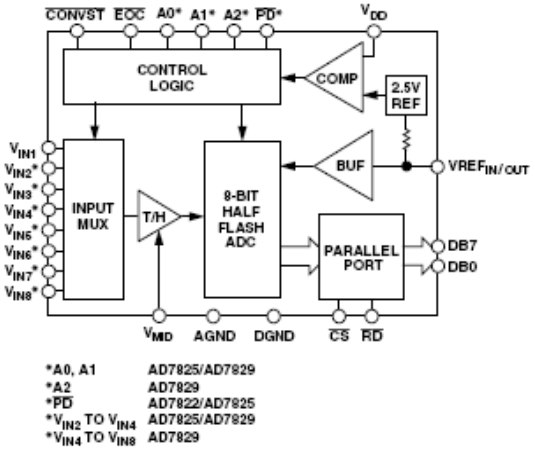
FEATURES

- 8-Bit Half-Flash ADC with 420 ns Conversion Time
- 1, 4 and 8 Single-Ended Analog Input Channels Available with Input Offset Adjust
- On-Chip Track-and-Hold
- SNR Performance Given for Input Frequencies Up to 10 MHz
- On-Chip Reference (2.5 V)
- Automatic Power-Down at the End of Conversion
- Wide Operating Supply Range
  - 3 V ± 10% and 5 V ± 10%
- Input Ranges
  - 0 V to 2 V p-p, V_{DD} = 3 V ± 10%
  - 0 V to 2.5 V p-p, V_{DD} = 5 V ± 10%
- Flexible Parallel Interface with EOC Pulse to Allow Stand-Alone Operation

APPLICATIONS

- Data Acquisition Systems, DSP Front Ends
- Disk Drives
- Mobile Communication Systems, Subsampling Applications

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7822, AD7825, and AD7829 are high speed, 1-, 4-, and 8-channel, microprocessor-compatible, 8-bit analog-to-digital converters with a maximum throughput of 2 MSPS. The AD7822, AD7825, and AD7829 contain an on-chip reference of 2.5 V (2% tolerance), a track/hold amplifier, a 420 ns 8-bit half-flash ADC and a high speed parallel interface. The converters can operate from a single 3 V ± 10% and 5 V ± 10% supply.

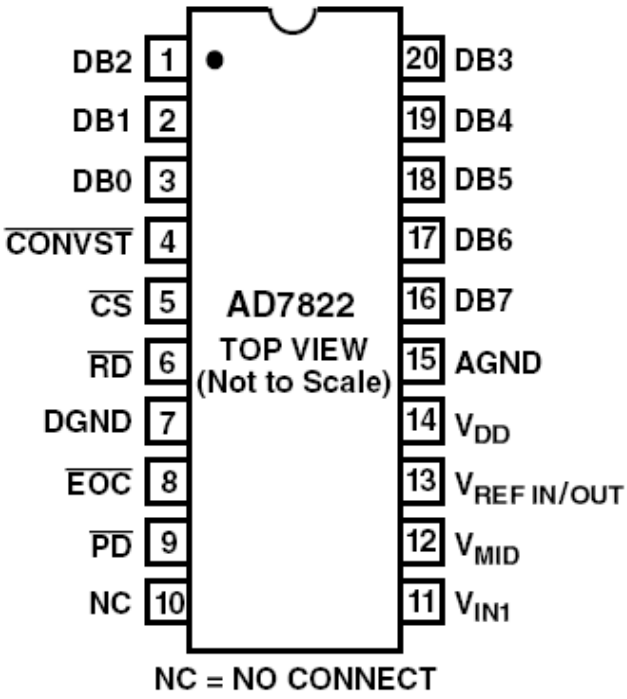
The AD7822, AD7825, and AD7829 combine the convert start and power-down functions at one pin, i.e., the $\overline{\text{CONVST}}$ pin. This allows a unique automatic power-down at the end of a conversion to be implemented. The logic level on the $\overline{\text{CONVST}}$ pin is sampled after the end of a conversion when an $\overline{\text{EOC}}$ (End of Conversion) signal goes high, and if it is logic low at that point, the ADC is powered down. The AD7822 and AD7825 also have a separate power-down pin. (See Operating Modes section of the data sheet.)

The parallel interface is designed to allow easy interfacing to microprocessors and DSPs. Using only address decoding logic, the parts are easily mapped into the microprocessor address space. The $\overline{\text{EOC}}$ pulse allows the ADCs to be used in a stand-alone manner. (See Parallel Interface section of the data sheet.)

The AD7822 and AD7825 are available in a 20-/24-lead 0.3" wide, plastic dual-in-line package (DIP), a 20-/24-lead small outline IC (SOIC) and a 20-/24-lead thin shrink small outline package (TSSOP). The AD7829 is available in a 28-lead 0.6" wide, plastic dual-in-line package (DIP), a 28-lead small outline IC (SOIC) and in a 28-lead thin shrink small outline package (TSSOP).

PRODUCT HIGHLIGHTS

1. Fast Conversion Time
   The AD7822, AD7825, and AD7829 have a conversion time of 420 ns. Faster conversion times maximize the DSP processing time in a real-time system.
2. Analog Input Span Adjustment
   The V_{MID} pin allows the user to offset the input span. This feature can reduce the requirements of single-supply op amps and take into account any system offsets.
3. FPBW (Full Power Bandwidth) of Track-and-Hold
   The track-and-hold amplifier has an excellent high-frequency performance. The AD7822, AD7825, and AD7829 are capable of converting full-scale input signals up to a frequency of 10 MHz. This makes the parts ideally suited to subsampling applications.
4. Channel Selection
   Channel selection is made without the necessity of writing to the part.



PIN FUNCTION DESCRIPTIONS

Mnemonic	Description
V_{IN1} to V_{IN8}	Analog Input Channels. The AD7822 has a single input channel; the AD7825 and AD7829 have four and eight analog input channels respectively. The inputs have an input span of 2.5 V and 2 V depending on the supply voltage (V_{DD}). This span may be centered anywhere in the range AGND to V_{DD} using the V_{MID} Pin. The default input range (V_{MID} unconnected) is AGND to 2 V (V_{DD} = 3 V ± 10%) or AGND to 2.5 V (V_{DD} = 5 V ± 10%). See Analog Input section of the data sheet for more information.
V_{DD}	Positive supply voltage, 3 V ± 10% and 5 V ± 10%.
AGND	Analog Ground. Ground reference for track/hold, comparators, reference circuit and multiplexer.
DGND	Digital Ground. Ground reference for digital circuitry.
$\overline{CONVST}$	Logic Input Signal. The convert start signal initiates an 8-bit analog-to-digital conversion on the falling edge of this signal. The falling edge of this signal places the track/hold in hold mode. The track/hold goes into track mode again 120 ns after the start of a conversion. The state of the $\overline{CONVST}$ signal is checked at the end of a conversion. If it is logic low, the AD7822/AD7825/AD7829 will power down. (See Operating Modes section of the data sheet.)
$\overline{EOC}$	Logic Output. The End of Conversion signal indicates when a conversion has finished. The signal can be used to interrupt a microcontroller when a conversion has finished or latch data into a gate array. (See Parallel Interface section of this data sheet.)
$\overline{CS}$	Logic input signal. The chip select signal is used to enable the parallel port of the AD7822, AD7825, and AD7829. This is necessary if the ADC is sharing a common data bus with another device.
$\overline{PD}$	Logic Input. The Power-Down pin is present on the AD7822 and AD7825 only. Bringing the $\overline{PD}$ pin low places the AD7822 and AD7825 in Power-Down mode. The ADCs will power up when $\overline{PD}$ is brought logic high again.
$\overline{RD}$	Logic Input Signal. The read signal is used to take the output buffers out of their high impedance state and drive data onto the data bus. The signal is internally gated with the $\overline{CS}$ signal. Both $\overline{RD}$ and $\overline{CS}$ must be logic low to enable the data bus.
A0–A2	Channel Address Inputs. The address of the next multiplexer channel must be present on these inputs when the $\overline{RD}$ signal goes low.
DB0–DB7	Data Output Lines. They are normally held in a high impedance state. Data is driven onto the data bus when both $\overline{RD}$ and $\overline{CS}$ go active low.
$V_{REF\ IN/OUT}$	Analog Input and Output. An external reference can be connected to the AD7822, AD7825, and AD7829 at this pin. The on-chip reference is also available at this pin. When using the internal reference, this pin can be left unconnected or, in some cases, it can be decoupled to AGND with a 0.1 μF capacitor.

AD7822/AD7825/AD7829

OPERATING MODES

The AD7822, AD7825, and AD7829 have two possible modes of operation, depending on the state of the $\overline{\text{CONVST}}$ pulse approximately 100 ns after the end of a conversion, i.e., upon the rising edge of the $\overline{\text{EOC}}$ pulse.

Mode 1 Operation (High-Speed Sampling)

When the AD7822, AD7825, and AD7829 are operated in Mode 1 they are not powered-down between conversions. This mode of operation allows high throughput rates to be achieved. Figure 20 shows how this optimum throughput rate is achieved by bringing $\overline{\text{CONVST}}$ high before the end of a conversion, i.e., before the $\overline{\text{EOC}}$ pulses low. When operating in this mode, a new conversion should not be initiated until 30 ns after the end of a read operation. This is to allow the track/hold to acquire the analog signal to 0.5 LSB accuracy.

Mode 2 Operation (Automatic Power-Down)

When the AD7822, AD7825, and AD7829 are operated in Mode 2 (see Figure 21), they automatically power down at the end of a conversion. The $\overline{\text{CONVST}}$ signal is brought low to initiate a conversion and is left logic low until after the $\overline{\text{EOC}}$ goes high, i.e., approximately 100 ns after the end of the conversion. The state of the $\overline{\text{CONVST}}$ signal is sampled at this point (i.e., 530 ns maximum after $\overline{\text{CONVST}}$ falling edge) and the AD7822, AD7825, and AD7829 will power down as long as $\overline{\text{CONVST}}$ is low. The ADC is powered up again on the rising edge of the $\overline{\text{CONVST}}$ signal. Superior power performance can be achieved in this mode of operation by only powering up the AD7822, AD7825, and AD7829 to carry out a conversion. The parallel interface of the AD7822, AD7825, and AD7829 is still fully operational while the ADCs are powered down. A read may occur while the part is powered down, and so it does not necessarily need to be placed within the $\overline{\text{EOC}}$ pulse as shown in Figure 21.

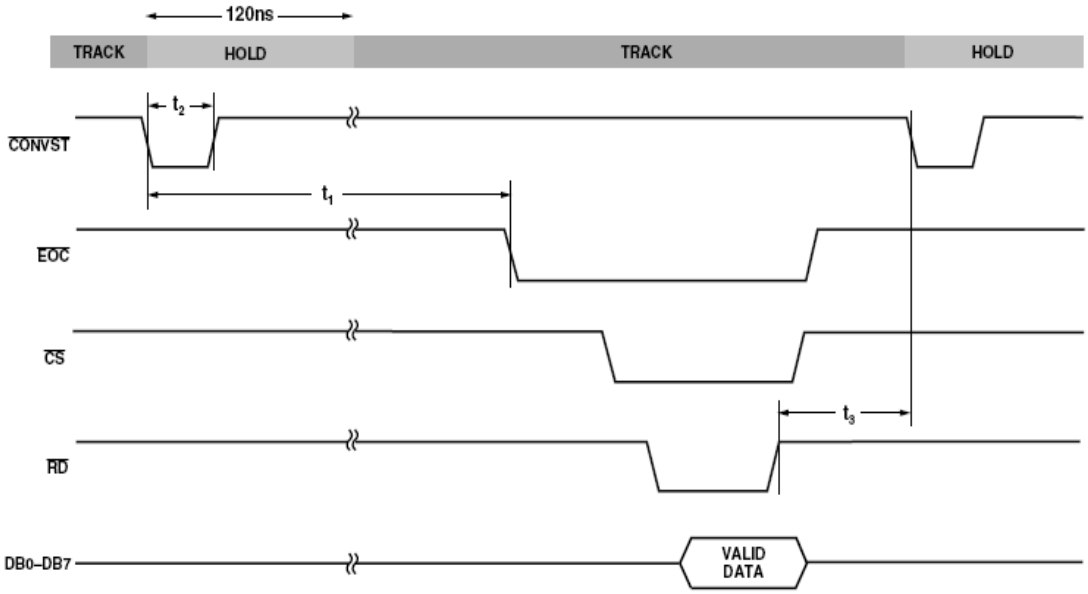


Figure 20. Mode 1 Operation

AD7822/AD7825/AD7829

TIMING CHARACTERISTICS[1, 2] ($V_{REF\ IN/OUT}$ = 2.5 V. All specifications –40°C to +85°C unless otherwise noted.)

Parameter	5 V ± 10%	3 V ± 10%	Unit	Conditions/Comments
t_1	420	420	ns max	Conversion Time.
t_2	20	20	ns min	Minimum $\overline{\text{CONVST}}$ Pulsewidth.
t_3	30	30	ns min	Minimum time between the rising edge of $\overline{\text{RD}}$ and next falling edge of convert start.
t_4	110	110	ns max	$\overline{\text{EOC}}$ Pulsewidth.
	70	70	ns min	
t_5	10	10	ns max	$\overline{\text{RD}}$ rising edge to $\overline{\text{EOC}}$ pulse high.
t_6	0	0	ns min	$\overline{\text{CS}}$ to $\overline{\text{RD}}$ setup time.
t_7	0	0	ns min	$\overline{\text{CS}}$ to $\overline{\text{RD}}$ hold time.
t_8	30	30	ns min	Minimum $\overline{\text{RD}}$ Pulsewidth.
t_9[3]	10	20	ns max	Data access time after $\overline{\text{RD}}$ low.
t_{10}[4]	5	5	ns min	Bus relinquish time after $\overline{\text{RD}}$ high.
	20	20	ns max	
t_{11}	10	10	ns min	Address setup time before falling edge of $\overline{\text{RD}}$.
t_{12}	15	15	ns min	Address hold time after falling edge of $\overline{\text{RD}}$.
t_{13}	200	200	ns min	Minimum time between new channel selection and convert start.
$t_{POWER\ UP}$	25	25	µs typ	Power-up time from rising edge of $\overline{\text{CONVST}}$ using on-chip reference.
$t_{POWER\ UP}$	1	1	µs max	Power-up time from rising edge of $\overline{\text{CONVST}}$ using external 2.5 V reference.

II) Convertisseur numérique/analogique AD7302

ANALOG DEVICES

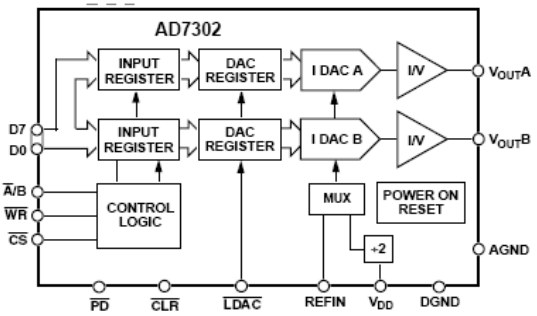
2.7 V to 5.5 V, Parallel Input Dual Voltage Output 8-Bit DAC

AD7302

FEATURES
Two 8-Bit DACs In One Package
20-Lead DIP/SOIC/TSSOP Package
+2.7 V to +5.5 V Operation
Internal and External Reference Capability
DAC Power-Down Function
Parallel Interface
On-Chip Output Buffer
Rail-to-Rail Operation
Low Power Operation 3 mA max @ 3.3 V
Power-Down to 1 μA max @ 25°C

APPLICATIONS
Portable Battery Powered Instruments
Digital Gain and Offset Adjustment
Programmable Voltage and Current Sources
Programmable Attenuators

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7302 is a dual, 8-bit voltage out DAC that operates from a single +2.7 V to +5.5 V supply. Its on-chip precision output buffers allow the DAC outputs to swing rail to rail. The AD7302 has a parallel microprocessor and DSP-compatible interface with high speed registers and double buffered interface logic. Data is loaded to the registers on the rising edge of $\overline{CS}$ or $\overline{WR}$ and the $\overline{A}$/B pin selects either DAC A or DAC B.

Reference selection for AD7302 can be either an internal reference derived from the V_{DD} or an external reference applied at the REFIN pin. Both DACs can be simultaneously updated using the asynchronous $\overline{LDAC}$ input and can be cleared by using the asynchronous $\overline{CLR}$ input.

The low power consumption of this part makes it ideally suited to portable battery operated equipment. The power consumption is less than 10 mW at 3.3 V, reducing to 3 μW in power-down mode.

The AD7302 is available in a 20-pin plastic dual-in-line package, 20-lead SOIC and a 20-lead TSSOP package.

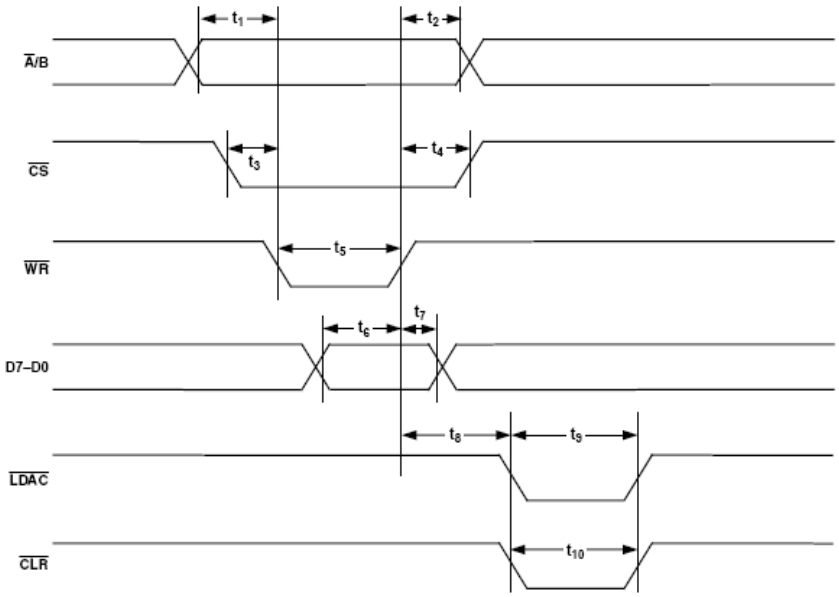
PRODUCT HIGHLIGHTS

1. Low Power, Single Supply Operation. This part operates from a single +2.7 V to +5.5 V supply and typically consumes 15 mW at 5 V, making it ideal for battery powered applications.
2. The on-chip output buffer amplifiers allow the outputs of the DACs to swing rail to rail with a settling time of typically 1.2 μs.
3. Internal or external reference capability.
4. High speed parallel interface.
5. Power-Down Capability. When powered down the DAC consumes less than 1 μA at 25°C.
6. Packaged in 20-lead DIP, SOIC and TSSOP packages.

TIMING CHARACTERISTICS[1, 2] (V_{DD} = +2.7 V to +5.5 V; GND = 0 V; Reference = Internal V_{DD}/2 Reference; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Units	Conditions/Comments
t_1	0	ns min	Address to Write Setup Time
t_2	0	ns min	Address Valid to Write Hold Time
t_3	0	ns min	Chip Select to Write Setup Time
t_4	0	ns min	Chip Select to Write Hold Time
t_5	20	ns min	Write Pulse Width
t_6	15	ns min	Data Setup Time
t_7	4.5	ns min	Data Hold Time
t_8	20	ns min	Write to $\overline{\text{LDAC}}$ Setup Time
t_9	20	ns min	$\overline{\text{LDAC}}$ Pulse Width
t_{10}	20	ns min	$\overline{\text{CLR}}$ Pulse Width

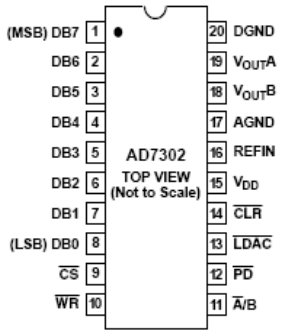
NOTES
[1]Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. tr and tf should not exceed 1 µs on any digital input.
[2]See Figure 1.



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1-8	D7–D0	Parallel Data Inputs. Eight-bit data is loaded to the input register of the AD7302 under the control of $\overline{CS}$ and $\overline{WR}$.
9	$\overline{CS}$	Chip Select. Active low logic input.
10	$\overline{WR}$	Write Input. $\overline{WR}$ is an active low logic input used in conjunction with $\overline{CS}$ and $\overline{A}$/B to write data to the selected DAC register.
11	$\overline{A}$/B	DAC Select. Address pin used to select writing to either DAC A or DAC B.
12	$\overline{PD}$	Active low input used to put the part into low power mode reducing current consumption to less than 1 μA.
13	$\overline{LDAC}$	Load DAC Logic Input. When this logic input is taken low both DAC outputs are simultaneously updated with the contents of their DAC registers. If $\overline{LDAC}$ is permanently tied low, the DACs are updated on the rising edge of $\overline{WR}$.
14	$\overline{CLR}$	Asynchronous Clear Input (Active Low). When this input is taken low the DAC registers are loaded with all zeroes and the DAC outputs are cleared to zero volts.
15	V_{DD}	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V and should be decoupled to AGND.
16	REFIN	External Reference Input. This can used as the reference for both DACs. The range on this reference input is 1 V to $V_{DD}/2$. If REFIN is directly tied to V_{DD} the internal $V_{DD}/2$ reference is selected.
17	AGND	Analog Ground reference point and return point for all analog current on the part.
18	$V_{OUT}B$	Analog output voltage from DAC B. The output amplifier can swing rail to rail on its output.
19	$V_{OUT}A$	Analog output voltage from DAC A. The output amplifier can swing rail to rail on its output.
20	DGND	Digital Ground reference point and return point for all digital current on the part.

PIN CONFIGURATION

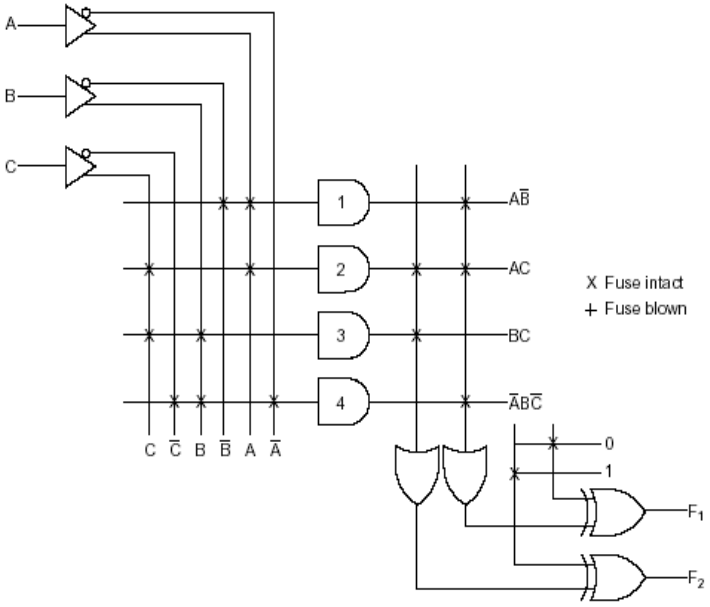


III) Field-Programmable Gate Array: FPGA

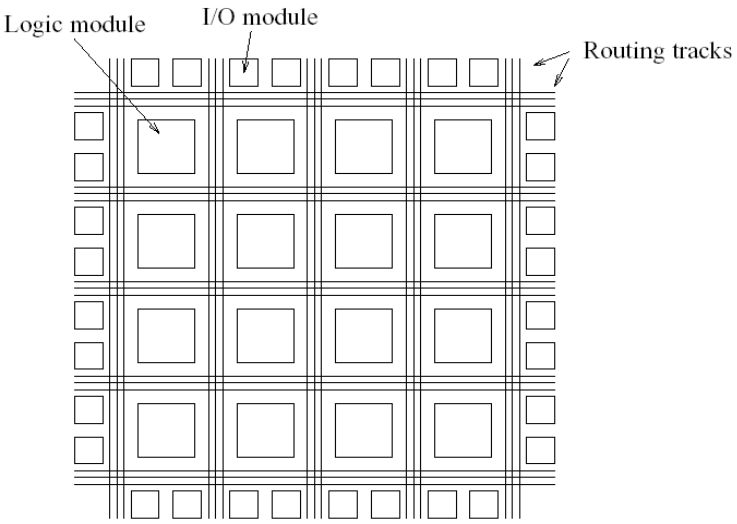
III.1) What is a FPGA?

The FPGA is a high capacity programmable logic arrays (PLA).

A PLA is based on the idea that logic functions can be realized in sum-of-products form (e.g._ A programmable AND array followed by a programmable OR array. See below).



A FPGA consists of an array of programmable basic logic cells surrounded by programmable interconnect. They have been introduced in 1985 by Xilinx.



FPGAs can be configured/programmed by end-users (field-programmable) to implement specific circuitry. They can implement combinational and sequential logic.

Capacity: 1K to 1M logic gates.

Speed: up to 100MHz.

Popular applications: prototyping, FPGA-based computers, on-site hardware reconfiguration, DSP, logic emulation, network components, etc.

Advantages: low engineering cost (ideal for low-volume production), fast turnaround time.

Disadvantages: lower performance than ASIC and larger chip size.

III.2) Architectures

III.2.1) Logic Cell Architecture

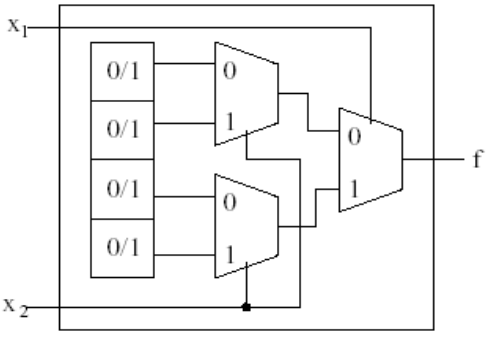
FPGA are made up of a set of basic logic cells (logic modules). A basic logic cell has a fixed number of inputs and outputs, and can implement a certain set of functions.

Logic cells used in FPGAs:

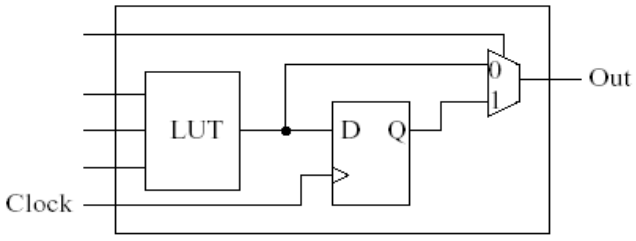
- multiplexer based (e.g. Actel)
- lookup-table based (e.g. Xilinx, Lucent)

Look-up table based logic cells :

- A lookup-table (LUT) is a segment of SRAM e.g. a 5-input LUT is a 32-bit SRAM. Any functions of up to K variables can be implemented by a K-input LUT.
- Flip-flop can be incorporated into a LUT-based logic cell to implement sequential logic.



A 2-input LUT



A fine-grained logic block with a flip-flop.

III.2.2) Routing Architecture

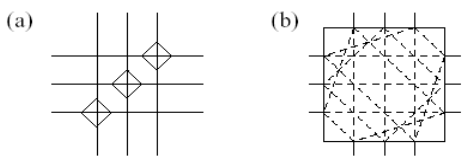
The routing architecture determines the way in which programmable switches and wiring segments are positioned.

Routability: capability of an FPLD to accommodate all nets of a typical design.

Speed: keep propagation delay low.

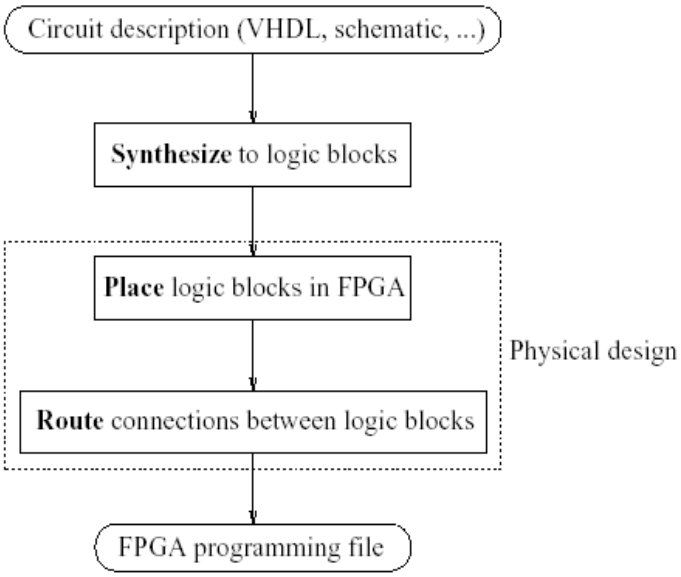
III.2.3) Switches

Programmable switches usually occupy large areas, so the number of switches that can be placed in a switch module is limited



(a) Xilinx XC4000-type switch module. (b) Its abstract representation showing what terminals can be connected.

III.3) The FPGA CAD Flow



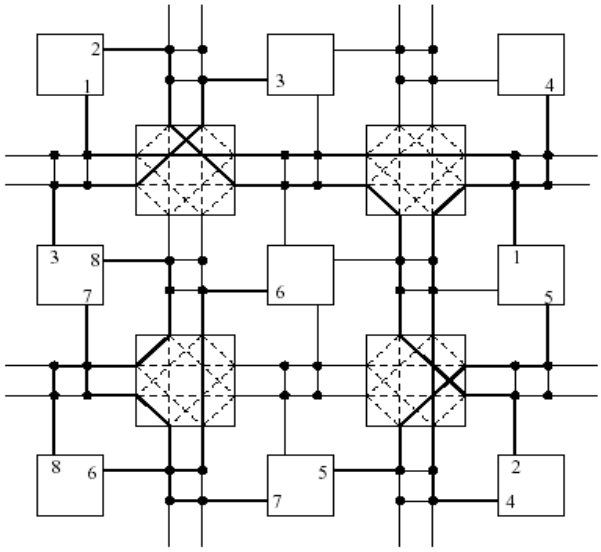
III.3.1) Placement

Goal: to determine which logic block within an FPGA should implement each of the logic blocks required by the circuit.

Objective: to minimize the required wiring (wire length driven placement), balance the wiring density across the FPGA (routability driven placement) and maximize circuit speed (timing driven placement).

III.3.2) Routing

The routing resources of an FPGA are made up of prefabricated wire segments of various lengths and programmable switches. Once the locations for all logic blocks in a circuit have been chosen, a router assigns the nets of the circuit to the routing segments of the FPGA and determines which programmable switches will be turned on/off, to connect the logic blocs as required by the circuit. The feasibility of FPGA design is constrained more by routing resources than by logic resources. The routing delays most limit the performances of the FPGA.



IV) Banc de test matériel pour le filtrage numérique

Le banc matériel pour tester le filtre numérique comporte deux cartes :

- une carte principale construite autour d'un FPGA Spartan 3 de Xilinx (carte *Spartan 3 Starter Board* de Digilent)
- une carte fille spécifique réalisée au CIME Nanotech

La carte fille réunie deux chaines (dénommées respectivement chaine A et chaine B) identiques. Chaque chaine est constituée d'un convertisseur analogique vers numérique AD7822 et d'un convertisseur numérique vers analogique AD7302 d'Analog Devices. Les signaux de contrôle de ces convertisseurs sont ressortis sur des plots de test. Ils sont reliés à la carte FPGA via deux connecteurs HE14. L'entré analogique du CAN (`AnaIn`) et la sortie analogique du CNA (`AnaOut`) sont branchées à des connecteurs SMB pour des connexions par câble coaxial.

Le CNA AD7302 est double. Seul le convertisseur DAC B est utilisé ici, aussi bien dans la chaine A que dans la chaine B. Les signaux $\overline{\texttt{PD}}$ et $\overline{\texttt{A/B}}$ sont en effet connectés directement au V_{DD} sur la carte fille.

La dynamique des signaux analogiques, `AnaIn` et `AnaOut`, est comprise entre 0 et 3 V.

La figure 1 donne un schéma d'implantation simplifié du banc de test matériel dont une image est donnée fig. 2

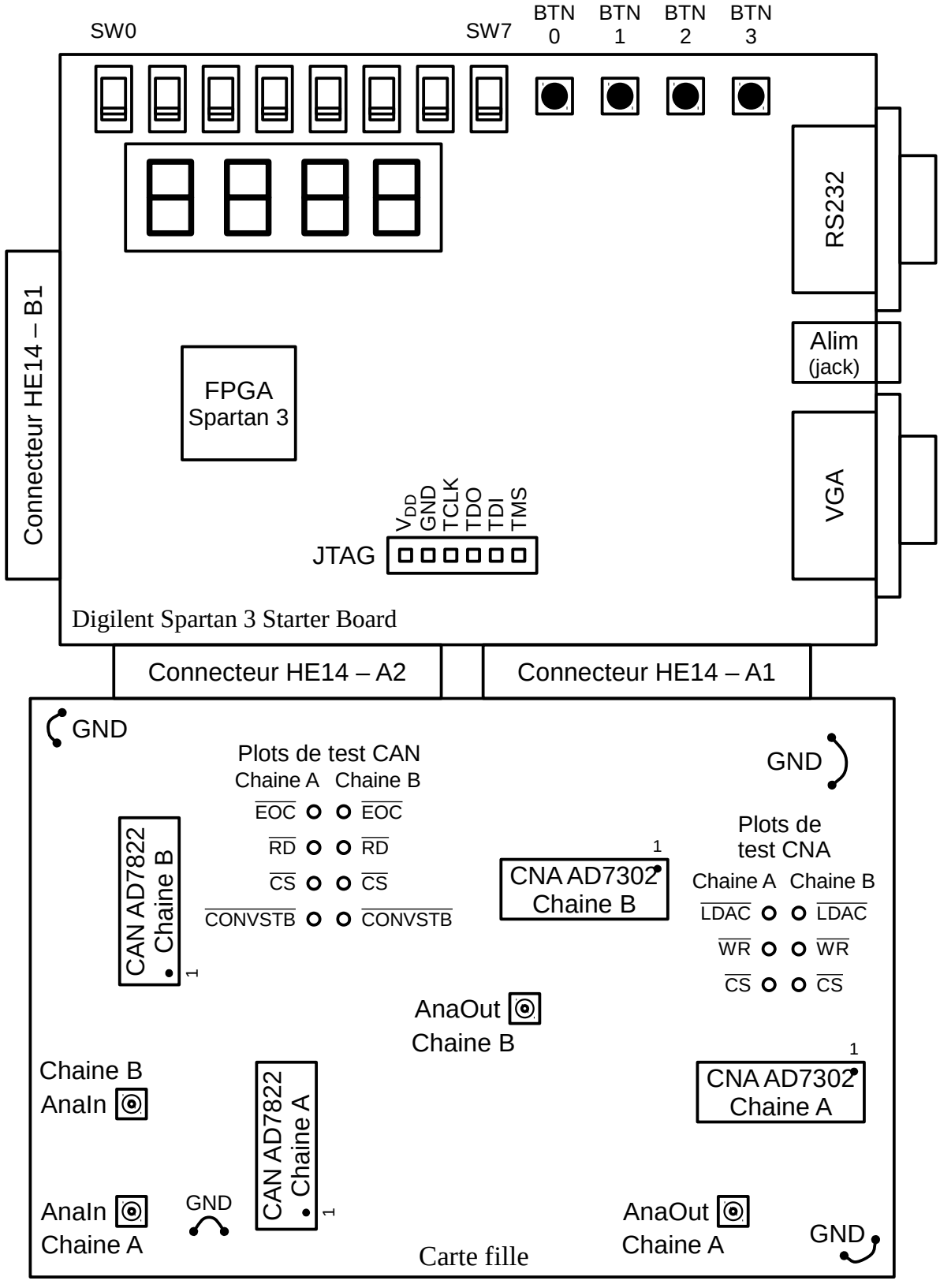
La tableau 1 indique le brochage du FPGA pour les signaux en entrée et en sortie du filtre numérique à implanter dans le FPGA.

ATTENTION
Les noms des signaux employés dans la description matérielle du filtre (voir fichier `filtre.vhd`) ne sont pas identiques aux noms dans les fiches techniques des convertisseurs (voir chapitres I et II). Le tableau 1 donne la correspondance entre les noms utilisés dans la description matérielle du filtre et ceux des convertisseurs.
Les noms des plots de test de la carte fille correspondent aux noms dans les fiches techniques des convertisseurs.

Tableau 1: brochage du FPGA pour le pilotage des CAN et des CNA

Nom du signal dans le VHDL	Nom du signal sur le banc de test ou le convertisseur	Broche du FPGA	Remarque
CLK	CLK	T9	Horloge 50 MHz
RESET	RESET	L14	Bouton poussoir BTN3 L'appui sur le bouton envoi un 1 logique
Filter_In(7)	DB7	B12	CAN AD7822
Filter_In(6)	DB6	A3	CAN AD7822
Filter_In(5)	DB5	C8	CAN AD7822
Filter_In(4)	DB4	D8	CAN AD7822
Filter_In(3)	DB3	L5	CAN AD7822
Filter_In(2)	DB2	N8	CAN AD7822
Filter_In(1)	DB1	N7	CAN AD7822
Filter_In(0)	DB0	B5	CAN AD7822
ADC_Eocb	$\overline{\text{EOC}}$	E6	CAN AD7822
ADC_Convstb	$\overline{\text{CONVST}}$	E7	CAN AD7822 Désigné par $\overline{\text{CONVSTB}}$ sur la carte fille
ADC_Rdb	$\overline{\text{RD}}$	D7	CAN AD7822
ADC_csb	$\overline{\text{CS}}$	C7	CAN AD7822

Nom du signal dans le VHDL	Nom du signal sur le banc de test ou le convertisseur	Broche du FPGA	Remarque
Filter_Out(7)	DB7	T8	CNA AD7302
Filter_Out(6)	DB6	M4	CNA AD7302
Filter_Out(5)	DB5	R6	CNA AD7302
Filter_Out(4)	DB4	M3	CNA AD7302
Filter_Out(3)	DB3	T5	CNA AD7302
Filter_Out(2)	DB2	L4	CNA AD7302
Filter_Out(1)	DB1	R5	CNA AD7302
Filter_Out(0)	DB0	C2	CNA AD7302
DAC_WRb	$\overline{WR}$	C6	CNA AD7302
DAC_csb	$\overline{CS}$	D5	CNA AD7302
LDACb	$\overline{LDAC}$	N5	CNA AD7302
CLRB	$\overline{CLR}$	C1	CNA AD7302



Dynamique du signal analogique
en entrée : 0 à 3V
en sortie : 0 à 3V

Fig. 1 : Implantation simplifiée du banc de test pour le filtre numérique

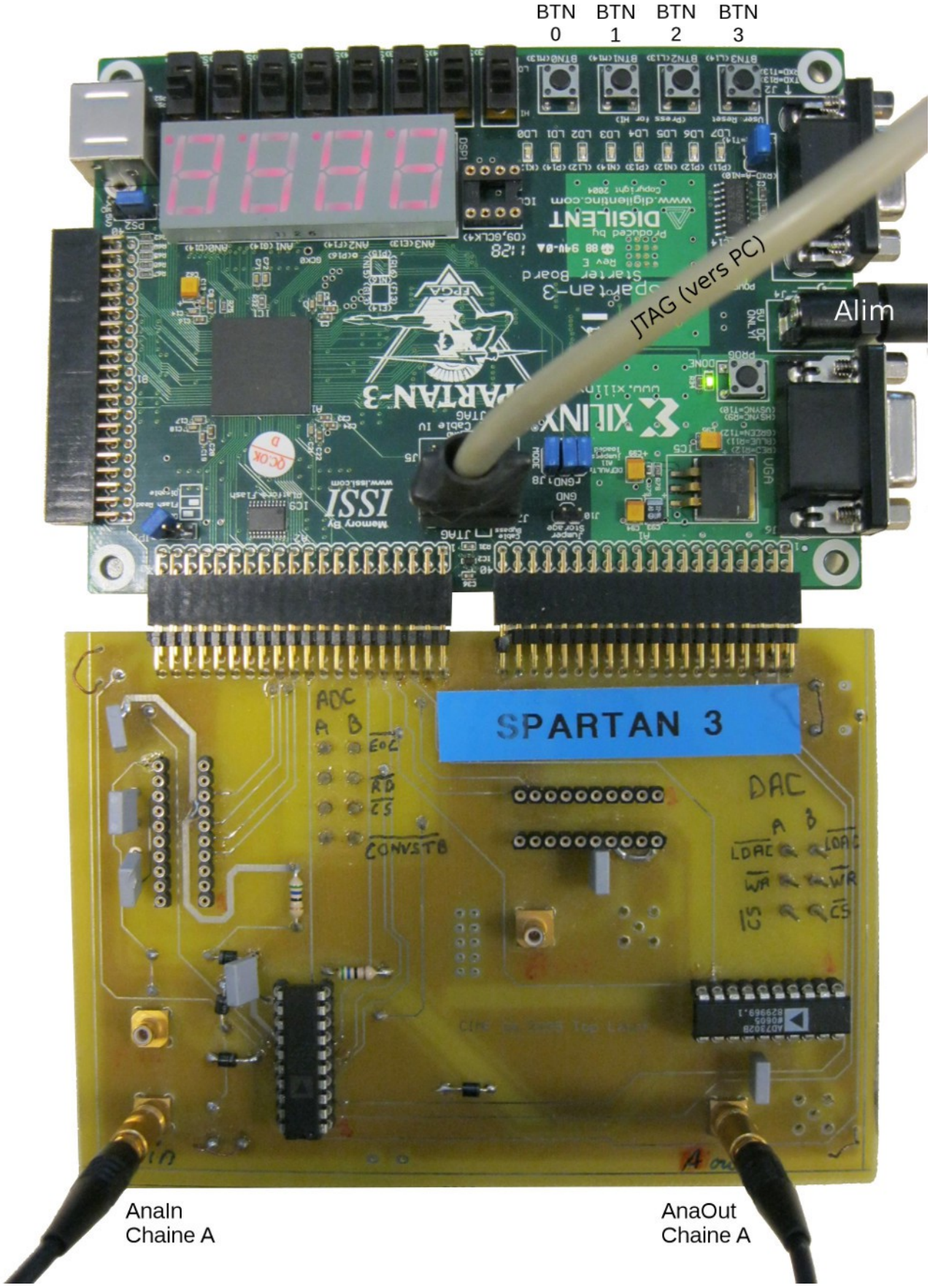


Fig. 2 : Vue du banc de test pour le filtre numérique