Georgia Tech Computer Science

CS2200
Systems and Networks
Spring 2024

Lecture 23: Programmed IO & DMA

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Lecture slides adapted from Bill Leahy and Charles Lively of Georgia Tech

Roadmap

- Wrap up parallel systems
  - Hardware support for threads
- Programmed IO and DMA
  - Chapter 10 (10.1 – 10.7)
- Networking
  - Chapter 13

Synchronization support in a uniprocessor

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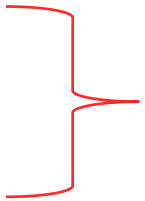

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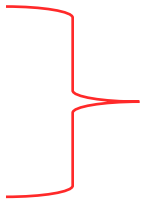
Synchronization support in a uniprocessor

- Thread creation/termination
- Communication among threads
- Synchronization among threads
  - How do we implement mutex_lock?



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But now we ARE the OS!

Lock() using machine instructions

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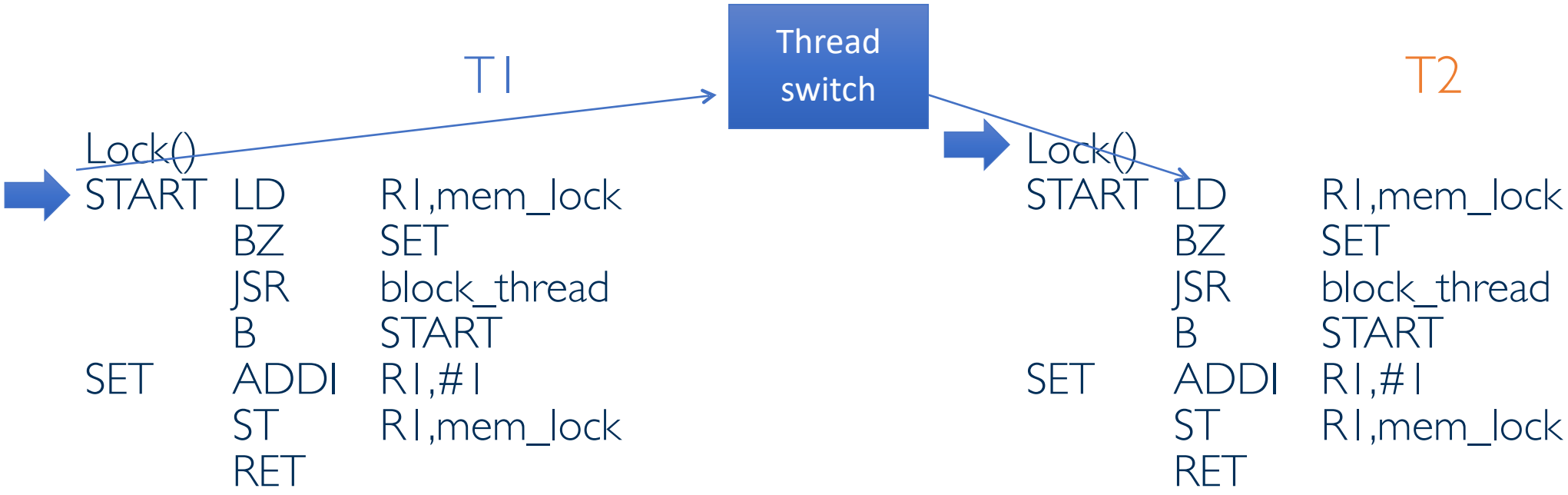

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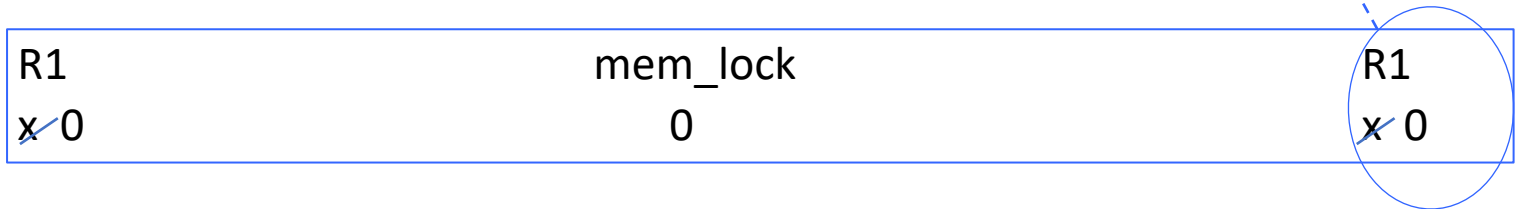

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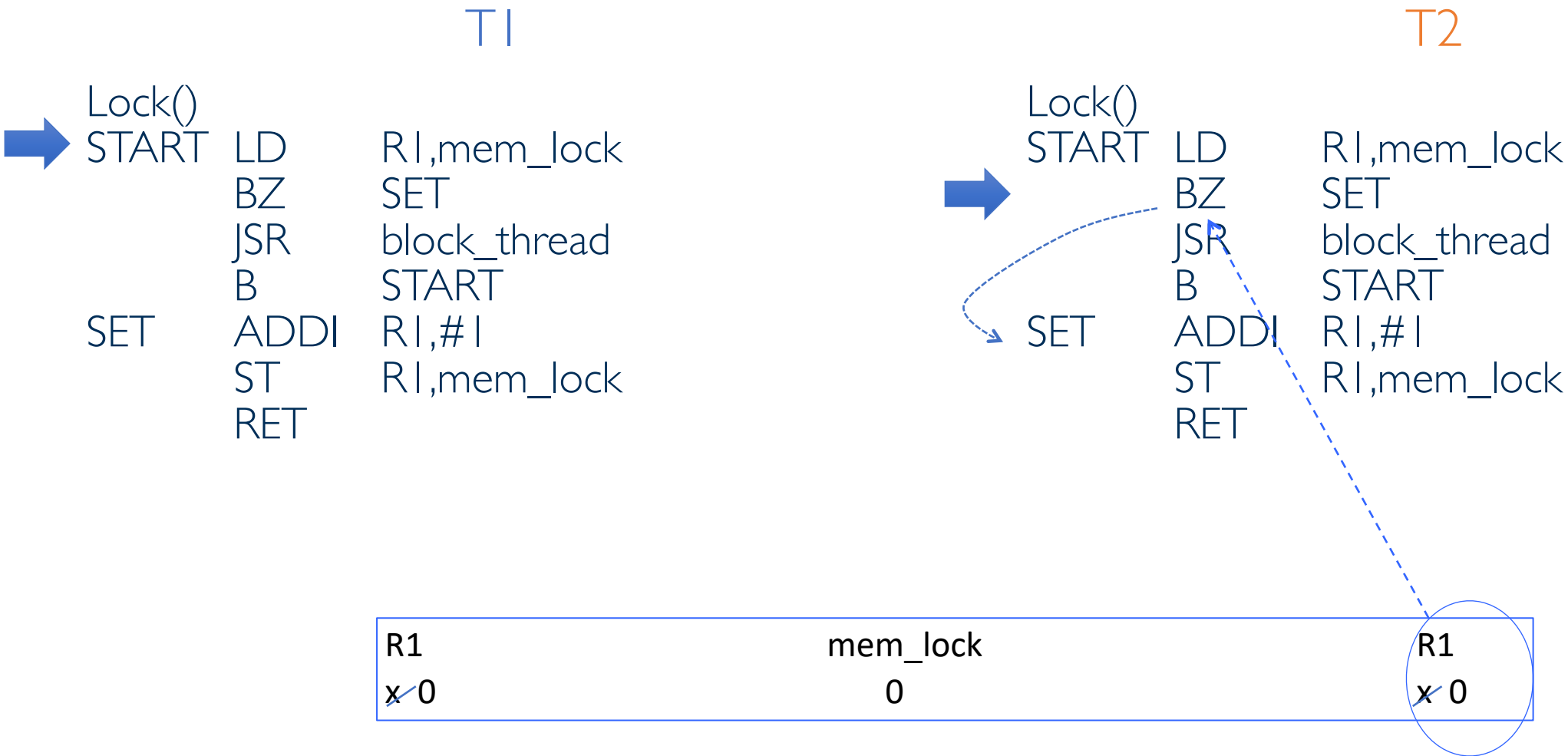

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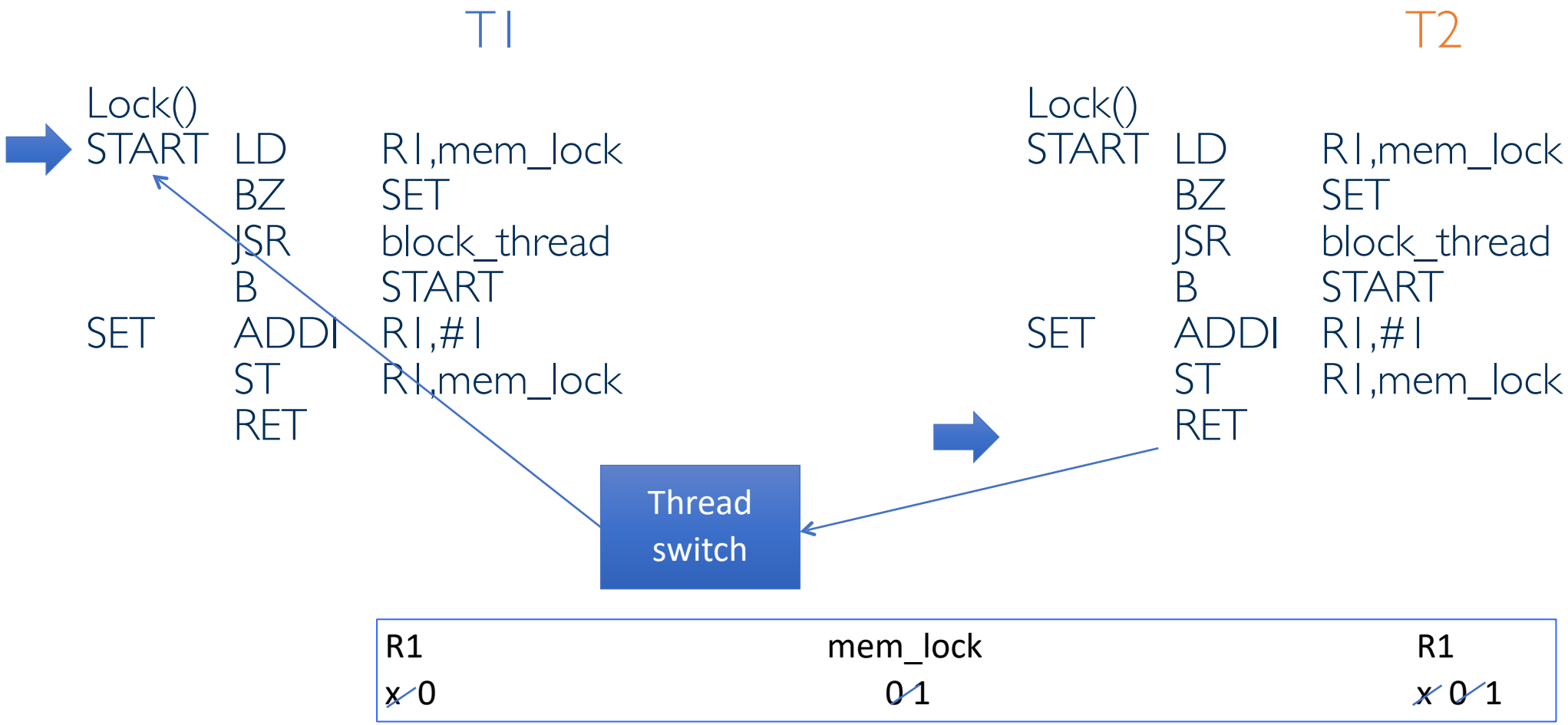

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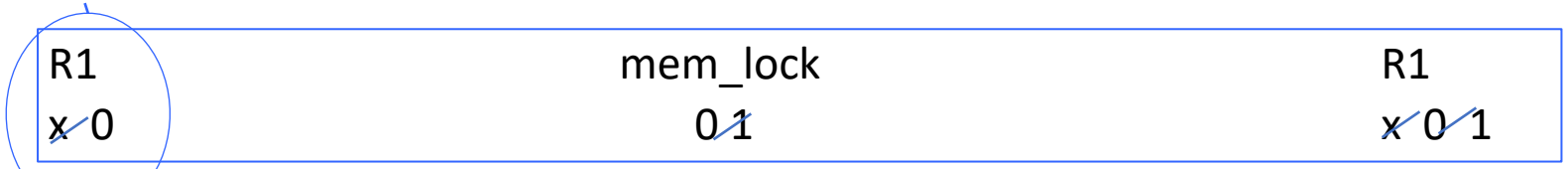

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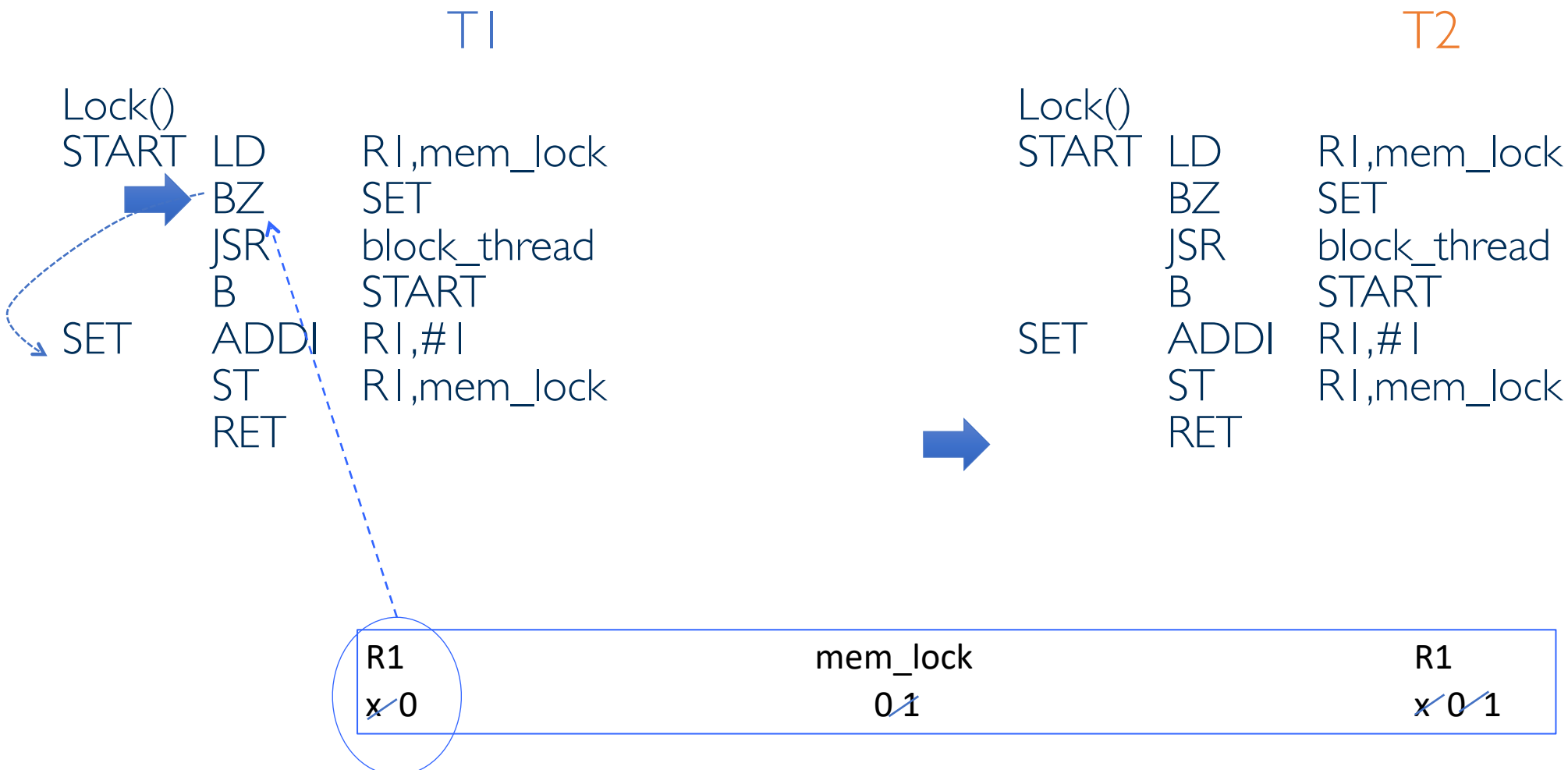

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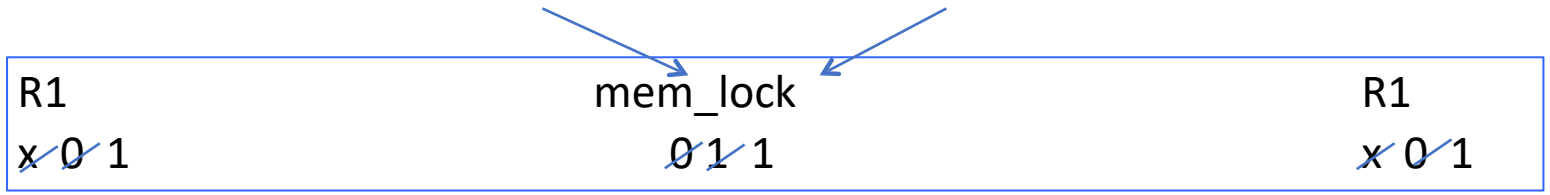

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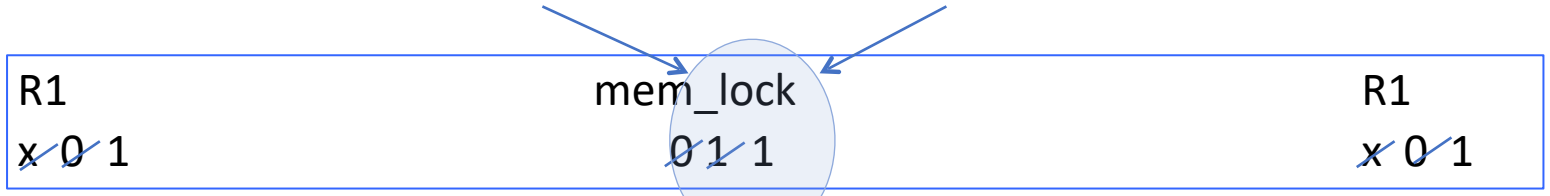

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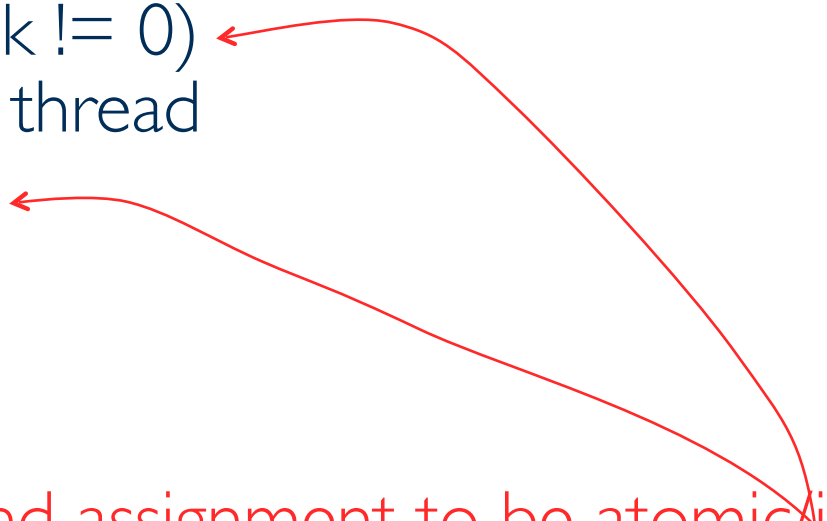

- We need the test and assignment to be atomic/indivisible!

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- Work-alikes
  - Compare-and-swap (IBM 370)
  - Fetch-and-add (Intel x86)
  - Load-linked/store-conditional (MIPS, ARM, …)

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- Lock():
  while (test-and-set (&mem_lock))
  block the thread

Unlock():
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Example: Implementing Mutex Lock

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static int shared-lock =  0; /* global variable to
                                both T1 and T2 */
/* shared procedure for T1 and T2 */
int binary-semaphore(int *L)
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        int X;

        X = test-and-set(L);

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Getting 0 0 isn't possible!

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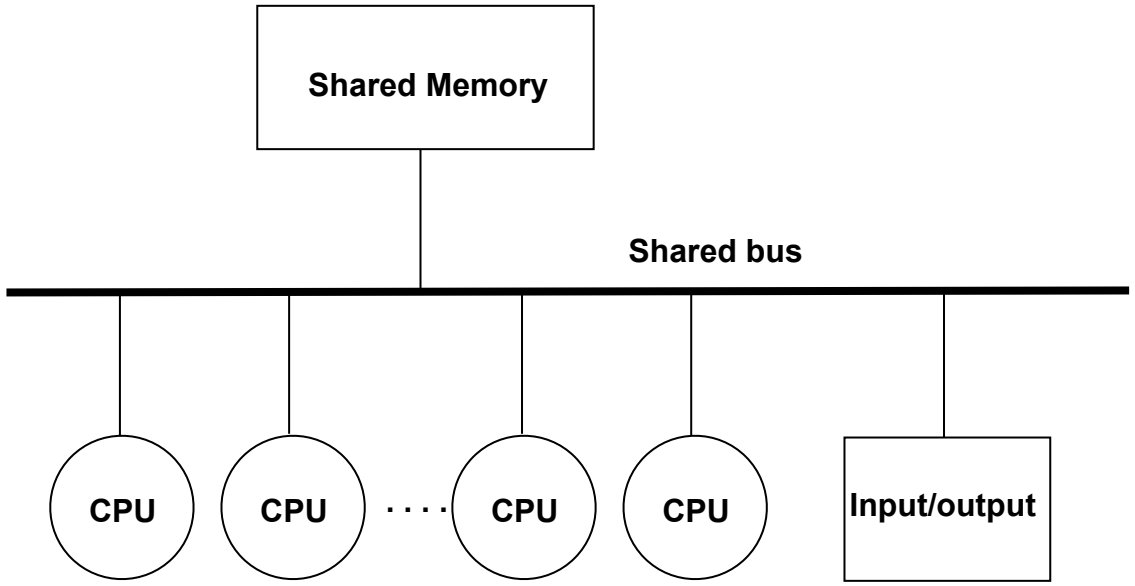

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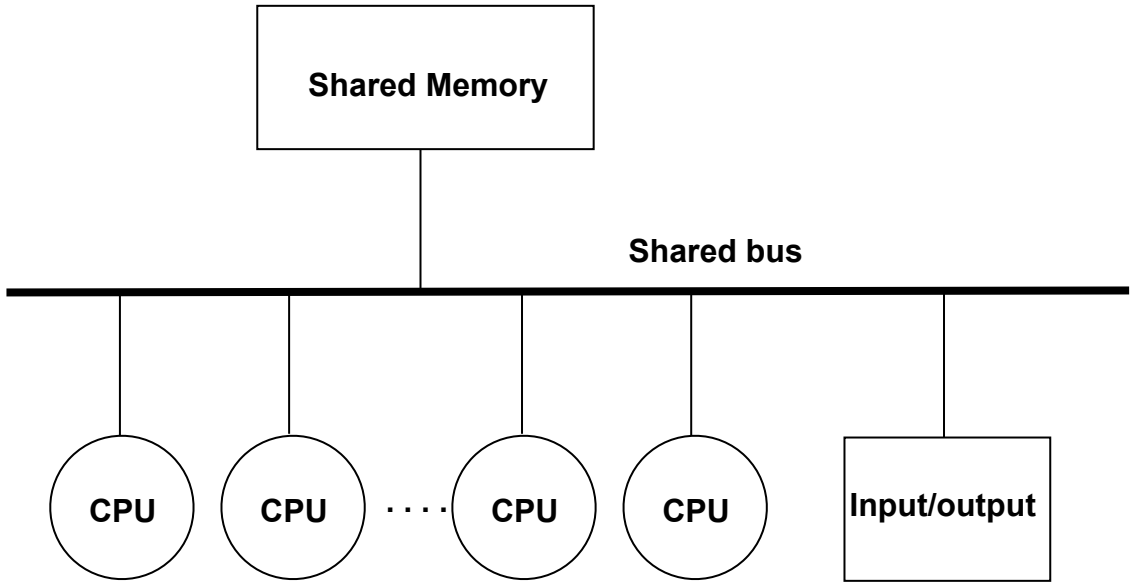

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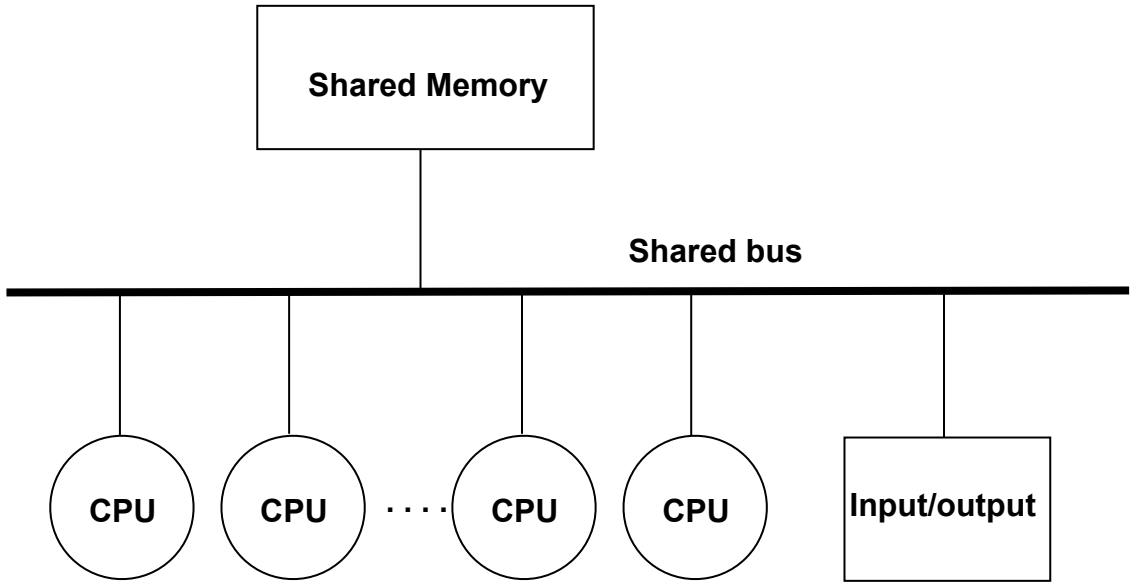

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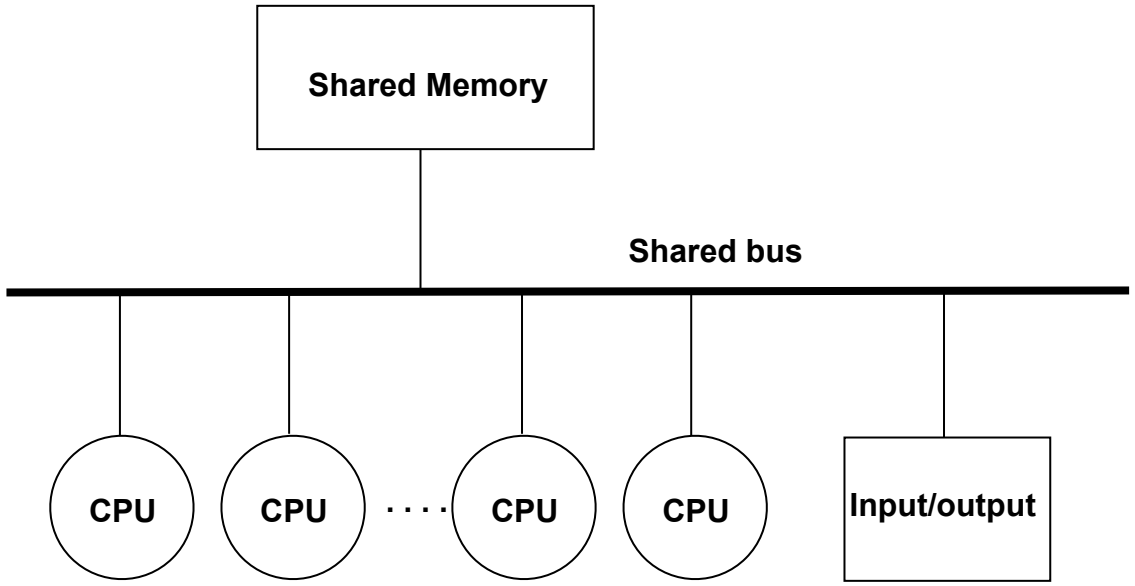

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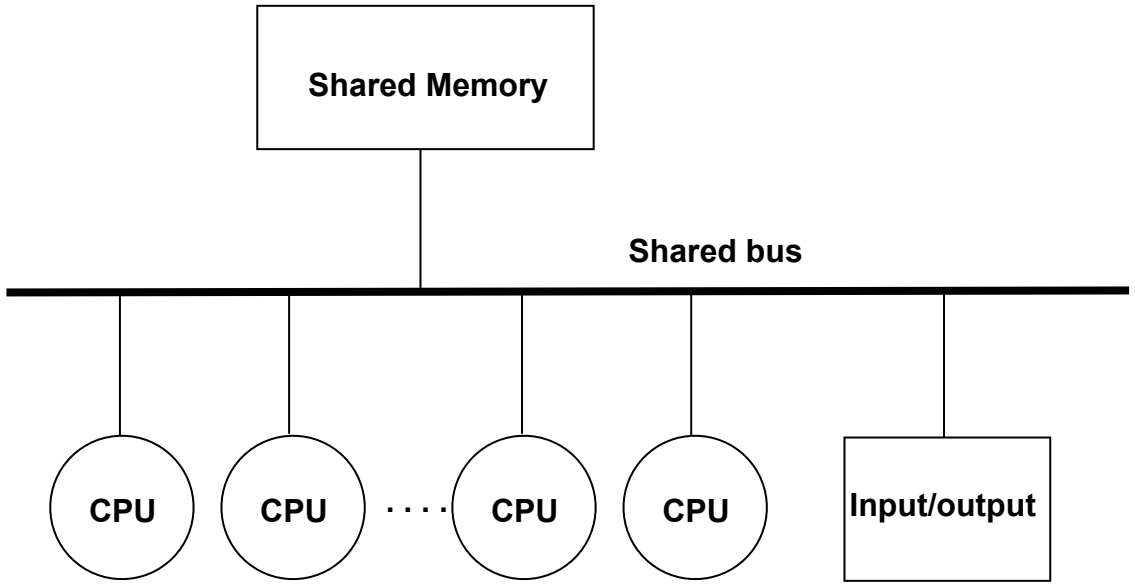

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2. Threads have synchronization atomicity
3. Threads have identical views of memory

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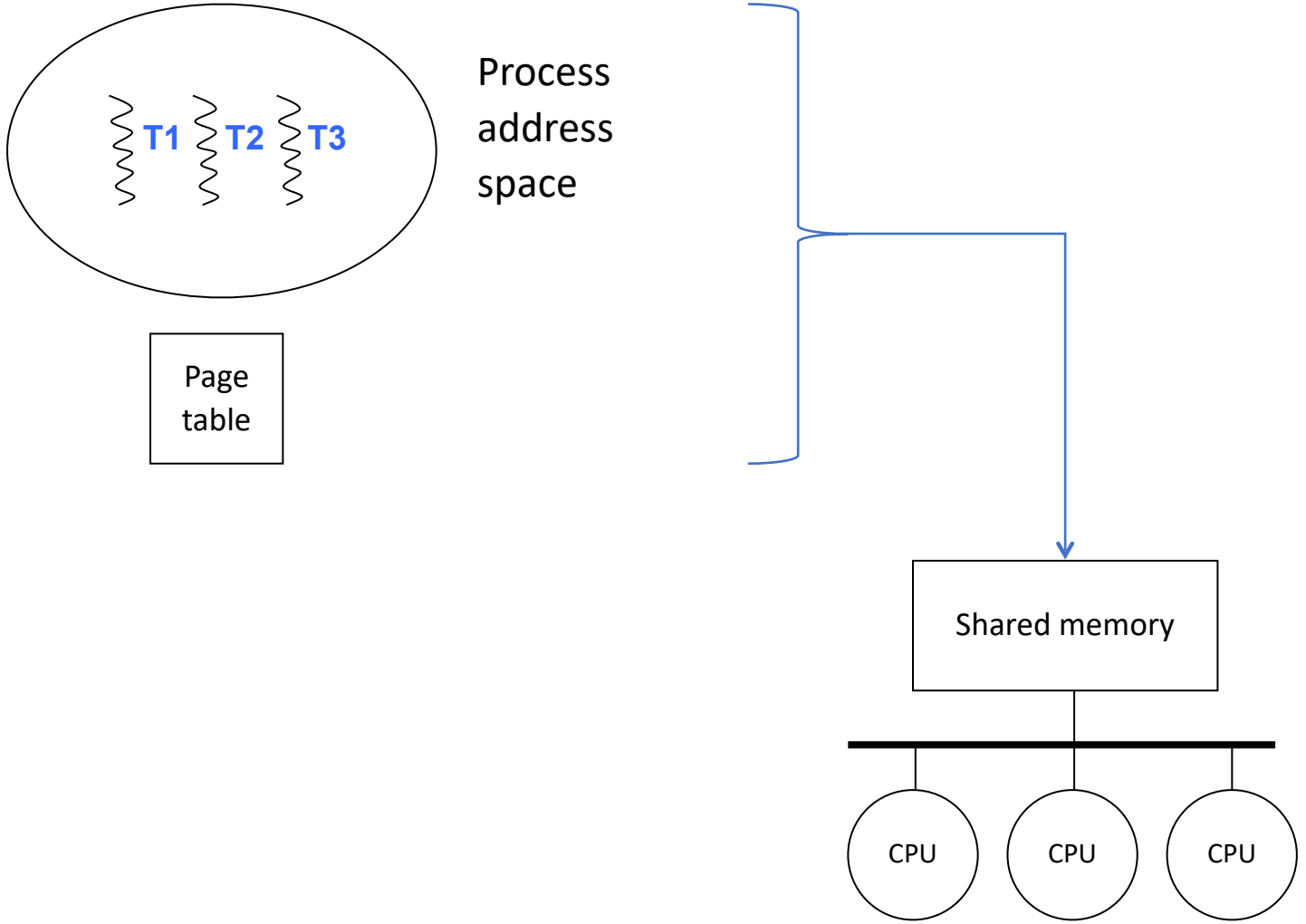

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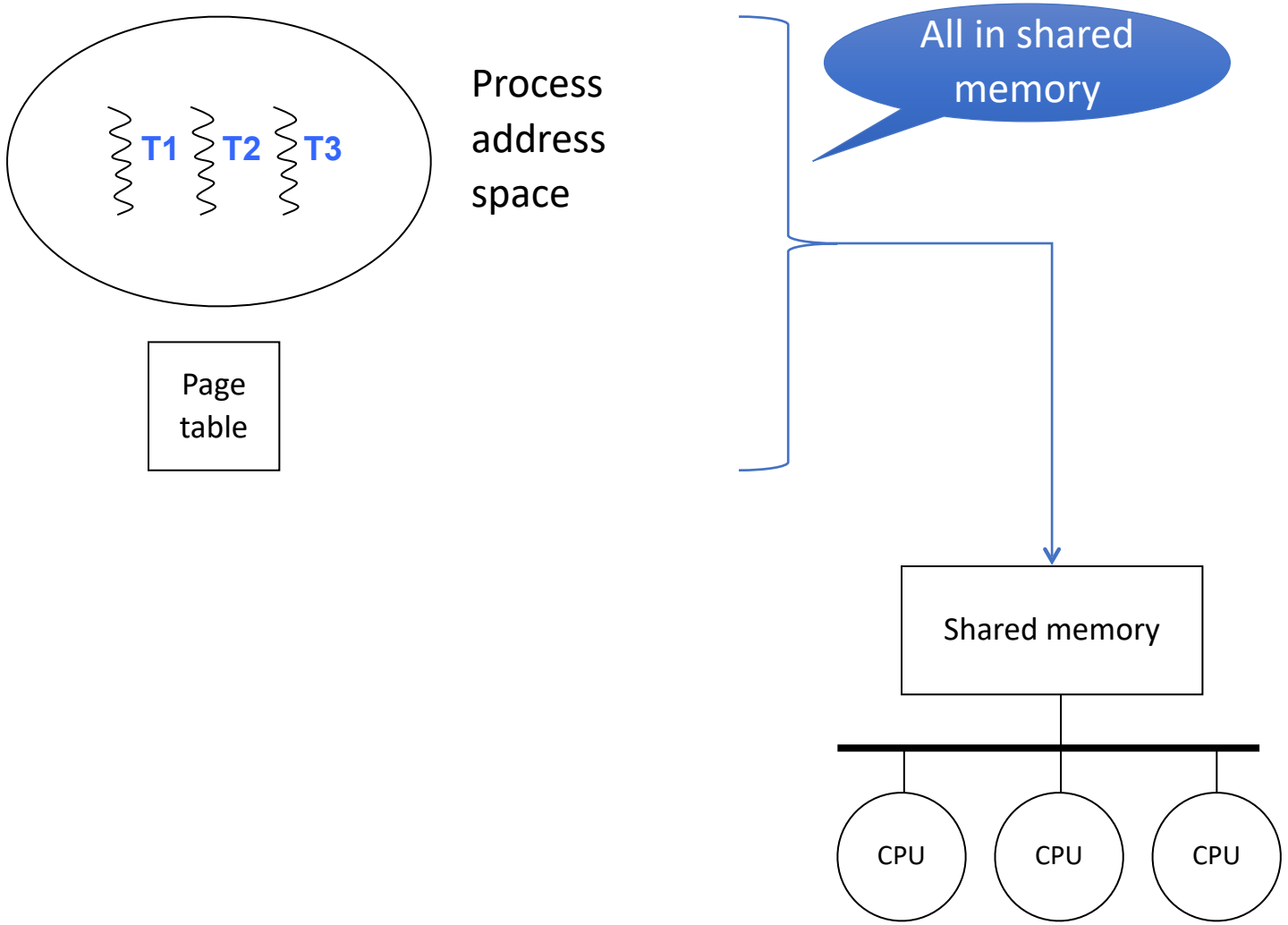

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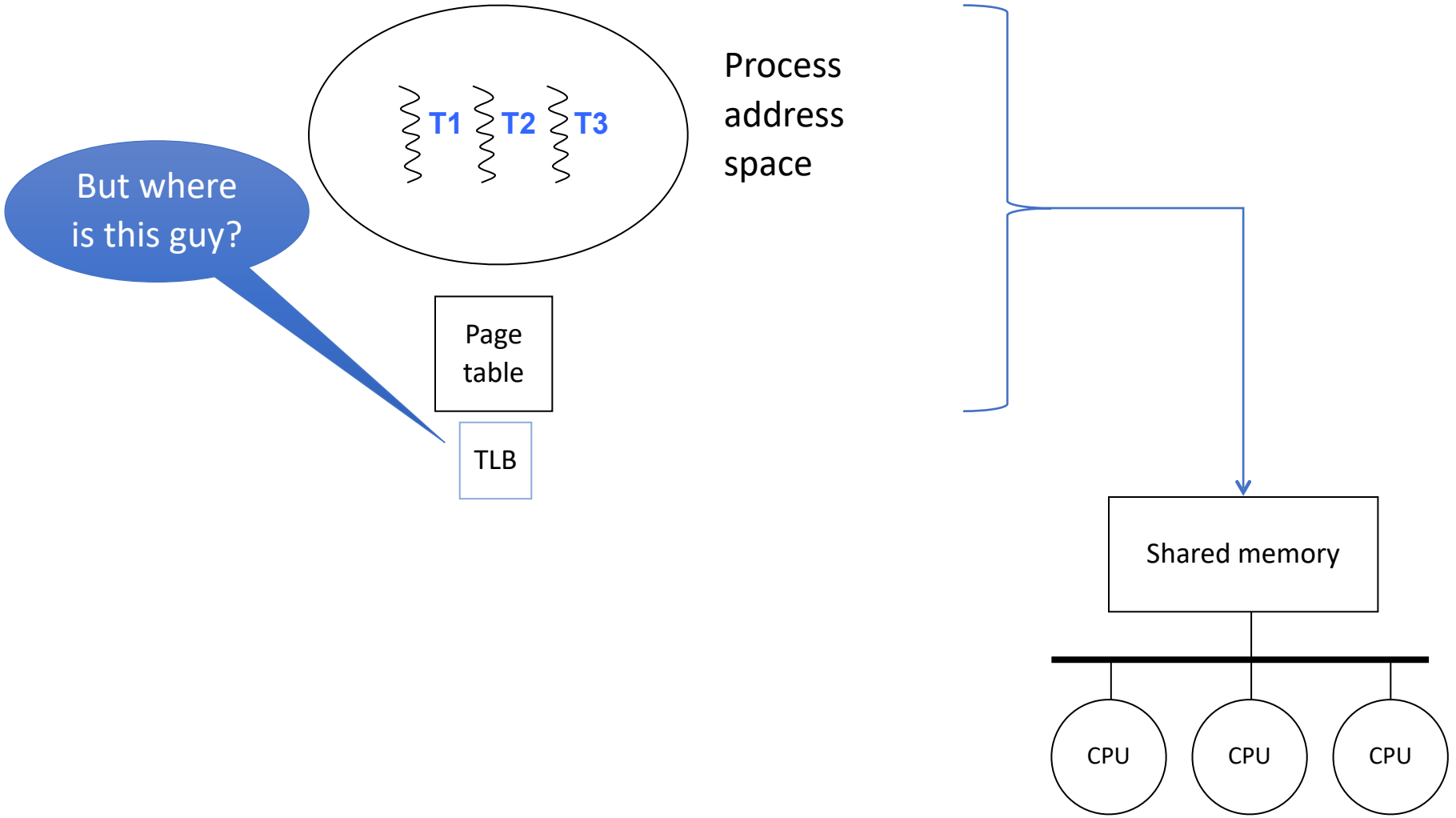

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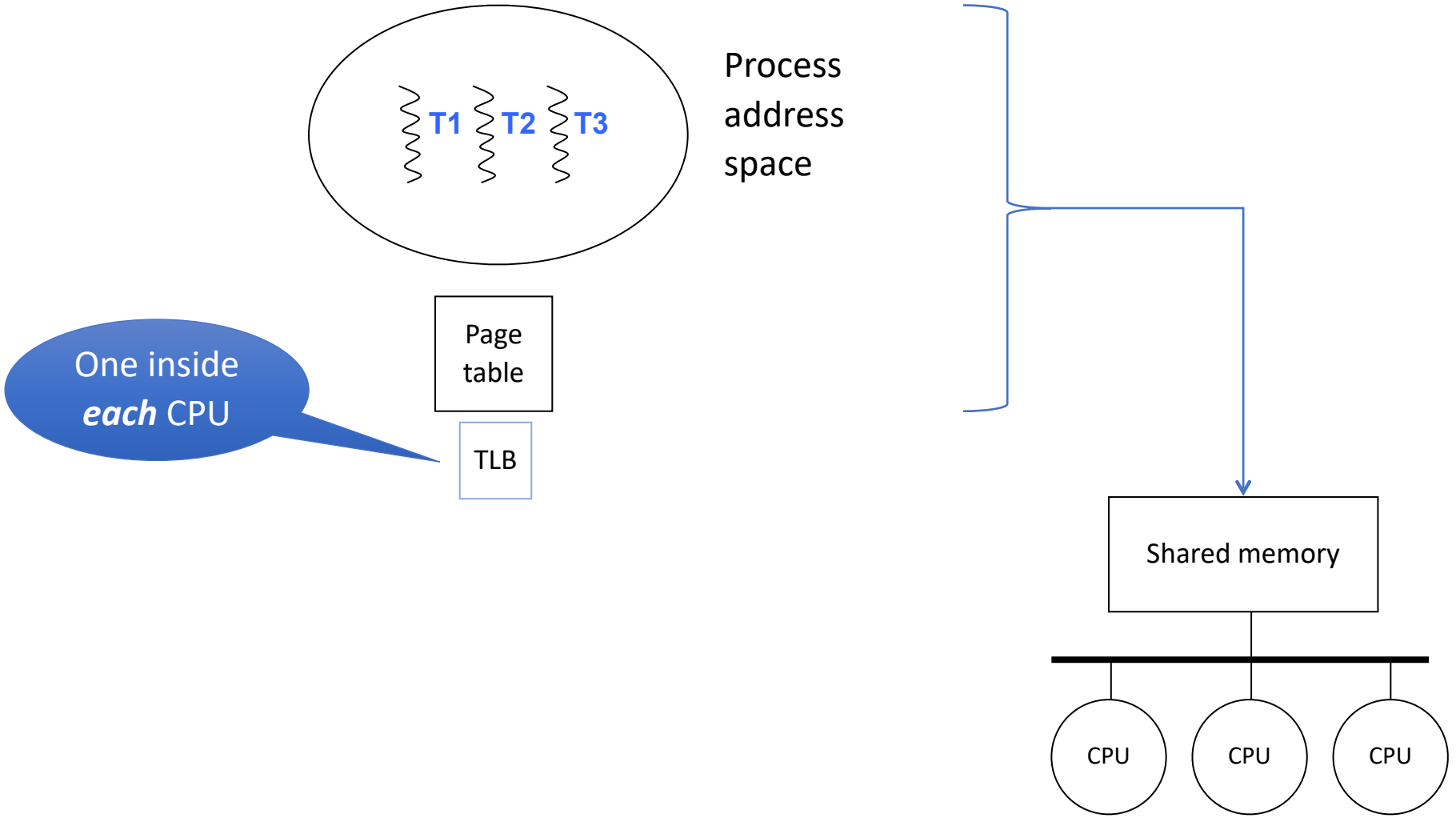

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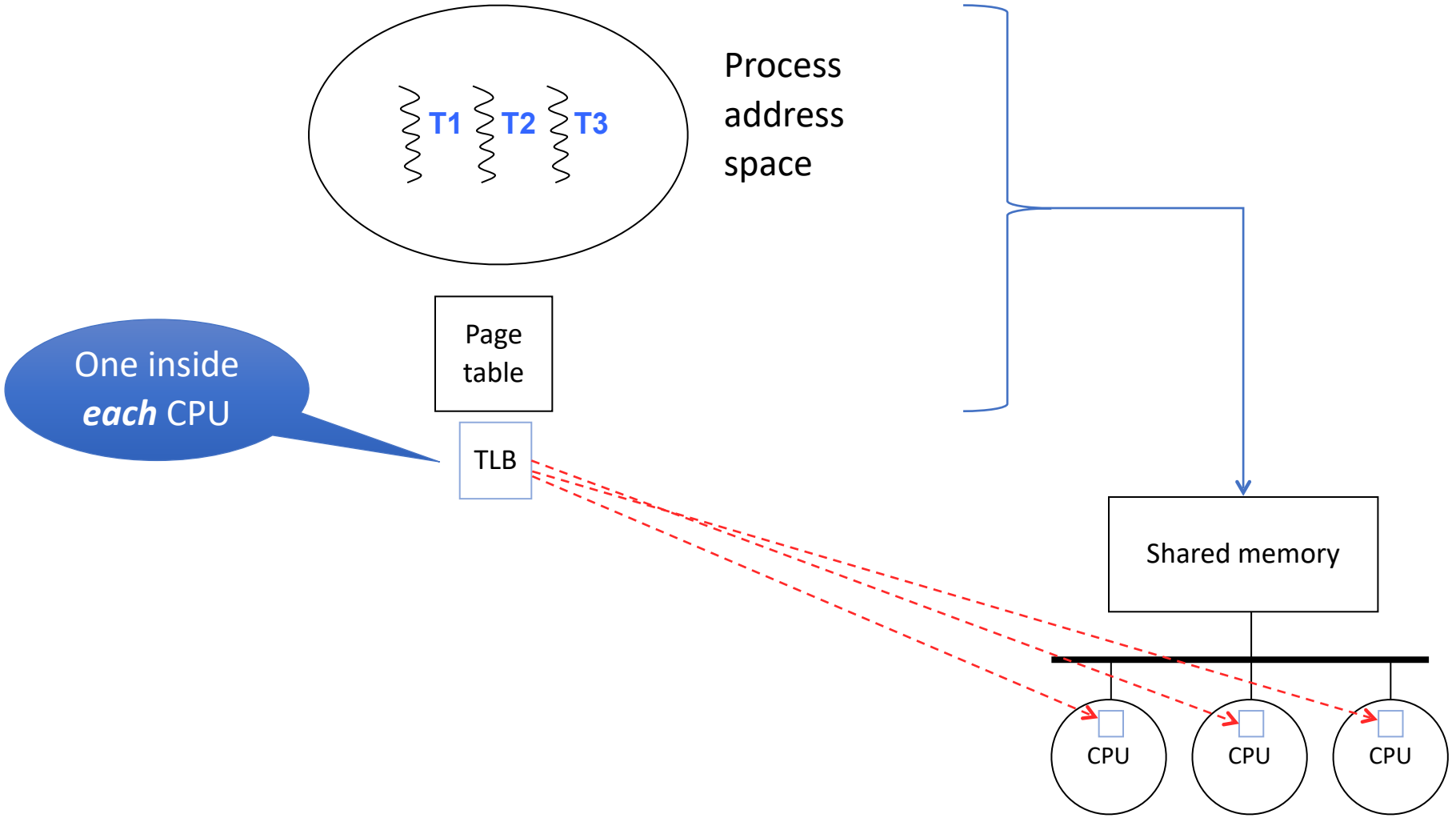

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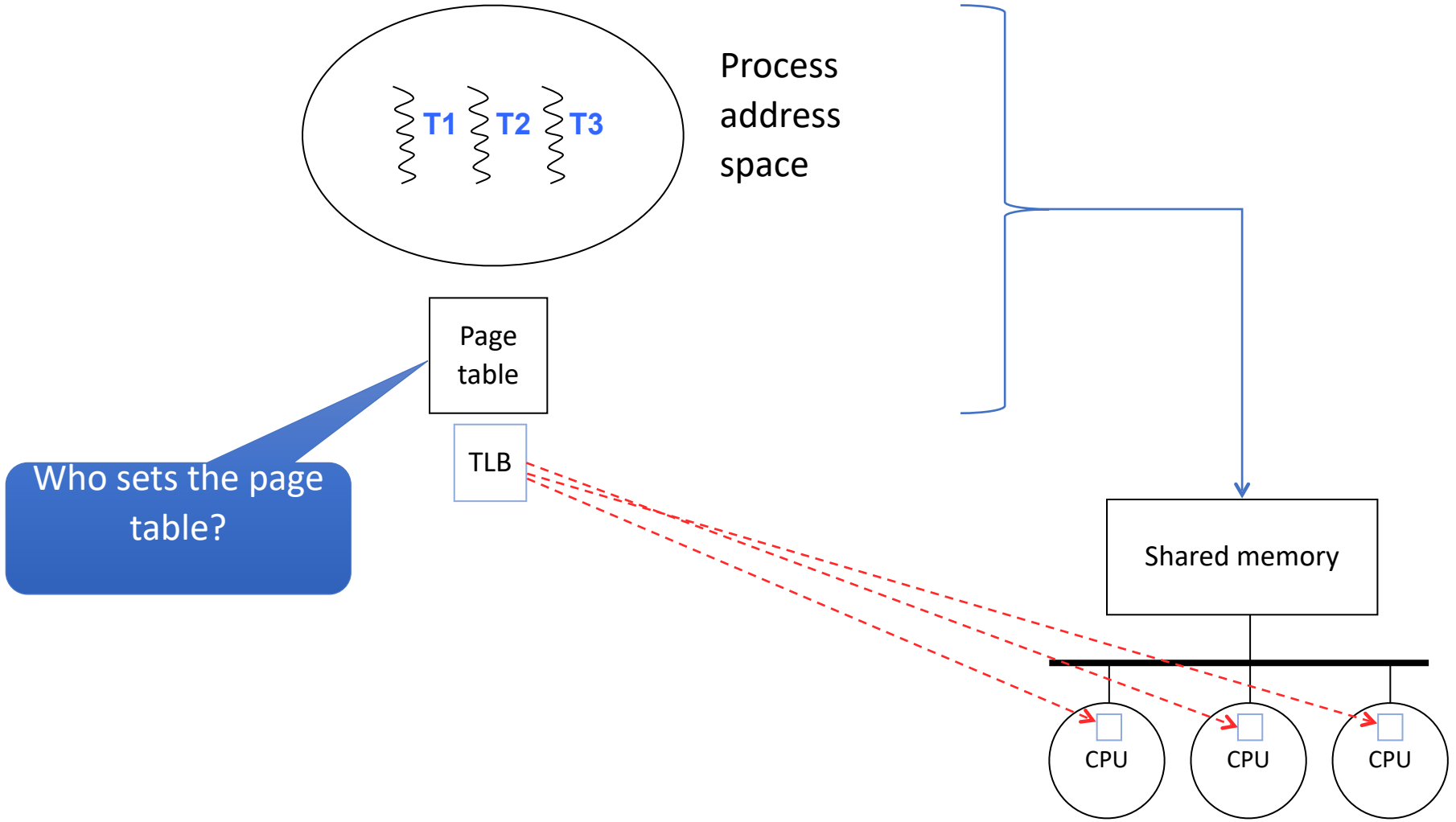

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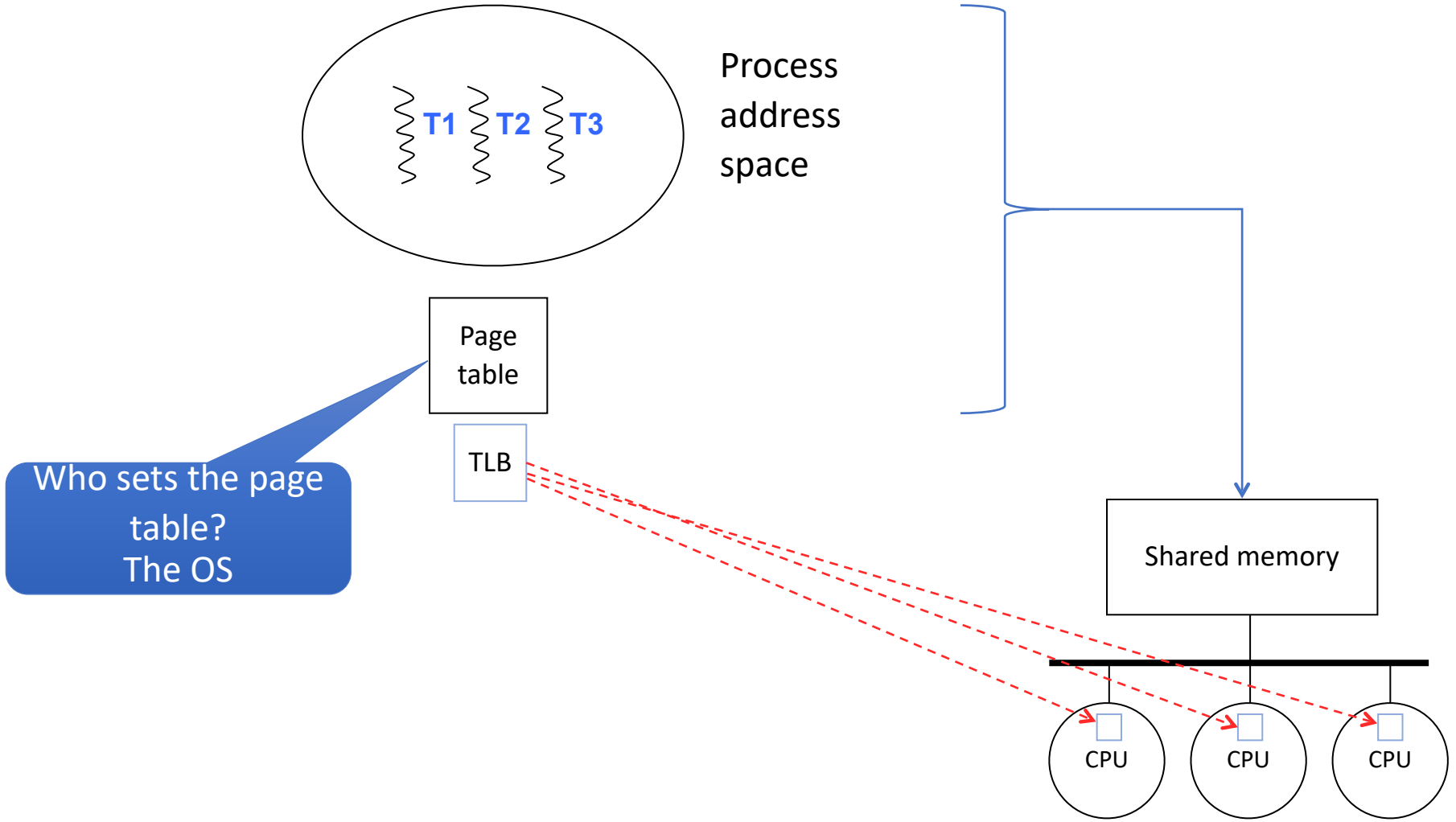

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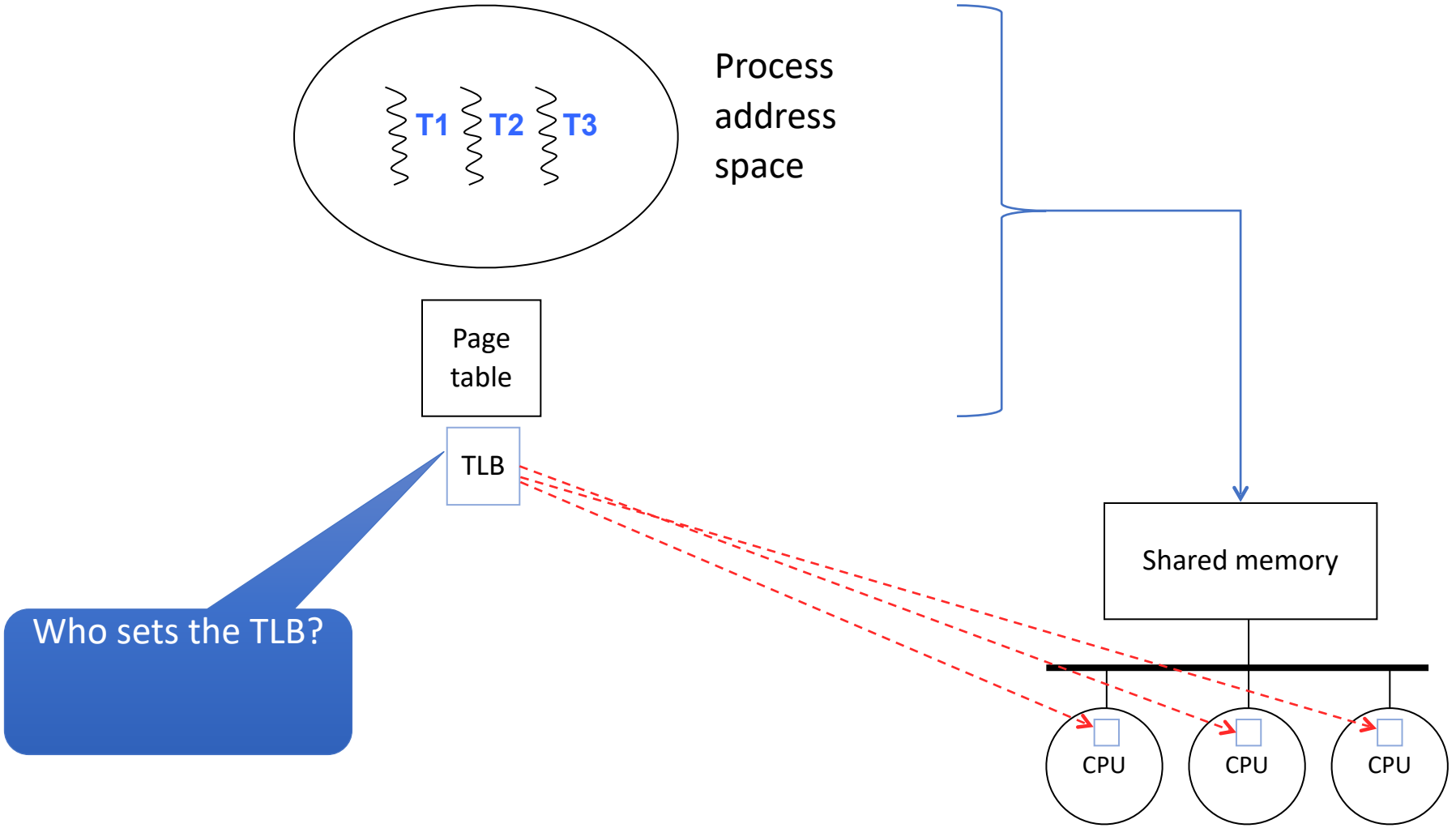

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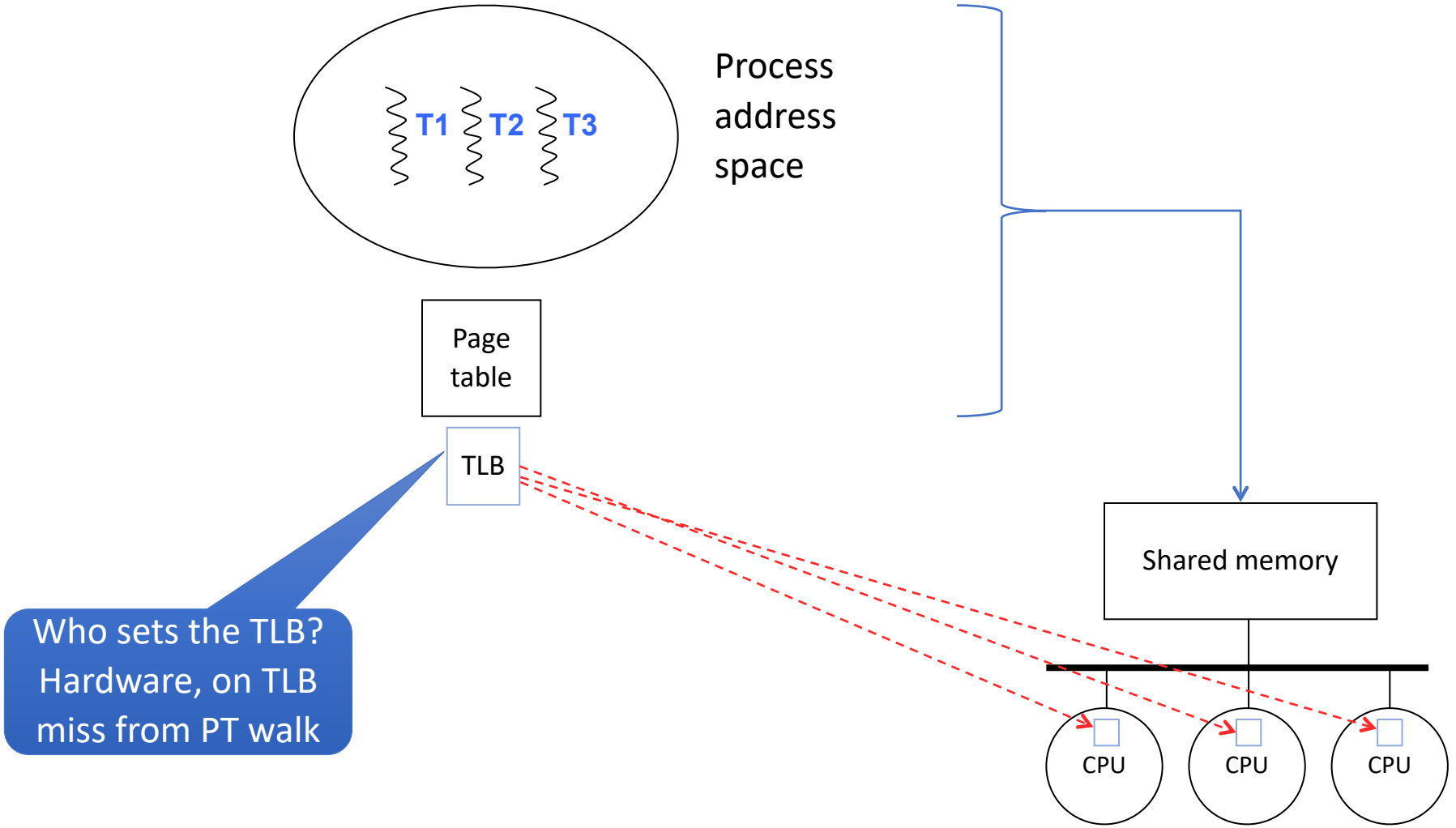

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SMP context switch handling

- As in the single-CPU case, the TLB must be flushed of user-space addresses on context switch
- How do multiple processors complicate this?
  - Basically, they don't
  - Any time a CPU is switched to a new thread, the OS flushes user entries from that CPU's TLB
  - There's no need to affect other TLBs

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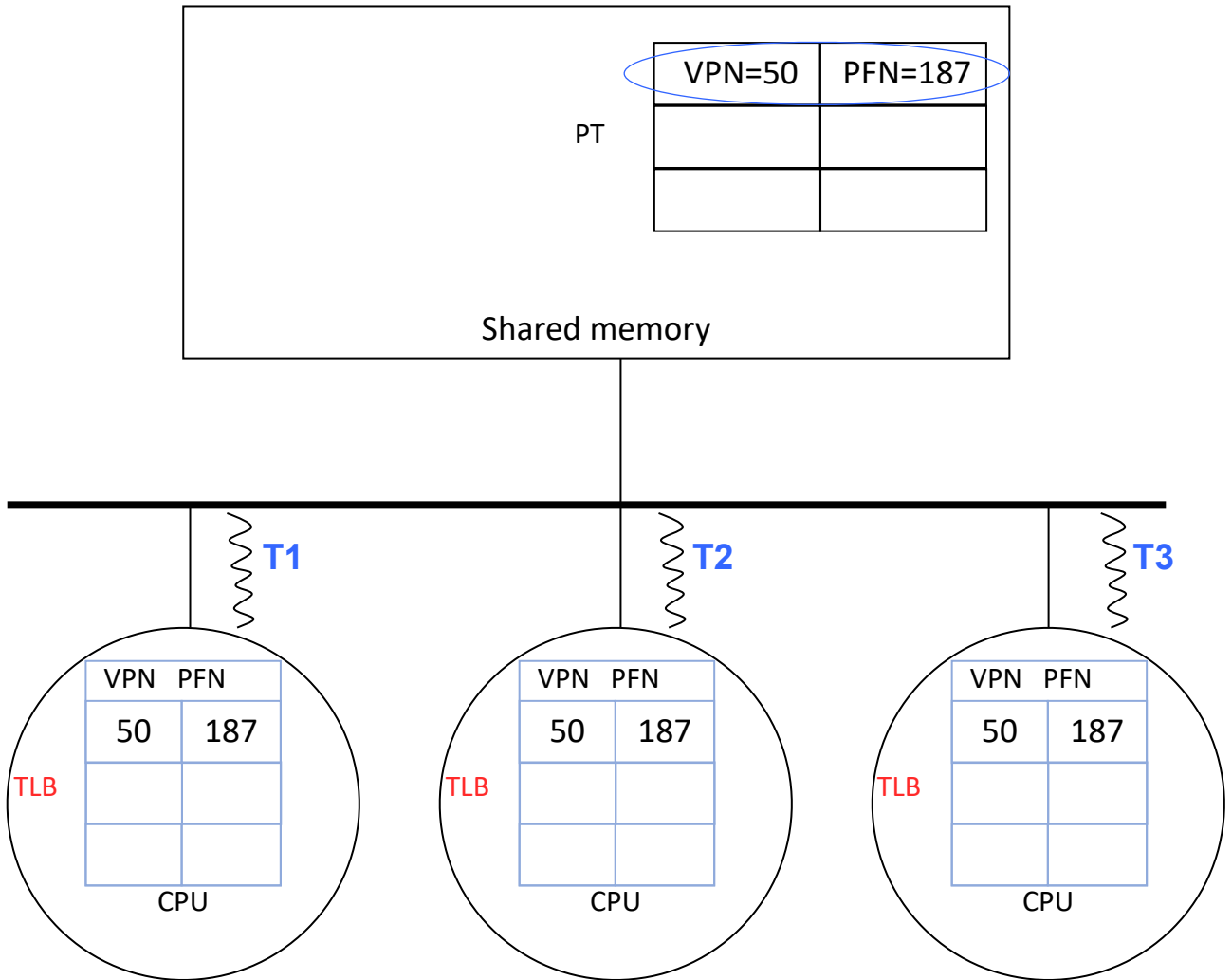
- All of this happens in software by the OS

➔ Another partnership of hardware and software

Example: Handling an SMP page fault

Note that the TLBs have each pulled in VPN=50 because each of the threads referenced that page



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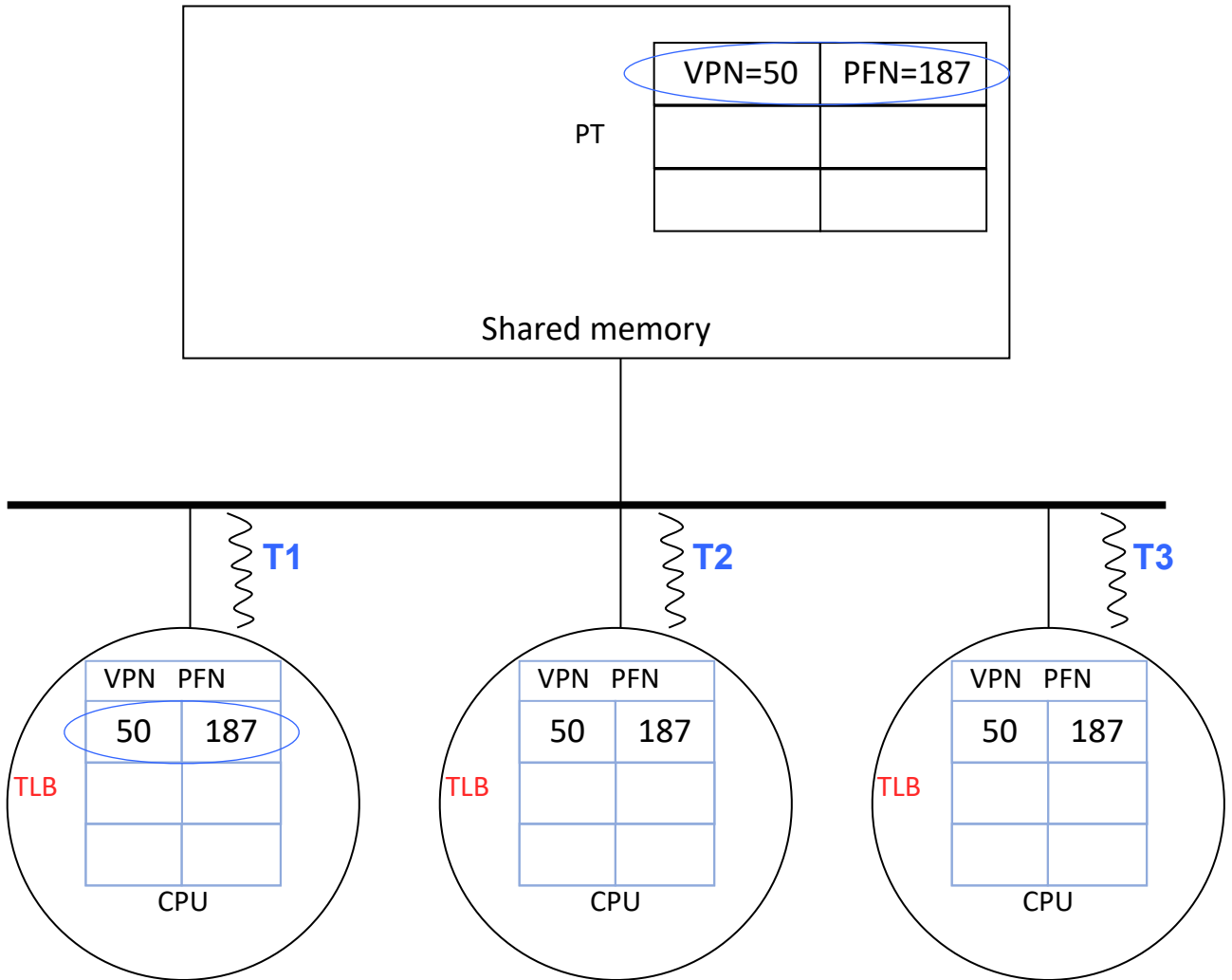

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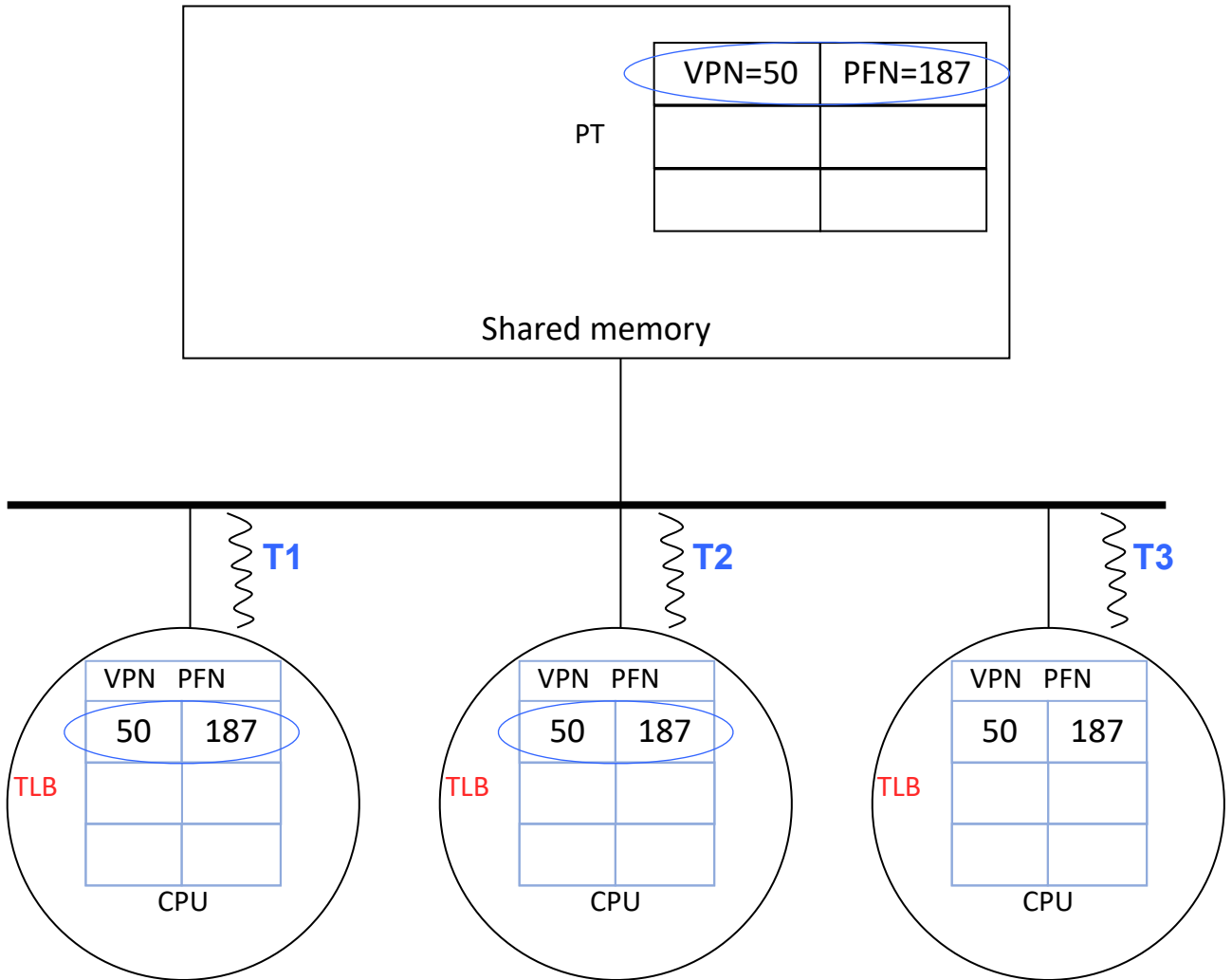

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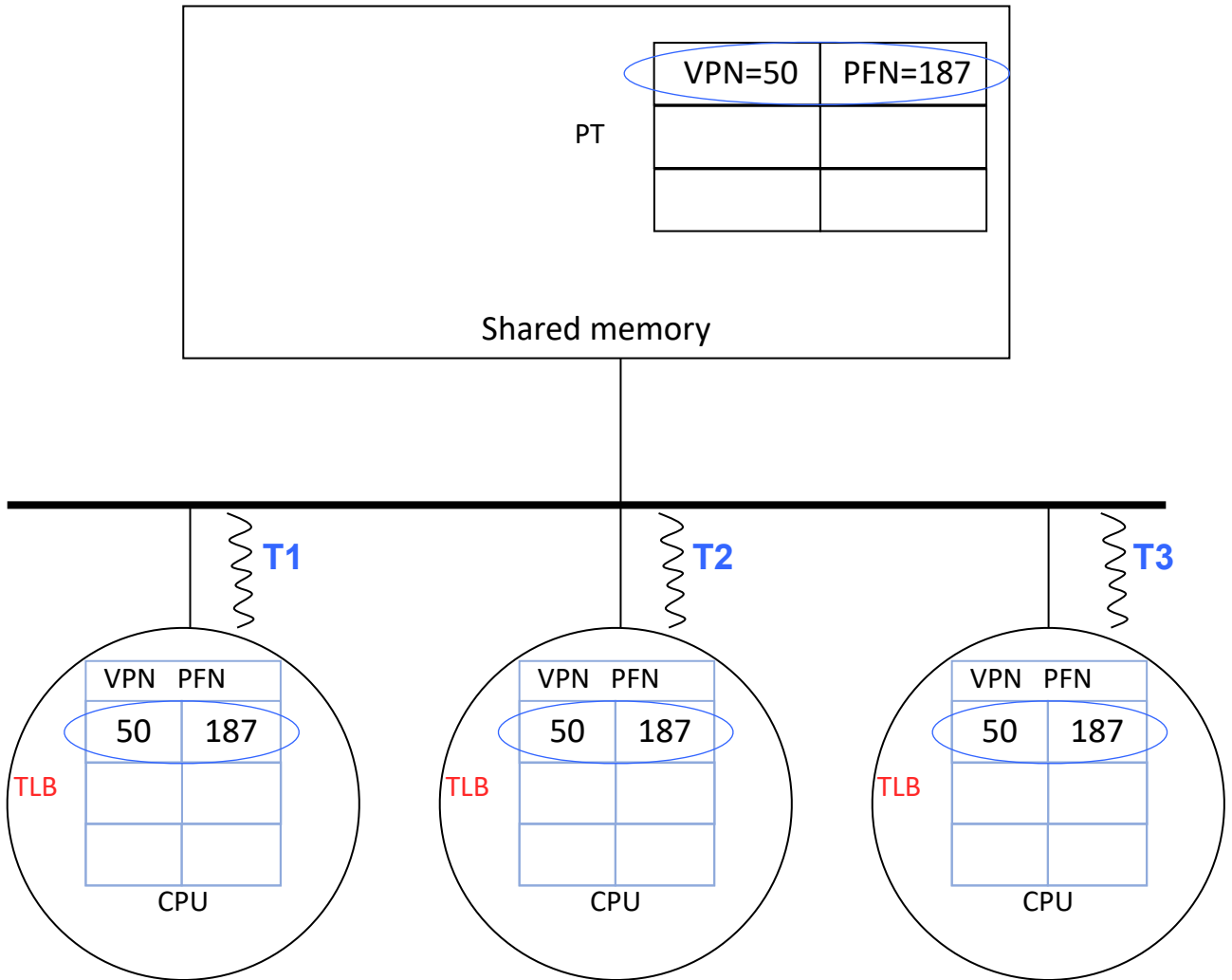

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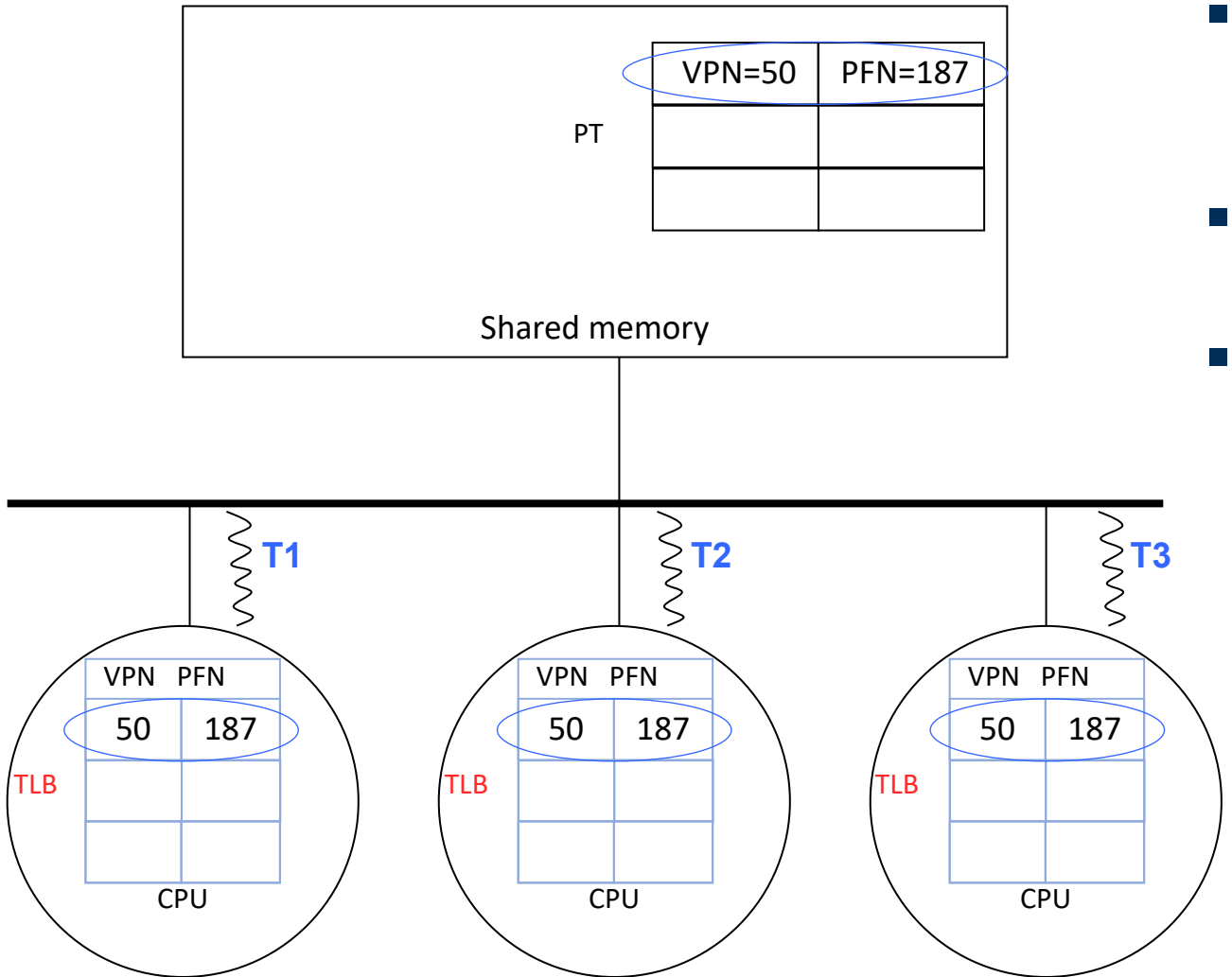
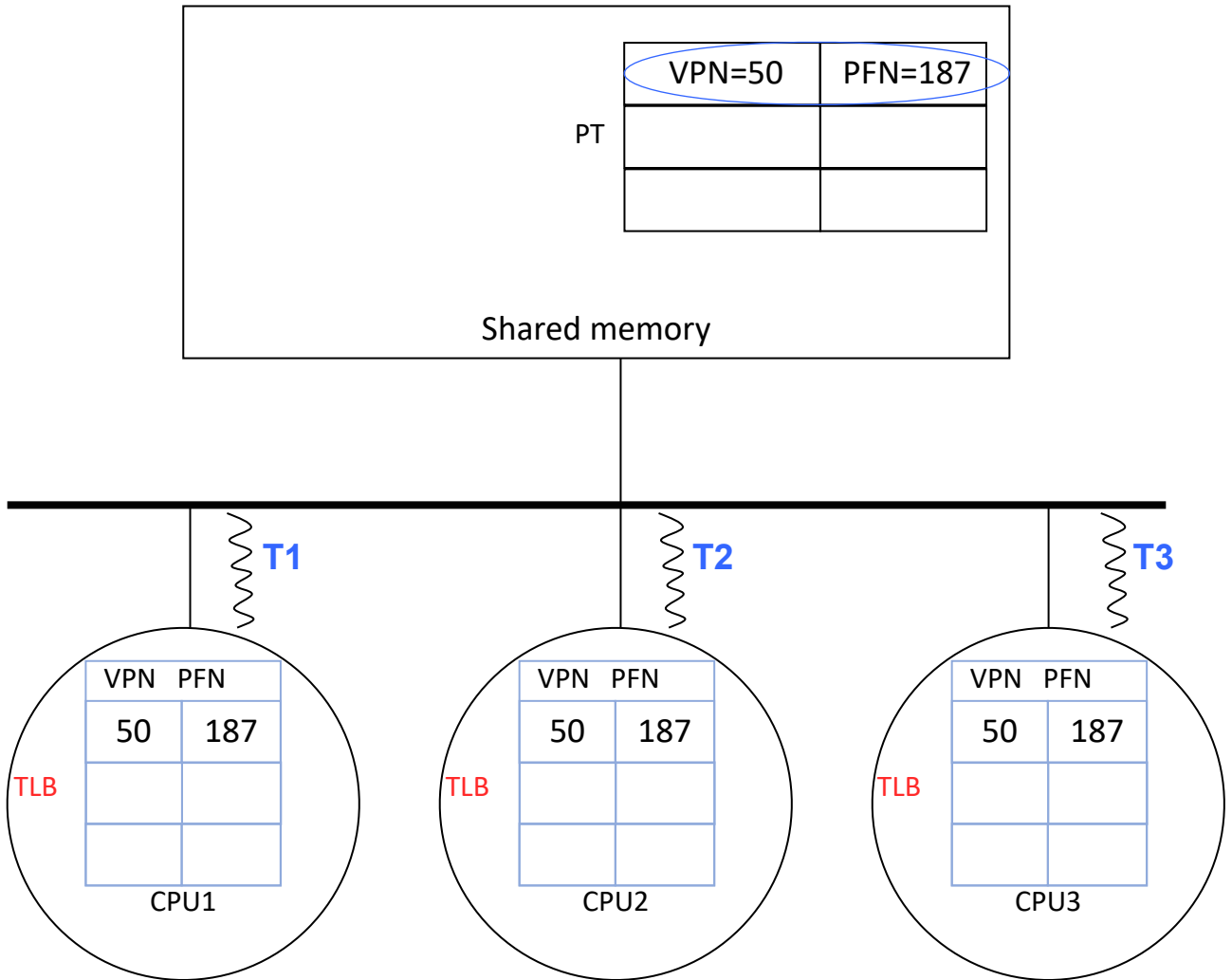


- Assume
  - T1 encounters a page fault on VPN=48
  - OS decides to evict VPN=50
  - And use PFN=187 for hosting VPN=48

Example: Handling an SMP page fault

OS changes the page table entry for VPN=50



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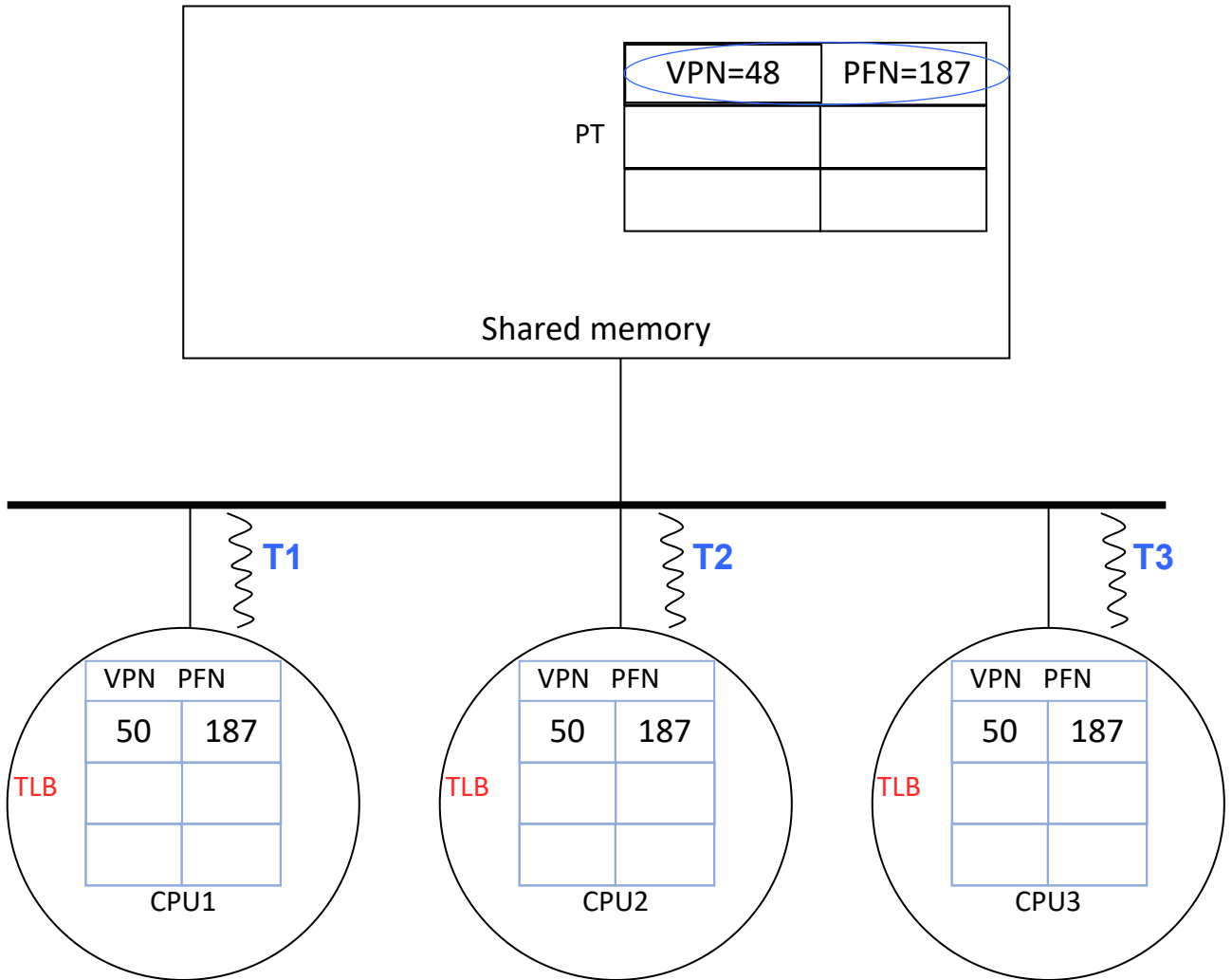

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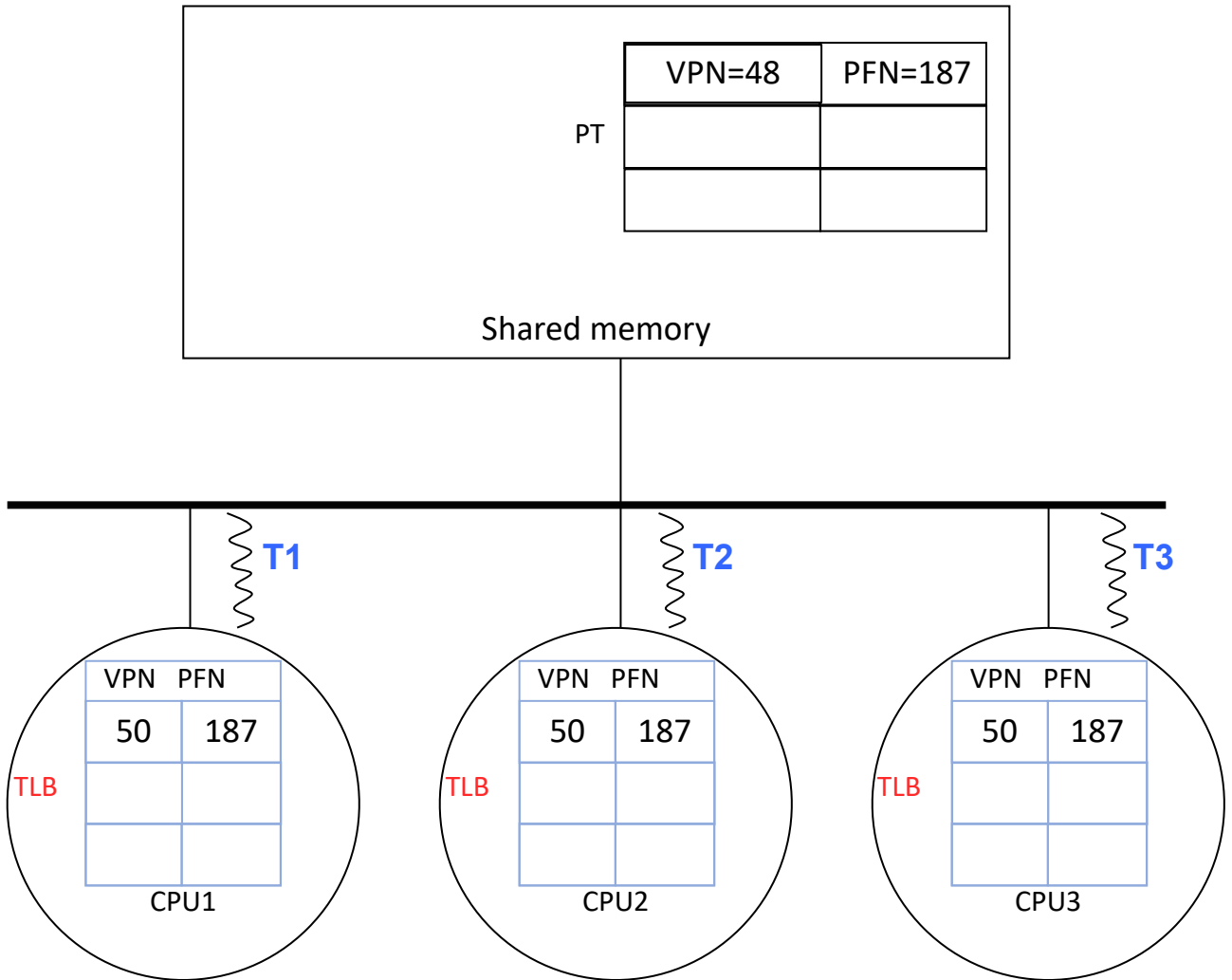

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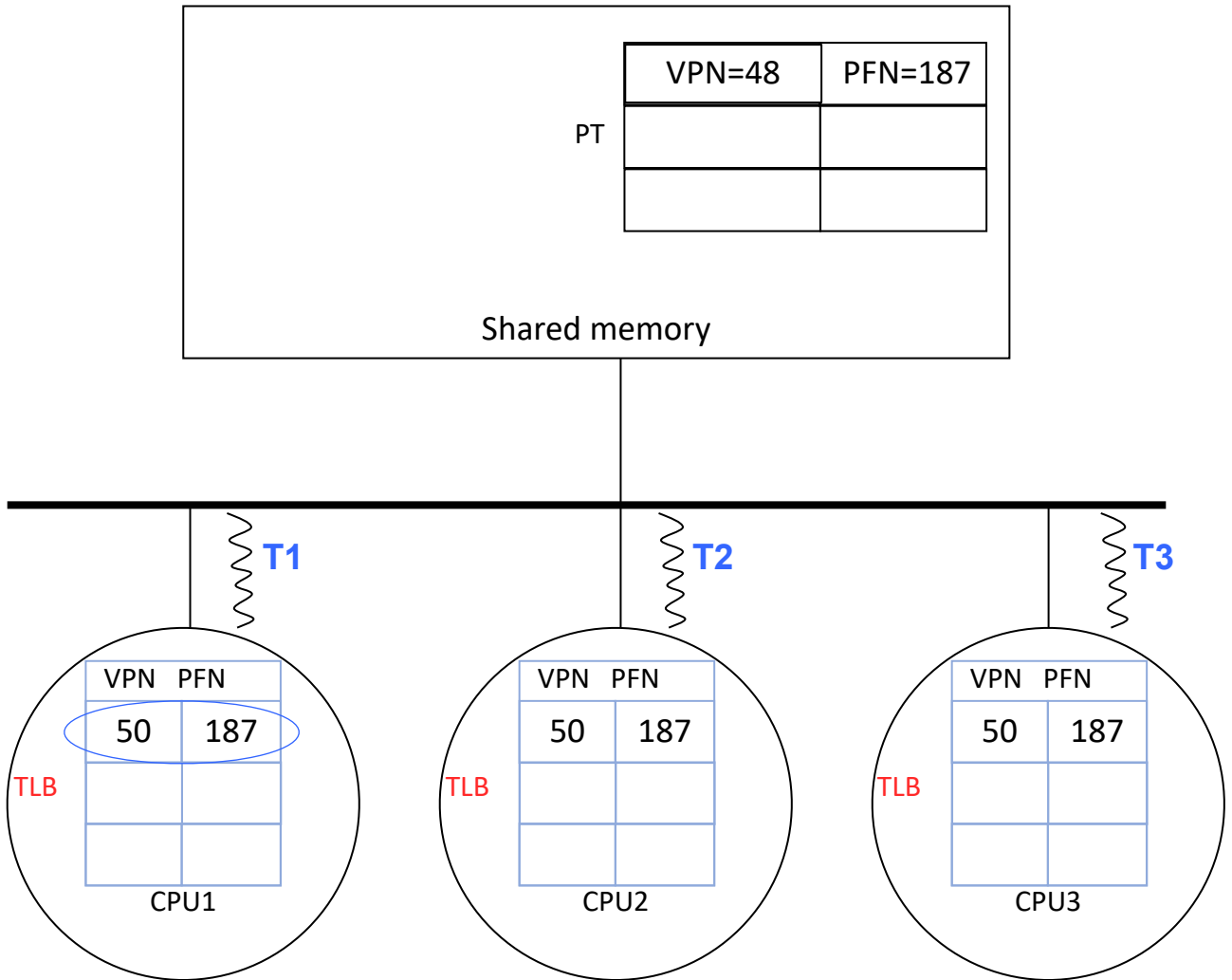

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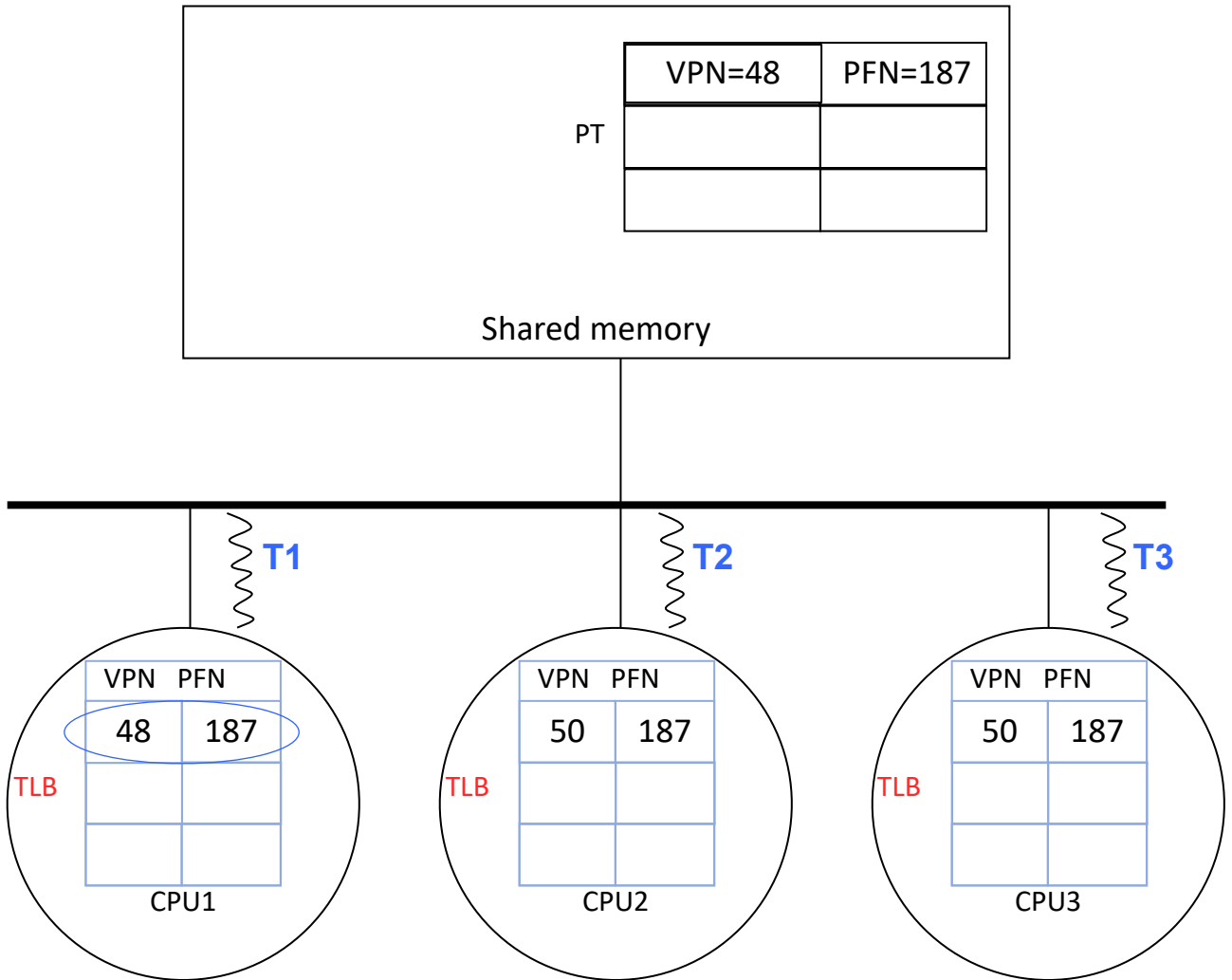

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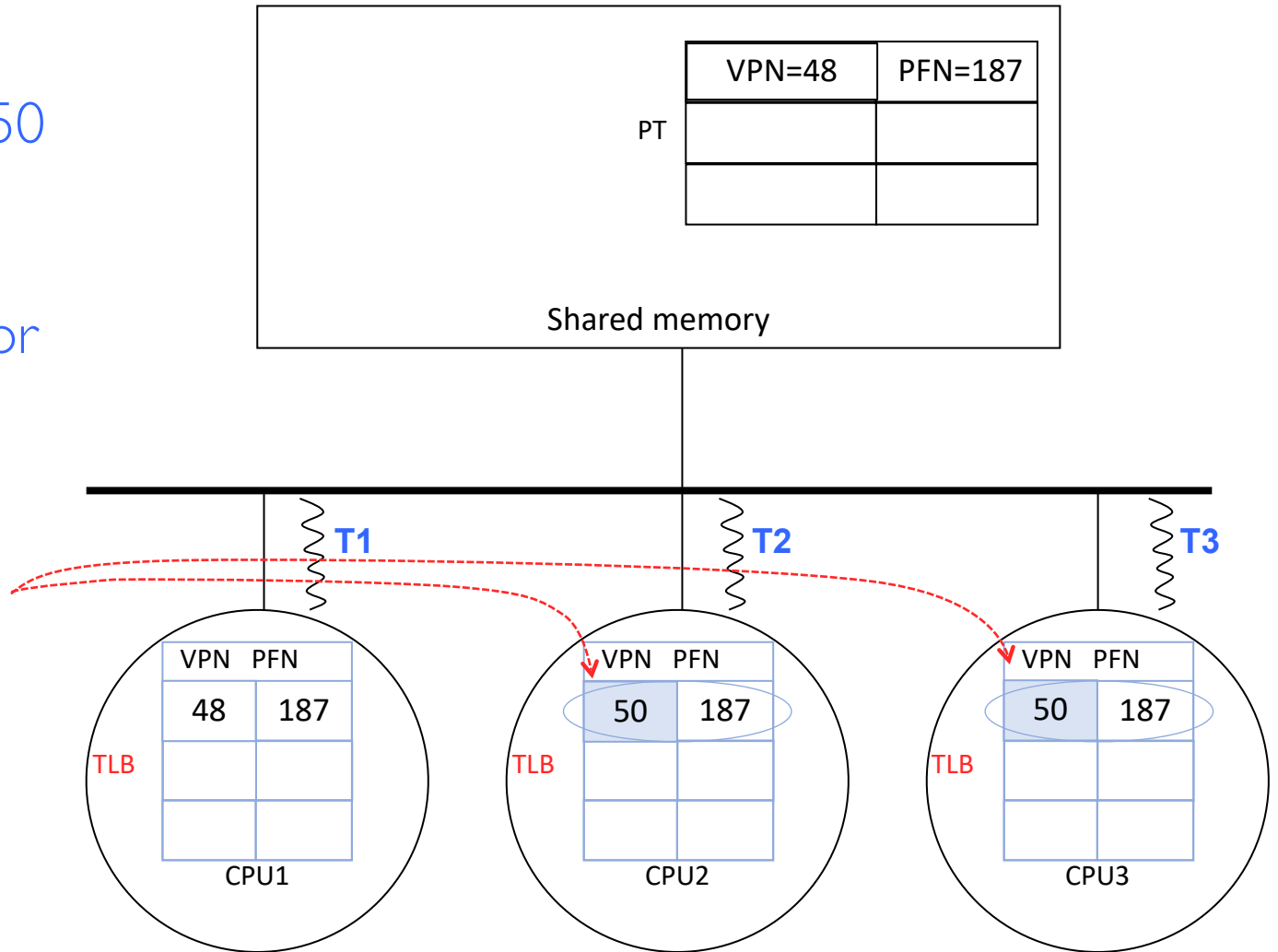
Now we've got stale TLB entries in CPU2 and CPU3



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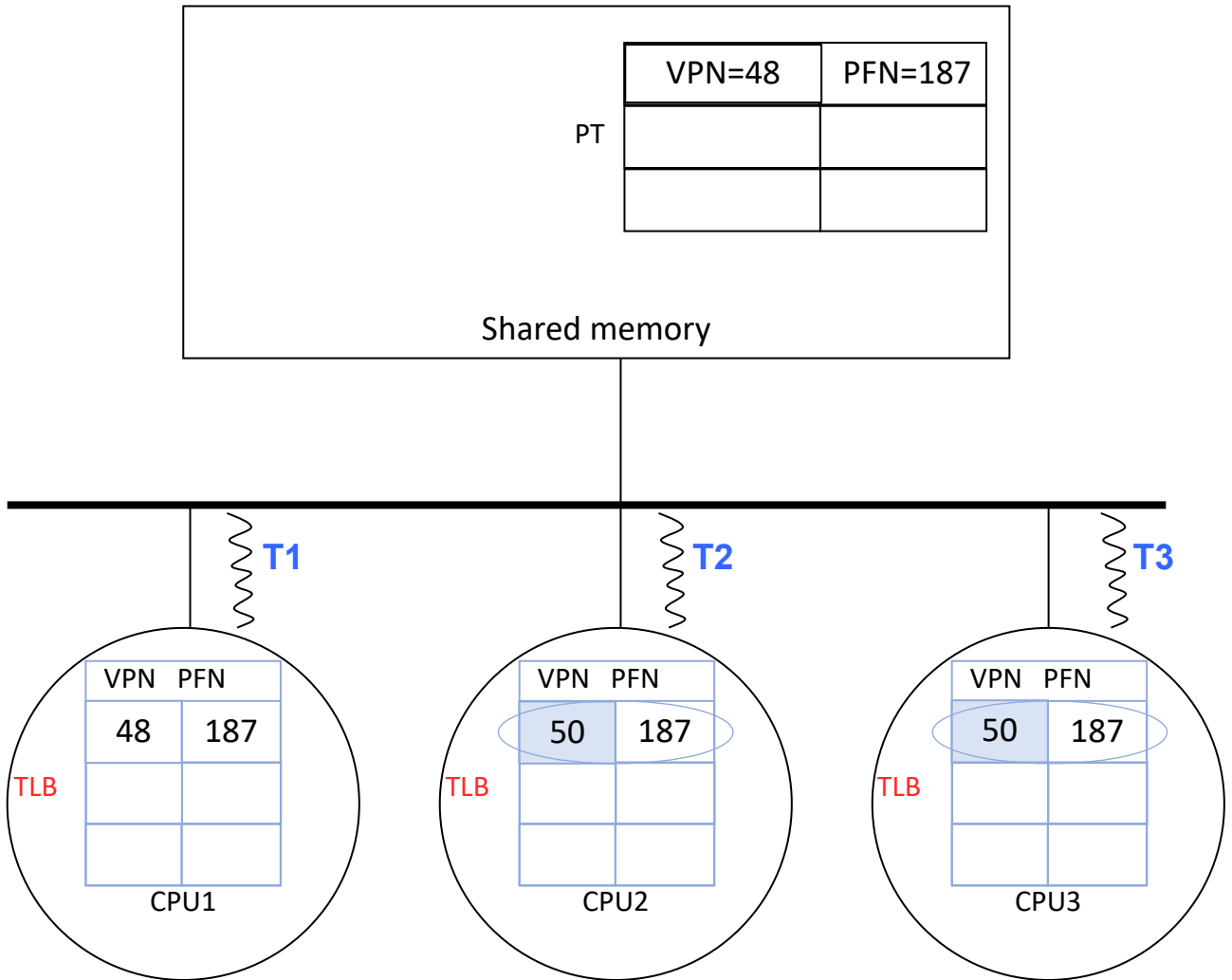

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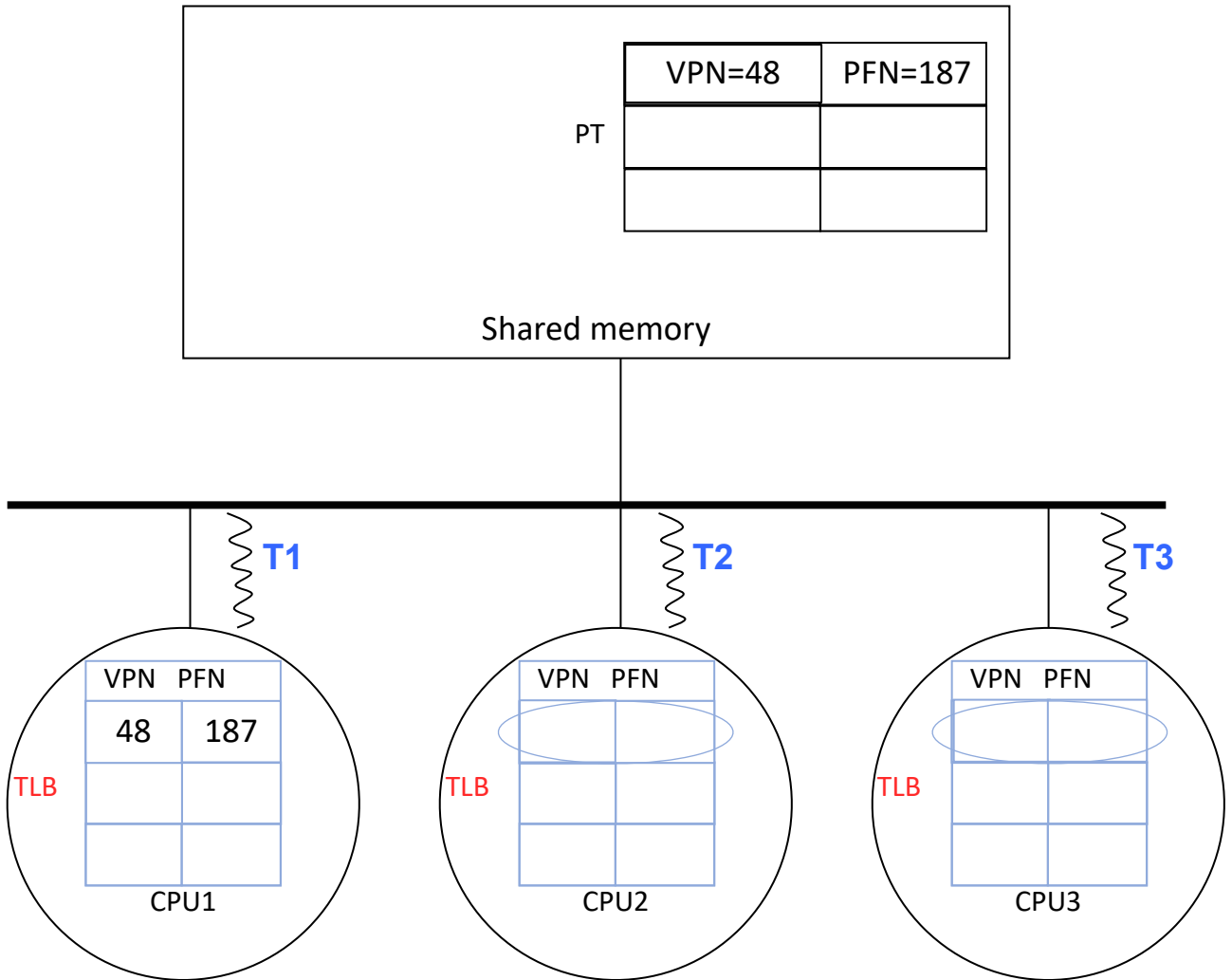

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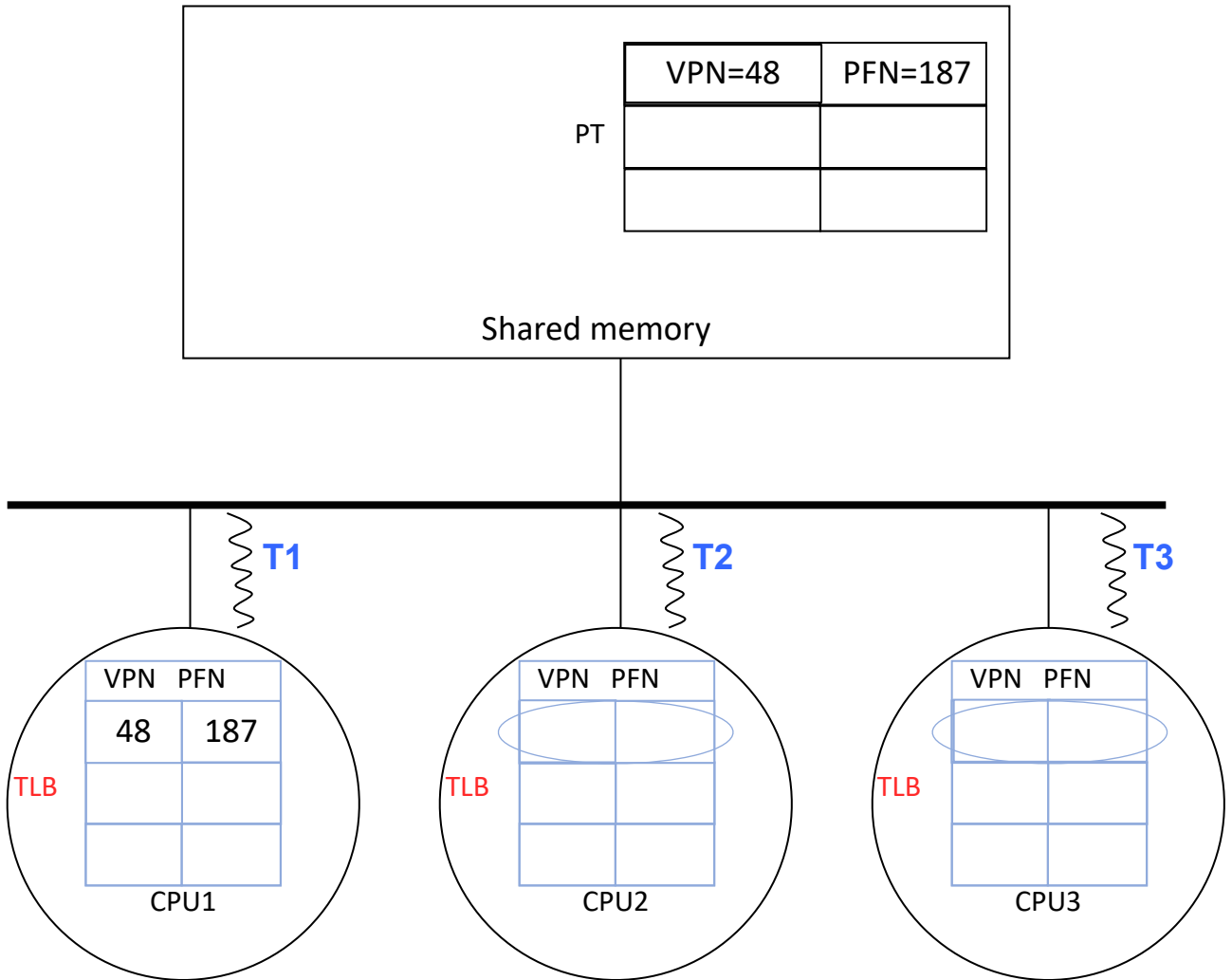
And the CPUs can pull in the updated PTE when (and if) they next reference VPN=48



Session ID:
dag2200

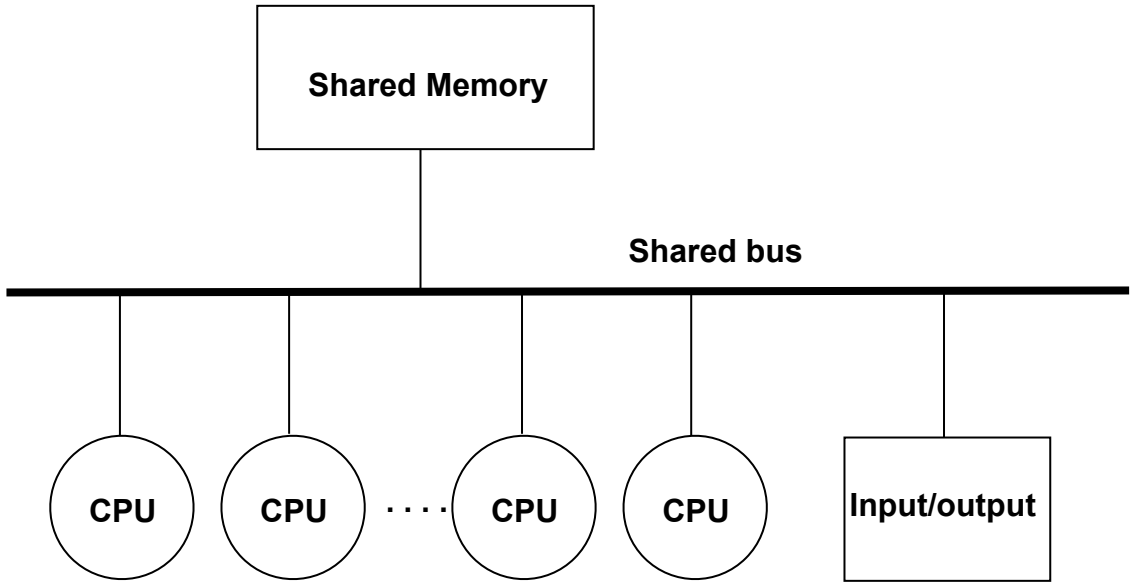
Ensuring that all threads of a process share an address space in an SMP is

A. Impossible
B. Trivially achieved since the page table resides in shared memory
C. Achieved by careful replication of the page table by the operating system for each thread
D. Achieved by special-purpose hardware that no one has told us about yet

Keeping the TLBs consistent in an SMP

A. Is the responsibility of the programmer
B. Is the responsibility of the hardware
C. Is the responsibility of the operating system
D. Is not possible

How do we implement Symmetric Multi Processing (SMP)?



The System (hardware+OS) has to ensure 3 things:

1. Threads of the same process share the same PT
2. Threads have synchronization atomicity
3. Threads have identical views of memory

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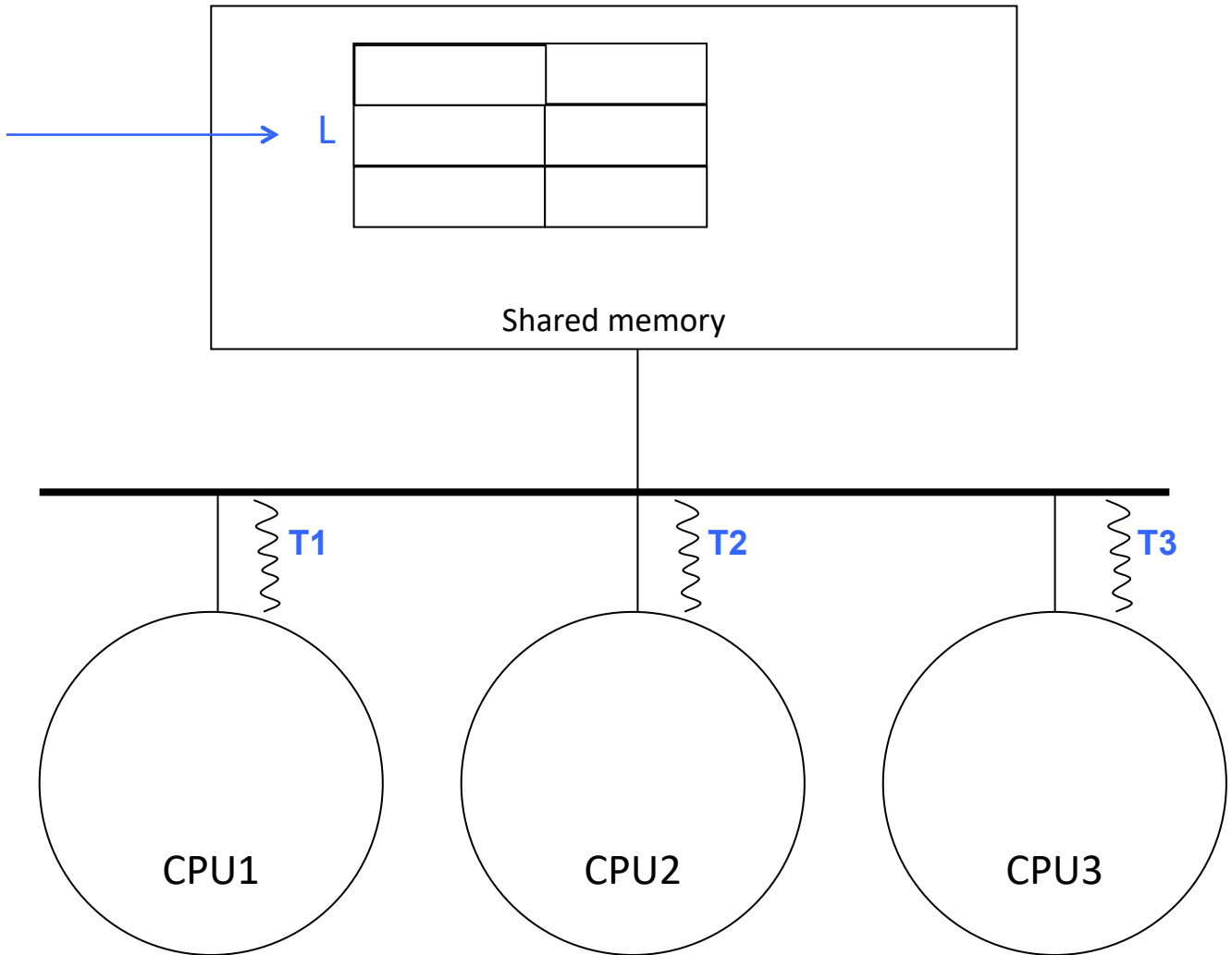
- What could go wrong?

2) Threads have synchronization atomicity

We have memory location L for TEST-AND-SET



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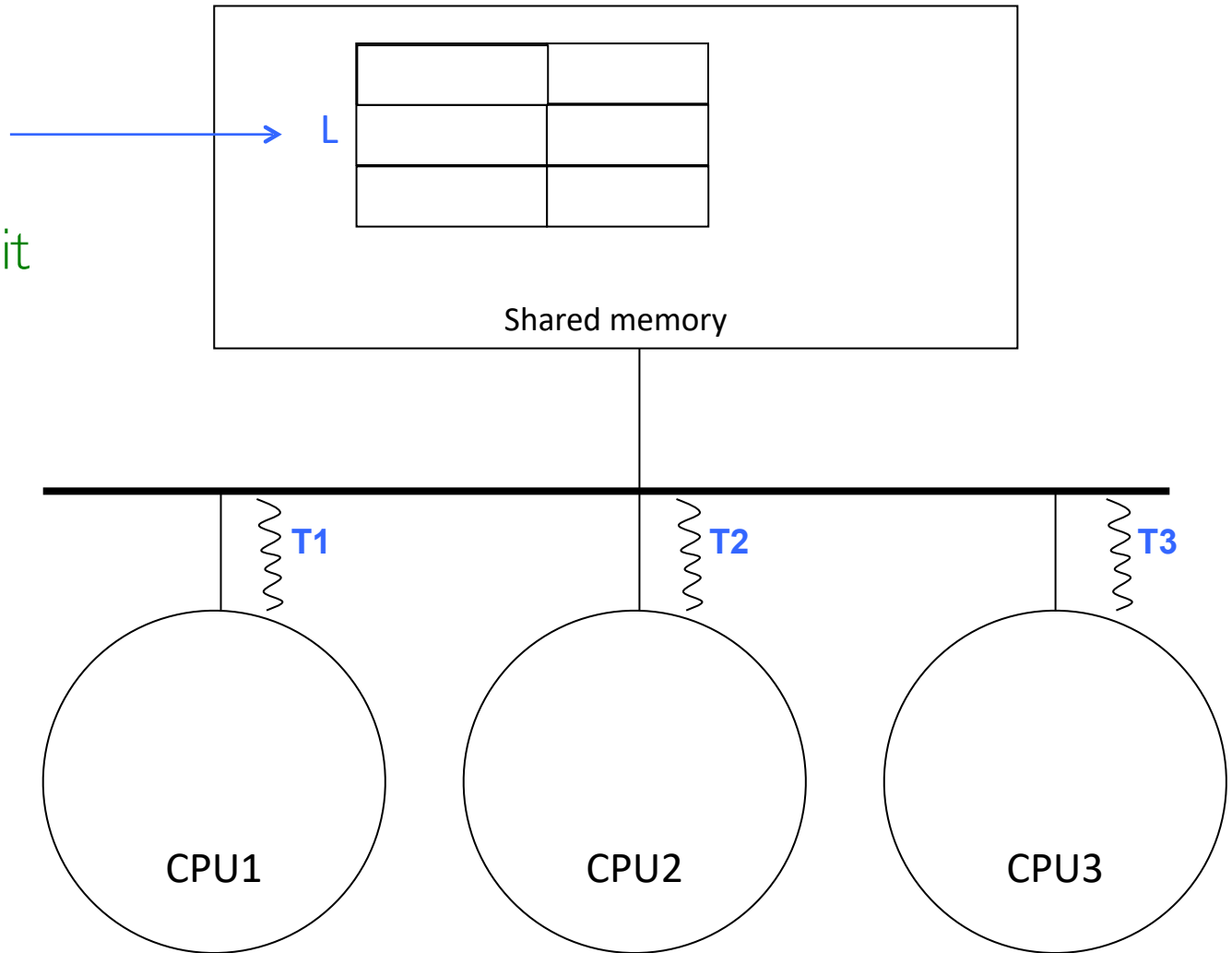

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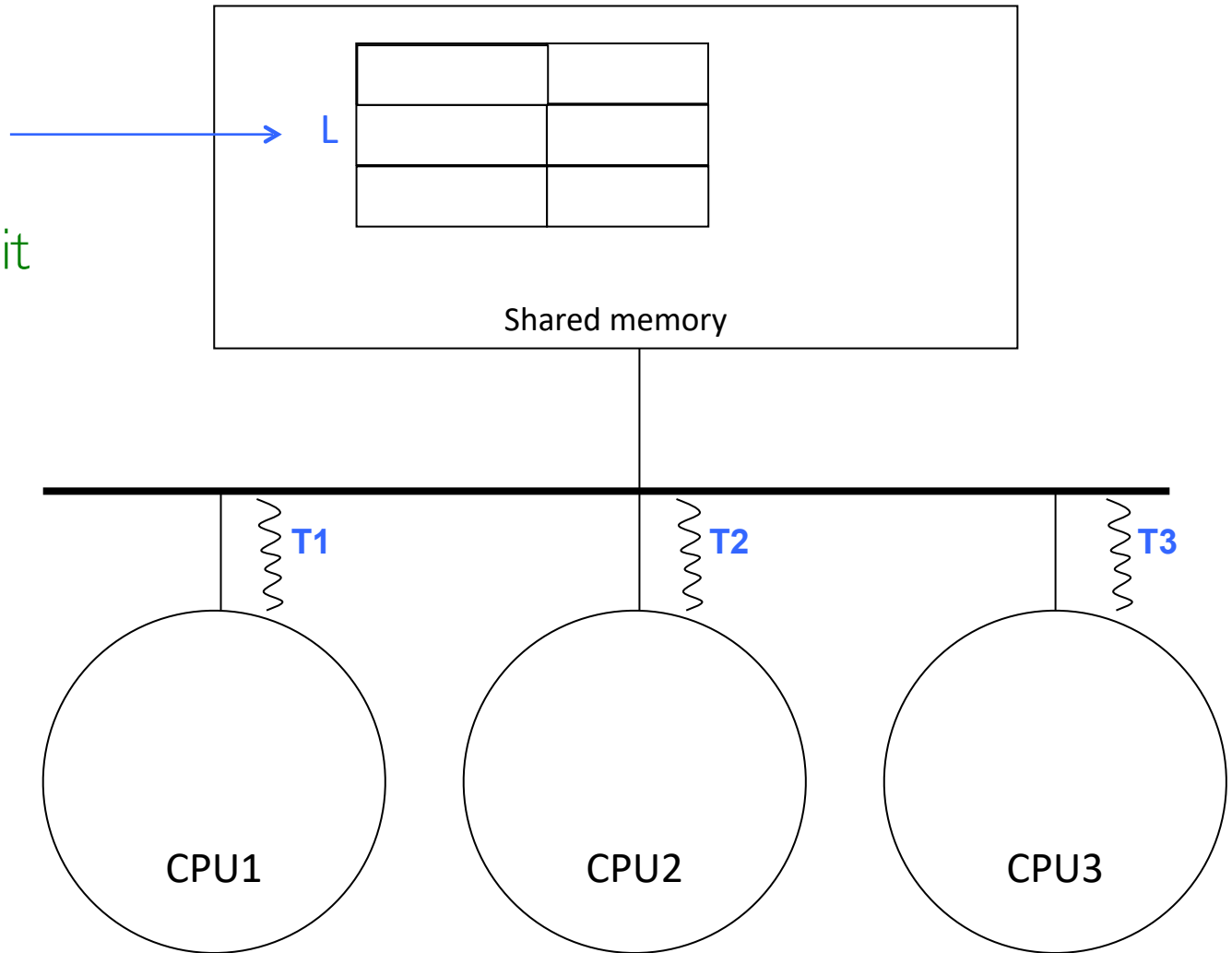

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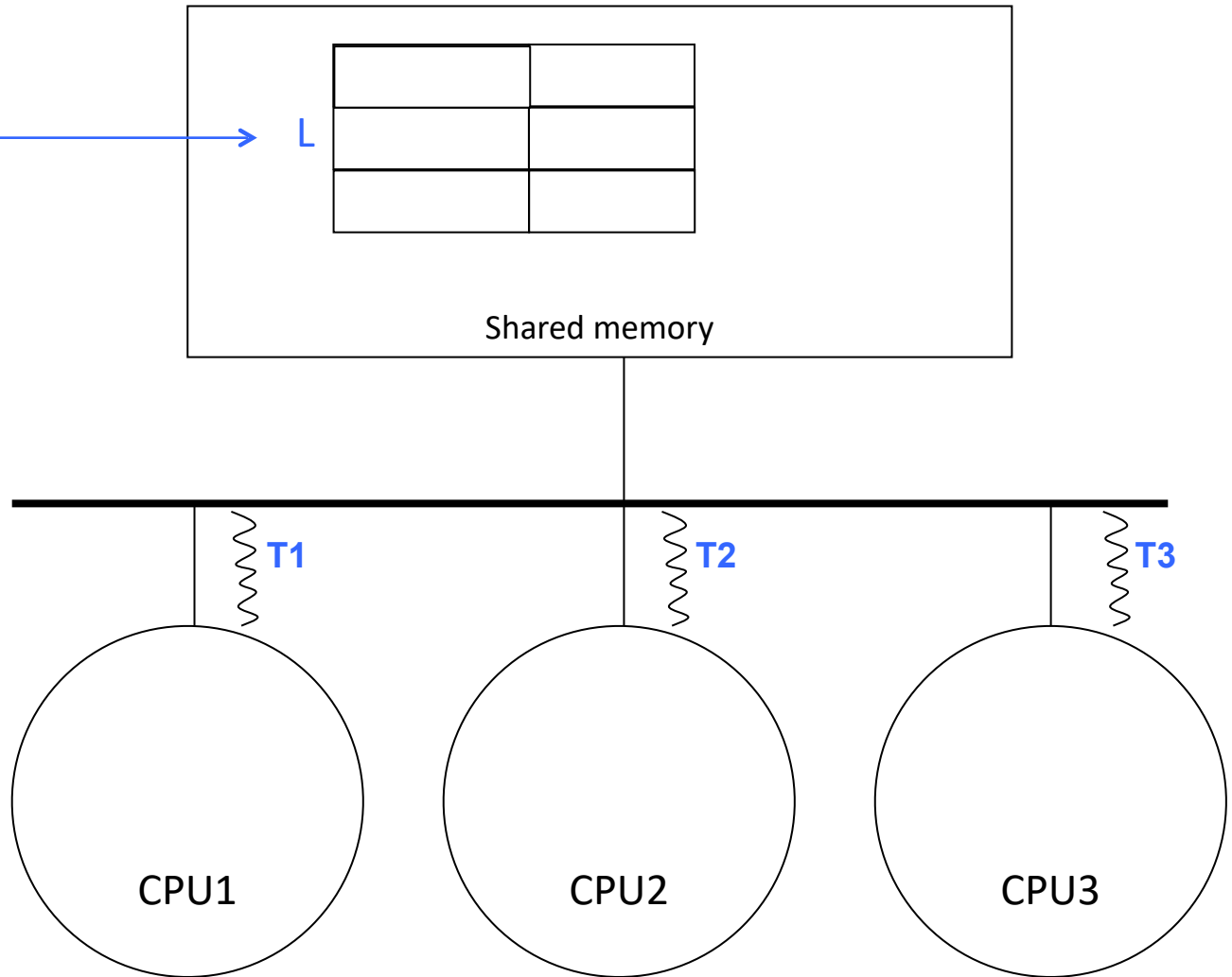

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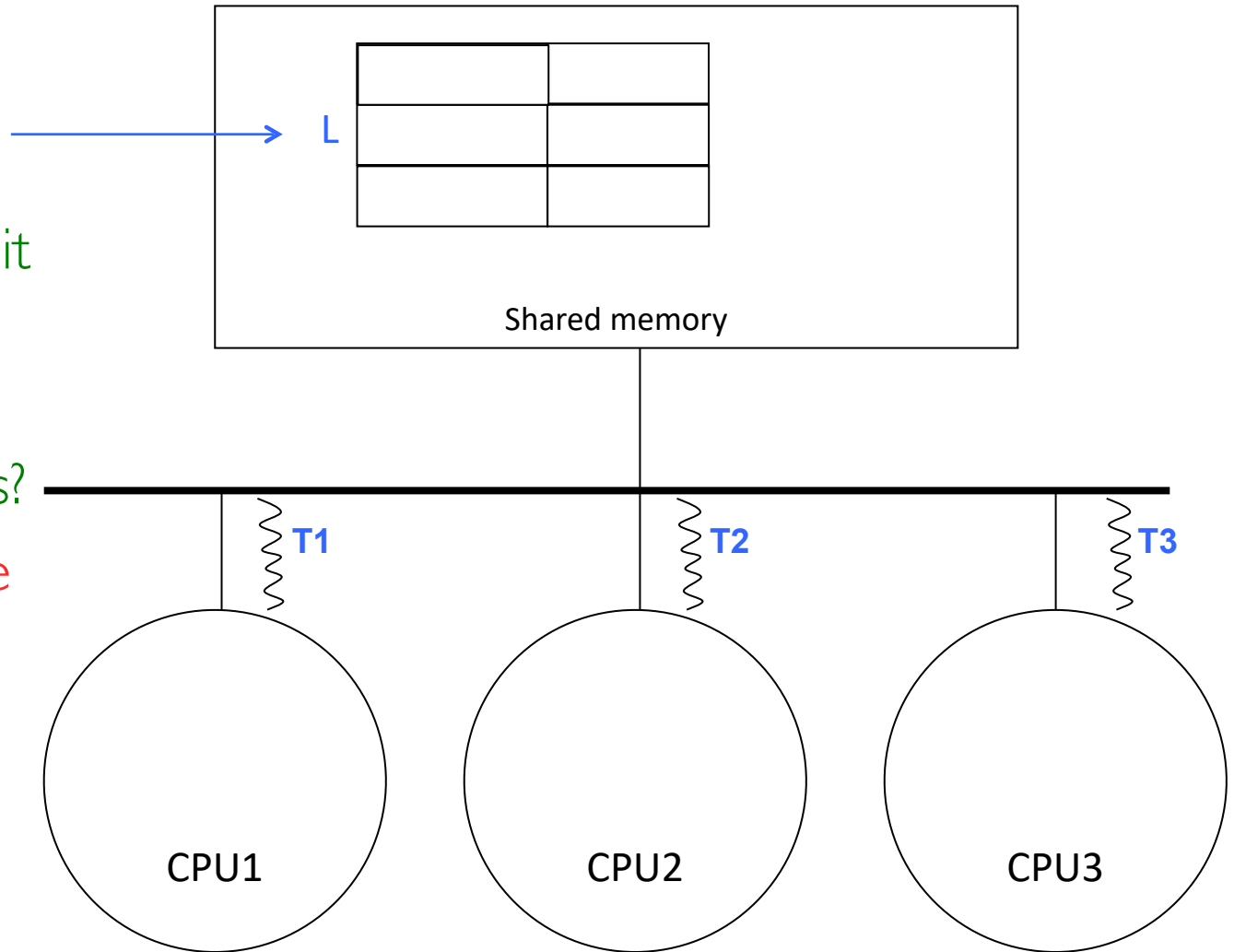

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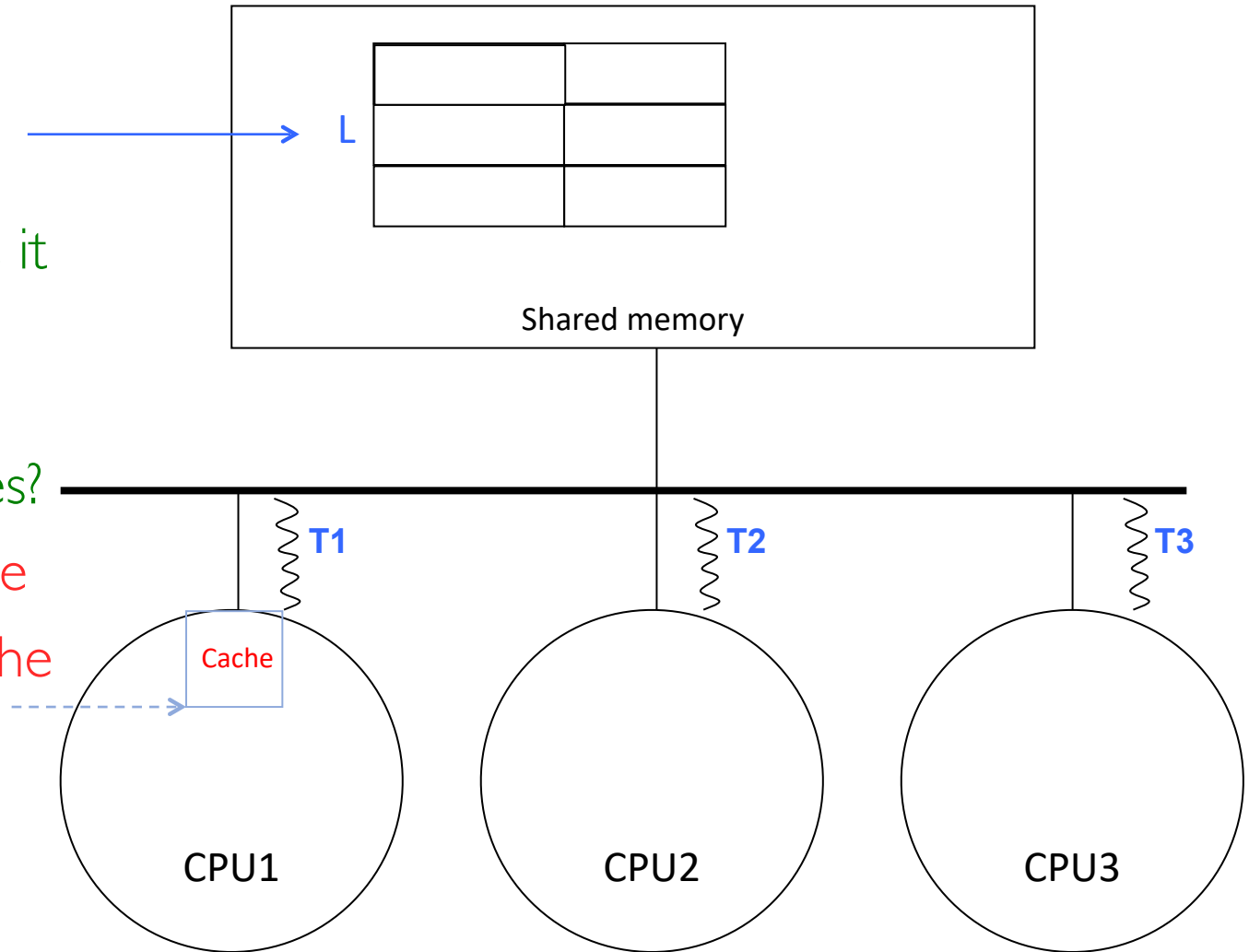

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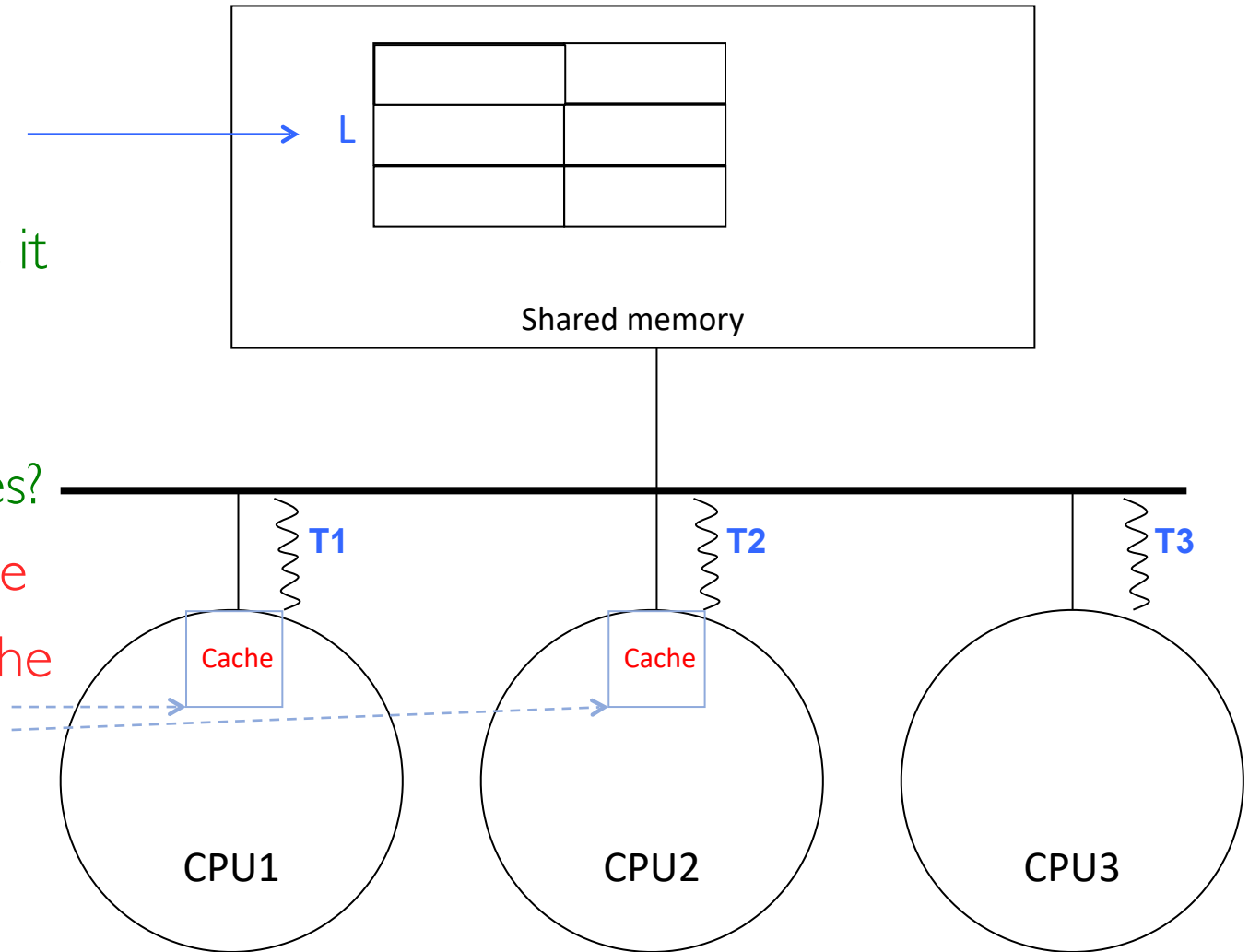

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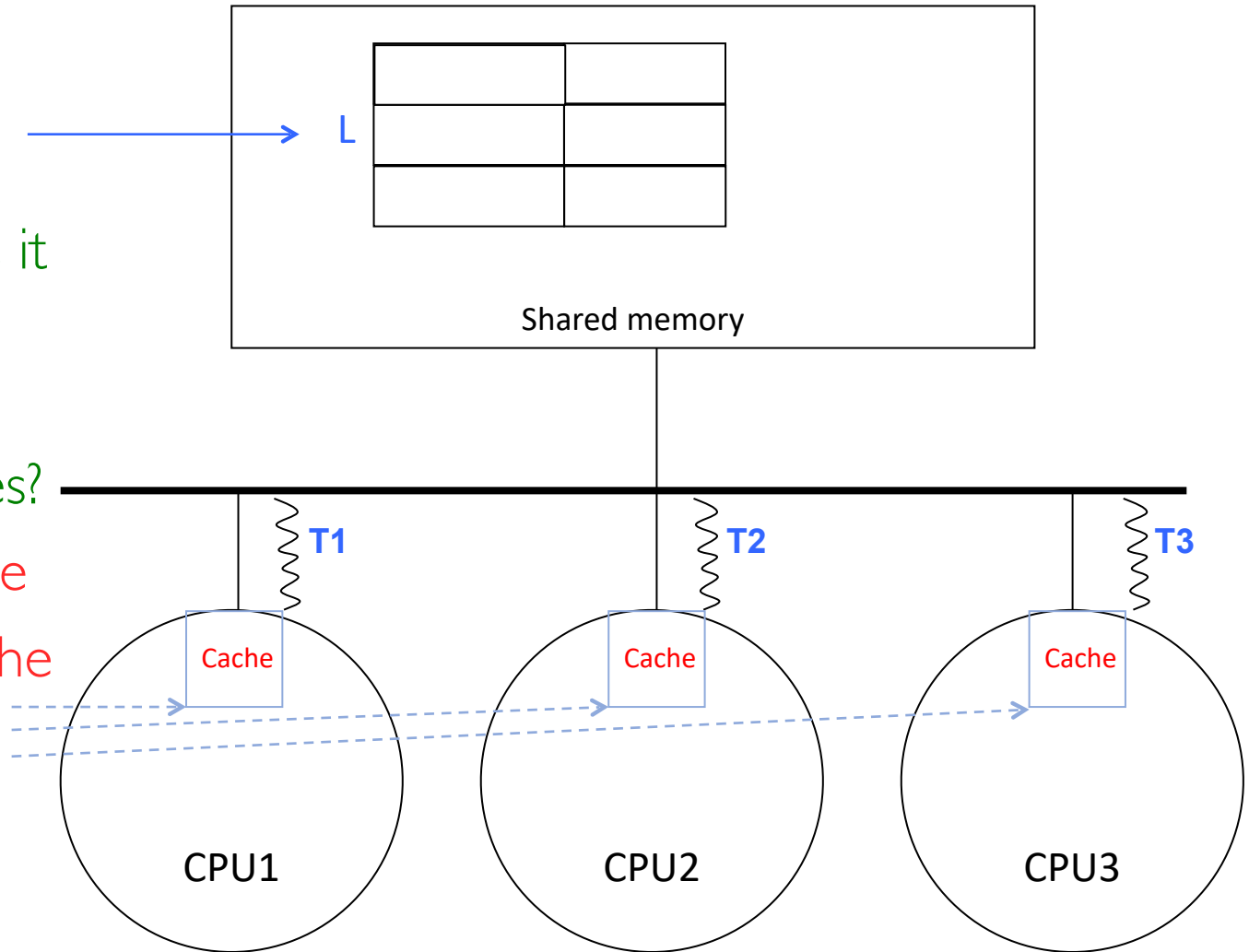

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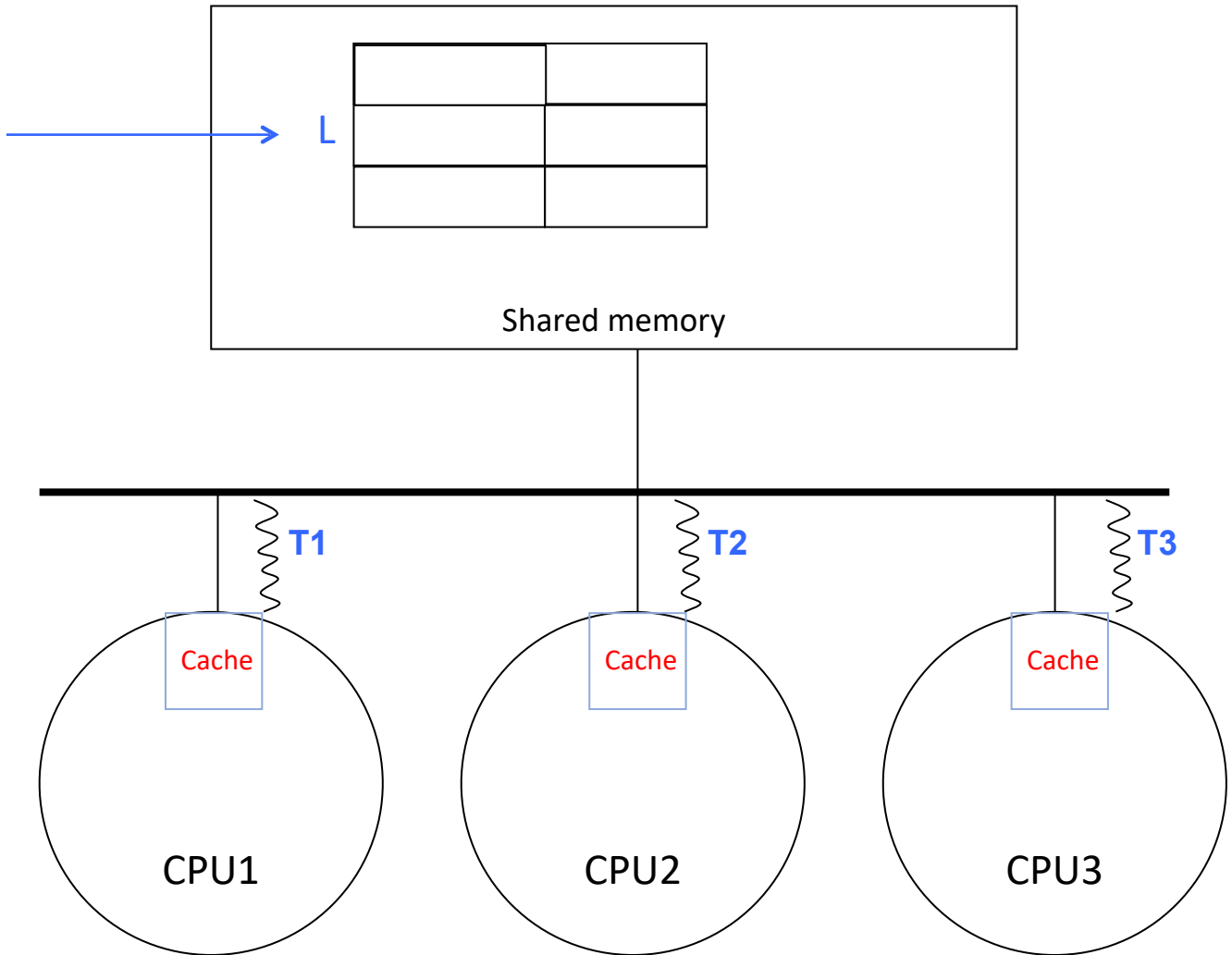

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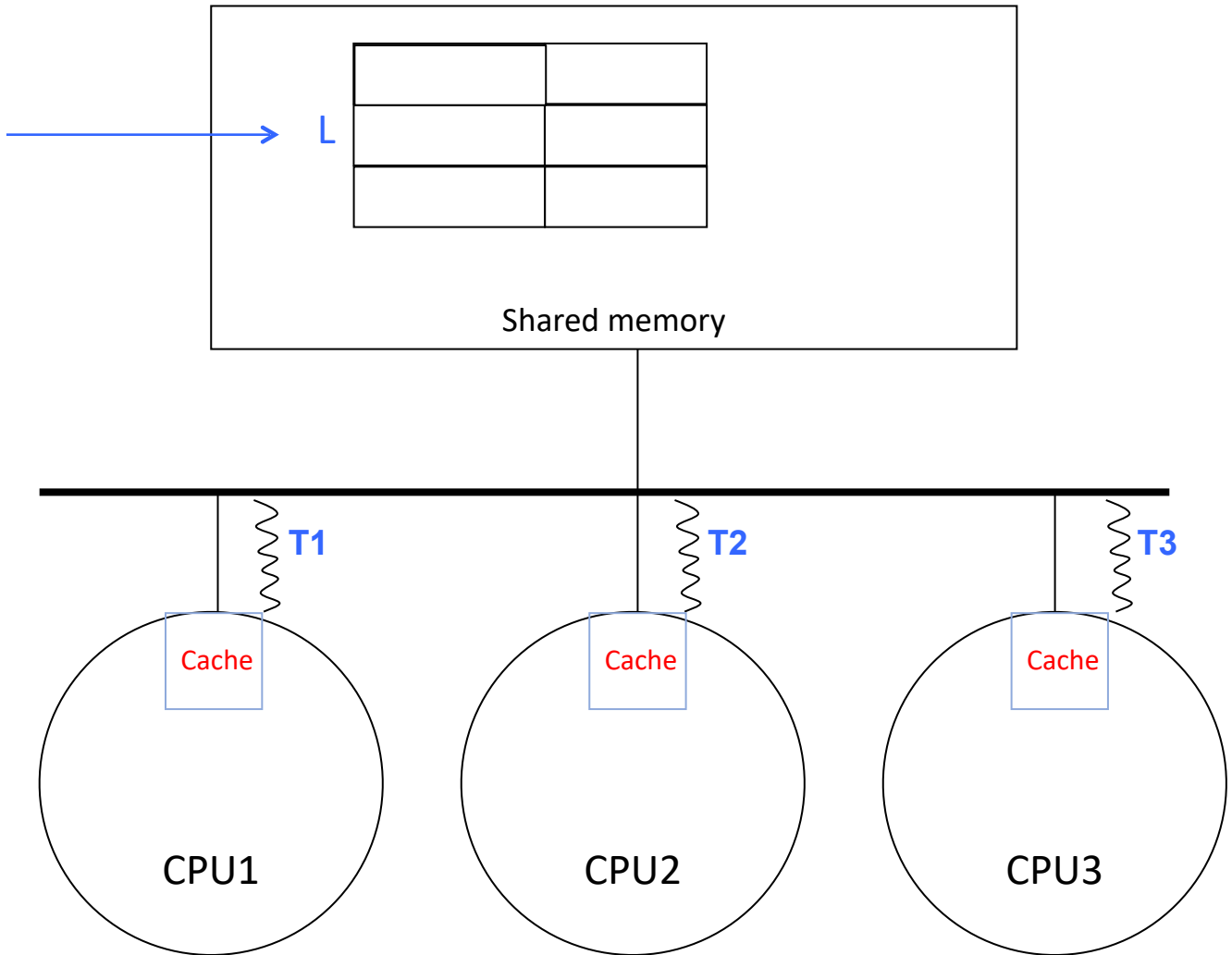
What shall we do?

One solution is to bypass the cache for the T&S instruction



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   - ➔ This implies that access to a memory location returns the same value on all CPUs
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   - ➔ We'll refer to the method of keeping all the copies of the same data across caches as a cache coherence protocol

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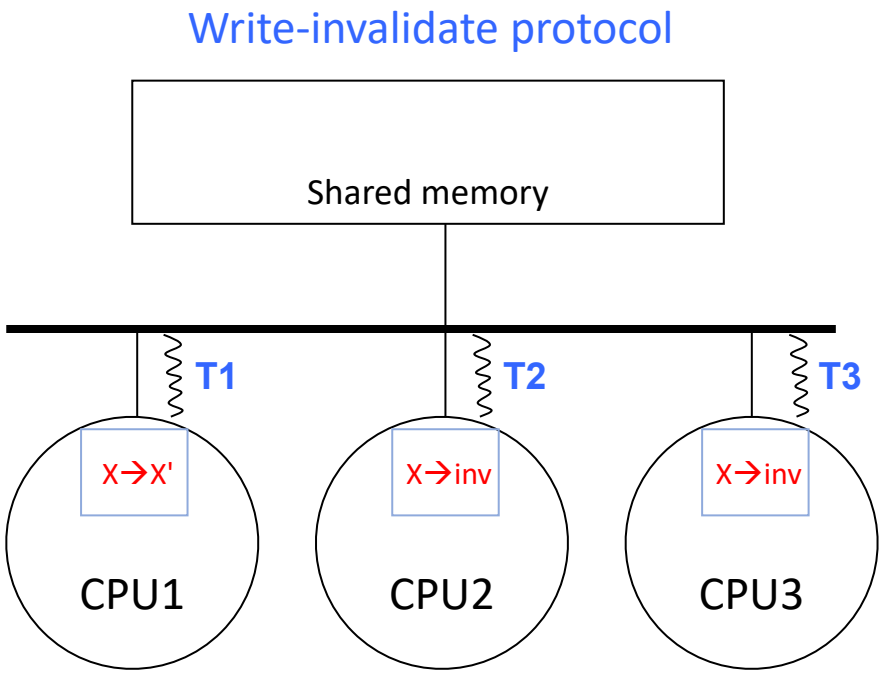

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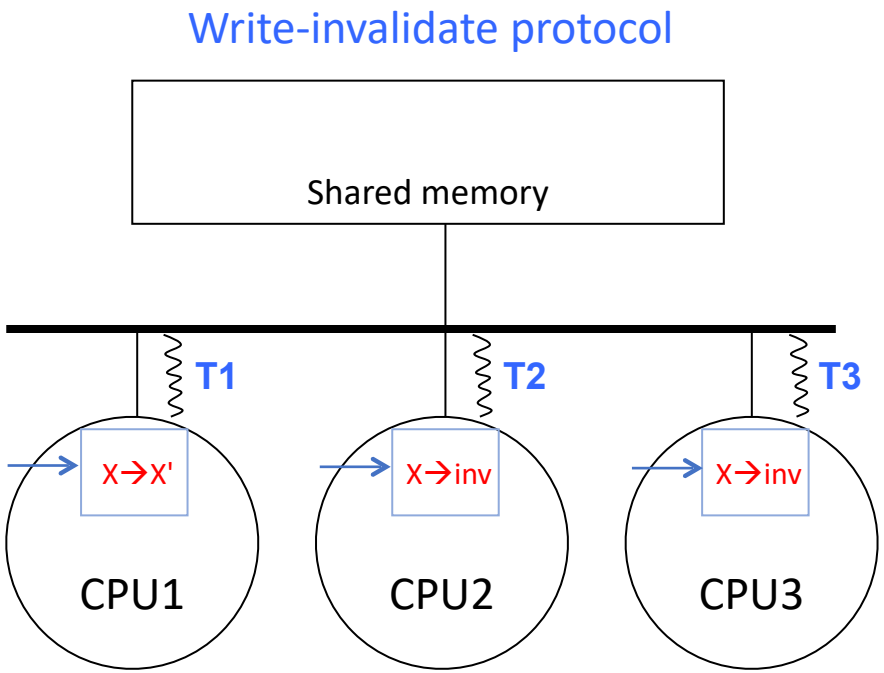

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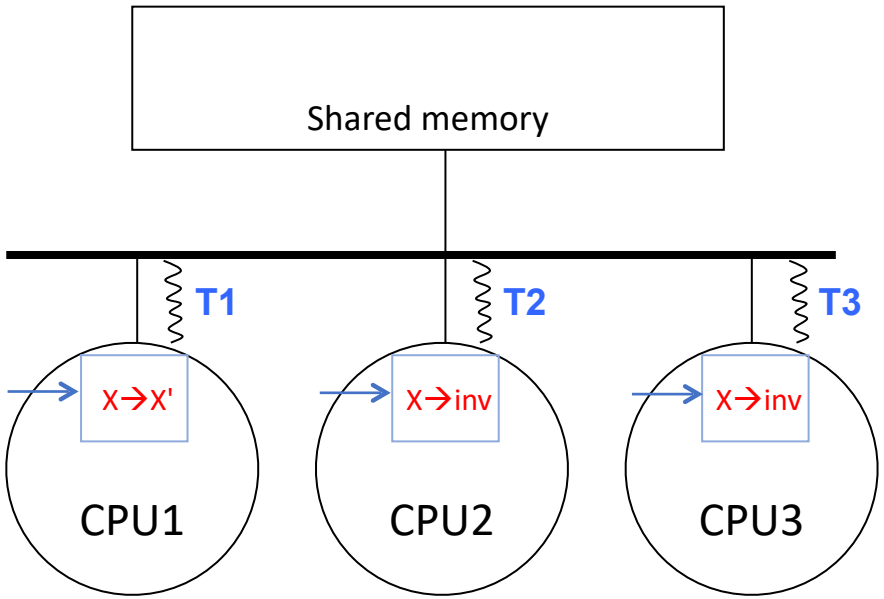

Write-update protocol

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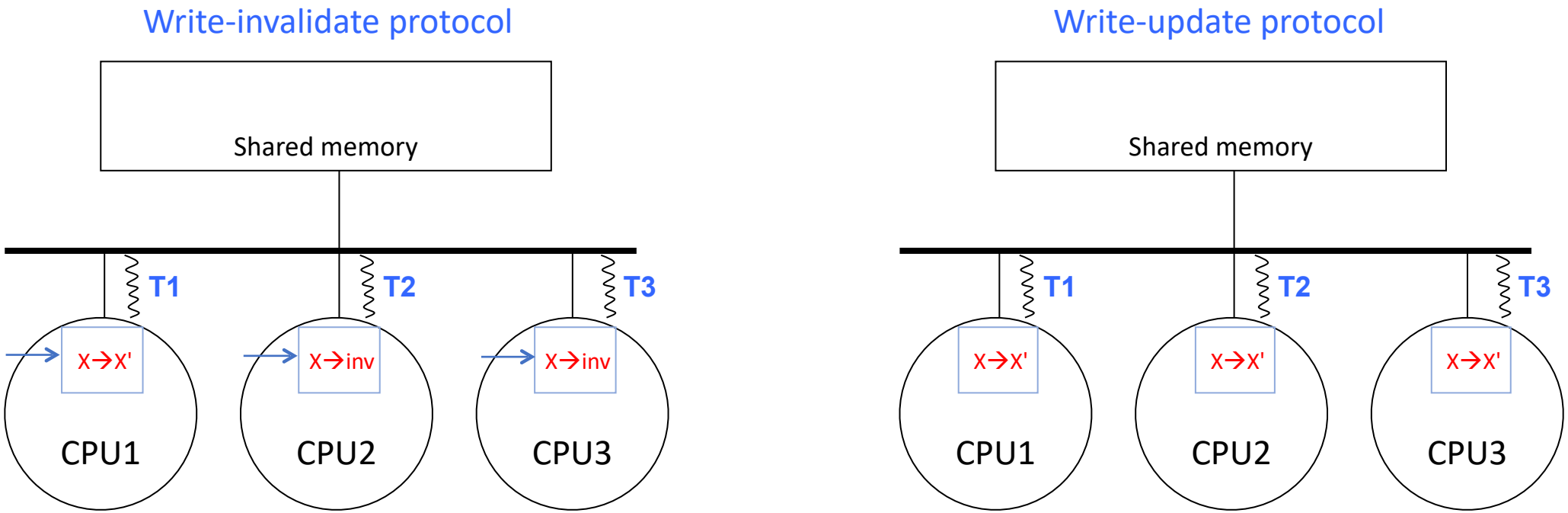
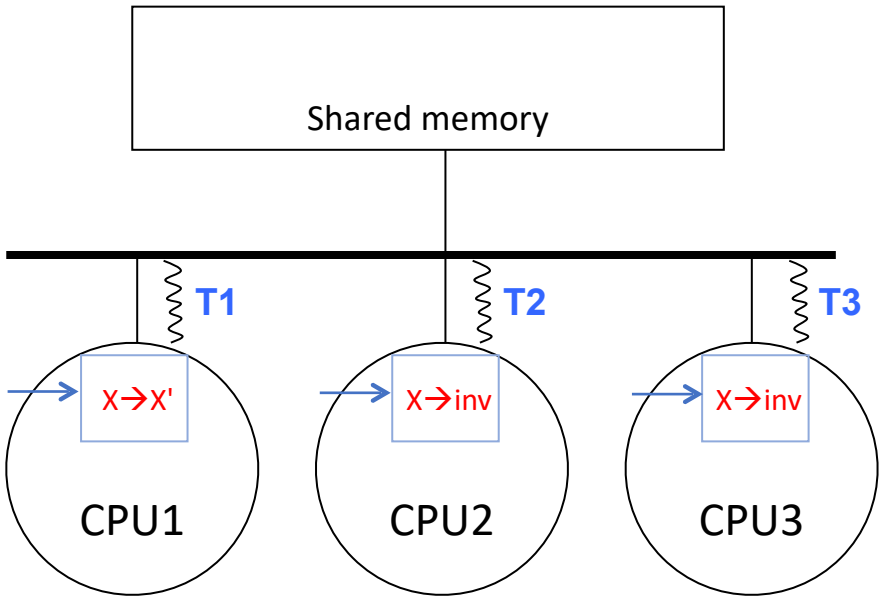


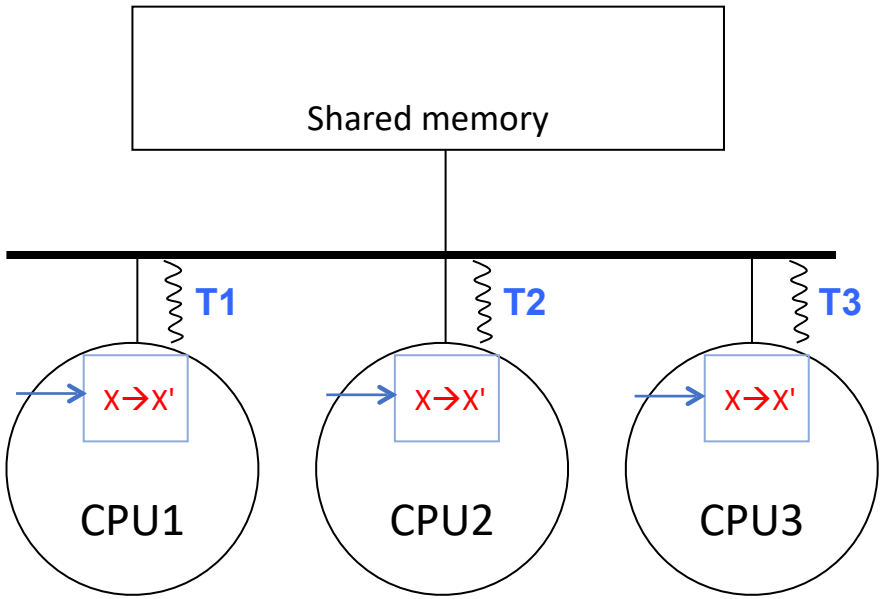
3) Threads have identical views of memory

- Two possible solutions, in hardware
- In both cases, cache becomes active and monitors or *snoops* the bus
- Let's watch a memory location change value from X to X'

Write-invalidate protocol



Write-update protocol



Session ID:
dag2200

Keeping the caches coherent in an SMP

A. …is the responsibility of the user program
B. …is the responsibility of the hardware
C. …is the responsibility of the operating system
D. …is impossible
E. …is why we don't allow caches in SMP systems

Session ID: dag2200

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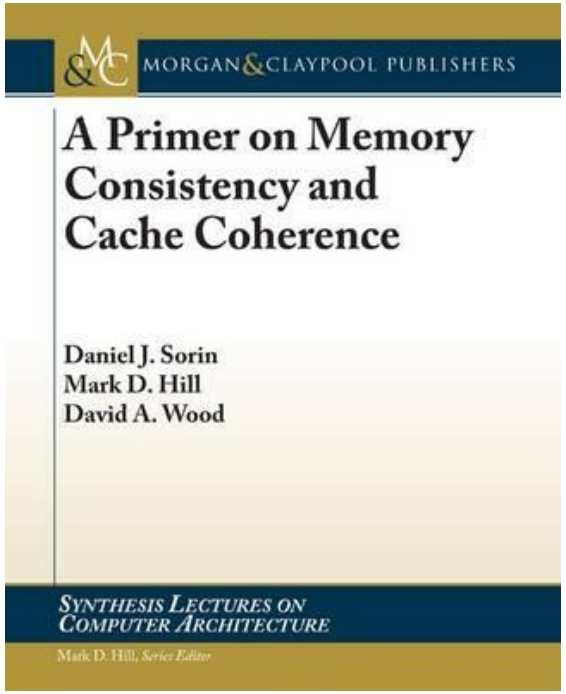


Summary

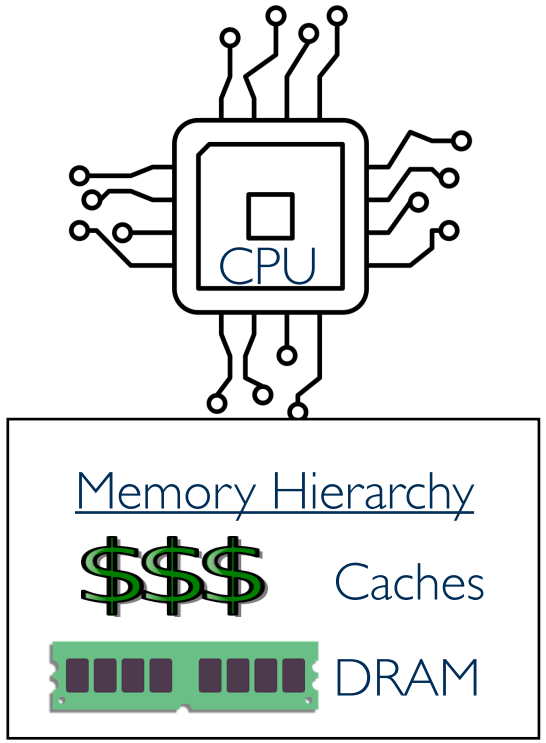
- Page tables in shared memory
  - Set up by the OS
  - Used by the hardware
- TLB consistency in software by the OS
  - Hardware brings PTE into the TLB from the PT
  - Page replacement algorithm changes the PT and does the TLB shoot-down
- Synchronized atomicity
  - Test-and-set instruction serialized by the shared bus
  - Atomic read-modify-write transaction
- Cache coherence in hardware
  - Invalidation based or update based

Roadmap

- Programmed IO and DMA
  - Chapter 10 (10.1 – 10.7)

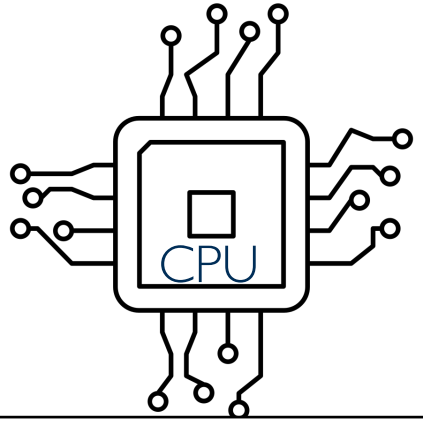
- Networking
  - Chapter 13

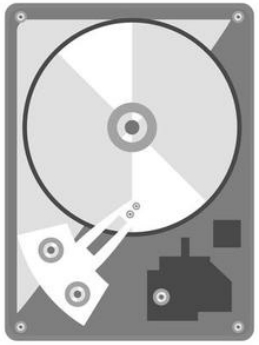
Beyond the processor and memory

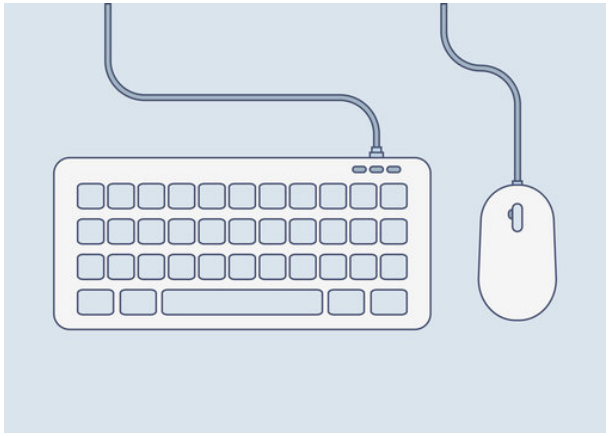


Anything else??

Beyond the processor and memory



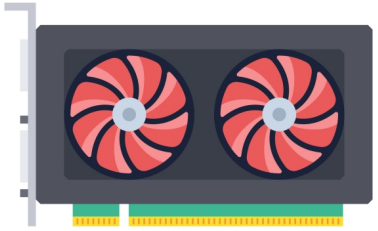


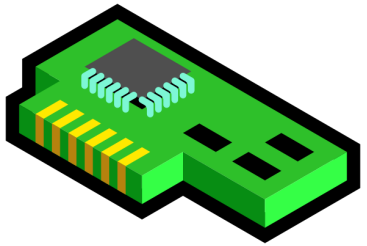


Memory Hierarchy

$$$ Caches

DRAM

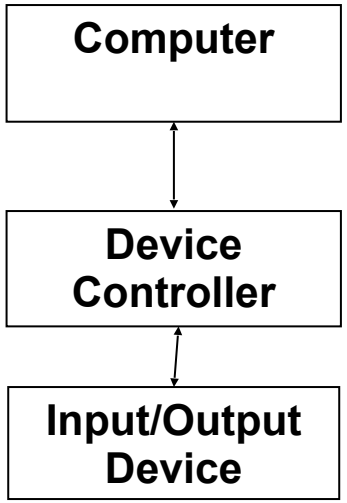




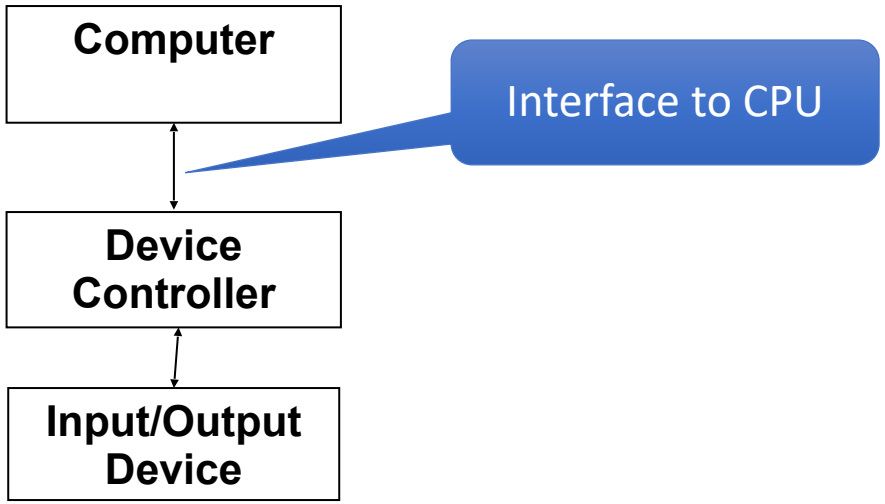
Anything else??

A lot of peripheral devices!

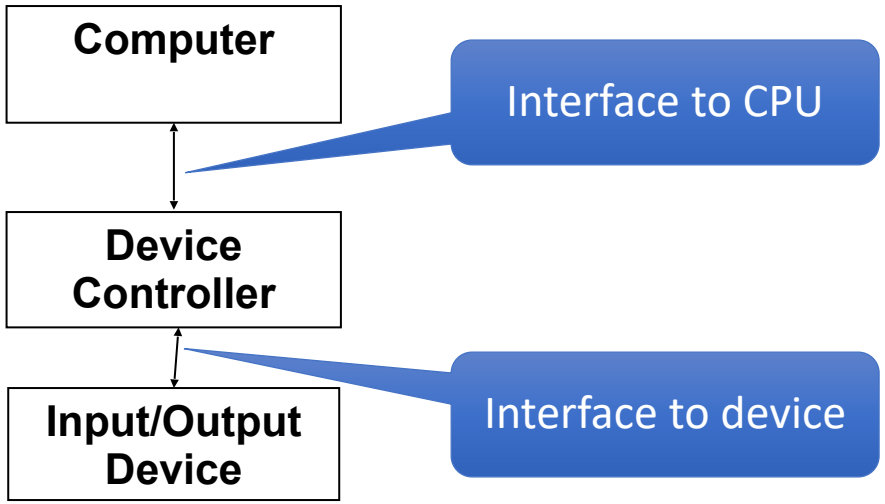
Communication: CPU and I/O Devices



Communication: CPU and I/O Devices

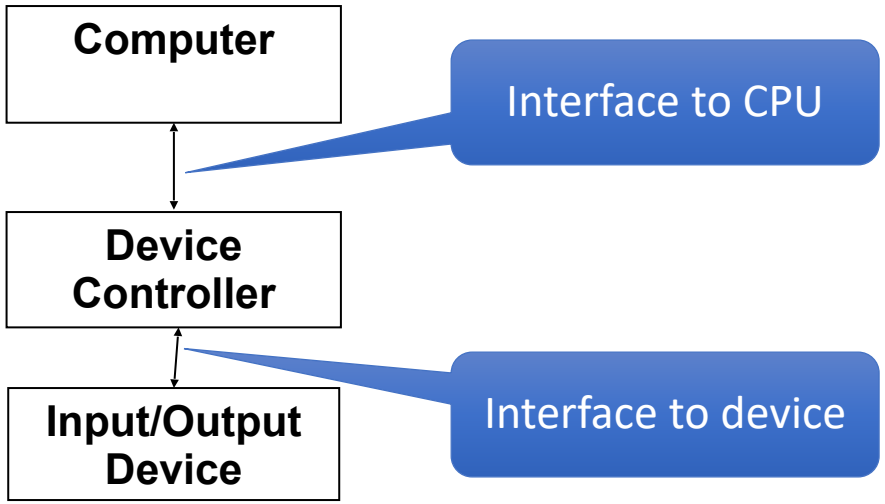


Communication: CPU and I/O Devices



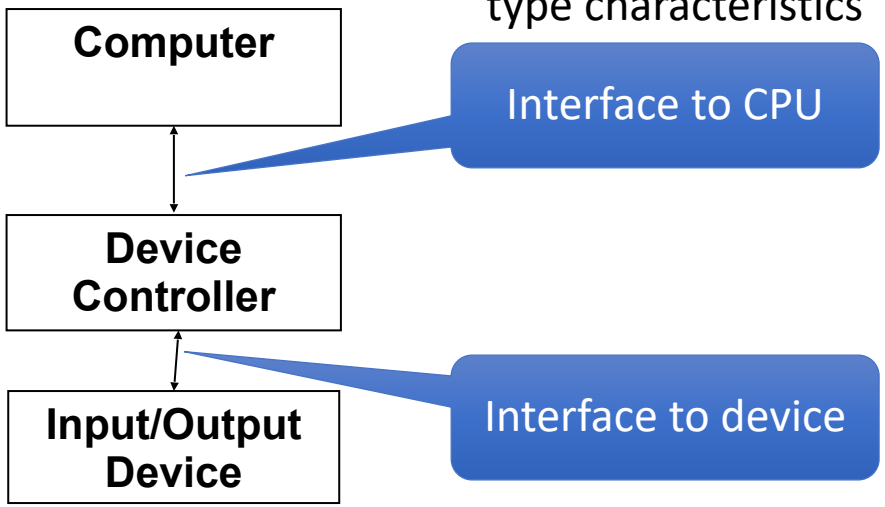
Communication: CPU and I/O Devices

- Generic part

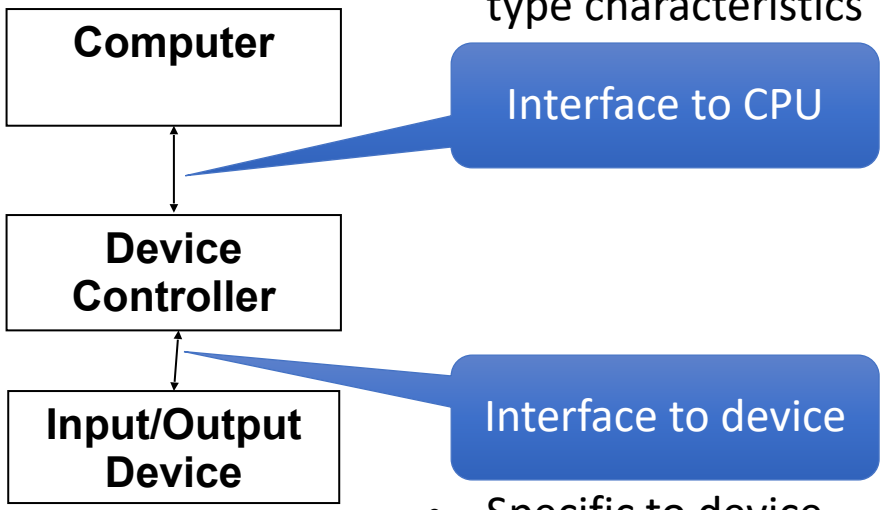


Communication: CPU and I/O Devices

- Generic part
- Specific to device-type characteristics

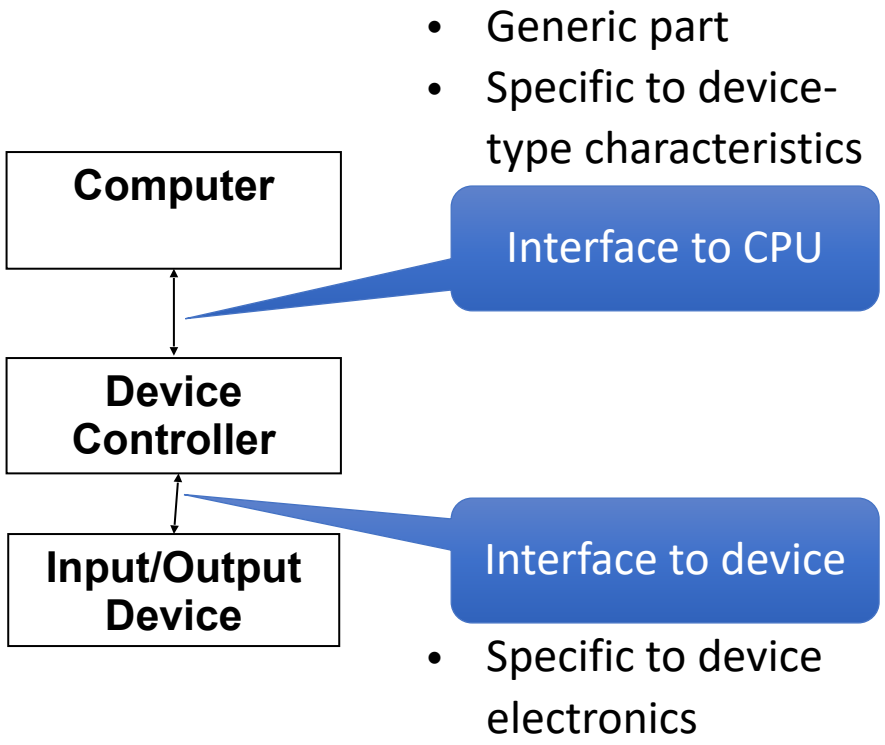


Communication: CPU and I/O Devices



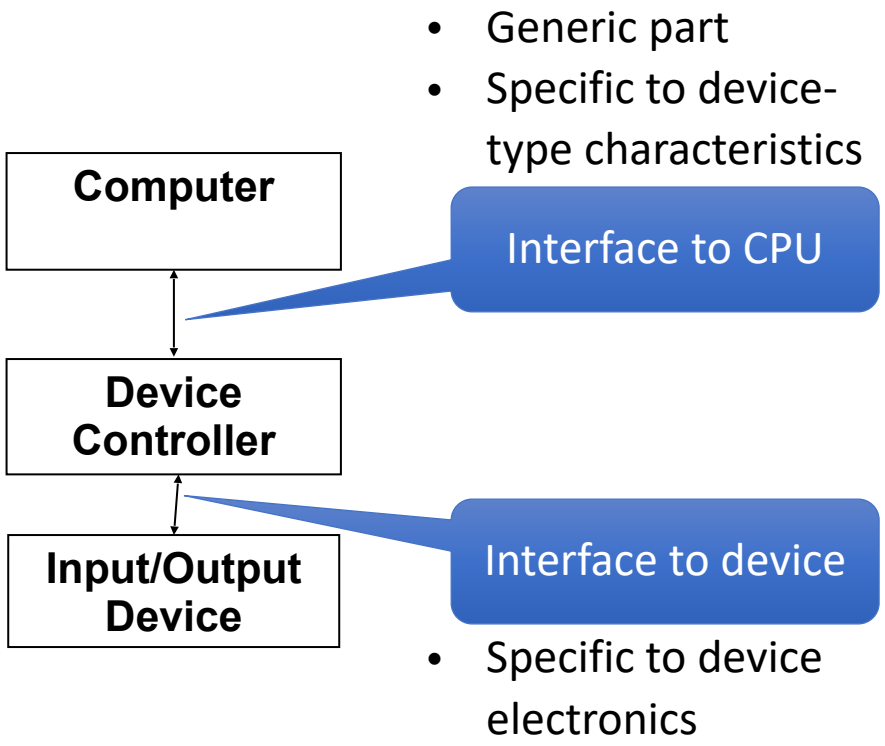
- Generic part
- Specific to device-type characteristics
- Specific to device electronics

Communication: CPU and I/O Devices



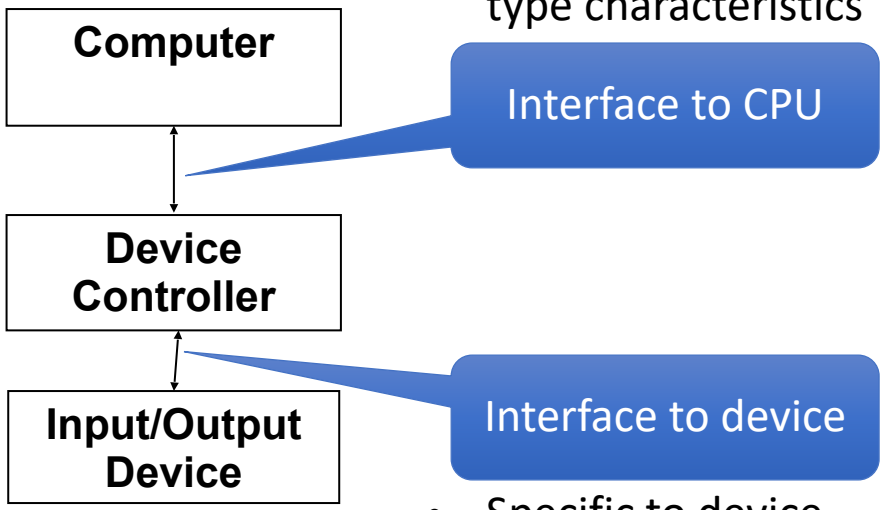
- How does the CPU "talk" to the controller
  - Memory-mapped I/O
  - Load/store instructions
  - (Alternative is special I/O instructions)

Communication: CPU and I/O Devices



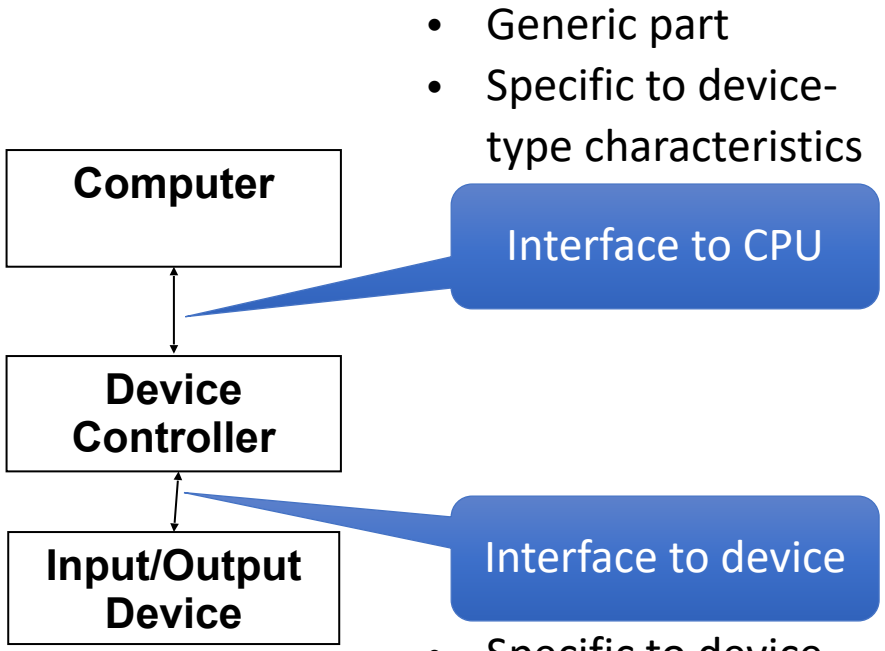
- How does the CPU "talk" to the controller
  - Memory-mapped I/O
  - Load/store instructions
  - (Alternative is special I/O instructions)
- How is data movement effected?
  - Slow speed
    - Programmed I/O
  - High speed
    - DMA & interrupts

Communication: CPU and I/O Devices



- Generic part
- Specific to device-type characteristics
- Specific to device electronics

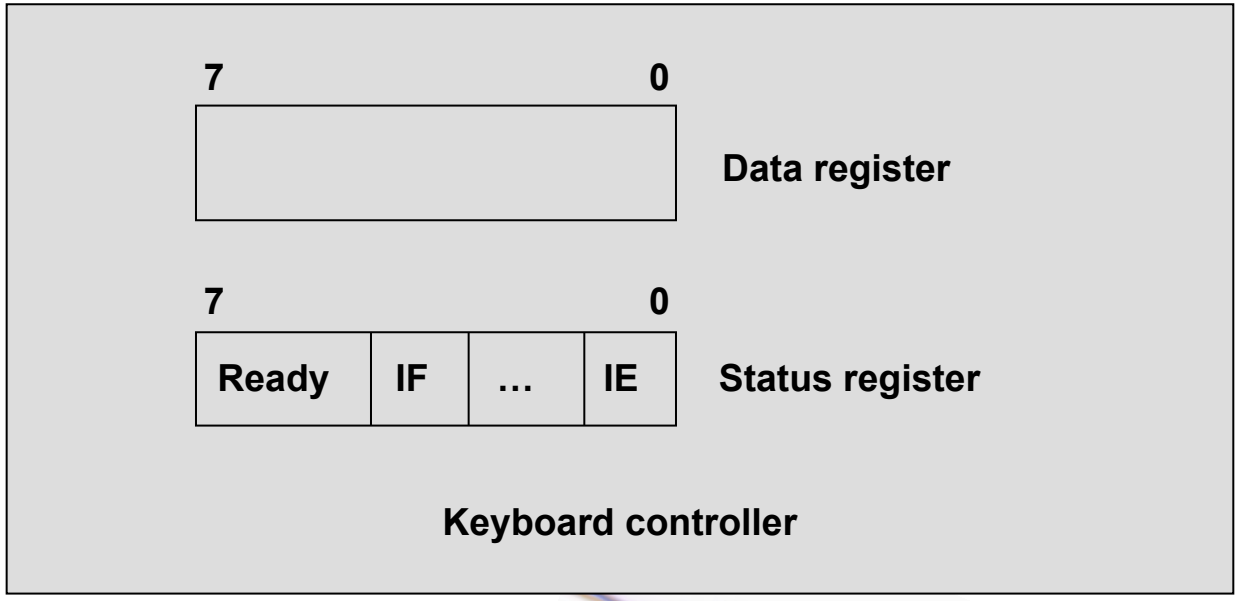
Communication: CPU and I/O Devices



- Generic part
- Specific to device-type characteristics
- Specific to device electronics

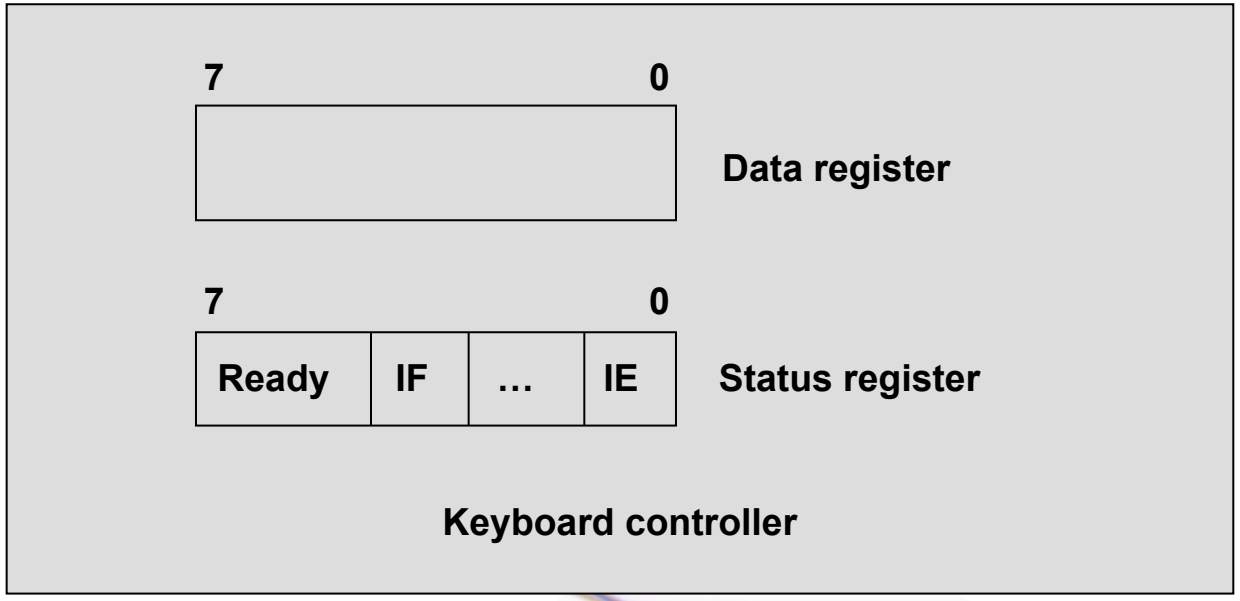
- What commands do we issue to devices?
  - Camera
  - Display
  - Audio
  - …

A keyboard device



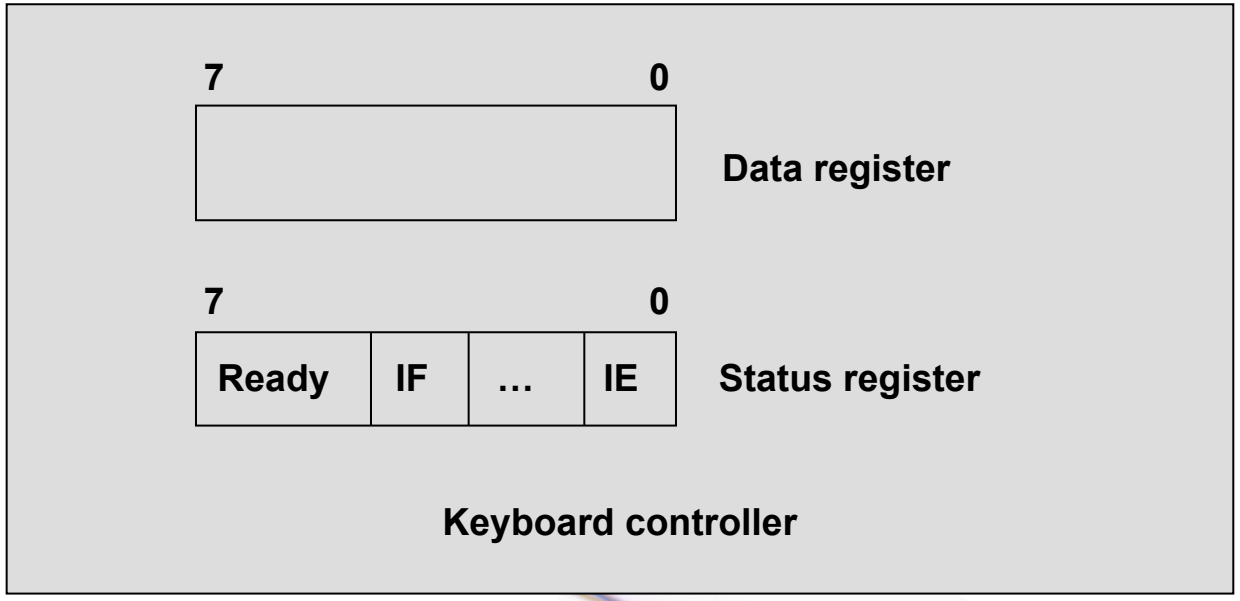
A keyboard device

Controller



A keyboard device

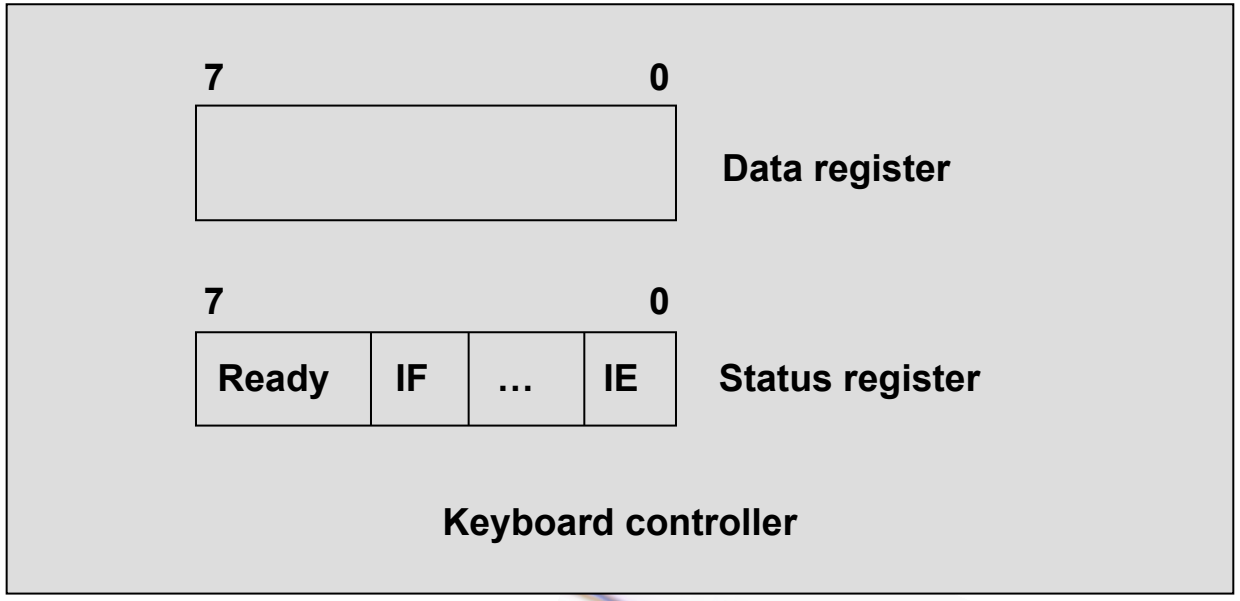
Controller



Device

A keyboard device

Controller

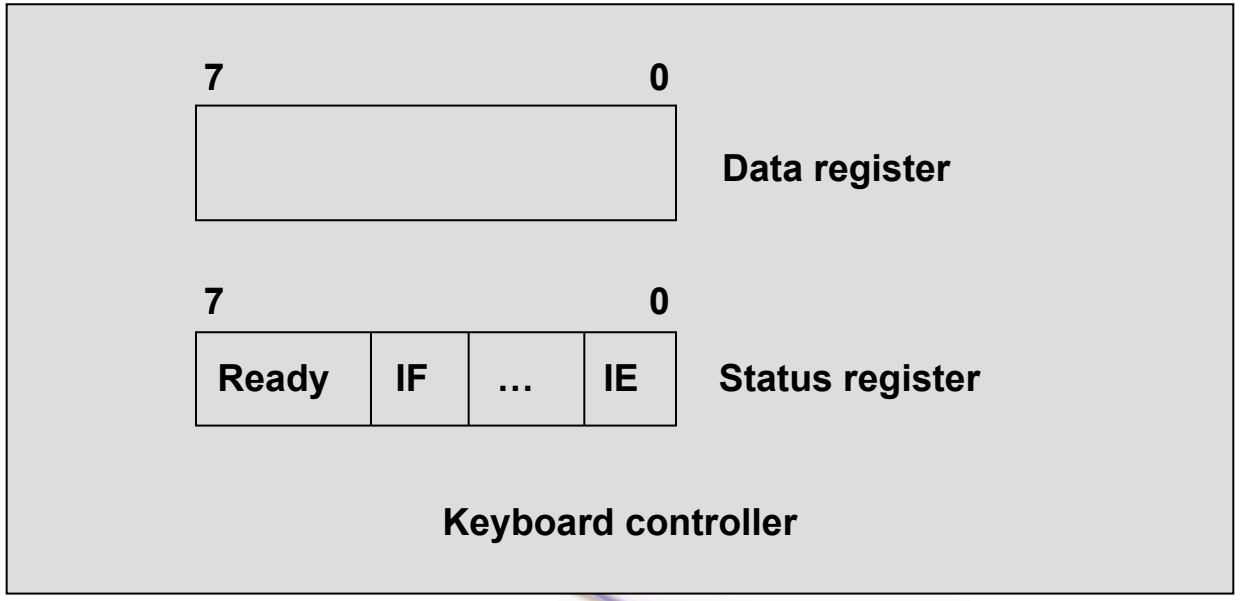


- Slow speed device

Device

A keyboard device

Controller

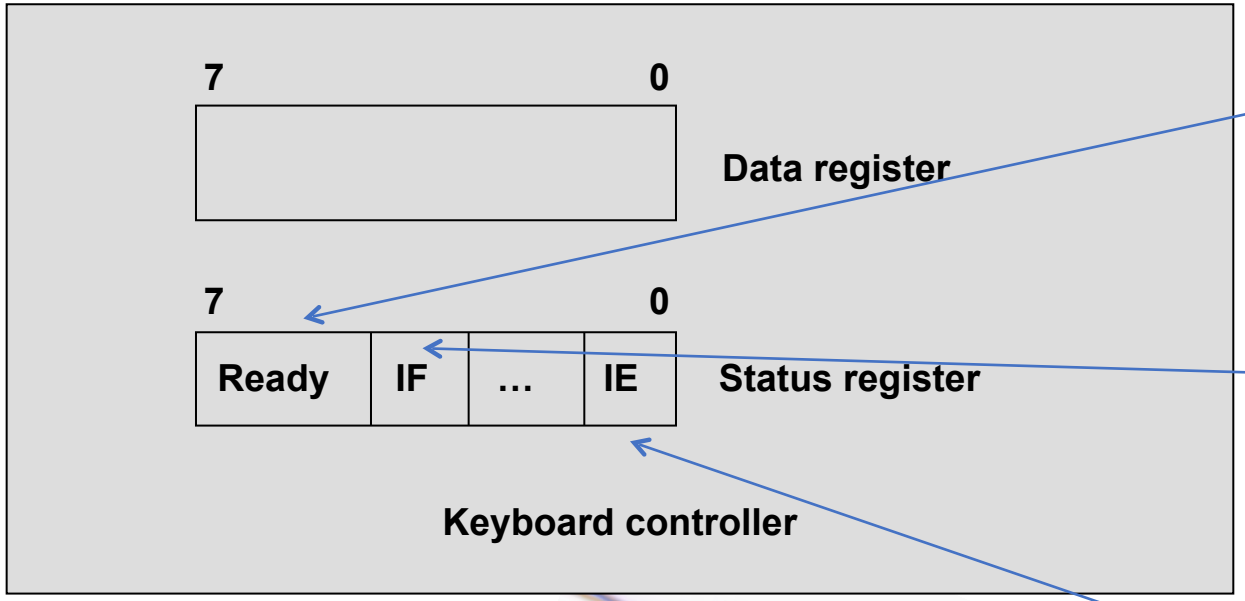


- Slow speed device
- Service it with programmed I/O (PIO)

Device

A keyboard device

Controller



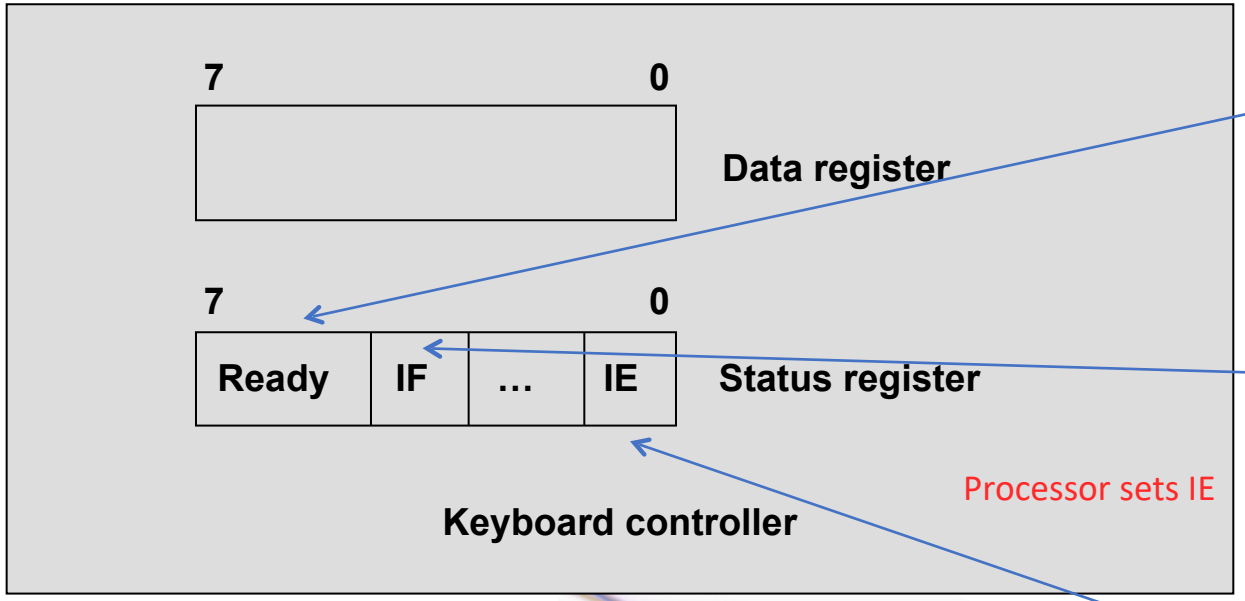
- Ready: there's a byte waiting in the data register
- IF: the device has produced data – controller ready to signal an interrupt
- IE: If 1 interrupt when Ready

- Slow speed device
- Service it with programmed I/O (PIO)

Device

A keyboard device

Controller



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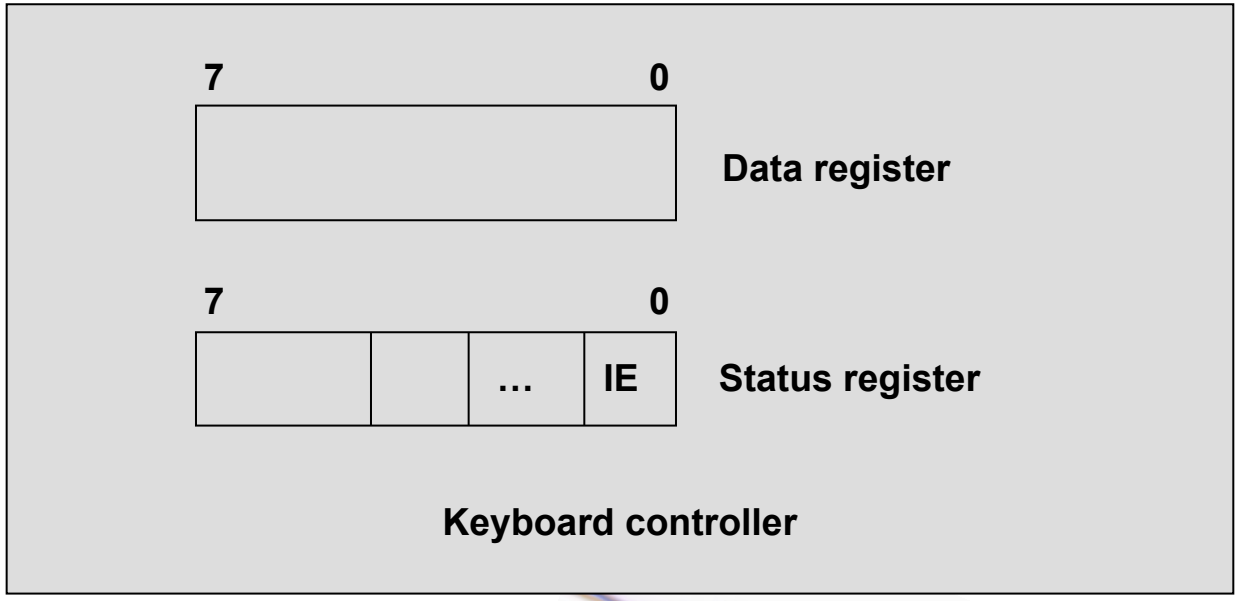
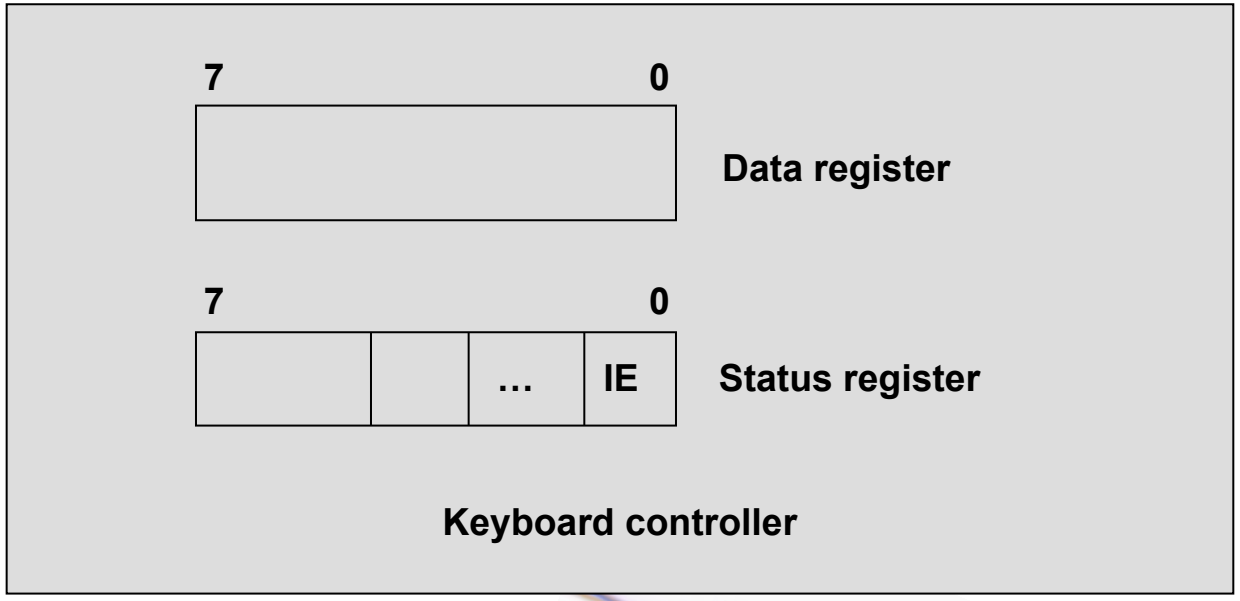
Device

A keyboard device

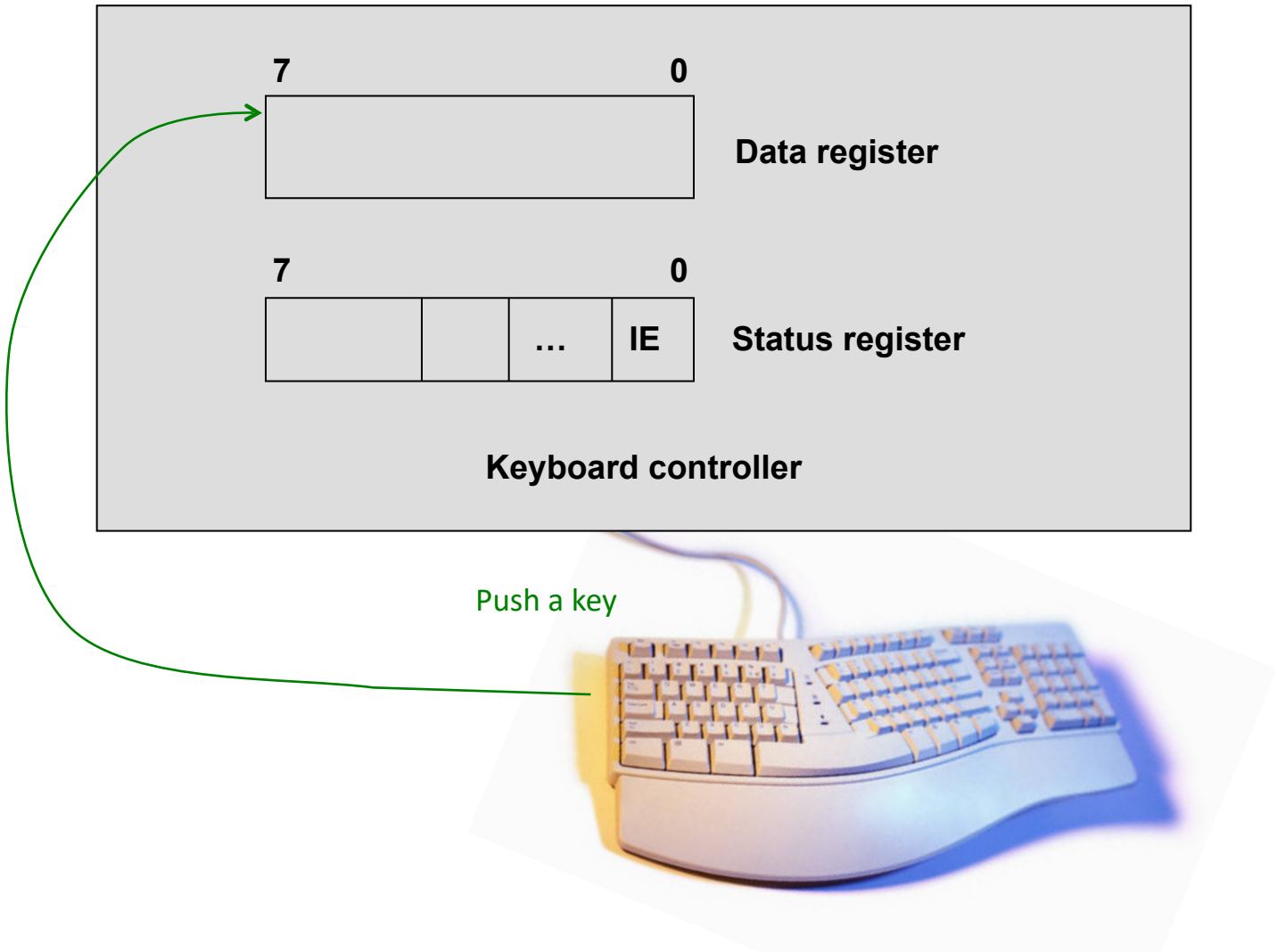


A keyboard device

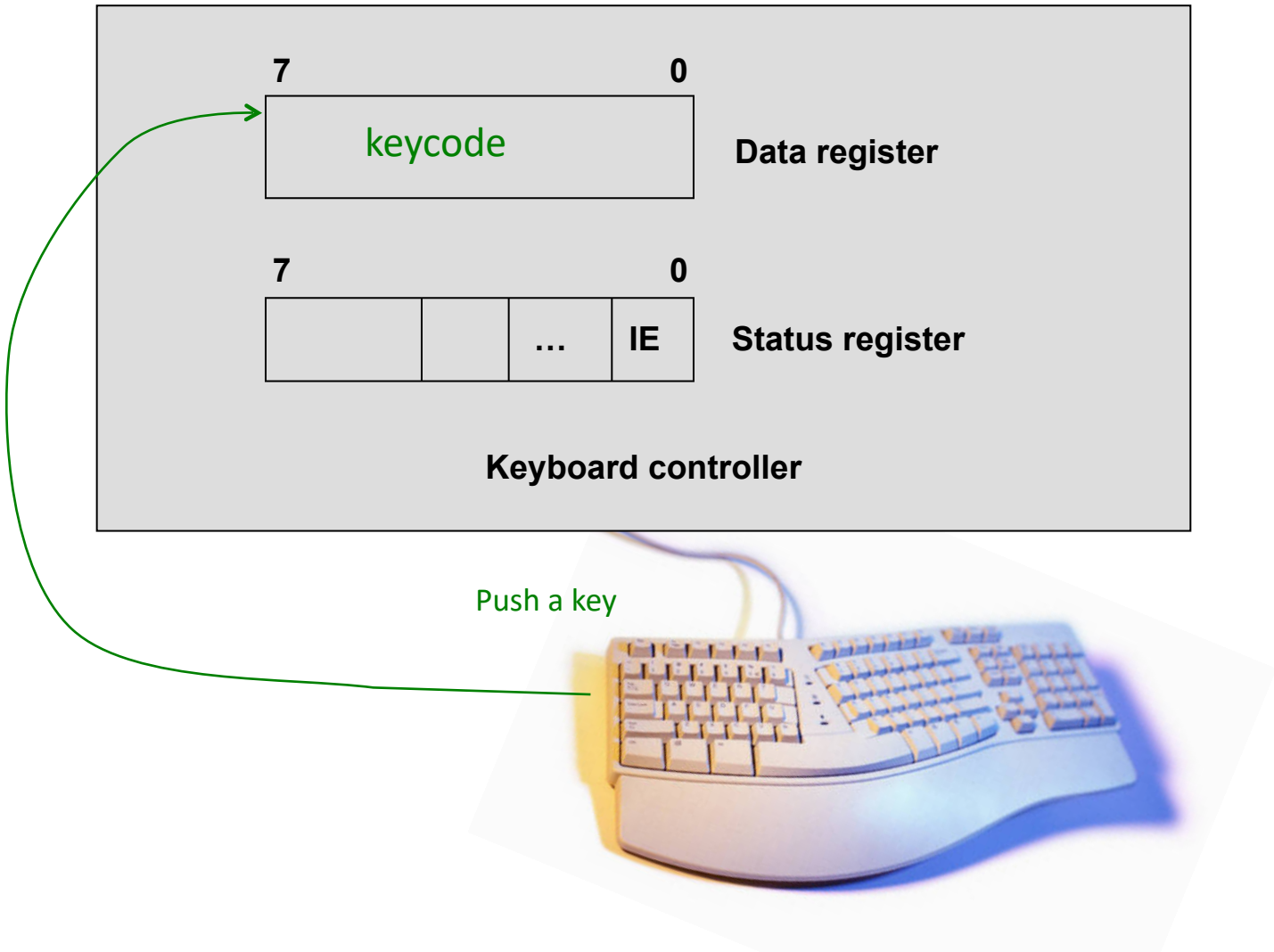


Push a key

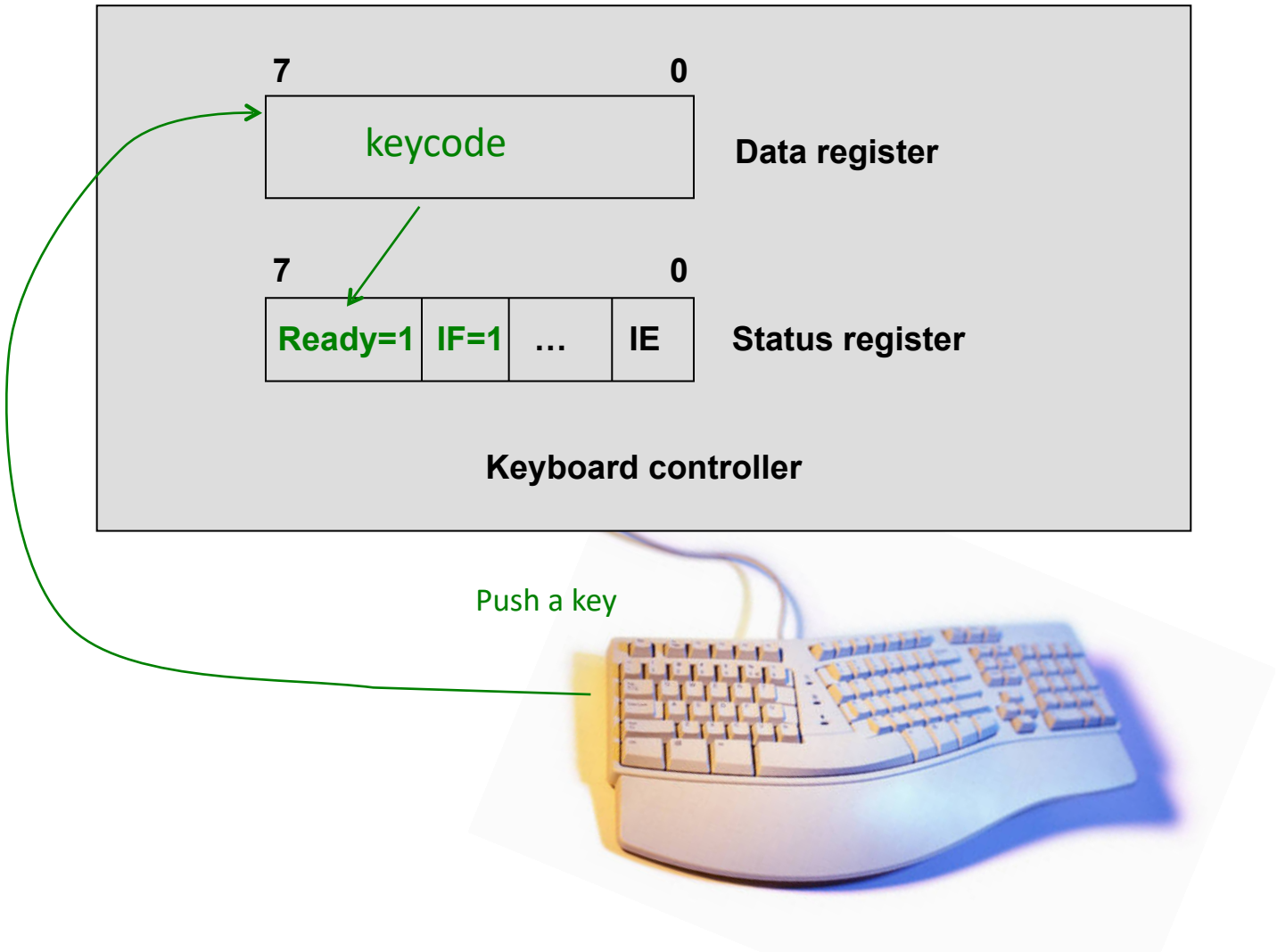
A keyboard device



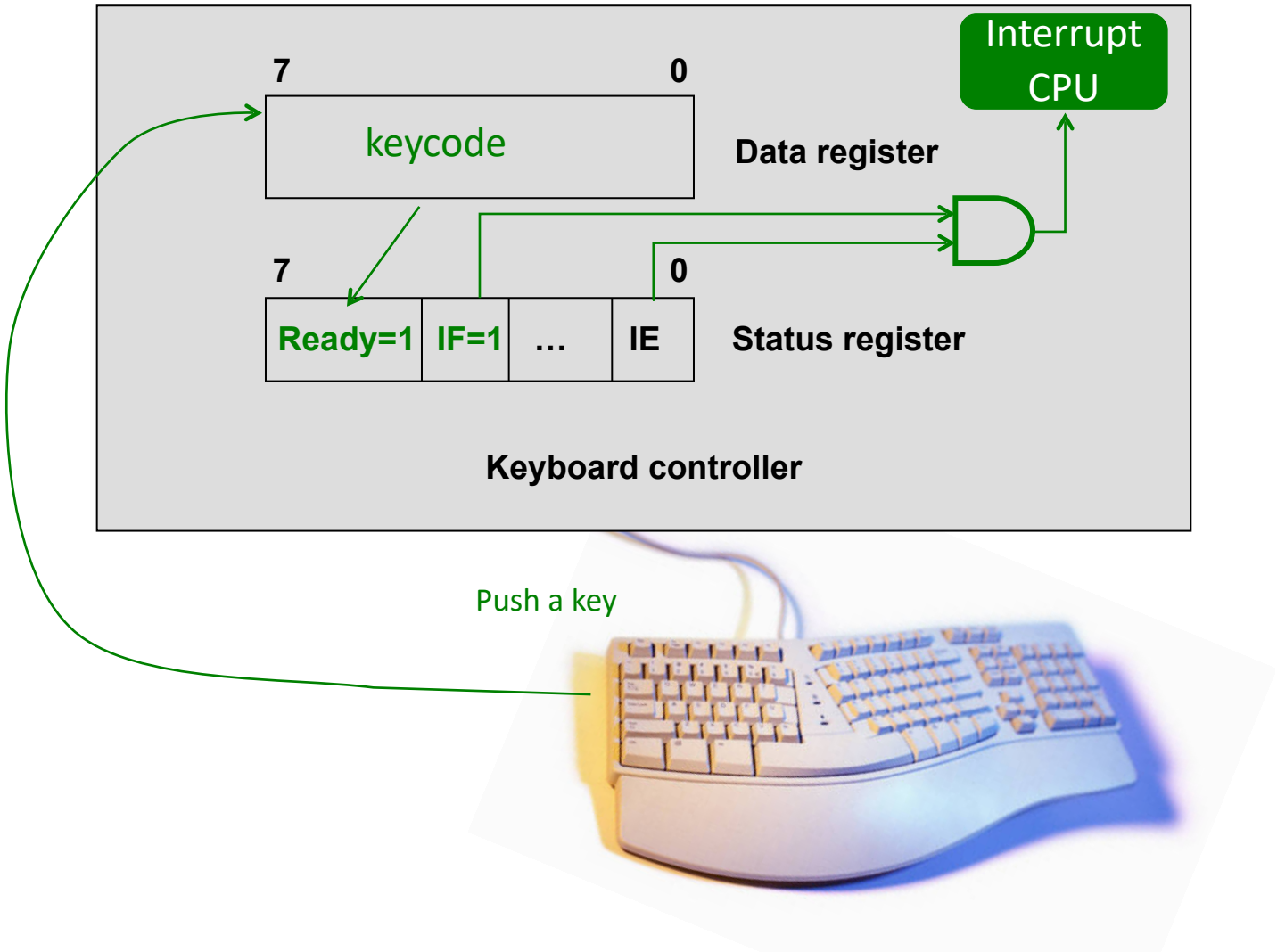
A keyboard device



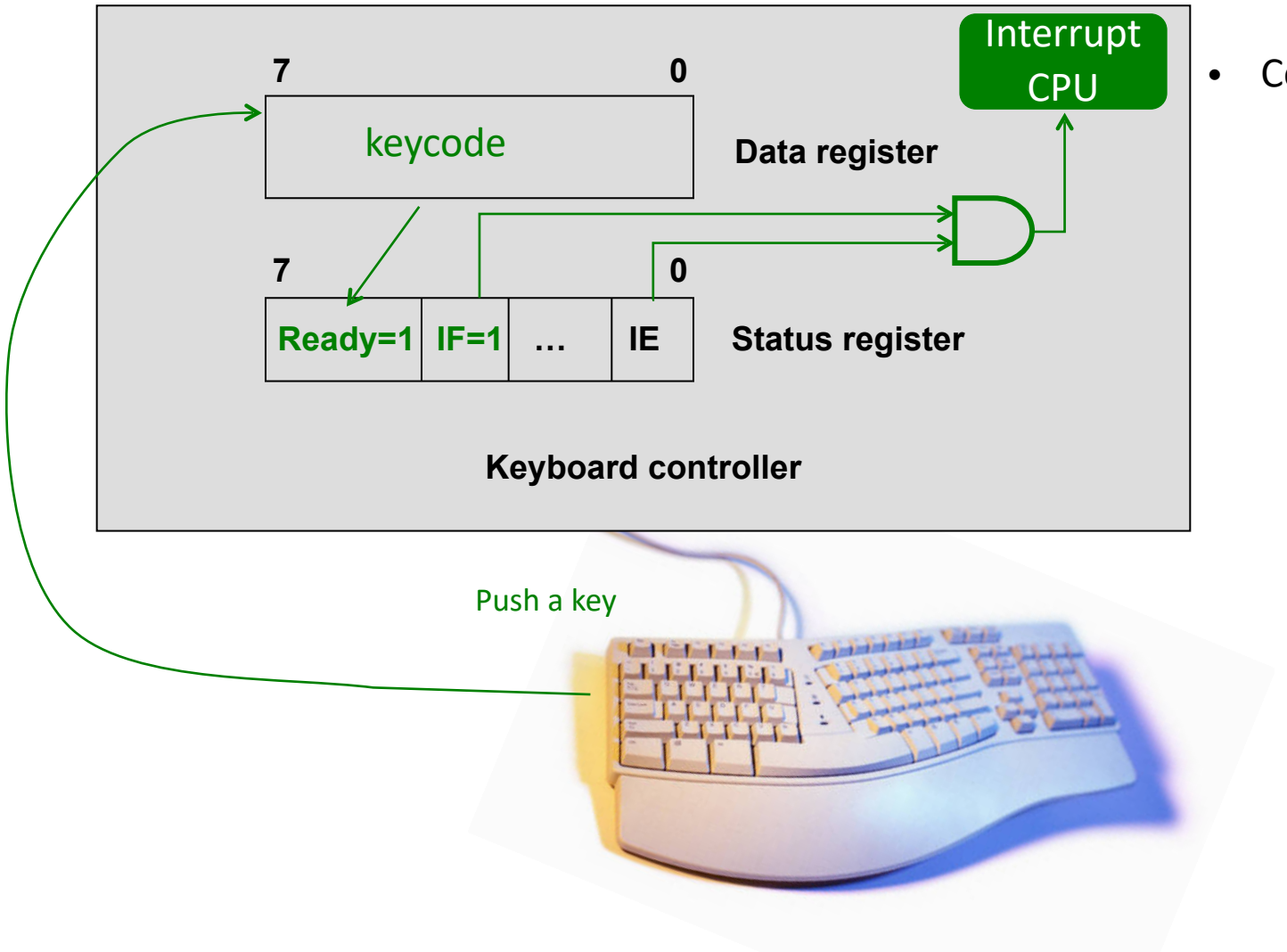
A keyboard device



A keyboard device

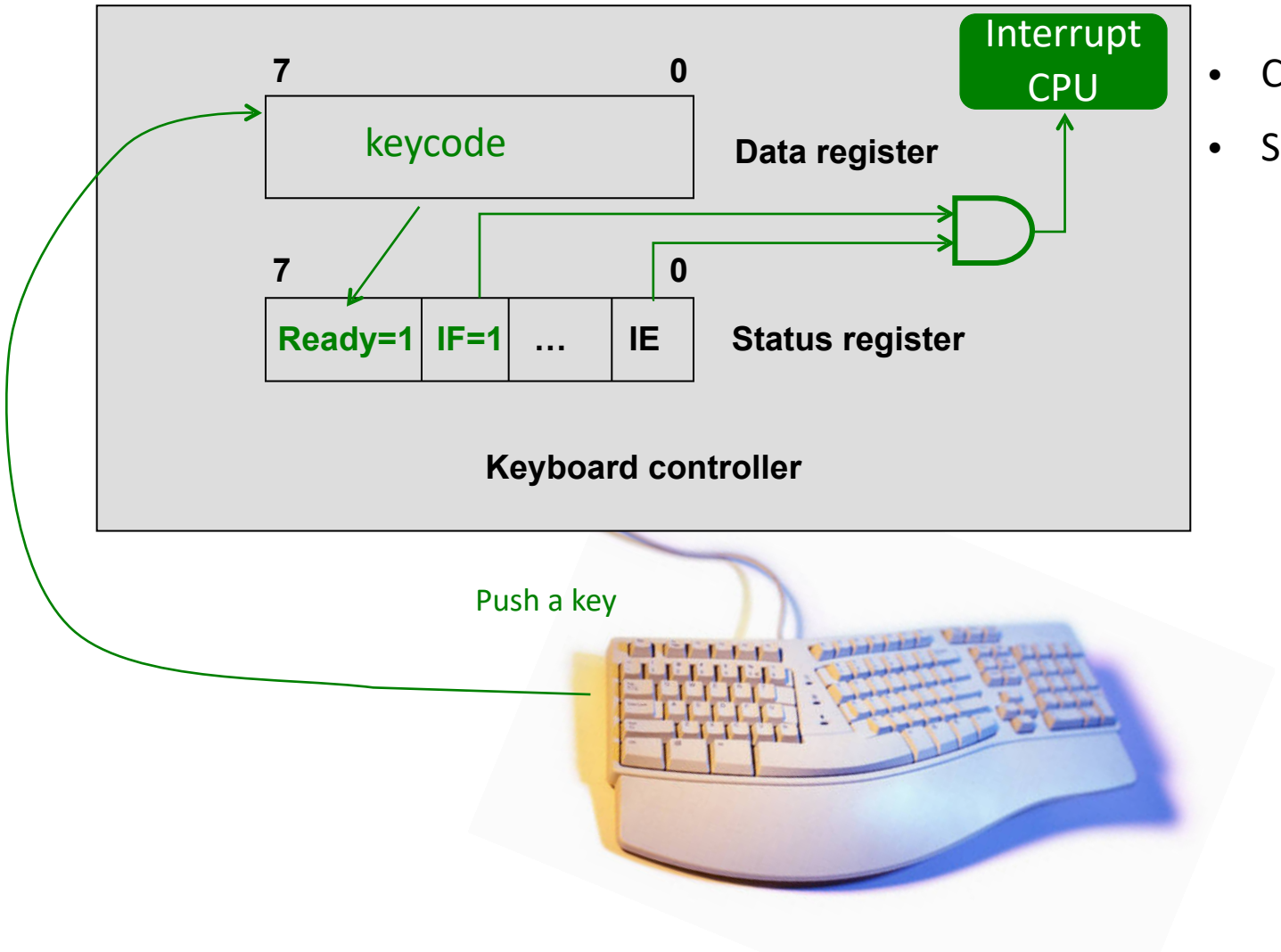


A keyboard device



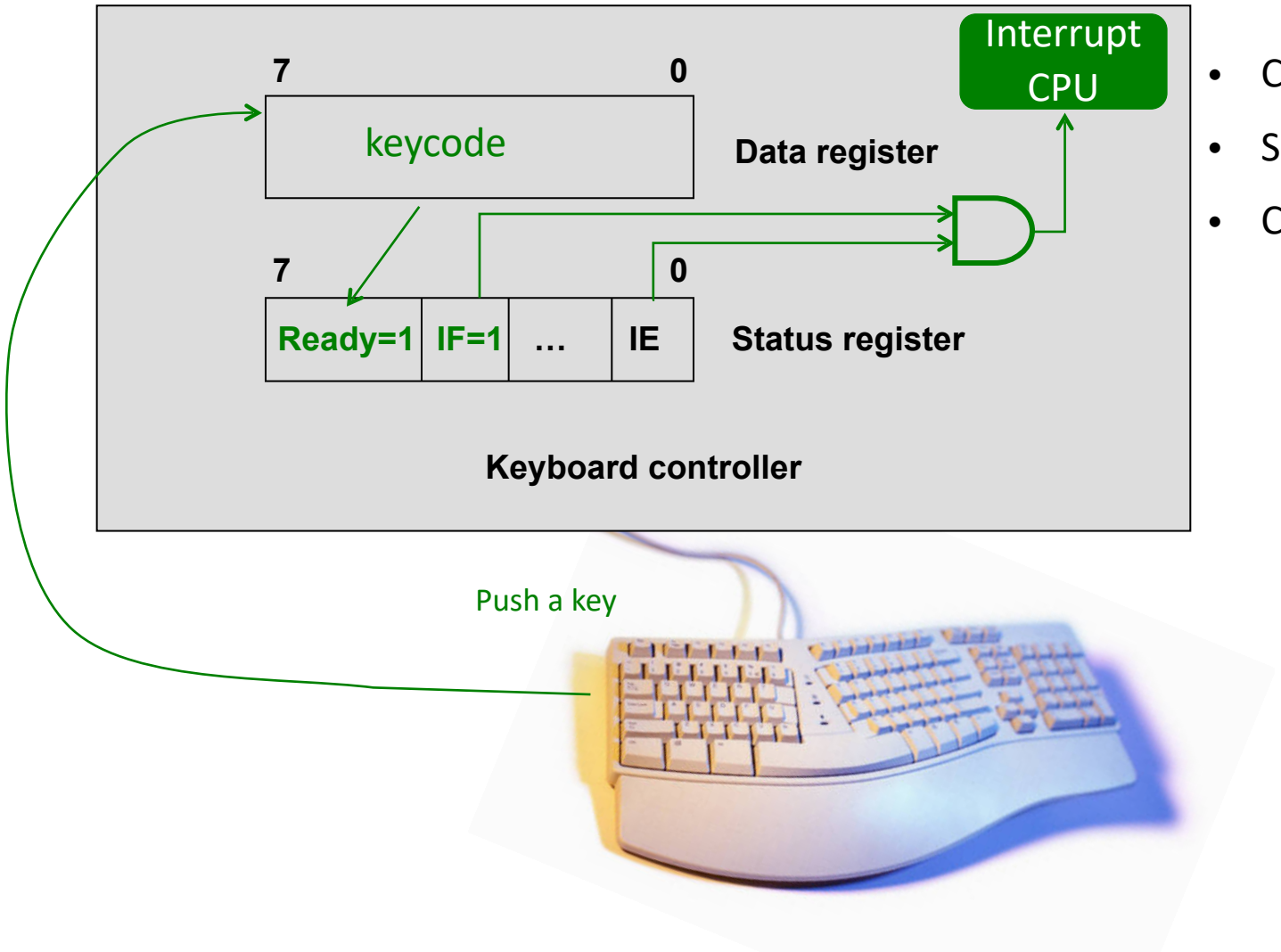
- Commands from the CPU:

A keyboard device



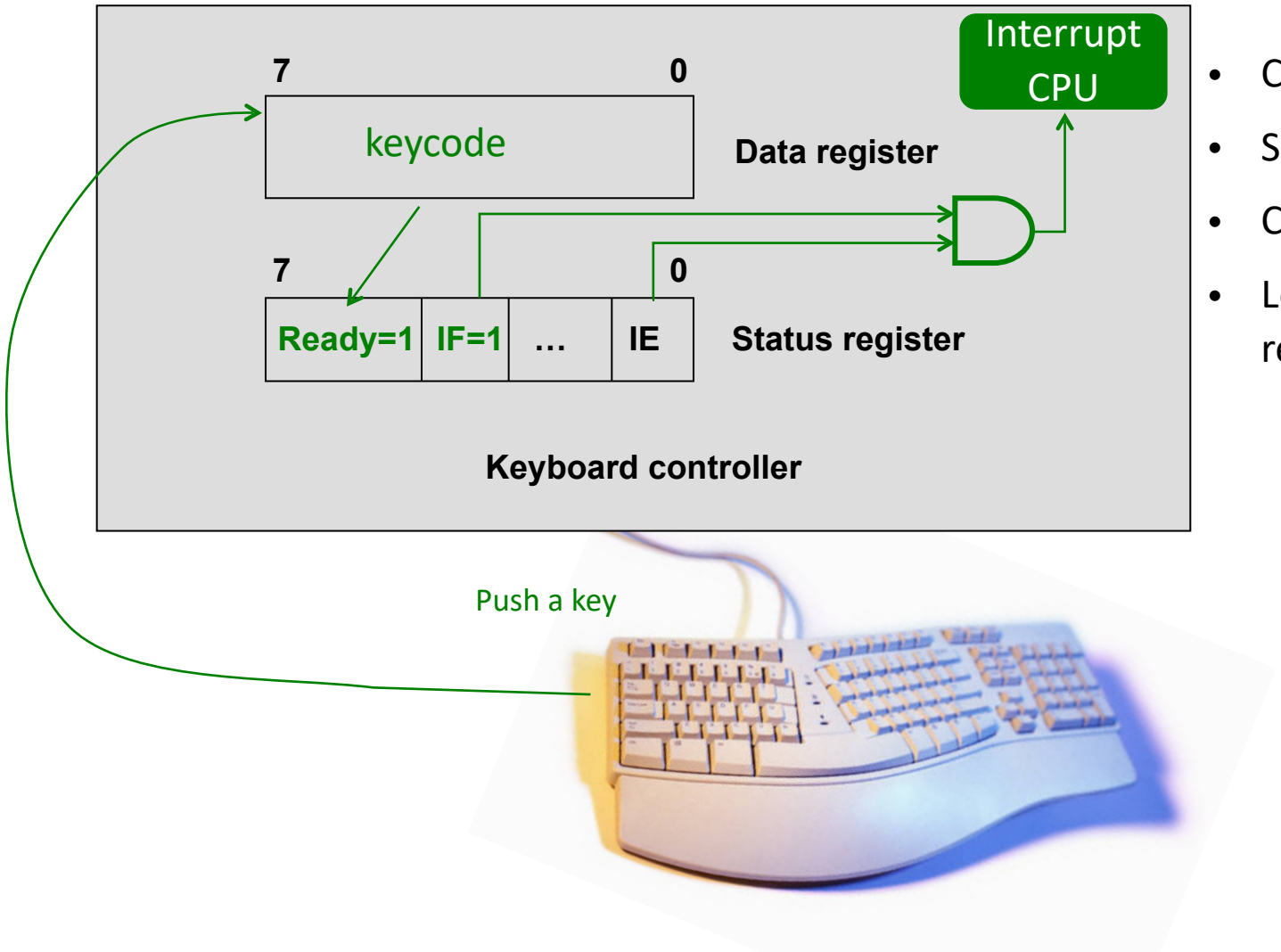
- Commands from the CPU:
- Set IE

A keyboard device



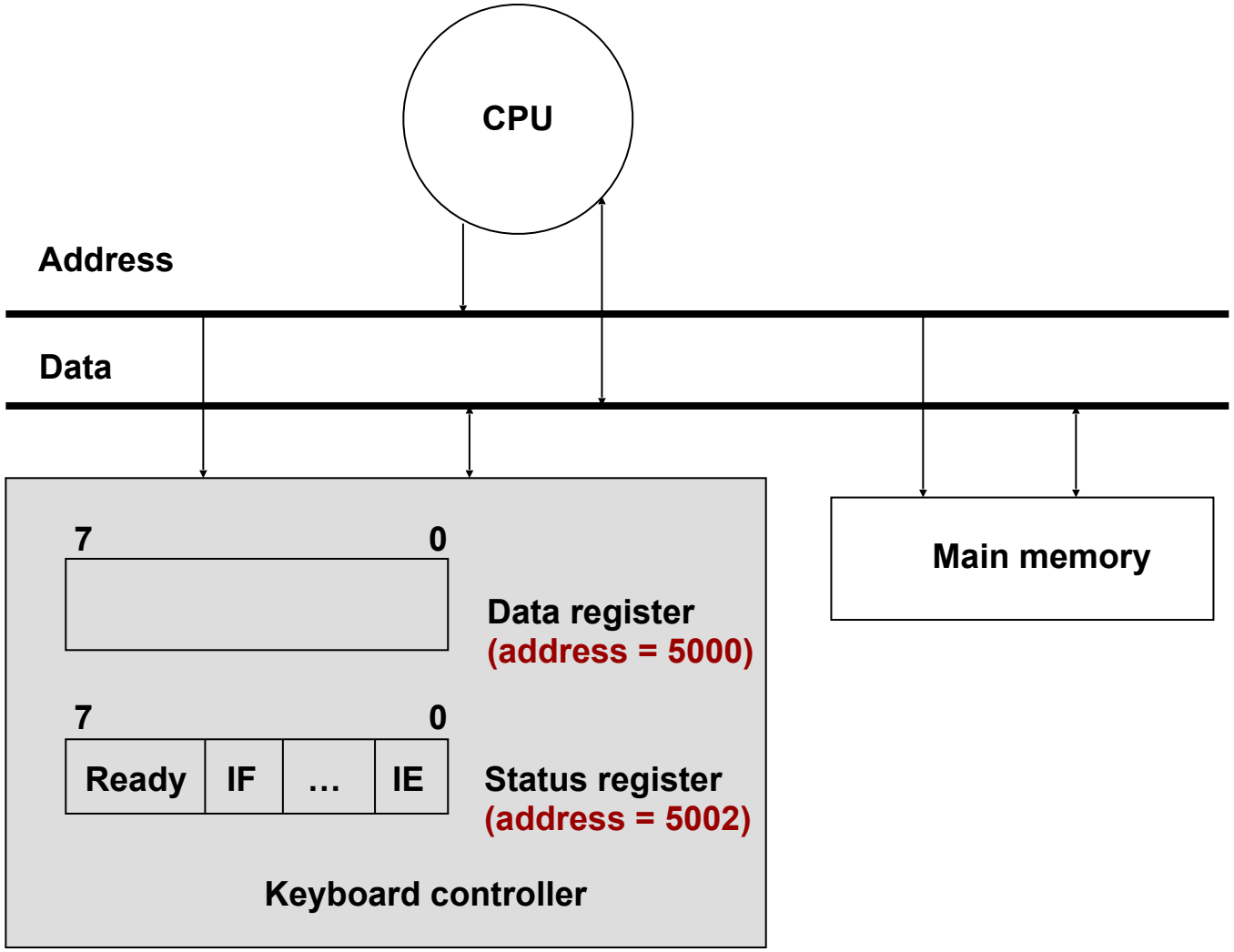
- Commands from the CPU:
- Set IE
- Check Ready equals 1

A keyboard device

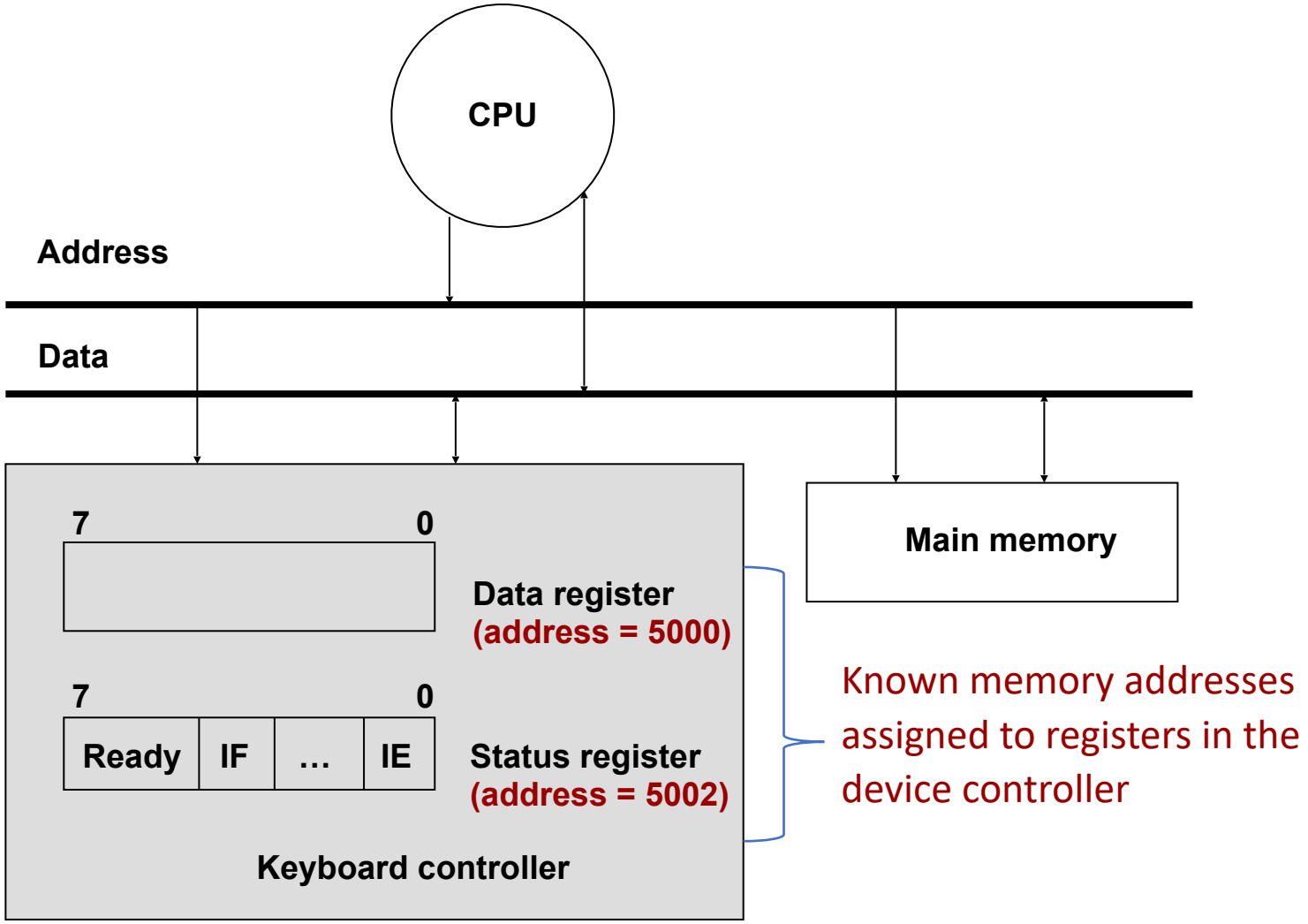


- Commands from the CPU:
- Set IE
- Check Ready equals 1
- Load keycode from data register

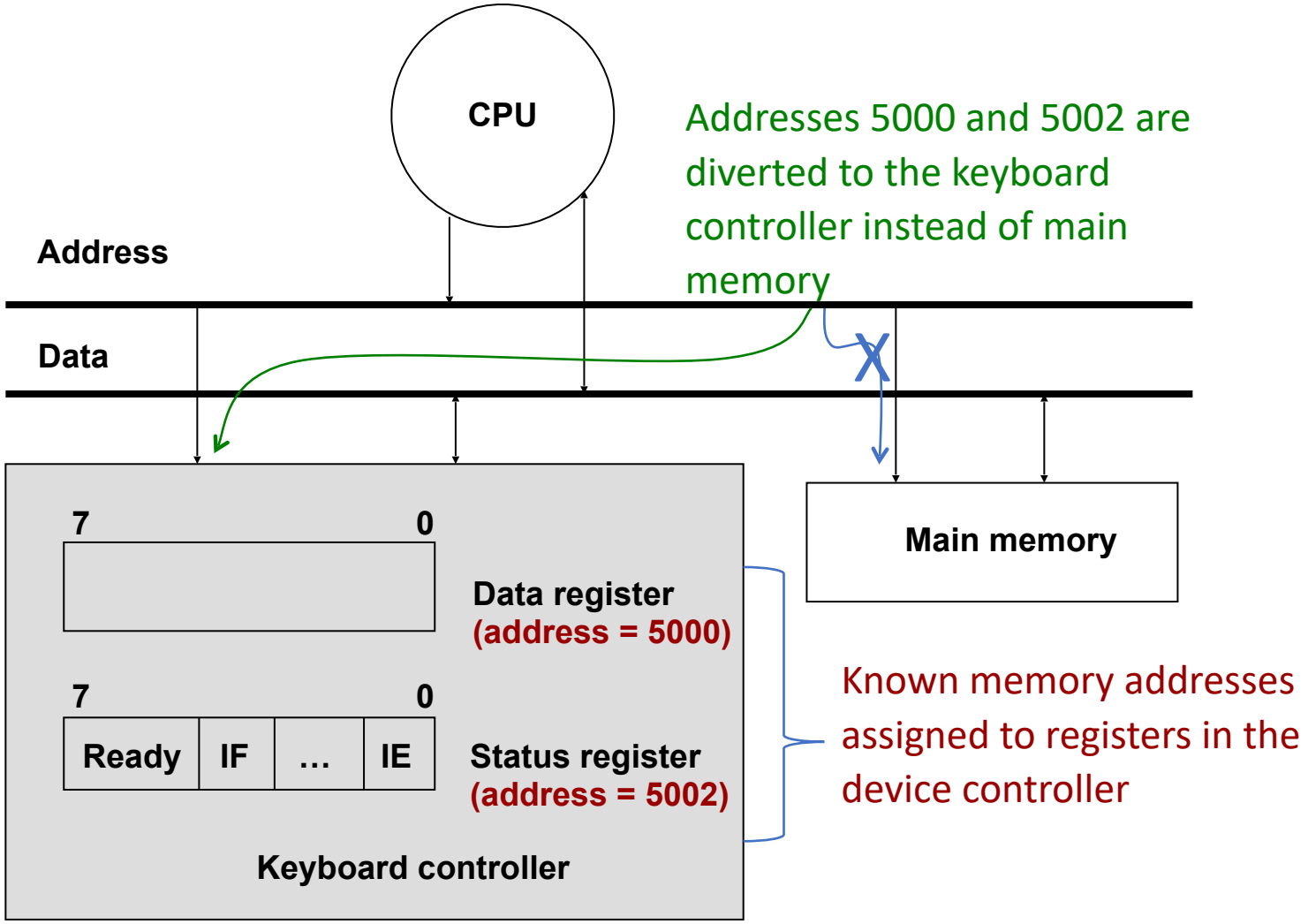
Memory mapped I/O



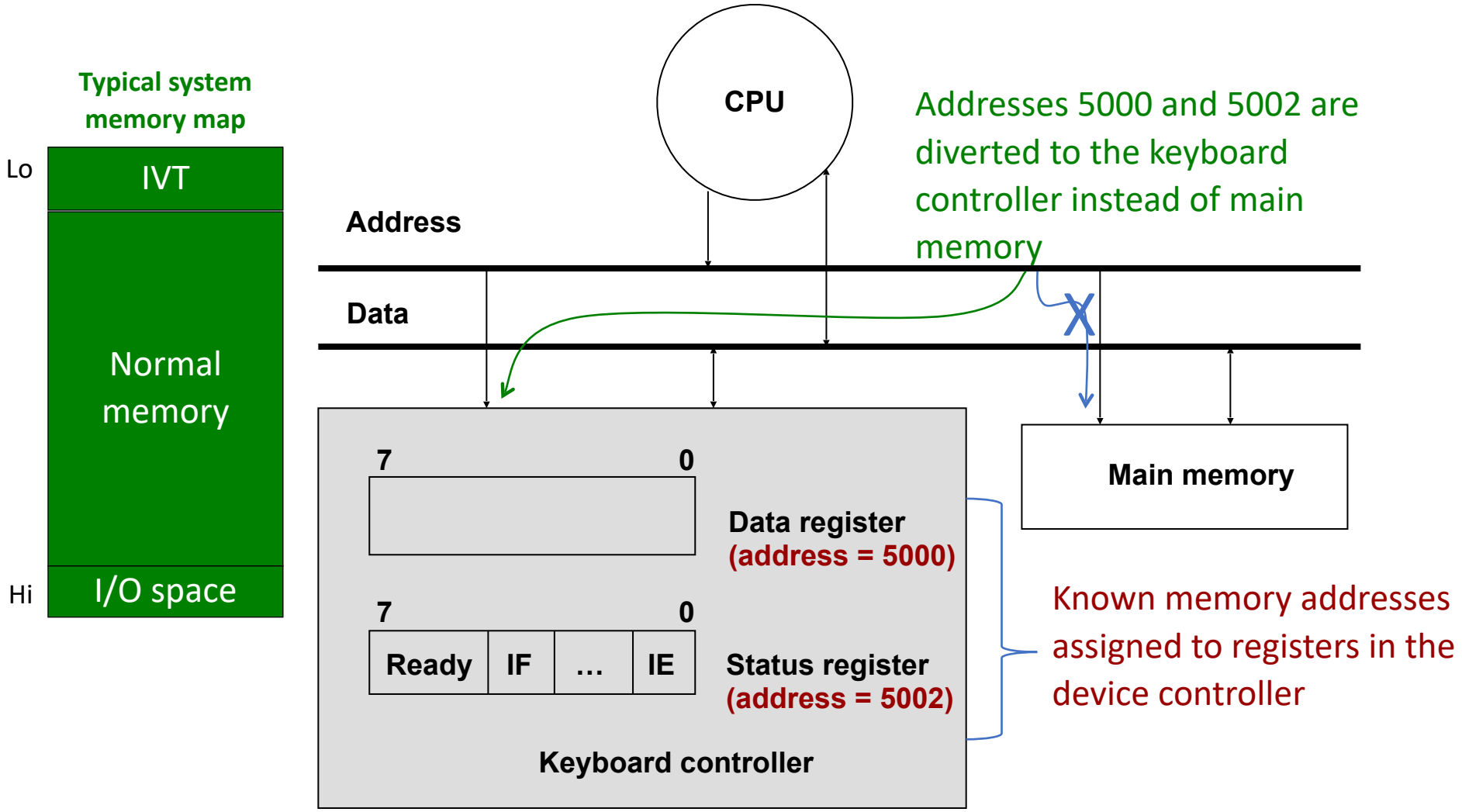
Memory mapped I/O



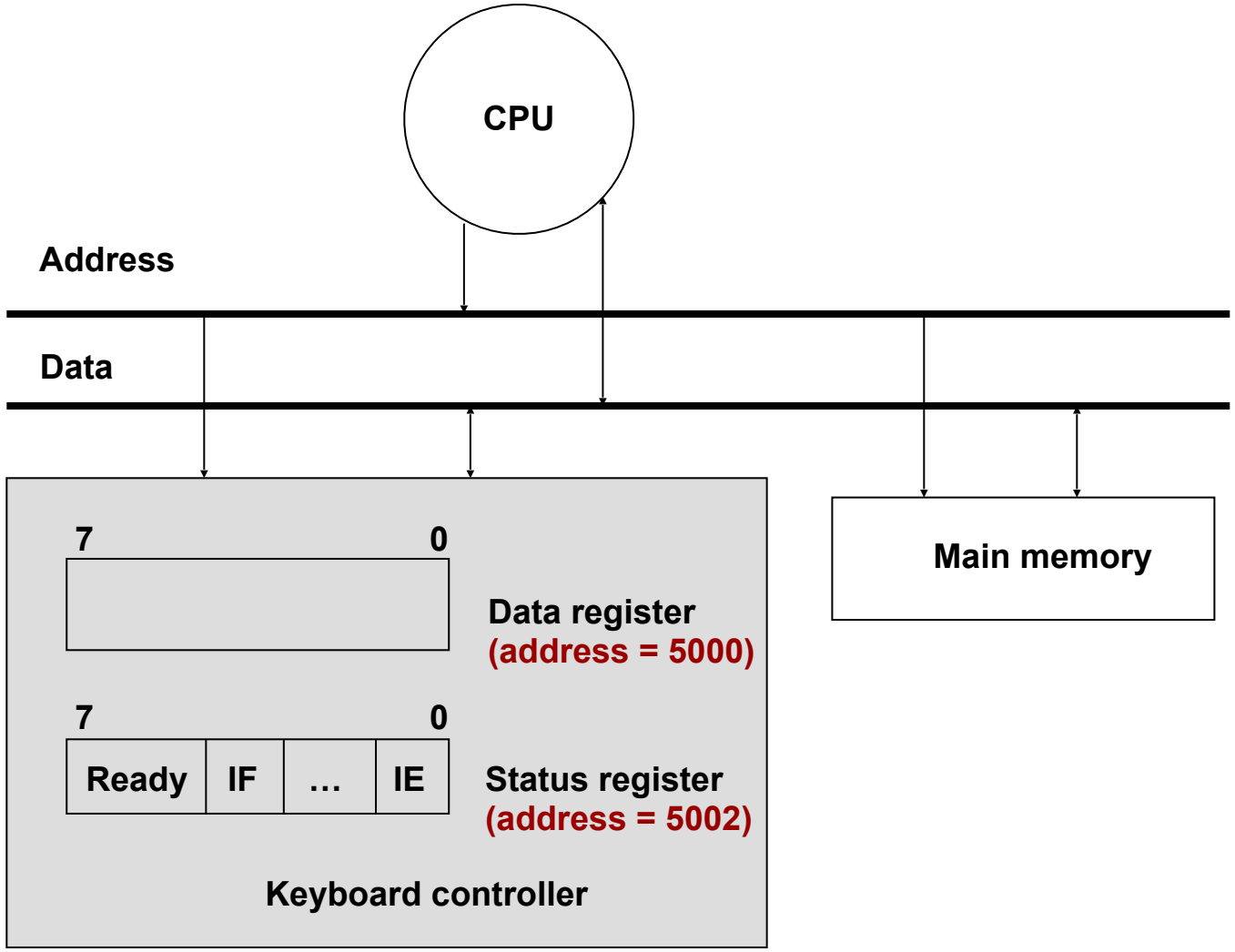
Memory mapped I/O



Memory mapped I/O

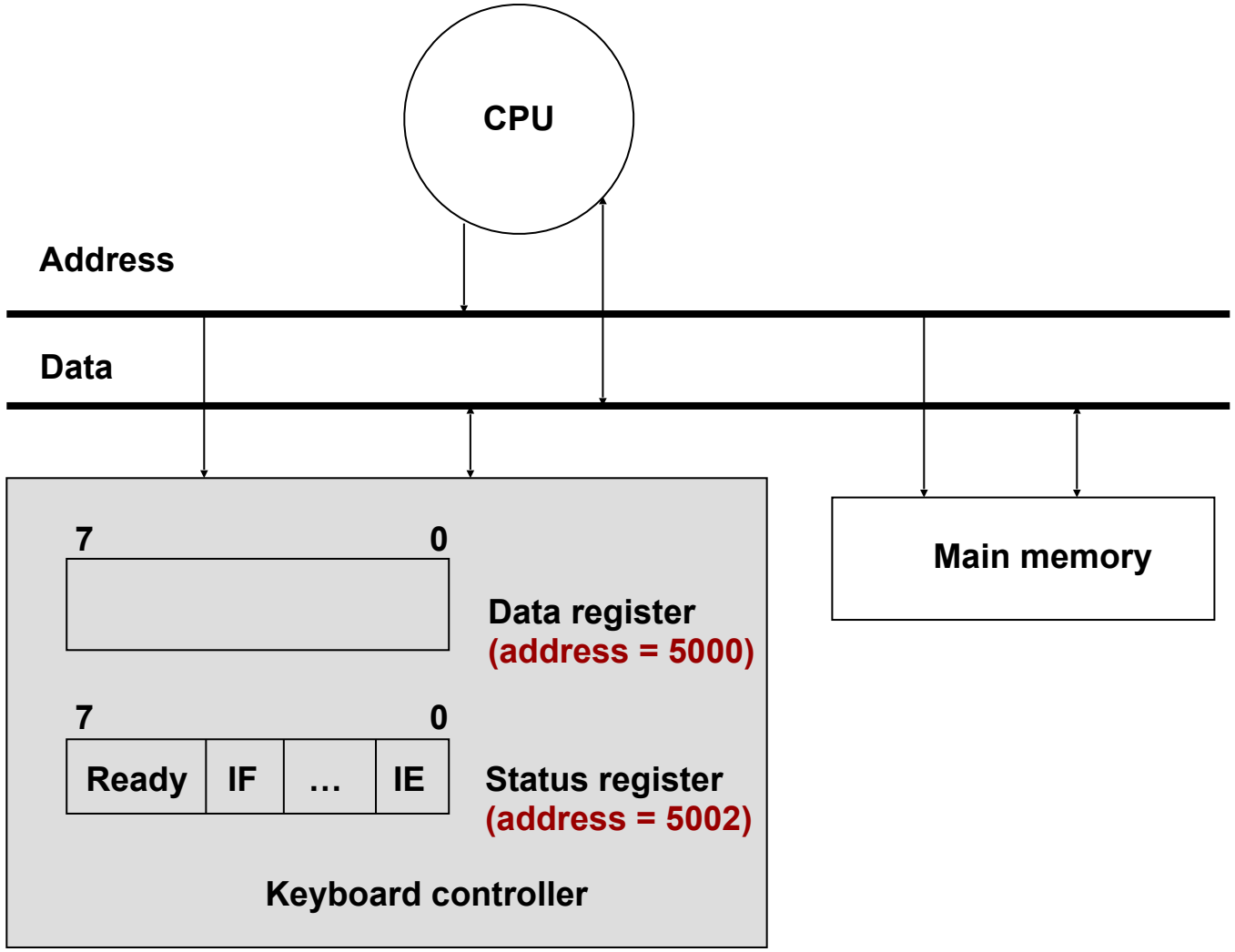


Memory mapped I/O



Memory mapped I/O

Commands?

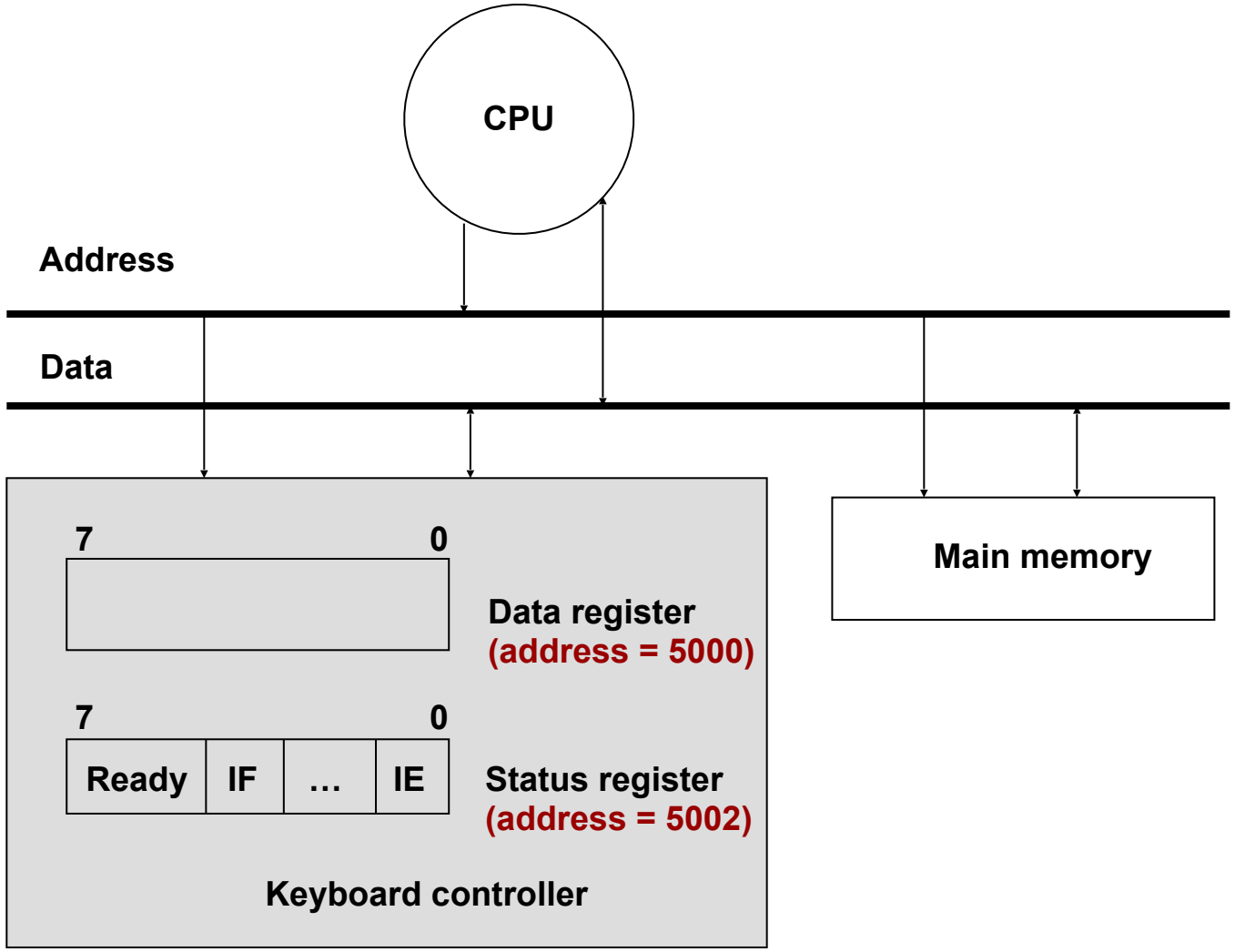


Memory mapped I/O

Commands?

Check for new data

LD R1,mem[5002]



Memory mapped I/O

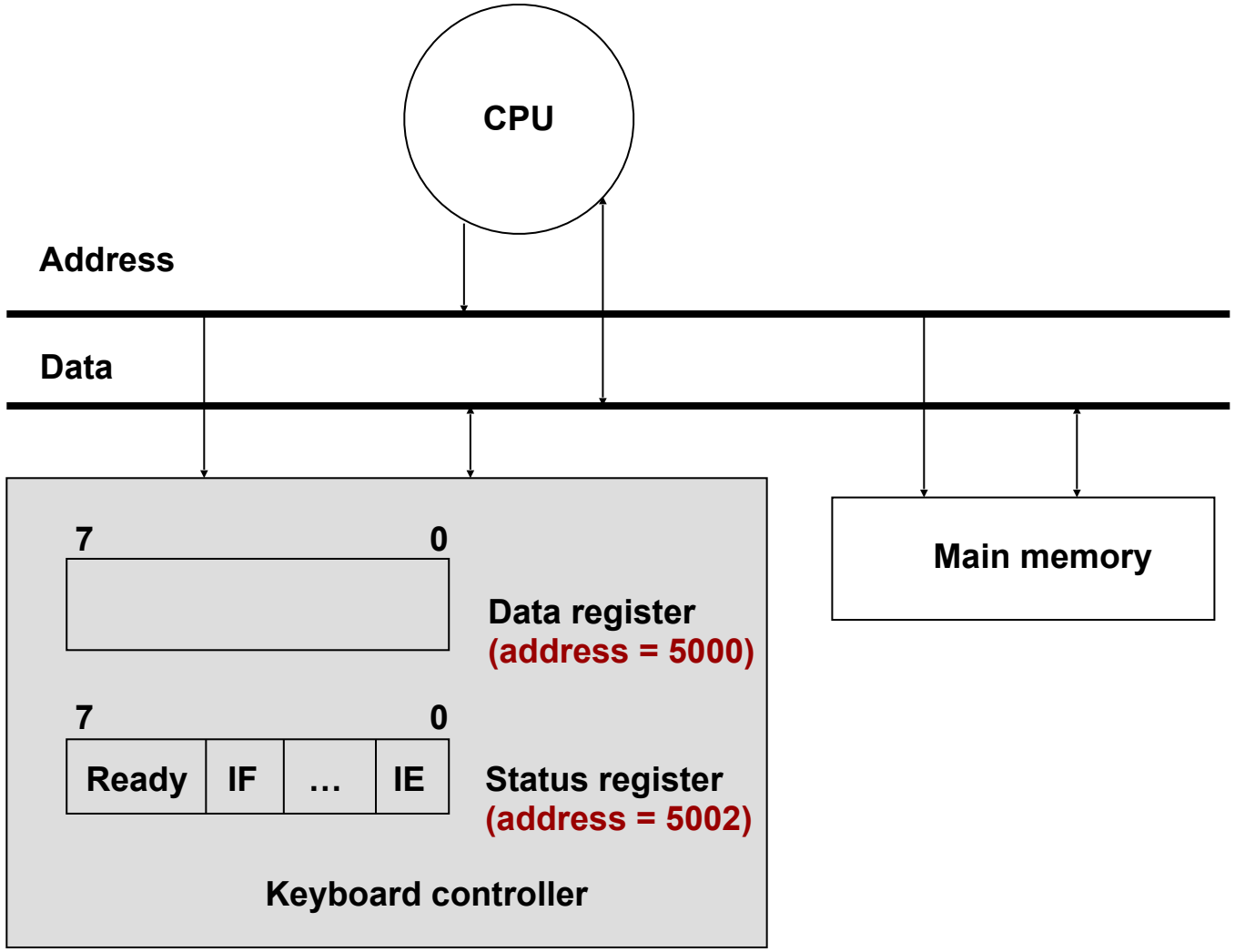
Commands?

Check for new data

LD R1,mem[5002]

Read data

LD R2,mem[5000]



Memory mapped I/O

Commands?

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Read data

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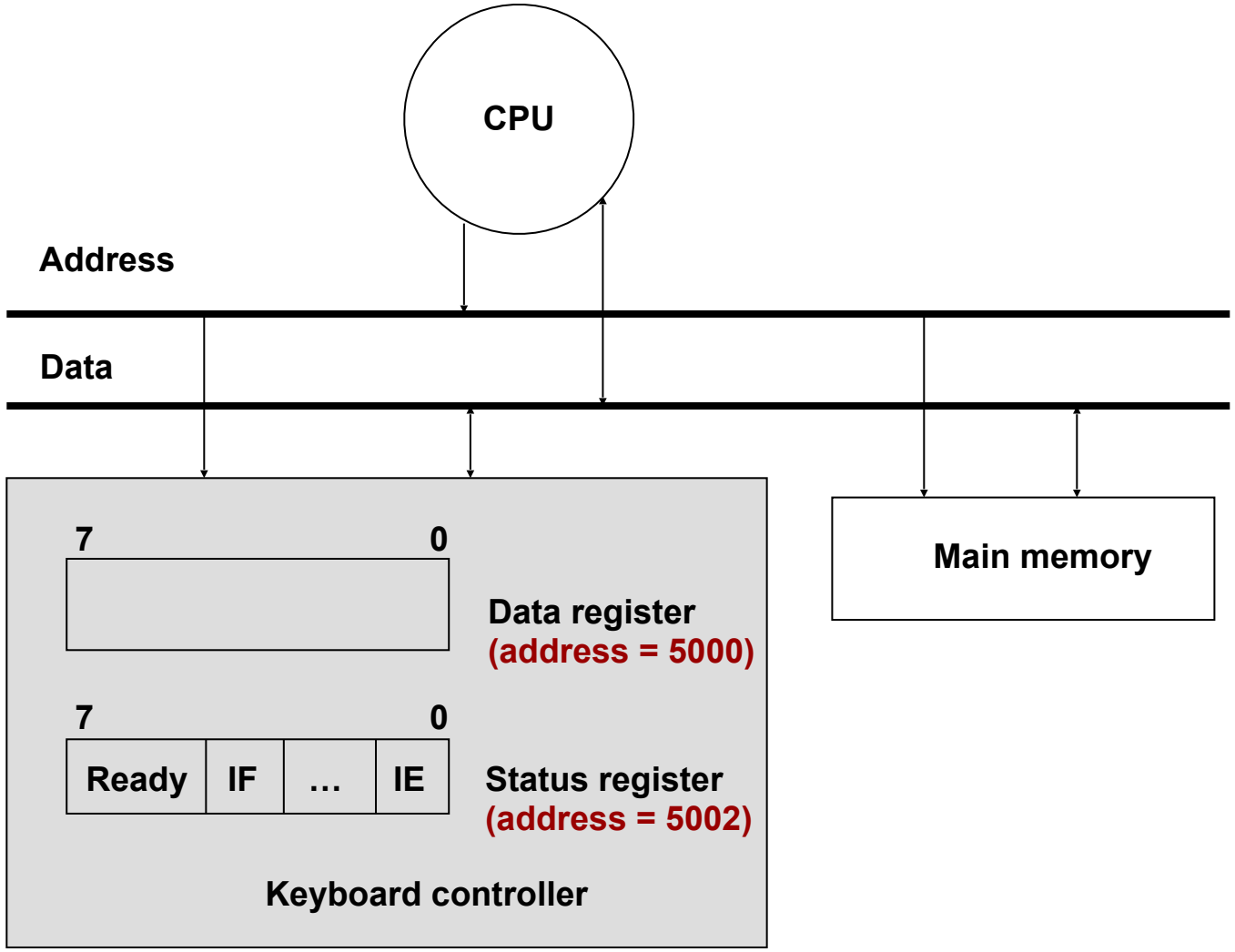
Set IE

ST #1,mem[5002]



Programmed I/O (PIO)

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X:  LD      R1, statusreg     ; Get the status register
    BRZP    X                 ; if high bit is 0, branch back one
    LD      R2, datareg       ; Load the data into R2
    ST      #0, statusreg     ; Clear the status register
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LD usually clears the ready bit as a side effect of reading the data register

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- Busy waiting – wastes processor resources

Interrupt-driven I/O

- Slow speed devices (Keyboard, mouse, etc.)
- CPU executes program for moving data
- Can be interrupt driven

```
ST      #1, statusreg ; Set the IE bit
```

Upon interrupt, handler code is executed:

```
LD      R2, datareg     ; Load the data into R2
```

High speed devices

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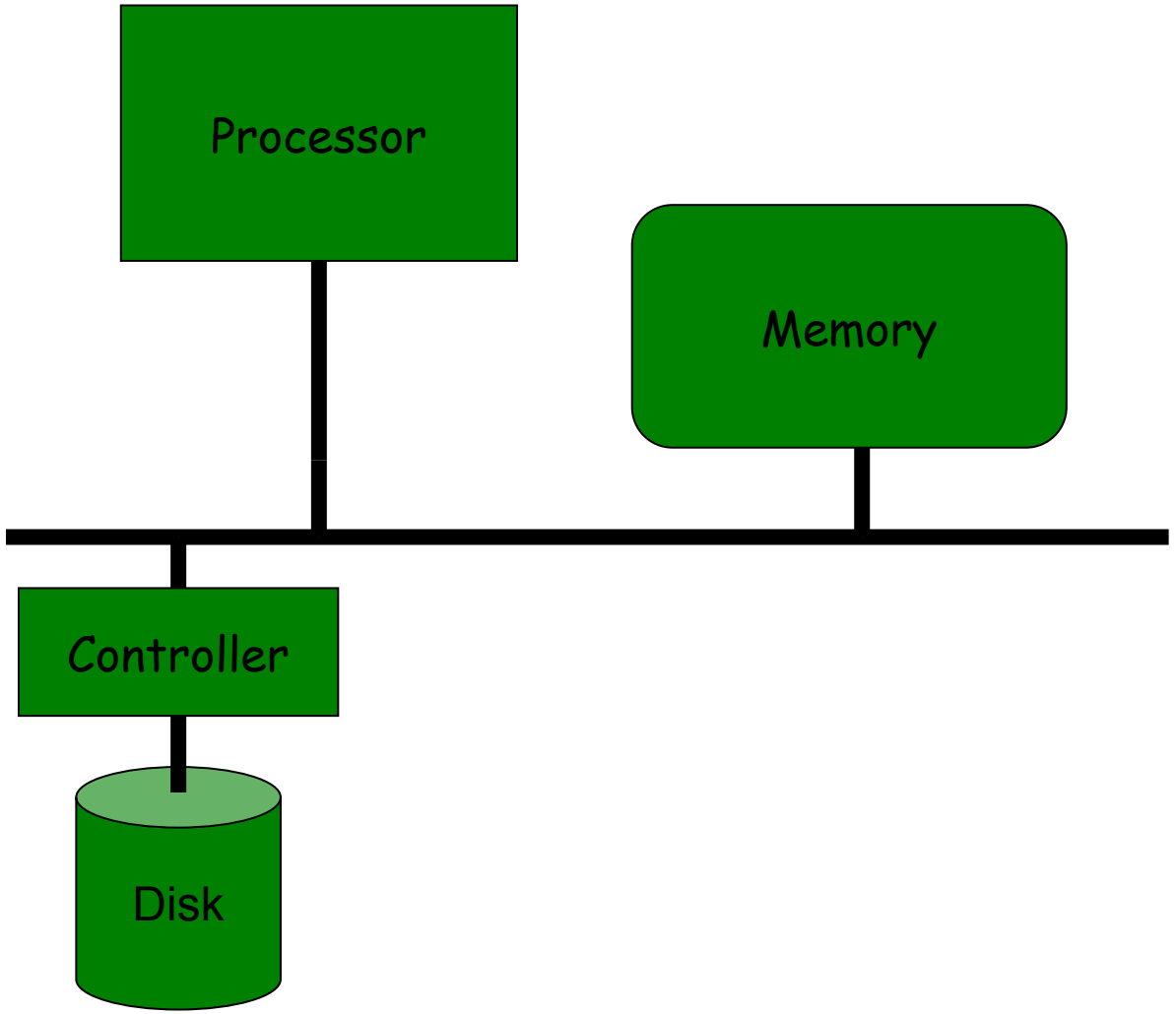
- The CPU to controller interface?
  - Convey commands (read/write, IE, etc.)
  - Check status (error, etc.)

Direct Memory Access - DMA



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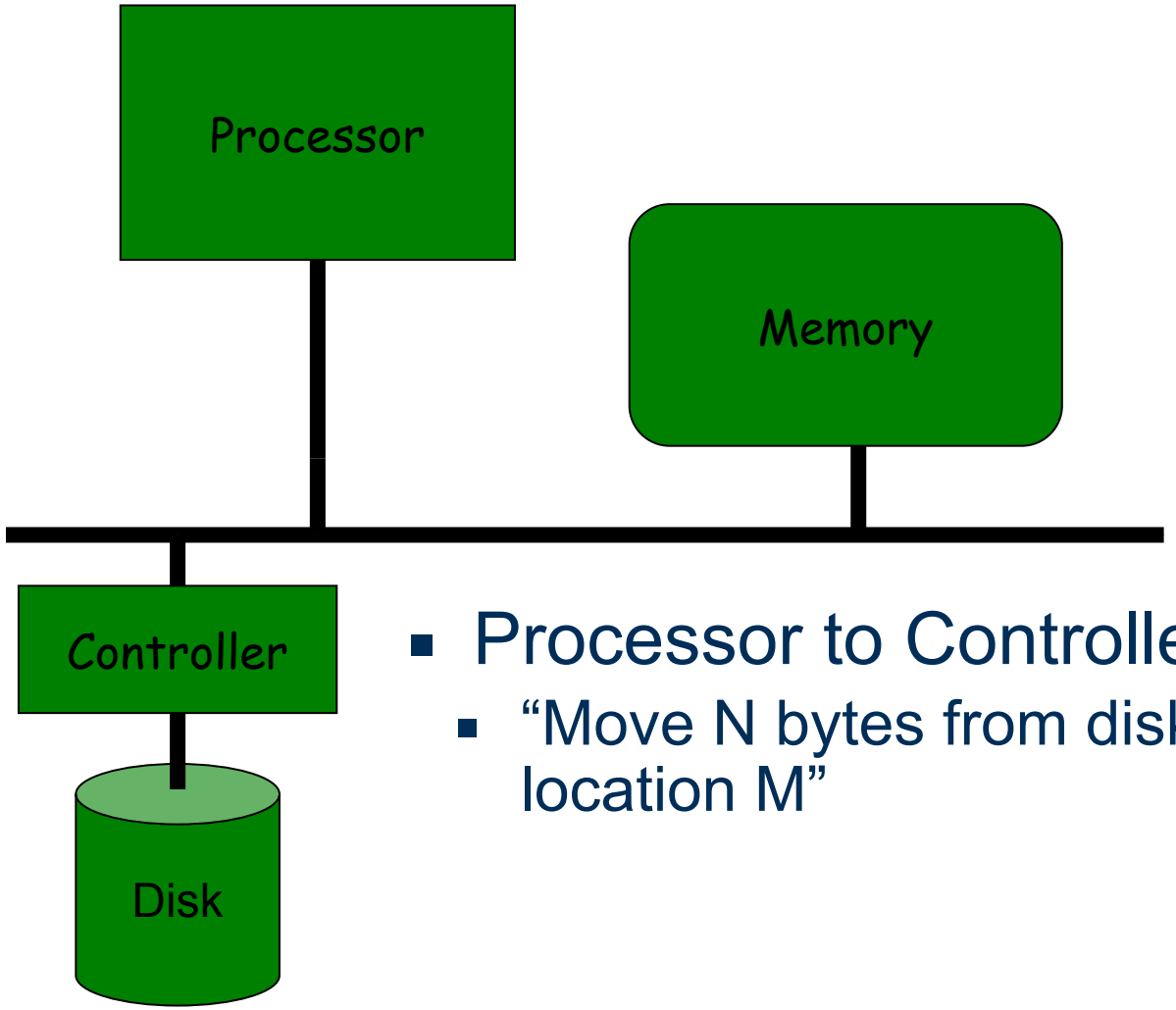
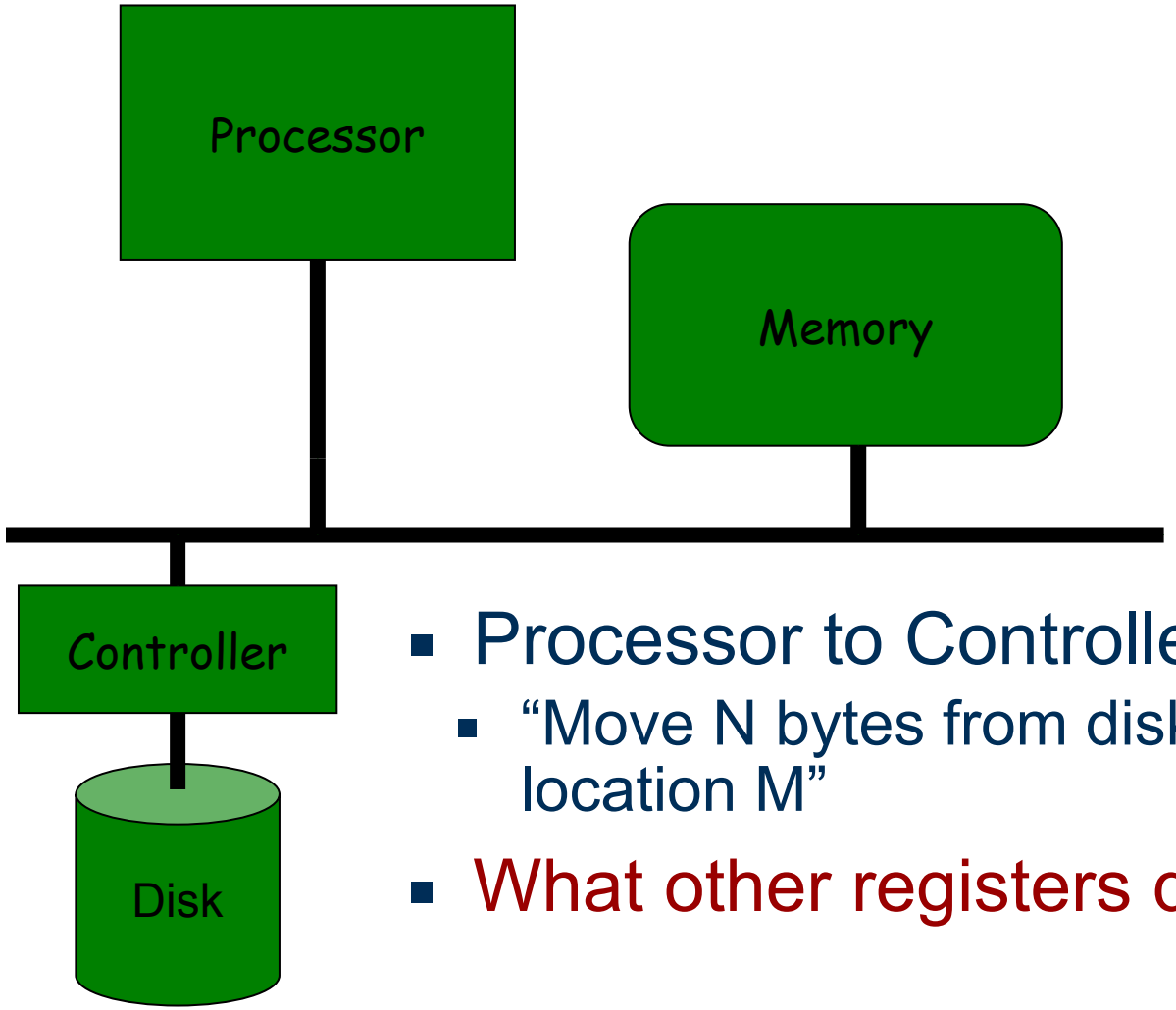


- Processor to Controller:
  - "Move N bytes from disk location X to memory location M"

Direct Memory Access - DMA



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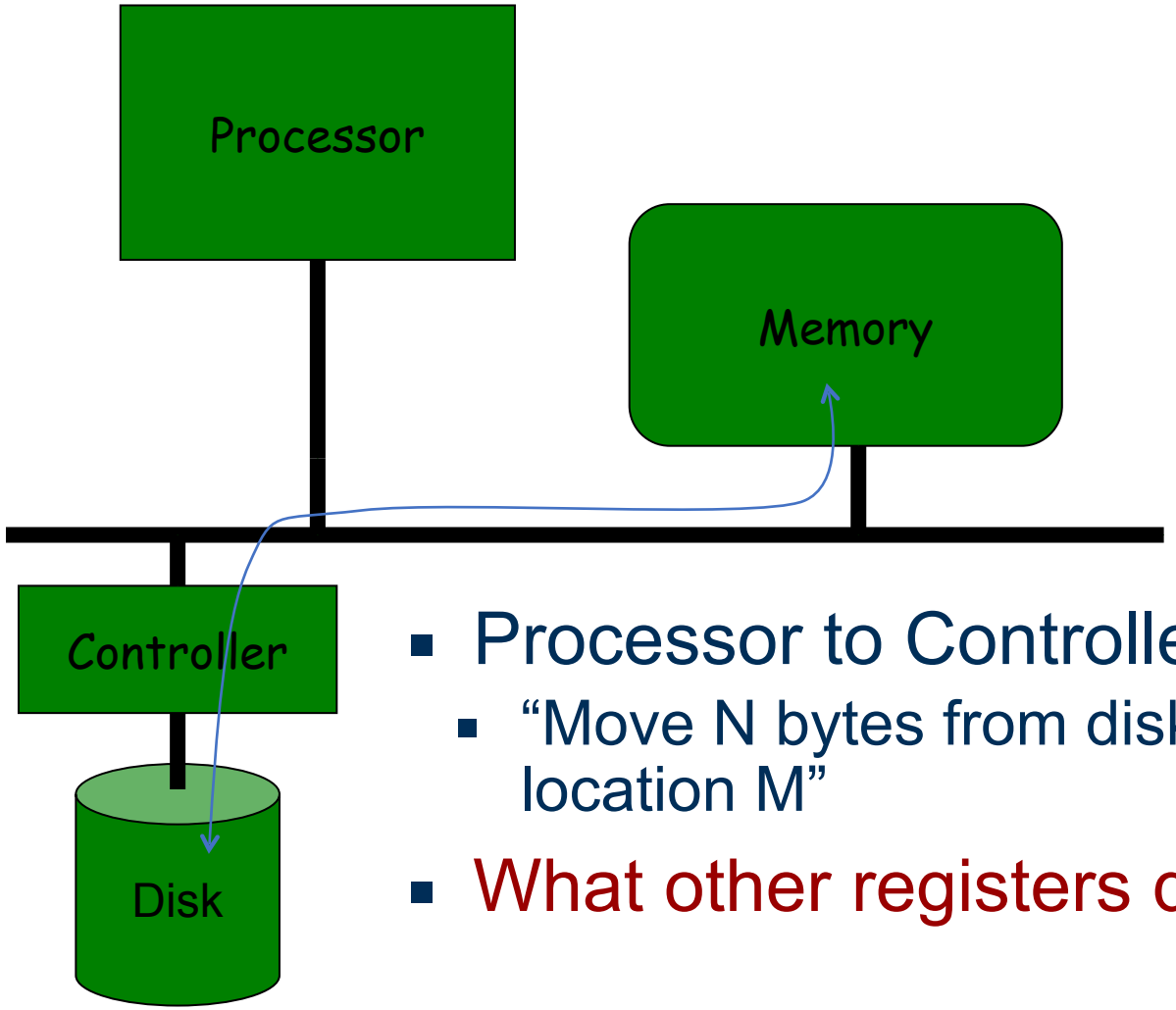
- What other registers do we need?

Direct Memory Access - DMA



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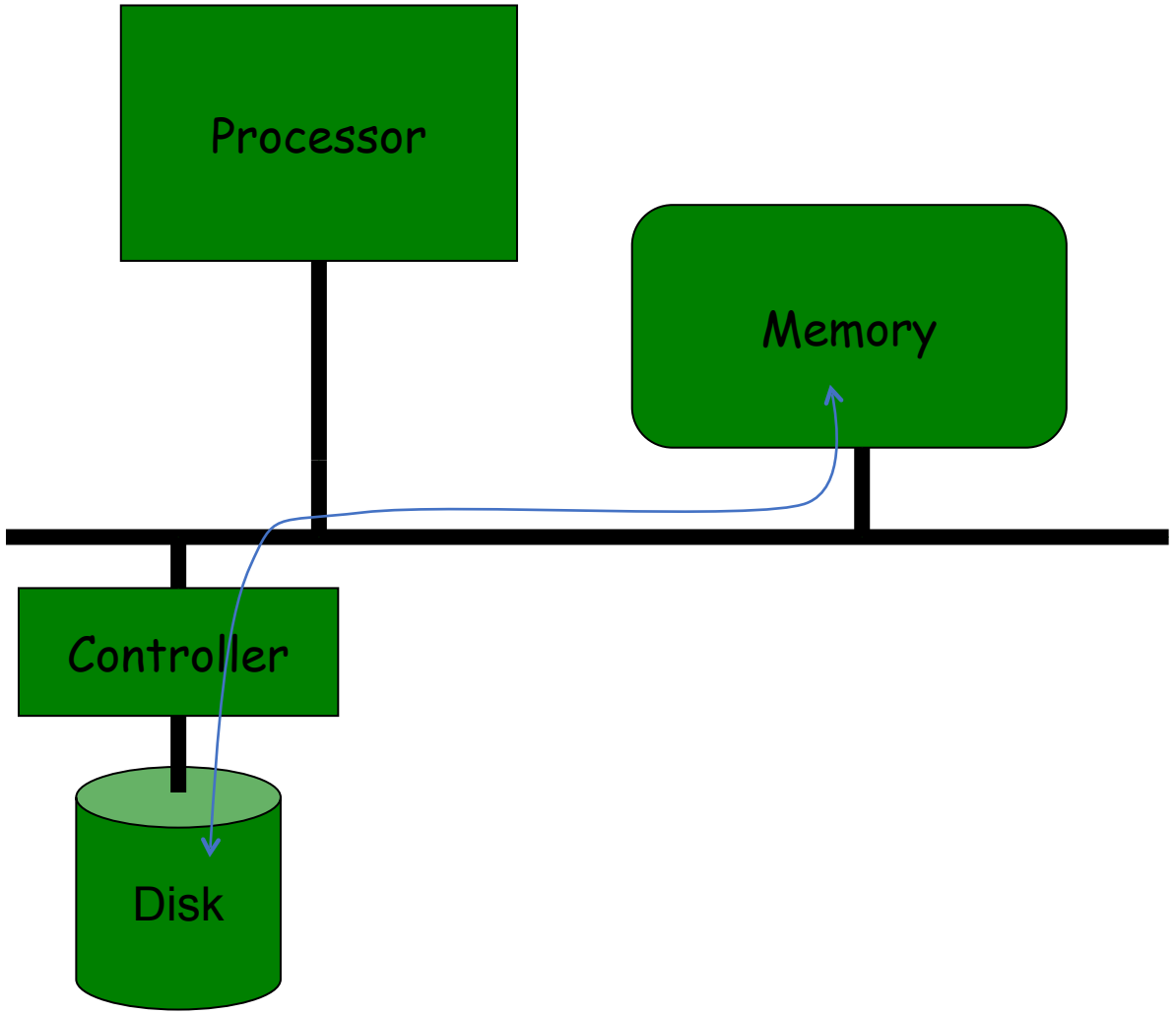
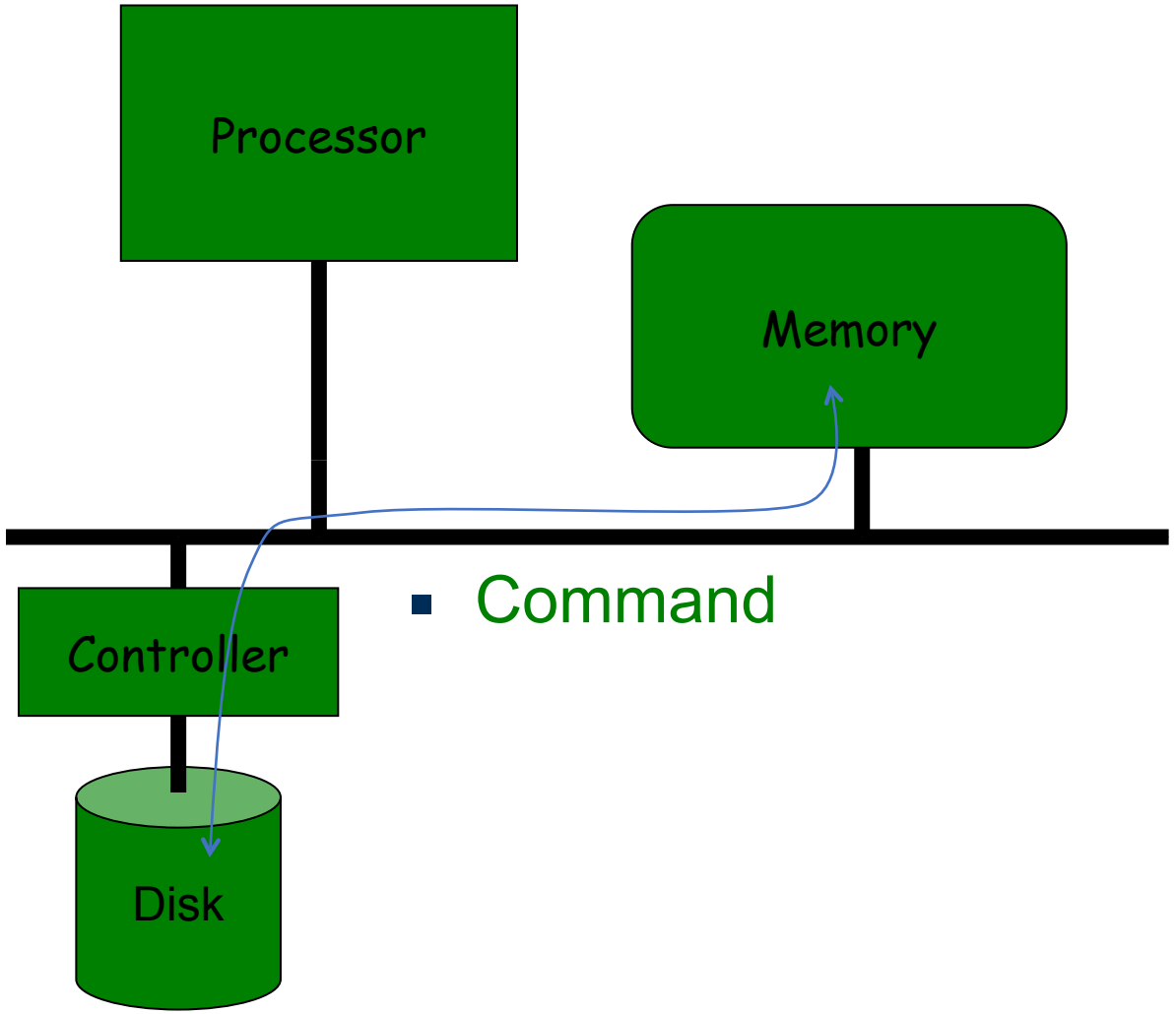
DMA registers

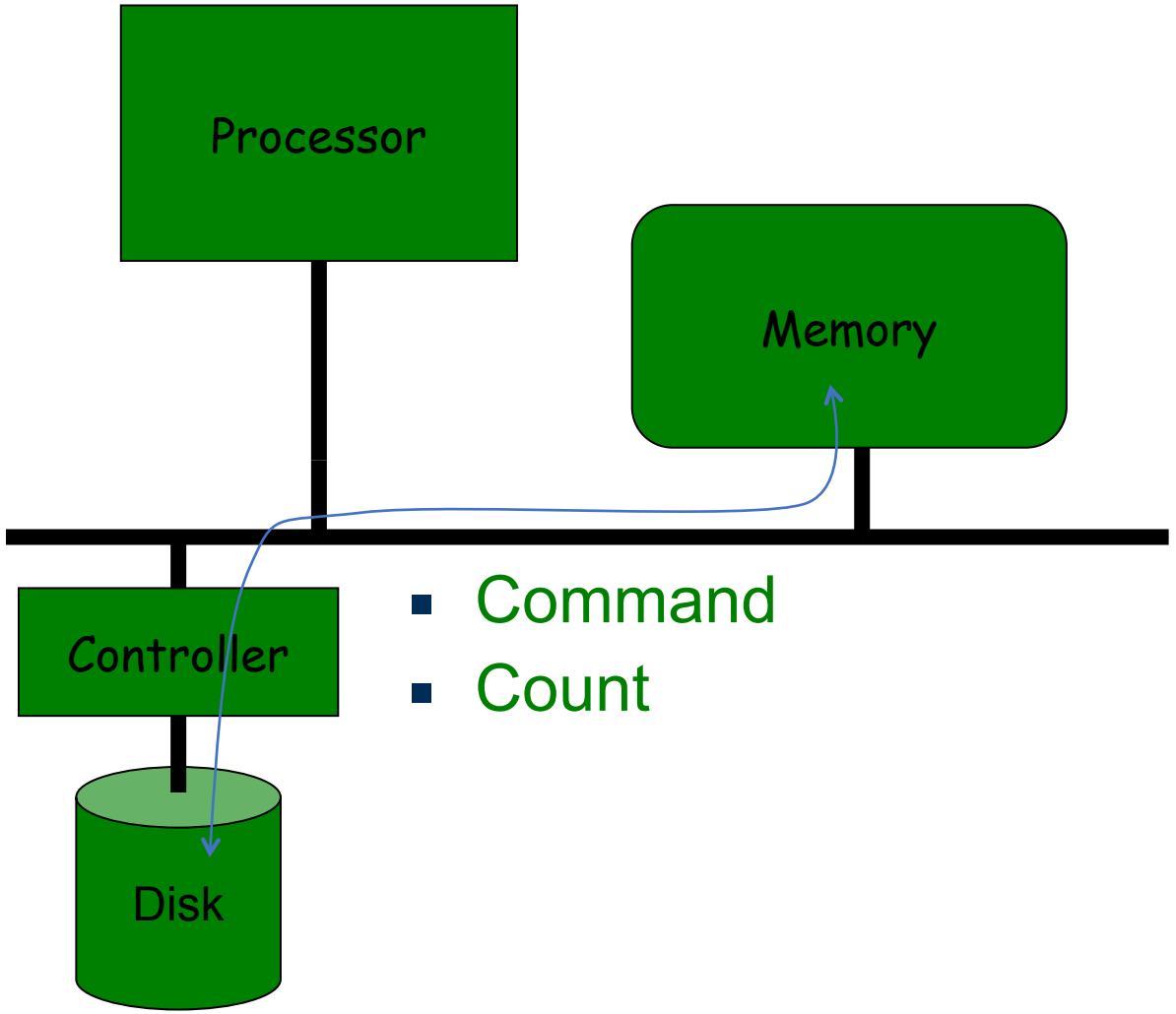


DMA registers



- Command

DMA registers



- Command
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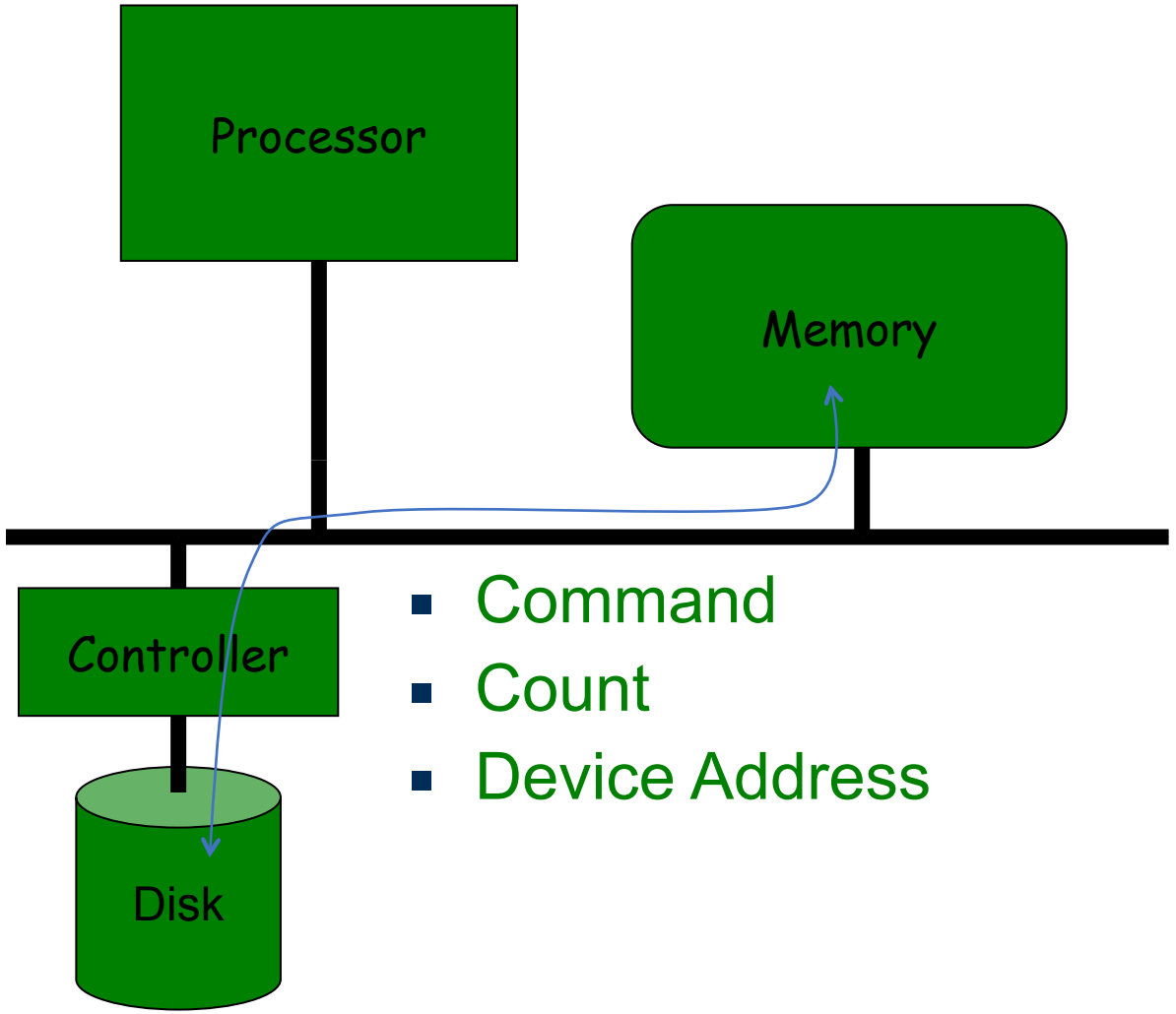
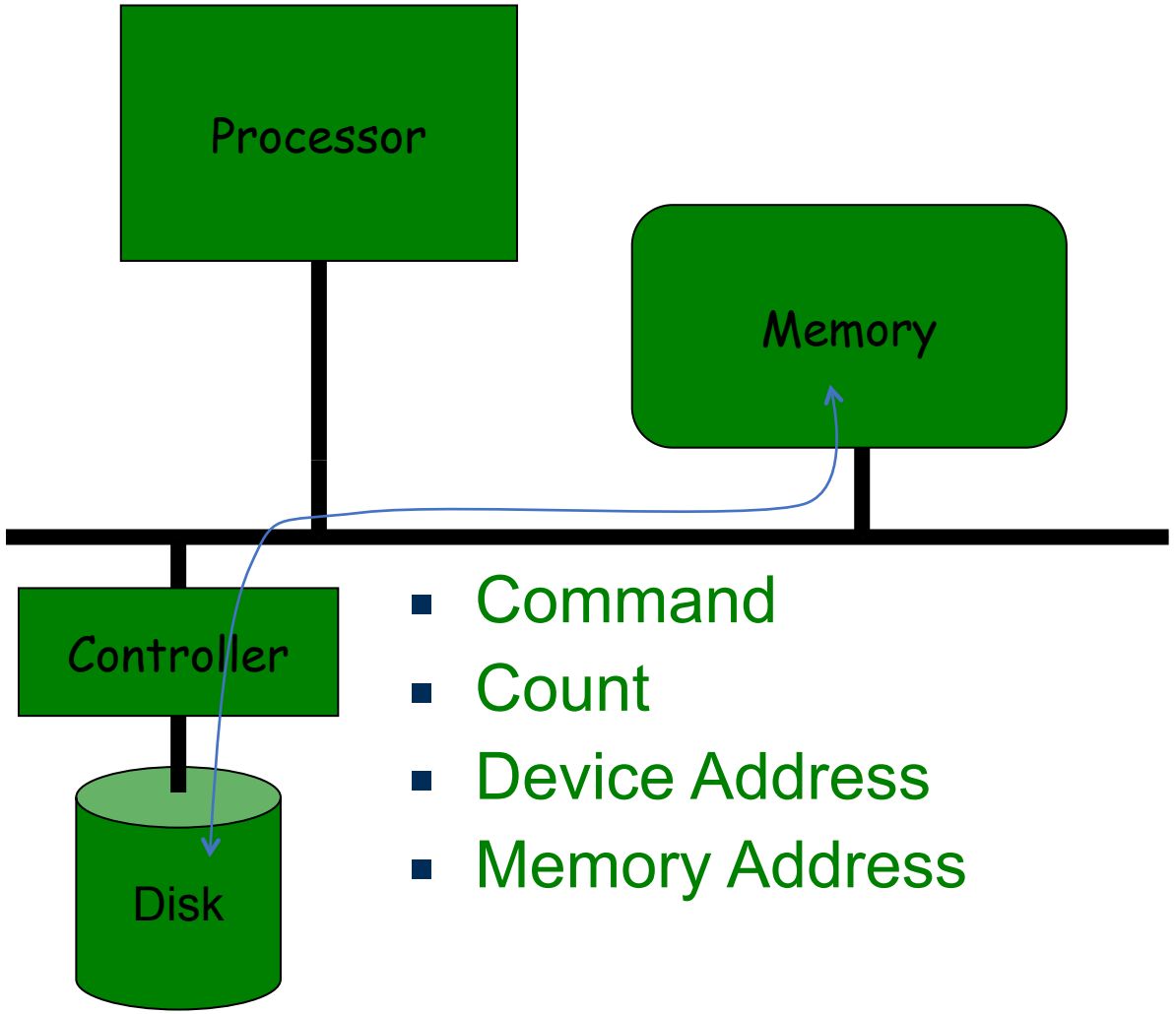
DMA registers



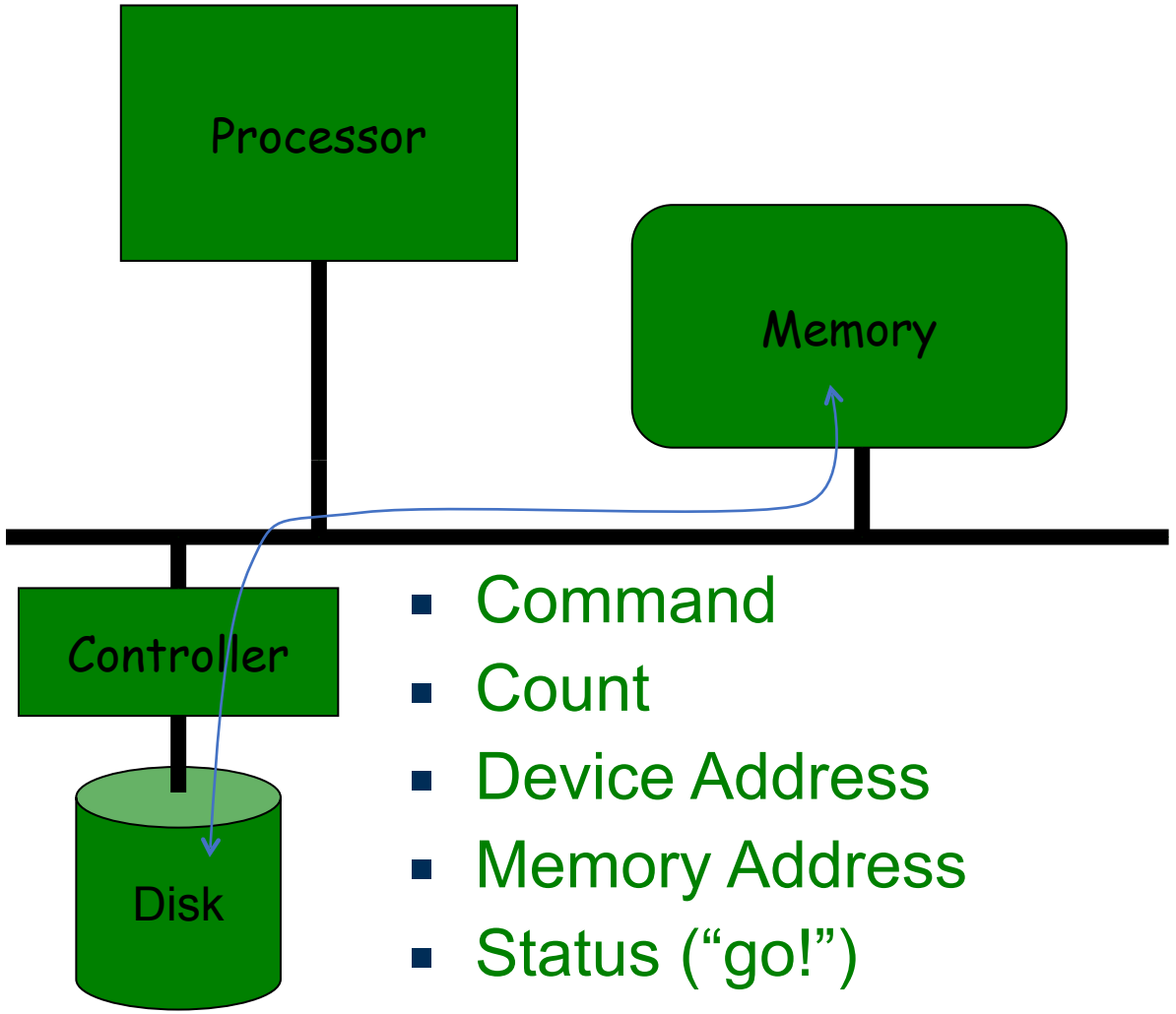
- Command
- Count
- Device Address

DMA registers



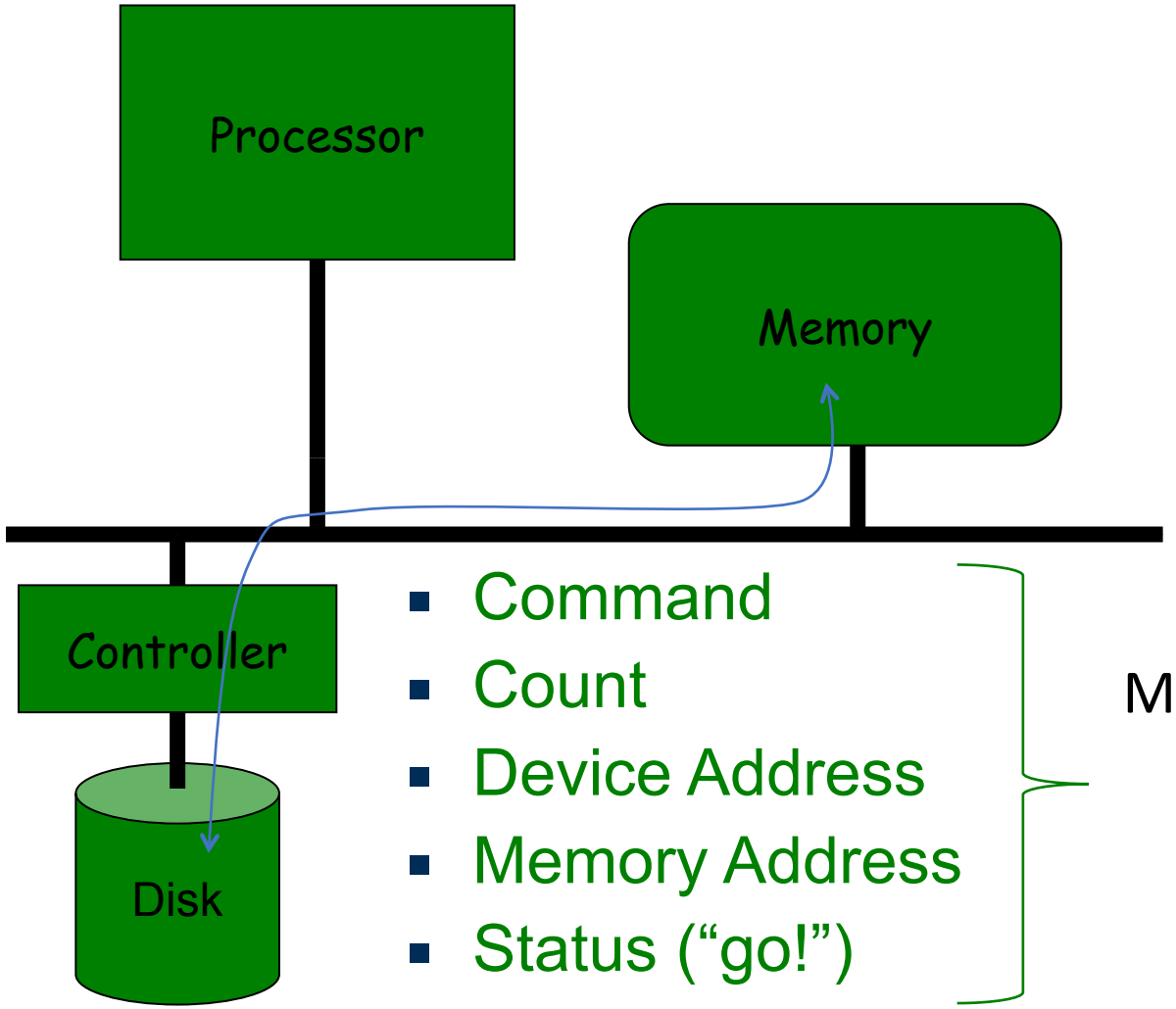
- Command
- Count
- Device Address
- Memory Address

DMA registers



- Command
- Count
- Device Address
- Memory Address
- Status (“go!”)

DMA registers



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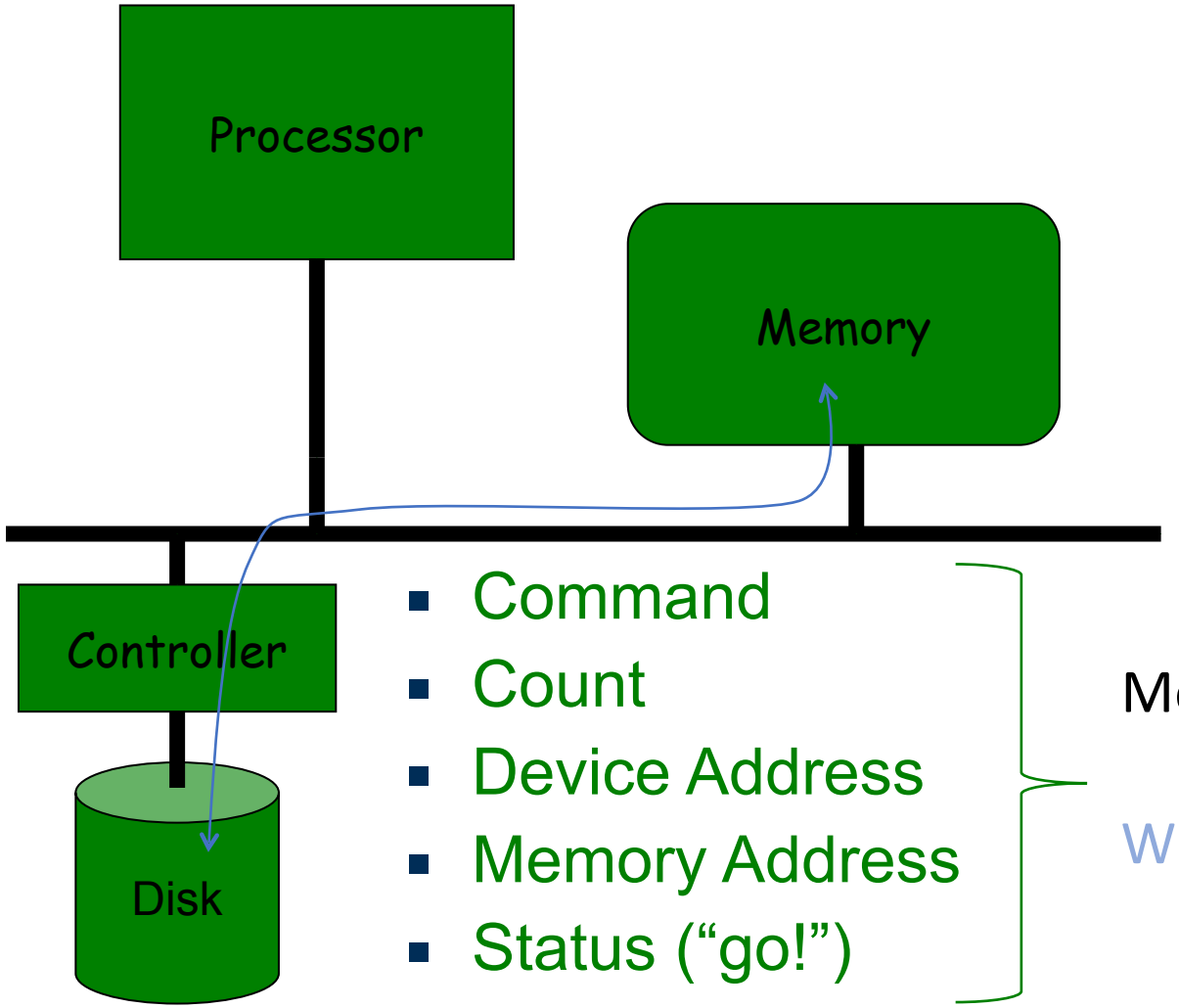
Memory mapped registers

DMA registers



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- Memory Address
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Memory mapped registers

Where have you seen this before?

Program for conveying I/O commands

Program for conveying I/O commands

```
Store  N, count
Store  #block_num, device_addr
Store  #mem_buf_addr, mem_addr
Store  #write_command, command
Store  #1, status  ;  the signal to execute the command
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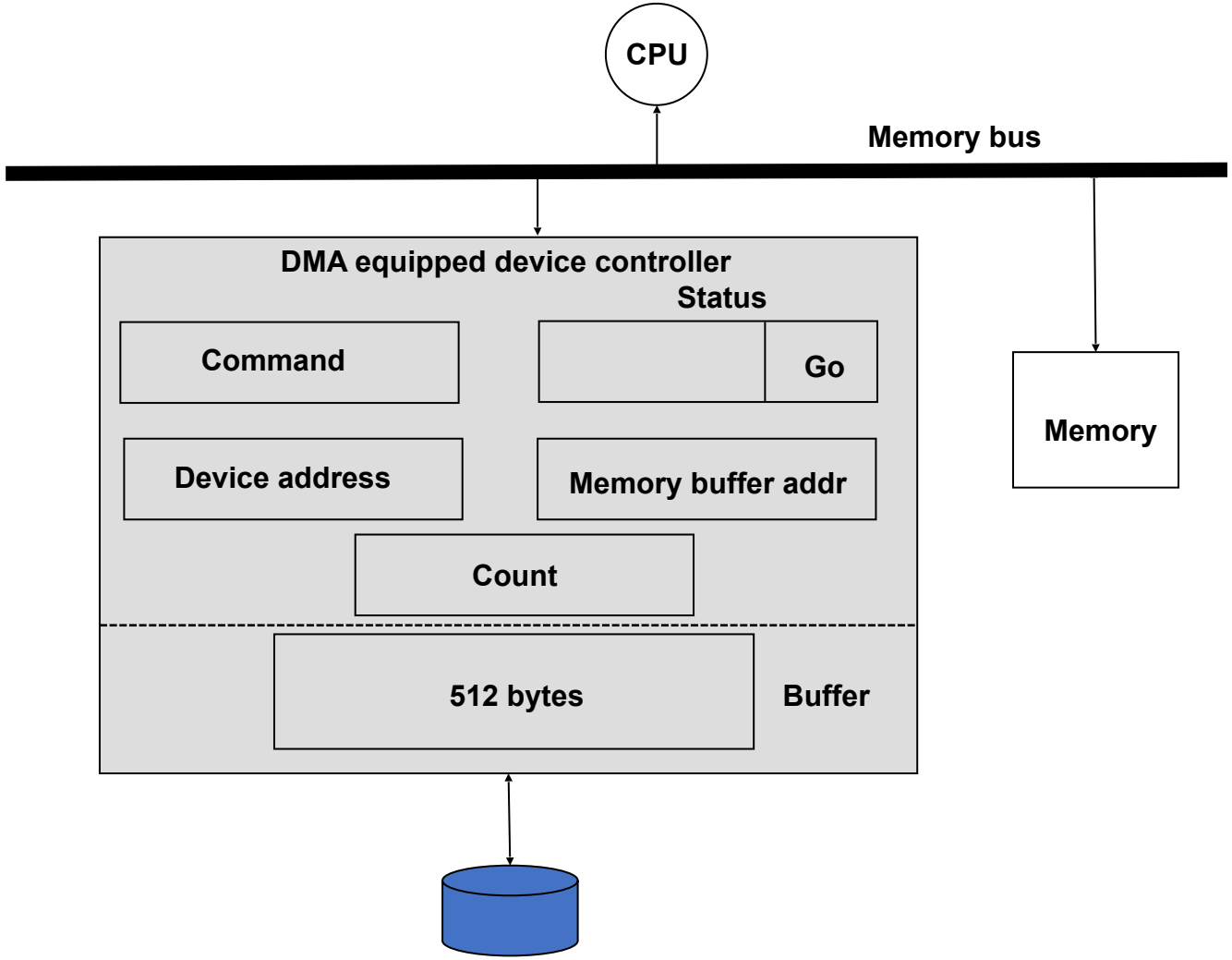
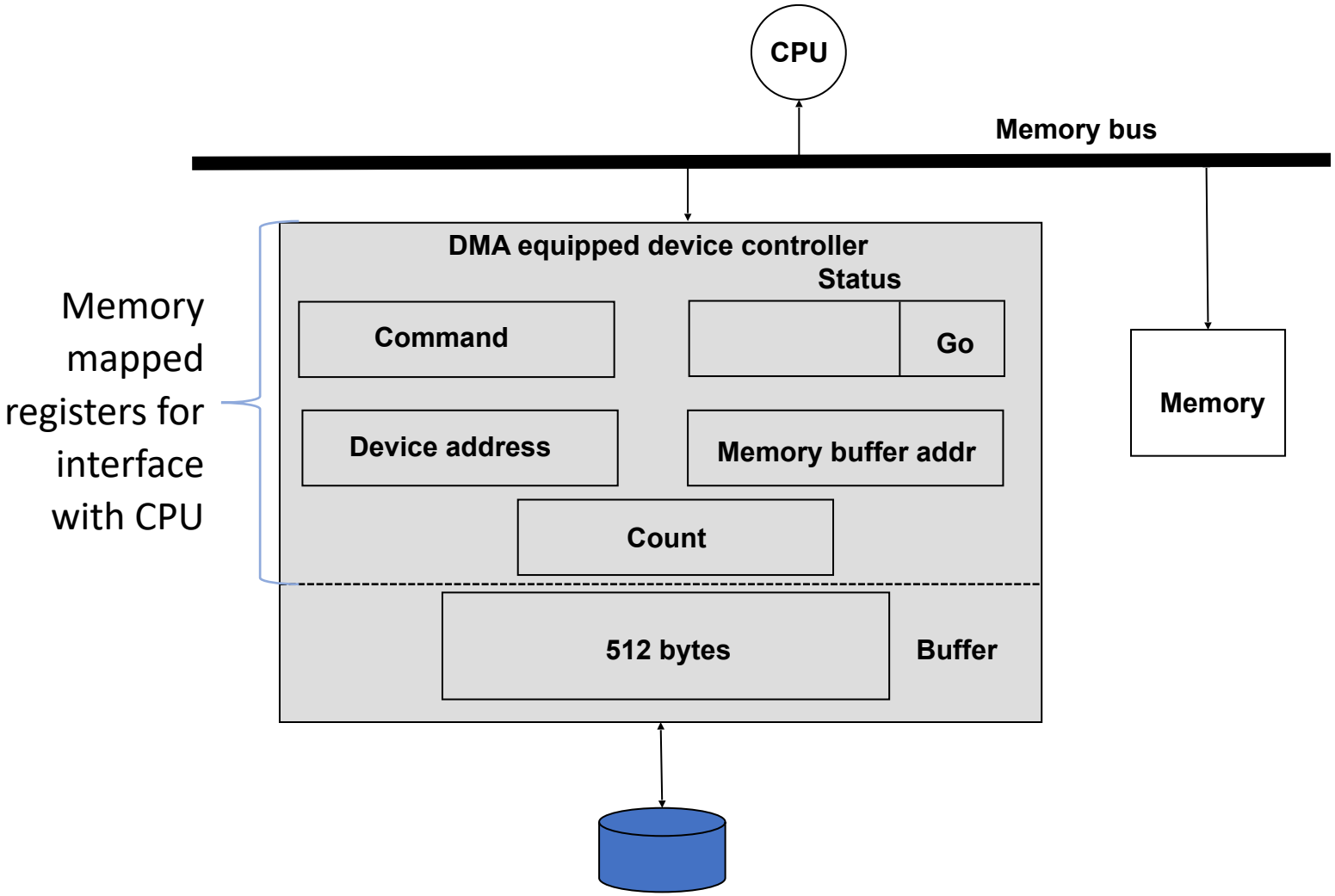
  - The device controller takes over to do the actual data movement
- Modern CPU chips already contain device controllers for PCI-E devices which share the on-chip memory controllers with the CPU cores

DMA


CPU
Memory bus
DMA equipped device controller
Status
Command
Go
Memory
Device address
Memory buffer addr
Count
512 bytes
Buffer

DMA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Memory bus
DMA equipped device controller
Status
Command
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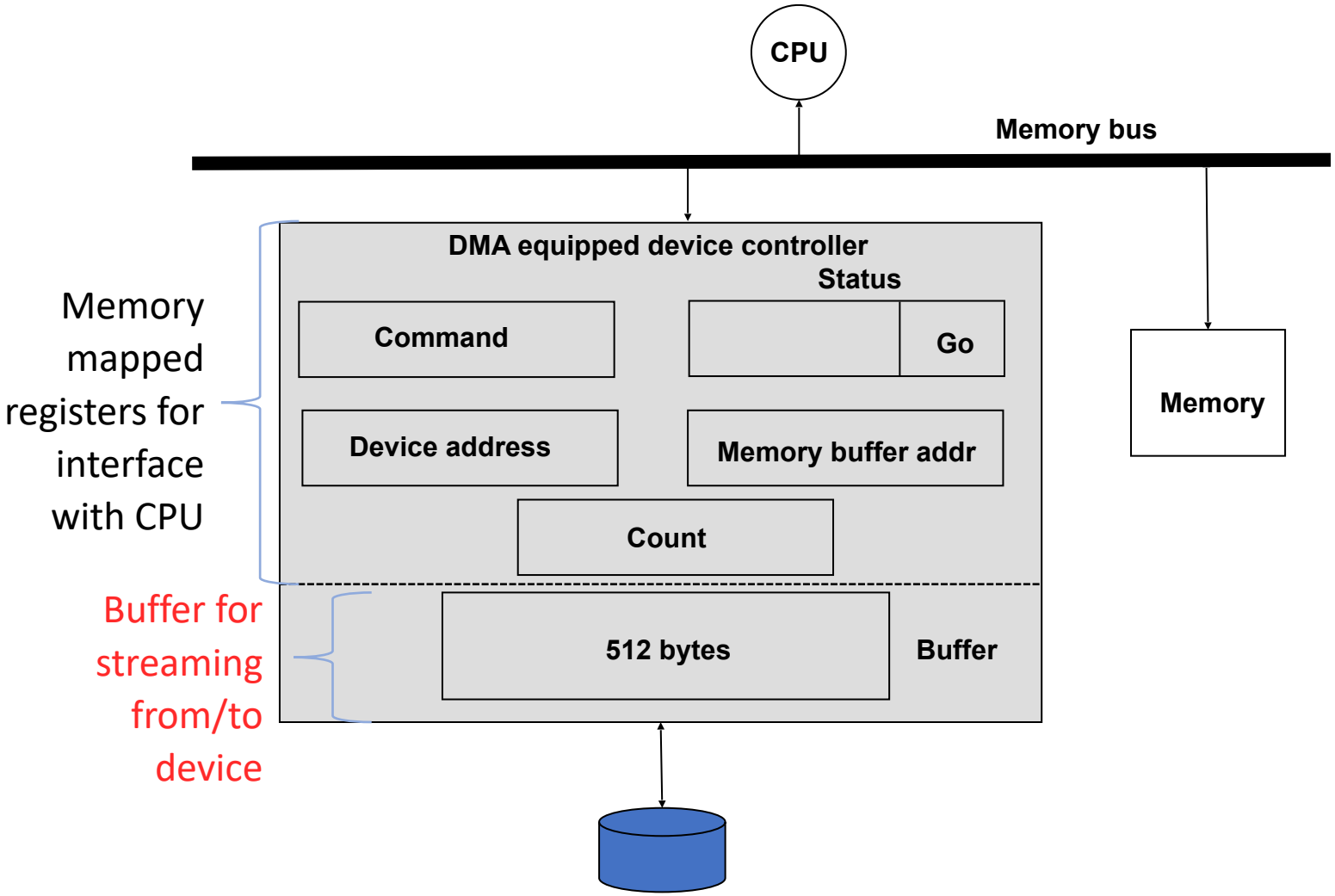
Memory buffer addr
Count
512 bytes
Buffer
Memory
Memory mapped registers for interface with CPU

DMA


CPU
Memory bus
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Status
Command
Go
Device address
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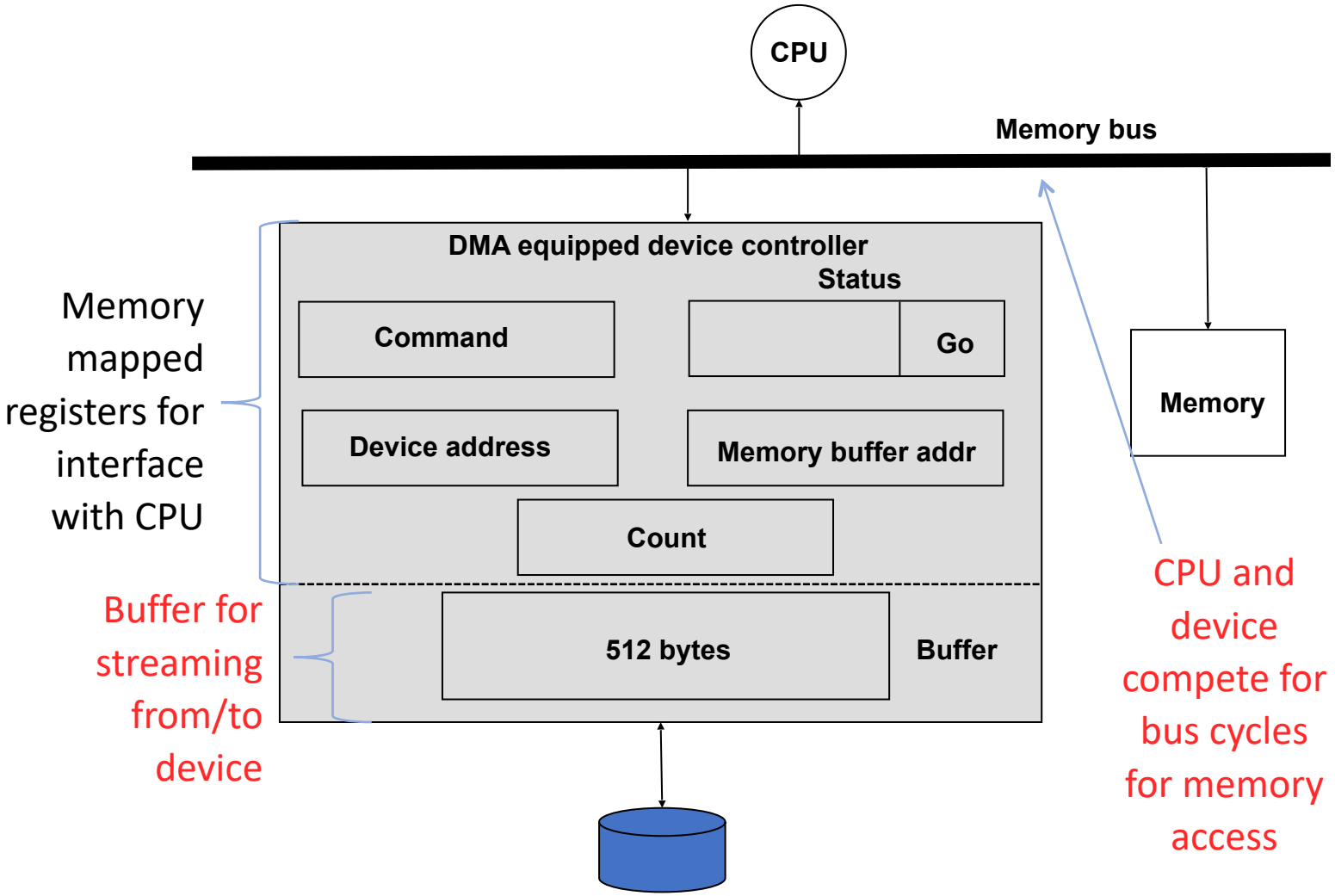
Count
512 bytes
Buffer
Memory
Memory mapped registers for interface with CPU
Buffer for streaming from/to device

DMA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Count
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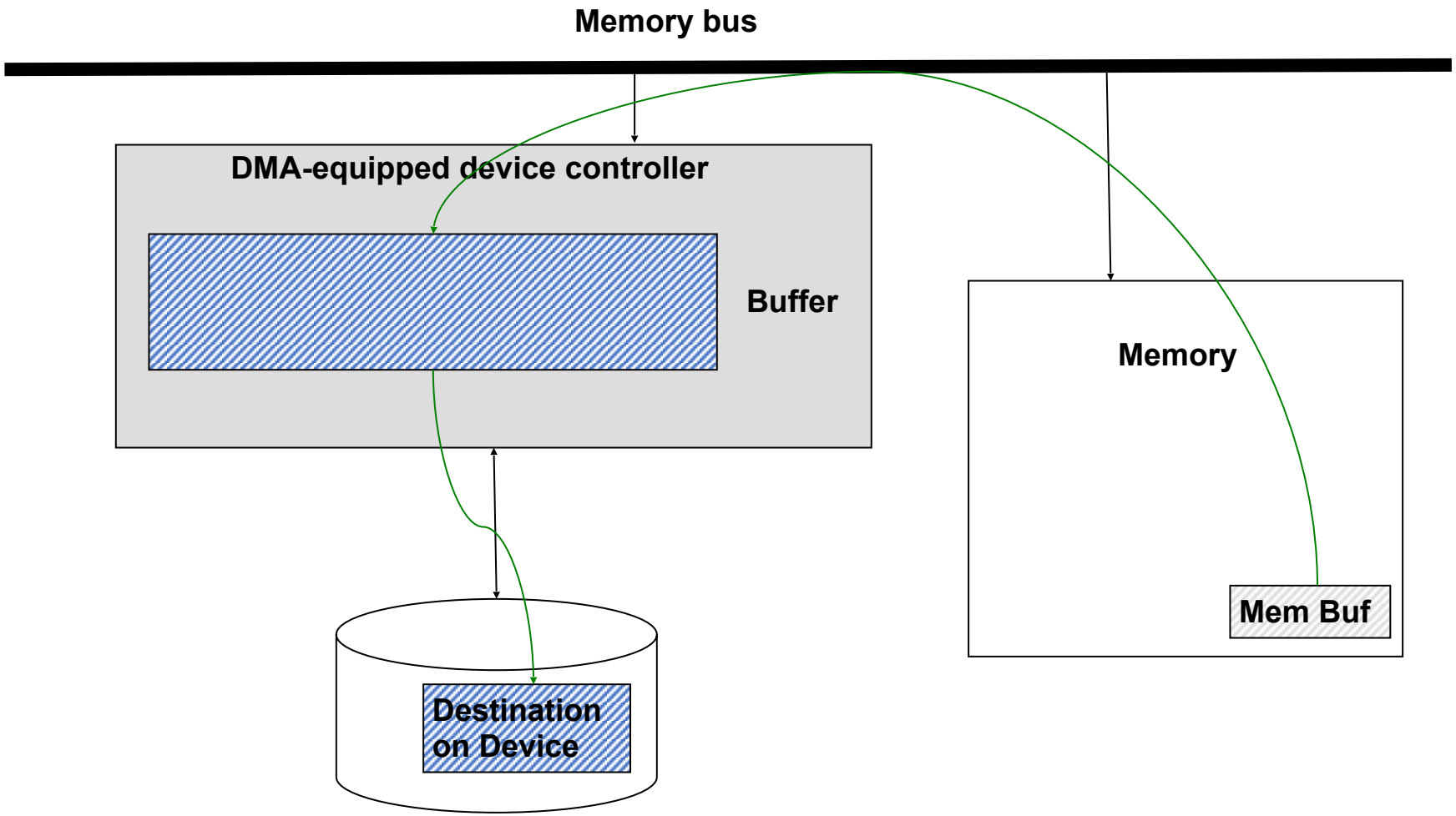
Memory
Memory mapped registers for interface with CPU
Buffer for streaming from/to device
CPU and device compete for bus cycles for memory access

DMA Transfer example



Data transfer speeds

Device	Input/ output	Human in the loop	Data rate (circa 2008)	Data rate (circa 2020)	PIO	DMA
Keyboard	Input	Yes	5-10 bytes/sec	5-10 bytes/sec	X	
Mouse	Input	Yes	80-200 bytes/sec	80-200 bytes/sec	X	
Graphics display	Output	No	200-350 MB/sec	200-350 MB/sec		X
Disk (hard drive)	I/O	No	100-200 MB/sec	500 MB/sec (each)		X
Network (LAN)	I/O	No	1 Gbit/sec	1-400 Gbit/sec		X
Modem	I/O	No	1-8 Mbit/sec	1-8 Mbit/sec		X
Inkjet printer	Output	No	20-40 KB/sec	20-40 KB/sec	X	X
Laser printer	Output	No	200-400 KB/sec	200-400 KB/sec		X
Voice (microphone/ speaker)	I/O	Yes	10 bytes/sec	10 bytes/sec	X	
Solid State (SSD)	I/O	No	10-50 MB/sec	0.1-7GB/sec		X
CD, DVD, Blu-Ray	I/O	No	10-20 MB/sec	10-20 MB/sec		X

DMA is used instead of PIO for I/O because

33% A. PIO can lose data if the CPU doesn't poll or respond to the interrupt quickly enough

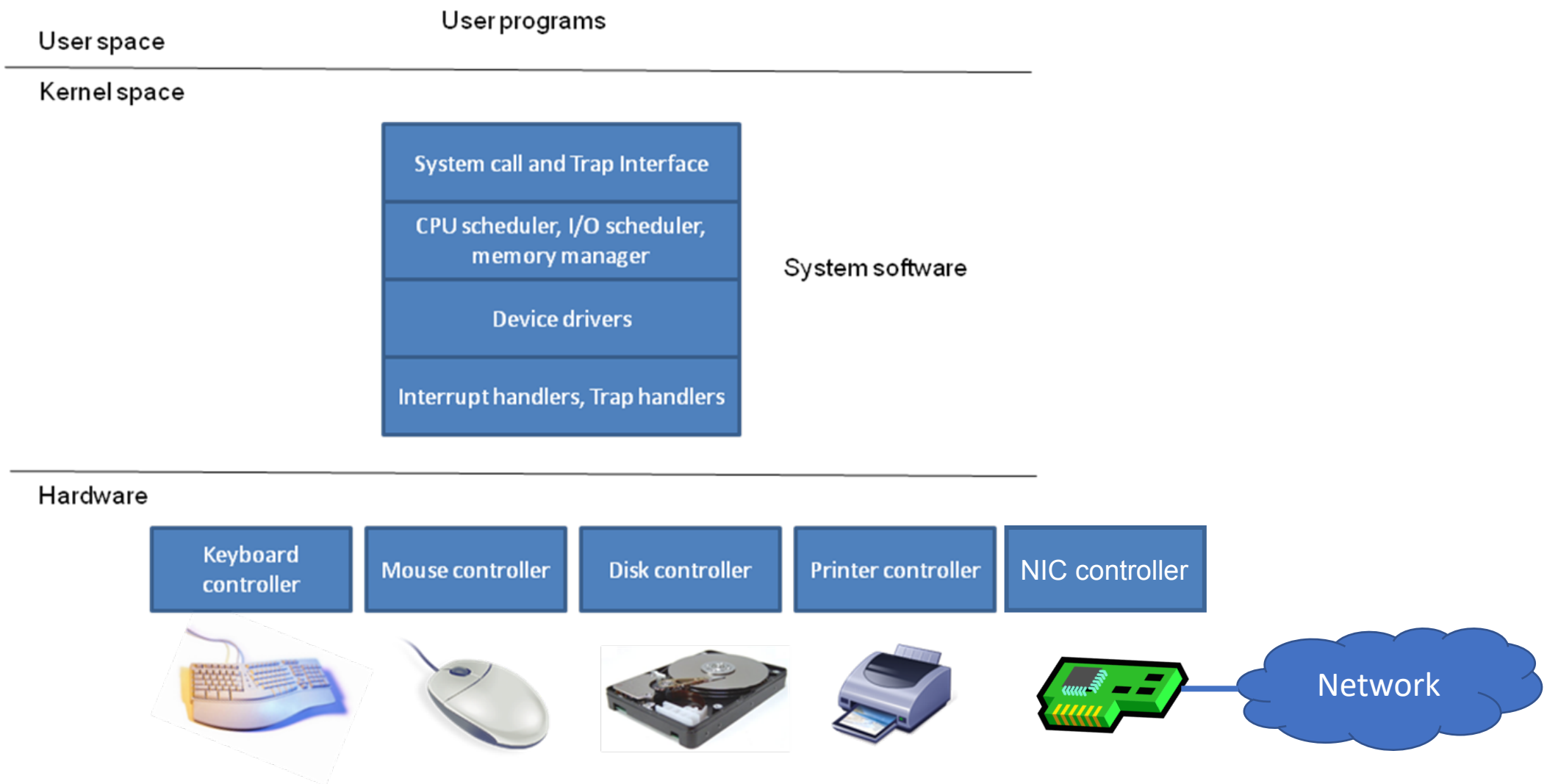
10% B. Servicing an interrupt in the CPU is expensive especially if it has to be done for every word of I/O

10% C. A DMA controller can transfer data into memory in fewer cycles than a programmed loop in the CPU

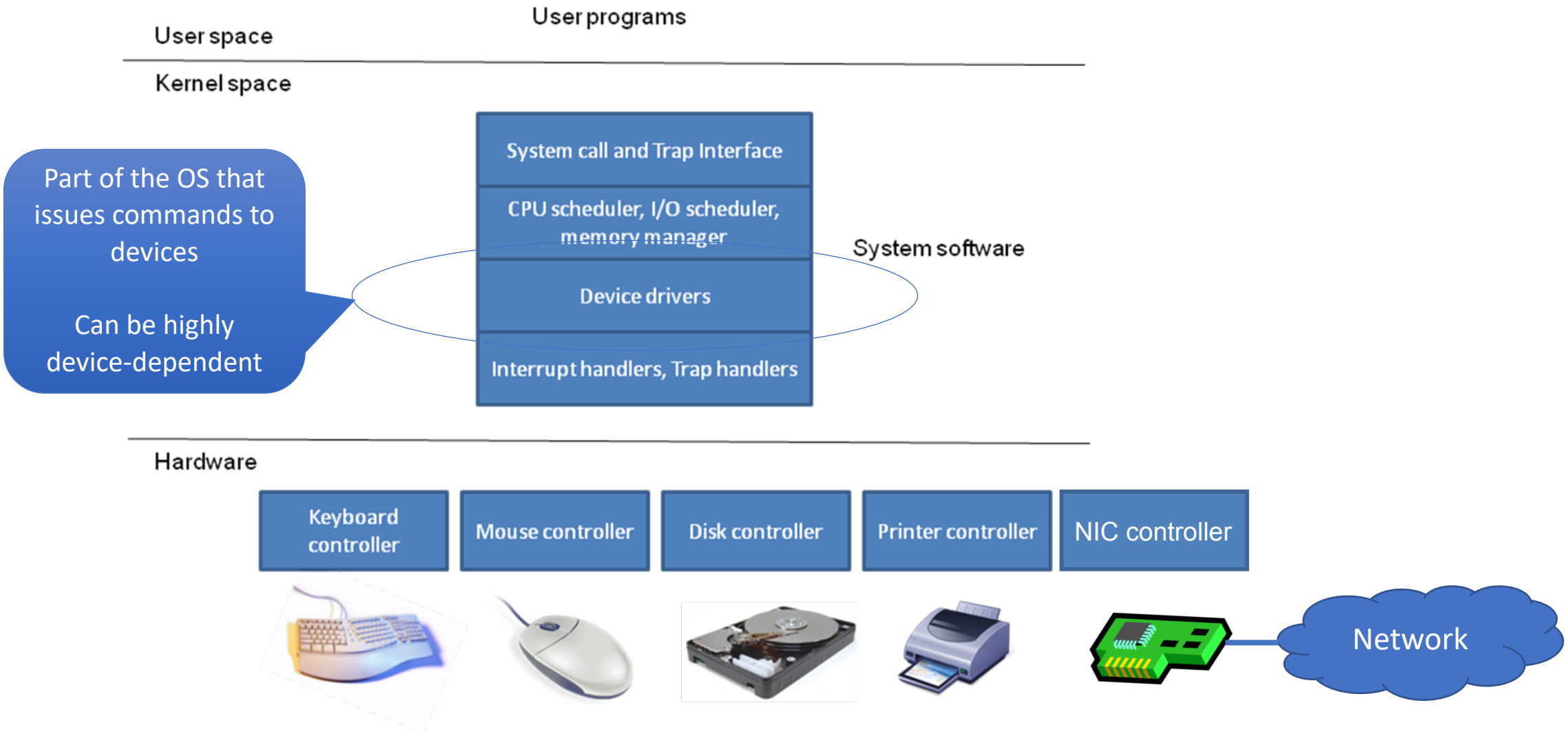
4% D. All of the above

42%

Device drivers and OS



Device drivers and OS



Device drivers and OS