Slow Vars

Aingura IIoT

Elaborado	Revisado	Aprobado
Imanol Ramajo *Software Engineer* Albert Diaz *Head Mechatronics Dpt.*	Jon Echevarria *Head Software Dpt.*	- -

Control de modificaciones		
Rev	**Descripción**	**Fecha**
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Índice

1. xI_PCF xV_PCF

1.1 Descripción

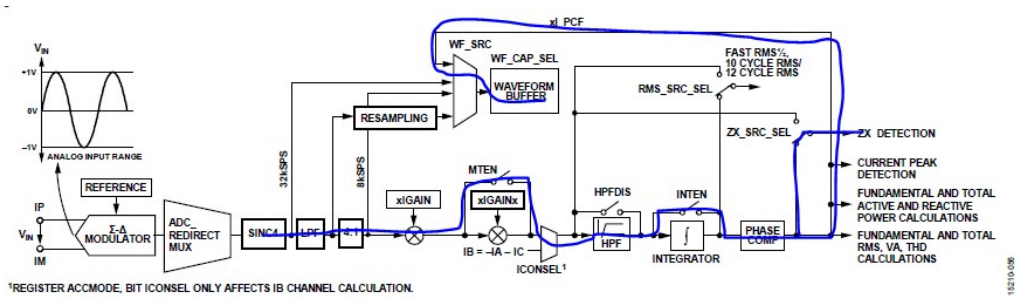

Figura 1: Datapath I

1.2 Frecuencia - Periodo

8kSPS

1.3 Parámetros

- `xIGAIN` = "default" = 1
- `MTEN` = "default" = 0 (Ganancia en función de rango. No se usa)
- `HPF` = 1 (es un valor por defecto en el AICT)
- `INTEN` = "default" = 0
- `ZX_SR_SEL` = valor default indica después de integrator

1.4 Conversión

1.5 Comentarios

Estos valores son la base sobre la que se calculan todos los demás valores del ADE9000.

REVISAR. No estamos seguros de que el paso de que los valores por defecto sean los que más nos interesan para nuestros algoritmos/cálculos.

2. xIRMS xVRMS

2.1 Descripción

The ADE9000 offers total and fundamental current and voltage rms measurements on all phase channels. The datapath is shown in:

The total rms calculations, one for each channel (AIRMS, BIRMS, CIRMS, NIRMS, AVRMS, BVRMS, and CVRMS), are updated every 8 kSPS. The fundamental rms calculations available in the AIFRMS, BIFRMS, CIFRMS, AVFRMS, BVFRMS, and CVFRMS registers are also updated every 8 kSPS. The fundamental rms is not available for the neutral channel.

The xRMS and xFRMS value at full scale is 52,702,092 decimals.

2.2 Frecuencia - Periodo

8kSPS

2.3 Parámetros

xRMSOS = 0 (este es un offset que actualmente no se utiliza)

2.4 Conversión

Tiene las mismas unidades que las intensidades o los voltages respectivamente. Ver conversión en xI_PCF xV_PCF.

2.5 Comentarios

Desconocemos que hace exactamente el LPF2 (que es la base del cálculo del RMS).

Es un valor que se usa o se tiene en cuenta a la hora de calcular algunos otros registros del ADE9000.

3. xWATT xVAr

3.1 Descripción

The ADE9000 offers total and fundamental active power measurements on all channels. The active power calculations, one for each channel (AWATT, BWATT, and CWATT), are updated every 8 kSPS. The fundamental active power is also updated every 8 kSPS and is available in the AFWATT, BFWATT, and CFWATT registers. With full-scale inputs, the xWATT and xFWATT value is 20,694,066 decimals. Enable the LPF2 (DISAPLPF $= 0$) for normal operation. Disable LFP2 by setting DISAPLPF in the CONFIG0 register to obtain instantaneous total active power. DISAPLPF is zero at reset.

The total and fundamental measurements can be calibrated for gain and offset. The following equations indicate how the gain and offset calibration registers modify the results in the corresponding power registers:

Fórmula

$$\mathtt{xWATT}_0 = \mathrm{LPF}(\mathtt{xI\_PCF} * \mathtt{xV\_PCF})$$

$$\mathtt{xVAR}_0 = \mathrm{LPF}(\mathtt{xI\_PCF}\angle\frac{\pi}{2} * \mathtt{xV\_PCF})$$

xPGAIN is a common gain to total and fundamental components of active, reactive, and apparent powers.

If the DISAPLPF bit in the CONFIG0 is equal to 1, xWATT reflects the instantaneous active power; and if it is equal to 0, xWATT reflects the low-pass filtered active power, in Technical reference manual Figure 16.

The low-pass filter, LPF2, extracts the total active power, attenuating harmonics of a 50 Hz or 60 Hz fundamental by 64 dB so that, at full scale, the variation in the low-pass filtered active power is very small, $\pm 0.062\,\%$.

The resulting xWATT signal has an update rate of 8 ksps and a bandwidth of 3.2 kHz.

Total reactive power includes reactive power on the fundamental and on the harmonics. The current channel, xI_PCF, is shifted by 90 at the fundamental and at all harmonics. This signal is then multiplied by the voltage waveform, xV_PCF. The result is then low-pass filtered, unless the DISRPLPF bit in the CONFIG0 register 1.

It is possible to disable the reactive power calculation by setting the VARDIS bit in the VAR_DIS register. This bit must be set before writing the RUN bit for proper operation.

3.2 Frecuencia - Periodo

8kSPS

3.3 Parámetros

Implícitamente aquellos que modifican `xI_PCF` y `xV_PCF`.

- LPF2 = Activo
- `xPGAIN` = 0 (es común para todas las potencias de una misma fase)
- `xWATTOS` / `xVAROS`
- `DISRPLPF` to disable the low-pass filter.
- `VARDIS` bit in `VAR_DIS` register to disable VAR calculation. Must be done before setting RUN bit.

$$\texttt{xWATT} = \left(1 + \frac{\texttt{xPGAIN}}{2^{27}}\right) \texttt{xWATT}_0 + \texttt{xWATTOS}$$

3.4 Conversión

3.5 Comentarios

Este cálculo se realiza para la energía activa y la energía reactiva. La aparente se realiza con los valores RMS.

4. xVA

4.1 Descripción

The total apparent power calculations, one for each channel (AVA, BVA, and CVA) are updated every 8 kSPS. The fundamental apparent power is also updated every 8 kSPS and is available in the AFVA, BFVA and CFVA registers. With full-scale inputs, the xVA and xFVA value is 20,694,066 decimals.

The ADE9000 offers a register (VNOM) that can be set to a value to correspond to the desired voltage rms value. If the VNOMx-EN bits in the CONFIG0 register are set, VNOM multiplies by xIRMS when calculating xVA.

Meter datapath

4.2 Frecuencia - Periodo

8kSPS

4.3 Parámetros

Implícitamente todos aquellos que afecten al cálculo de xIRMS y xVRMS.

- VNOMx_EN verificar este parámetro

4.4 Conversión

4.5 Comentarios

Error en la imagen del datasheet: La mitad inferior que corresponde a la tensión es un reflejo de la parte superior y aparece AI_PCF donde debería aparecer AV_PCF.

5. xPF

5.1 Descripción

The power factor calculation, one for each channel (APF, BPF, and CPF), is updated every 1.024 sec. The sign of the APF calculation follows the sign of AWATT. To determine if power factor is leading or lagging, refer to the sign of the total or fundamental reactive energy and the sign of the xPF or xWATT value, as indicated meter imagen The power factor result is stored in 5.27 format. The highest power factor value is 0x07FF_FFFF, which corresponds to a power factor of 1. A power factor of -1 is stored as 0xF800_0000.

5.2 Frecuencia - Periodo

1.024s

5.3 Parámetros

5.4 Conversión

Power Factor $= \mathtt{xPF} * 2^{-27}$
REVISAR. Esta fórmula gestiona correctamente los PF negativos?

5.5 Comentarios

6. xITHD xVTHD

6.1 Descripción

A THD calculation is available on the IA, IB, IC, VA, VB, and VC channels in the AITHD, BITHD, CITHD, AVTHD, BVTHD, and CVTHD registers, respectively. THD updates once every second. The THD calculation is stored in signed 5.27 format. The highest THD value is 0x2000 0000, which corresponds to a THD of 400 %.

5.27 format: es un formato de coma fija, con 5 bits para la parte entera y 27 bits para la parte decimal

Fórmula:

$$\texttt{xITHD} = \sqrt{\frac{\texttt{AIRMS}^2 - \texttt{AIFRMS}^2}{\texttt{AIFRMS}^2}}$$

6.2 Frecuencia - Periodo

1s

6.3 Parámetros

Implícitamente todos aquellos que repercuten en `xIRMS`, `xIFRMS`, `xVRMS` y `xVFRMS`

6.4 Conversión

Power Factor $= \texttt{xPF} * 2^{-27}$

% THD on Current Channel A $= \texttt{AITHD} * 2^{-27} * 100$

6.5 Comentarios

No se sacan valores al iniciar hasta pasado 1s ya que saca 400 y si hay cálculos estadísticos quedan falseados.

7. Energy Accumulation

7.1 Descripción

The energy is accumulated into a 42-bit signed internal energy register at 8 kSPS. The internal register can accumulate a user defined number of samples or half line cycles configured by EGY_TMR_MODE bit in the EP_CFG register. When half line cycle accumulation is enabled, configure the zero-crossing source using the ZX_SEL bits in the ZX_LP_SEL register. The number of samples or half line cycles is set in the EGY_TIME register. The maximum value of EGY_TIME is 8191d. With full-scale inputs, the internal register overflows in 13.3 sec. For a 50 Hz signal, EGY_TIME must be lower than 1329 decimals to prevent overflow during half line cycle accumulation. After EGY_TIME + 1 samples or half line cycles, the EGYRDY bit is set in the STATUS0 register and the energy register is updated. The data from the internal energy register is added or latched to the user energy register depending on the EGY_LD_ACCUM bit setting in the EP_CFG register.

The energy register is signed and is 45 bits wide, split between two 32-bit registers, as shown in Figure 65. The user energy can reset on a read using the RD_RST_EN bit in the EP_CFG register. With full-scale inputs, the user energy register overflows in 106.3 sec.

Figura página 18

7.2 Frecuencia - Periodo

Depende de la configuración EGY_TMR_MODE, EGY_TIME samples o EGY_TIME half line cycles.

Actualemente lo configuramos a EGY_TMR_MODE = 0 (samples) y EGY_TIME = 3999 (0.5s)

7.3 Parámetros

En caso de EGY_TMR_MODE = 1 (por half line cycles) implícitamente aquellos que definen la detección de zero-crossings.

- EGY_TMR_MODE = 0 (por samples. Como está ahora)
- EGY_TIME = 3999 (+1 = 4000 = 0.5s) REVISAR. Igual nos interesa poner un número más pequeño aquí para suavizar los valores en caso de leer demasiado rápido o demasiado lento.
- EGY_LD_ACCUM = 0 (modo acumulador)
- RD_RST_EN = 1 (resetea después de lectura)

7.4 Conversión

7.5 Comentarios

Estabá en modo samples a 0.5s con lo que se podia dar el caso en que llegasemos a perder datos. De ahí la propuesta de cambio de parámetros para pasar a un modo acumulador y se resetea el dato una vez se ha leído. Esto hace que si la lectura no es determinista no se pierdan datos y evita ese problema que siempre ha habido de todos los valores a 0 aproximadamente cada 10.2s. Ahora se ha cambiado a 0.1s el periodo de acumulación.

La función de configuración en el remote estaba escribiendo 3999 en float en un registro del ADE9000 que espera un valor entero. Así pues, se estaba escribiendo un valor que no se corresponde con lo que queremos. Ya se ha cambiado para que escriba un enetero.

8. IPEAK VPEAK

8.1 Descripción

The ADE9000 records the peak value measured on the current and voltage channels, from the xI_PCF and xV_PCF waveforms. The PEAKSEL[2:0] bits in the CONFIG3 register allow the user to select which phases to monitor. Set PEAKSEL[2] to monitor Phase C, PEAKSEL[1] for Phase B, and PEAKSEL[0] for Phase A. Set PEAKSEL[2:0] = 111 (binary) to monitor all three phases.

The IPEAK register stores the peak current value in IPEAKVAL[23:0] and indicates which phase(s) currents reached the value in the IPPHASE[2:0] bits. IPEAKVAL is equal to $\texttt{xI\_PCF}/2^5$. IPPHASE[2] indicates that Phase C had the peak value, IPPHASE[1] indicates Phase B, and IPPHASE[0] indicates Phase A.

Similarly, VPEAK stores the peak voltage value in VPEAKVAL[23:0]. VPEAKVAL is equal to $\texttt{xV\_PCF}/2^5$. VPPHASE[2] indicates if Phase C had the peak voltage value, VPPHASE[1] indicates Phase B, and VPPHASE[0] indicates Phase A.

When the user reads the IPEAK register, its value is reset. The same is true for reading VPEAK.

8.2 Frecuencia - Periodo

8 kSPS

8.3 Parámetros

Implícitamente aquellos que modifican a xI_PCF y xV_PCF.
PEAKSEL[2:0] para seleccionar qué fases tener en cuenta.

8.4 Conversión

El registro tiene 2 partes: 3 bits (IPPHASE[2:0] o VPPHASE[2:0]) indicando el canal en el que ha ocurrido el pico y 24 bits (IPEAKVAL[23:0] o VPEAKVAL[23:0]) con el valor.

El valor es $\texttt{yPEAKVAL}[23:0] = \texttt{xy\_PCF}/2^5$.

8.5 Comentarios

Esta variable indica en cual de las 3 phases se ha producido el pico y el valor de este pico en 32 bits. Si se hacen peticiones puntuales cada Xs únicamente se tendrá el peak value de ese instante lo que no aporta mucha información ya que no es el pico durante ese periodo Xs.

9. OIx

9.1 Descripción

Overcurrent indication monitors the RMS current measurements. If a RMS current is greater than the user configured OILVL, the overcurrent threshold, this is indicated in the OI bit in the STATUS1 register.

$$\texttt{OILVL} = \texttt{xIRMSONE}/2^5$$

The OC_EN[3:0] bits in the CONFIG3 register select which phases to monitor for overcurrent events. The OIPHASE[3:0] bits in the OISTATUS register indicate which current channels had RMS measurements greater than the threshold. If a phase is enabled, with the corresponding OC_EN bit set and RMS current greater than the threshold, the OI status is set and the RMS value is stored in the corresponding OIx register. If a phase is disabled, or an overcurrent event does not occur on that phase, the OIx register keeps the last value.

9.2 Frecuencia - Periodo

La condición se comprueba según la variable RMS1/2 (medio ciclo) ∼10ms (a 50 Hz). En realidad depende de la detección de zero-crossings.

9.3 Parámetros

Implícitamente aquellos que afectan xRMSONE.

- OC_EN = 1 (bits 12, 13 y 14 a 1)
- $\texttt{OILVL} = \texttt{xIRMSONE}/2^5$
- $\texttt{xIRSMONE} = \texttt{OI\_THR}/i\_factor$ (OI_THR = 1A)

9.4 Conversión

REVISAR. Alguna vez hemos visto que los valores no se corresponden con la RMS. Unido al hecho de que el threshold/level se divide en 2^5 y hay otros registros en los que esto también pasa hay que verificar si tenemos que hacer $\texttt{OIx} * 2^5$ para obtener el valor real. Tanto en el datasheet como en el technical reference manual no pone que haga falta una conversión. Hay que repasar como se calcula el xRMSONE.

Antes, xRMSONE estabá precalculado, era un define que se dividía entre 2^5. Ahora se le pasa el valor de threshold que queremos (1A, que en siguientes versiones será el parametro que venga del AICT) y se divide entre el factor de coversión de corriente y entre 2^5.

9.5 Comentarios

La variable OIx mantiene el último valor que ha superado el threshold no el máximo desde el arranque.

Este valor puede variar en cada aplicación. Tendría que ser configurable desde el AICT.

10. SWELLx

10.1 Descripción

the swell indication has a SWELL_LVL register to set the swell threshold, according to this equation:

$$\texttt{SWELL\_LVL} = \texttt{xVRMSONE} * 2^{-5}$$

There is also a SWELL_CYC register. The maximum RMS voltage value measured during the swell is stored in the corresponding SWELLA, SWELLB, and SWELLC registers. If the DIP_SWELL_IRQ_MODE bit is set to 0 in the CONFIG1 register, an interrupt is generated every DIP_CYC/ SWELL_CYC cycles. If DIP_SWELL_IRQ_MODE is set to 1, one interrupt is generated when dip/swell mode is entered and another interrupt is generated on exit. The mode is changed after DIP_CYC cycles. Note that if DIP_CYC/SWELL_CYC = 1, an extra interrupt is generated on exit of the dip/swell condition, and the dip/swell value, DIPx/SWELLx, is updated at that time, which exceeds the DIP_LVL/SWELL_LVL value.

10.2 Frecuencia - Periodo

según configuración SWELL_CYC

10.3 Parámetros

- $\texttt{SWELL\_LVL} = \texttt{xVRMSONE}/2^5$
- $\texttt{xVRMSONE} = \texttt{SEWLL\_THR}/v\_factor$ (SEWLL_THR = 240v, configurable por AICT en siguientes versiones)
- SWELL_CYC = 3000.

10.4 Conversión

Hay que multiplicar por 2^5 el valor que se lee de los registros xSWELL.

10.5 Comentarios

un valor correcto para detectar SWELL sería entre 30s y un minuto.

REVISAR. Una vez se ha cumplido la condición sobre la duración especificada, no sabemos si el contador de duración se resetea o continúa creciendo. Para simplificar supongamos que la condición se cumple siempre. Si el contador de duración se resetea, cada duración el valor del SWELLx se actualizaría. Si el contador no se resetea, cada vez que se evalúa la RMSONE se actualizaría el valor de SWELLx.

11. DIPx

the DIP_LVL register to correspond to the RMS value to trigger the dip event, according to this equation:

$$\texttt{DIP\_LVL} = \texttt{xVRMSONE} * 2^{-5}$$

Configure the number of cycles to observe the RMS value over in the DIP_CYC register. The RMS voltages on Phase A, Phase B, and Phase C is compared to the DIP_LVL over the specified DIP_CYC. If the RMS voltage is low for the specified number of DIP_CYC, the dip event has occurred on that phase and the corresponding DIPA, DIPB, and DIPC bits are set in the STATUS1 register. The dip event can be configured to generate an interrupt on the IRQ1 pin.

The dip event can be configured to generate an event on the CF4/EVENT/DREADY pin, if the corresponding bits are set in the EVENT_MASK register. This allows the user to precisely time the duration of a dip or swell, using the CF4/EVENT/DREADY pin in combination with a timer on an external microcontroller.

The minimum RMS value measured during the dip is stored in the corresponding DIPA, DIPB, and DIPC registers.

11.1 Frecuencia - Periodo

según configuración DIP_CYC

11.2 Parámetros

- $\texttt{DIP\_LVL} = \texttt{xVRMSONE}/2^5$
- $\texttt{xVRMSONE} = \texttt{DIP\_THR}/v\_factor$ (DIP_THR = 220v, configurable por AICT en siguientes versiones)
- DIP_CYC = 3000.

11.3 Conversión

Hay que multiplicar por 2^5 el valor que se lee de los registros DIPx.

11.4 Comentarios

12. Angle Measurement

12.1 Descripción

The ADE9000 measures the time between zero-crossings on each phase. This measurement helps to determine if the system is balanced properly or to figure out if there

was an installation error. The user can check if the phase angles correspond to the ones in the phasor diagrams in the Applying the ADE9000 to Different Metering Configurations section. The times between positive to negative zero-crossings are measured using a CLKIN/24 = 24.576/24 = 1024 kHz clock. The time between the zero-crossing on Phase A and Phase B is stored in the ANGL_VA_VB register. The resolution of the ANGLx_x2x register is (1/(1024 1000))/20 ms 360 = 0.017578125 at 50 Hz. The time between the zero-crossing on Phase B and C is stored in the ANGL_VB_VC register, and the time in between the zero-crossings on Phase A and C is stored in the ANGL_VA_VC register, as shown in Figure poner imagen

The angle in degrees can be calculated from the following equation with a 50 Hz line period: Angle (degrees) = ANGL_VA_VB 0.017578125/LSB For a 4-wire wye configuration, the expected ANGL_VA_VB and ANGL_VB_VC is 120/0.017578125 = 3413 (decimal). Note that the expected ANGL_VA_VC from the Phase A voltage to Phase C voltage is 240/0.017578125 = 13653 (decimal), which corresponds to a 120 angle between Phase C and Phase A. The current to current zero-crossings are also measured. This measurement is done similarly to the voltage to voltage phase angle described previously, except the current channel zero- crossings are used as the reference. The time between the zero-crossing on Phase A and Phase B is stored in the ANGL_IA_IB register. The time between the zero-crossing on Phase B and Phase C is stored in the ANGL_IB_IC register, and the time in between the zero-crossings on Phase A and Phase C is stored in the ANGL_IA_IC register. The voltage to current phase angles are measured as well. These angles can be used to determine the power factor at the fundamental. ANGL_VA_IA reflects the phase angle between the Phase A voltage and current, as shown in Figure 32. ANGL_VB_IB holds the Phase B voltage to current phase angle, and ANGL_VC_IC holds the Phase C voltage to current phase angle. poner imagen Note that if the magnitude of the voltage channel is below the user configured zero-crossing threshold, the zero-crossing output for that phase is not generated. In this event, the corresponding ANGLx_x2x measurements are not updated; the last value remains in the register. The current channel does not have these thresholds. With a low input signal level, spurious zero-crossing events may be generated on the current channel, which results in ANGLx_I2I and ANGLx_V2I readings that are not meaningful.

12.2 Frecuencia - Periodo

REVISAR. Parece que los valores de ángulos dependen de xPERIOD y no me queda claro xPERIOD cada cuanto se actualiza. Entiendo que este registro está sincronizado con xPERIOD.

Datasheet page 31, también aparece en el Technical Reference Manual:

> The zero-crossing detection circuits have two different output rates: 8 kSPS and 1024 kSPS (ERRATA. Debería ser “1024 SPS”). The 8 kSPS zero-

crossing signal calculates the line period, updates the ZXx bits in the STATUS1 register, and monitors the zero-crossing timeout, phase sequence error detection, resampling, and energy accumulation functions. The 1024 kSPS (ERRATA. Debería ser "1024 SPS") zero-crossing signal calculates the angle and updates the zero-crossing output on the CF3/ZX pin.

Technical Reference Manual table 17. Zero-Crossing Use in Other Functions: Angle measurements: Negative to positive.

Así se entiende que la granularidad de actualización son 1024 SPS pero esto solo ocurre cuando hay un ZX de negativo a positivo.

12.3 Parámetros

Indicar la frecuencia (50-60Hz) es un valor de AICT

12.4 Conversión

For a 50 Hz system, Angle (Degrees) = $\texttt{ANGL\_x\_y} * 0{,}017578125$
For a 60 Hz system, Angle (Degrees) = $\texttt{ANGL\_x\_y} * 0{,}02109375$
Angle (degrees) = ANGL_VA_VB * 0.017578125/LSB (? Que es esto de LSB?)

12.5 Comentarios

Se han verificado los valores de ángulo entre V y parece Ok. Faltan verificaciones de intensidad y de V-I.

El remote ya contempla la conversión de 50 Hz y 60Hz.

13. PHNOLOAD

13.1 Descripción

The PHNOLOAD register indicates whether each phase of energy is in no-load. For example, the PHATNL[2:0] bits in the PHNOLOAD register indicate whether the Phase A total apparent energy, reactive energy, and active energy are in phase on Bit 2 through Bit 0, respectively. If a bit is set, it indicates that the phase energy is in no-load; if it is clear, the phase is not in no-load. The user can enable an interrupt to occur when one of the per phase energy no-load status changes, either going into or out of no-load. There is an interrupt enable bit for each type of energy. Set the VAFNOLOAD, RFNOLOAD, AFNOLOAD, VANLOAD, RNLOAD, and ANLOAD bits in the STATUS1 register to enable an interrupt on IRQ1 when one or more phases of fundamental VA, fundamental VAR, fundamental watt, total VA, total VAR, and total watt no-load changes status. There is also an option to indicate the no-load status on the EVENT pin; see the Interrupts/EVENT section for more information. Figure 22 shows what happens when the xWATT, low-pass filtered watt, value goes above the user configured no-load threshold and then back down below it again. The same concept applies to all of the energy values (total and fundamental VAR, total VA) with the corresponding REACT_NL_LNL and APP_NL_LVL no-load thresholds.

13.2 Frecuencia - Periodo

13.3 Parámetros

- NOLOAD_TMR = 8ms 'default'. No sería necesario este periodo. Estado deseado DISABLED = 0b111.
- ACT_NL_LVL... no hace falta configurar ya que no vamos a utilizar esta variable

13.4 Conversión

13.5 Comentarios

la función principal de esta variable es detectar que cae de un valor de potencia definido en un threshold. Cuando lo detecta desactiva la acumulación de energía. Para la funcionalidad que realmente tiene no es adecuada para nosotros en el caso de coger energía paralelamente ya que este concepto se utilizada para determinar cuando la máquina está en running o en standby pero en todo caso se querría guardar energía. Se deshabilita si se puede o sino se verifica si el valor es en absoluto y se configura a 0. También se tendría que calcular a cuánto está configurado a día de hoy

14. ISUMRMS

14.1 Descripción

The ADE9000 also calculates the rms of the sum of IA + IB + IC IN and stores the result in the ISUMRMS register. The ISUMRMSOS register allows offset calibration of this measurement. The scaling is the same as for the other xIRMS and xIRMSOS registers (see the Filter-Based Total RMS section for more information). If a neutral current sensor is not used, write the ISUM_CFG[1:0] bits in the CONFIG0 register equal to 0, and then ISUMRMS approximates the neutral current from the sum of IA, IB, and IC. If the measured neutral current, NI_PCF, deviates from the sum of AI_PCF + BI_PCF + CI_PCF current channel waveforms, there may be a fault in the system. To determine how large the mismatch is between the measured neutral current and the measured A, B, and C currents, select ISUM_CFG[1:0] to 01 or 10 based on the direction of the neutral current with respect to the other current channel waveforms.

poner tabla

ISUMRMS has the same scaling as xIRMS. Note that if AI_PCF, BI_PCF, and CI_PCF are all at full scale and in phase with each other, with the ISUM_CFG[1:0] equal to 00 or 11, ISUMRMS is 3 52,702,092 = 158,106,276 (decimal). If AI_PCF, BI_PCF, CI_PCF, and NI_PCF are all at full scale and in phase with each other, with the ISUM_CFG[1:0] equal to 01, ISUMRMS is 4 52,702,092 = 210,808,368 (decimal). To obtain an indication if ISUMRMS exceeds a threshold, configure ISUMLVL. Then the MISMTCH bit in STATUS0 and associated interrupt indicate if there is a change in the relationship between ISUMRMS and ISUMLVL. Calculate the desired value of ISUMLVL according to the following equation:

$$\texttt{ISUMLVL} = \frac{\texttt{xRMS\_FULL\_SCALE}}{X}$$

where: xIRMS_Full_Scale is the nominal xIRMS value with full-scale inputs, 52,702,092. X is the desired current level to indicate a MISMTCH error.

14.2 Frecuencia - Periodo

8kSPS

14.3 Parámetros

- ISUM_CFG = 00/11 (ISUM=IA+IB+IC)
- ISUM_LVL = 0 'default'

14.4 Conversión

14.5 Comentarios

Inicialmente se deja como sumatorio de la intensidades xI_PCF

15. xPeriod

15.1 Descripción

The ADE9000 line period measurement is done by taking the values low-pass filtered by LPF1, as described in the Zero-Crossing Detection section, and then using the two values near the positive to negative zero-crossing to calculate the exact zero-crossing point using linear interpolation. This information is used to precisely calculate the line period, which is stored in the xPERIOD register. The line period, TL , can be calculated from the xPERIOD register according to the following equation:

$$T_L = \frac{(xPERIOD + 1)}{8000 \times 2^6}(sec)$$

Similarly, the line frequency can be calculated from the xPERIOD register, using the following equation:

$$f_L = \frac{8000 * 2^16}{\texttt{xPERIOD} + 1}(Hz)$$

With a 50 Hz input, the xPERIOD register is 0x00A0_0000, 10485760 (decimal), and with 60 Hz, it is 0x0085_5554, 8738132 (decimal).

15.2 Frecuencia - Periodo

8kSPS

15.3 Parámetros

- SELFREQ en el registro ACCMODE. 0 para 50Hz o 1 para 60Hz

15.4 Conversión

Aplicamos la fórmula de la explicación para pasar el valor del registro a segundos. Nos interesa el valor en milisegundos, por lo que al resultado le multiplicamos 1000.

$$T_L = \frac{(xPERIOD + 1)}{8000 \times 2^6} * 1000$$

15.5 Comentarios

Da información acerca del periodo de la señal. Tiene vinculación con la detección de ángulos

16. Phase Sequence Error Detection

16.1 Descripción

If one to two ZX events are missing, SEQERR is generated. If all ZX are missing then SEQERR bit is note set.

Write SEQ_CYC to indicate how many consecutive incorrect transitions must be observed before raising the SEQ_ERR interrupt. It is recommended to set SEQ_CYC to 1.

16.2 Frecuencia - Periodo

Cada vez que ocurre un zero-crossing.

16.3 Parámetros

- VCONSEL en el registro ACCMODE. Dependiendo de la configuración HW que tengamos.
- SEQ_CYC recomendado a 1

16.4 Conversión

Leer el bit 18 del regsitro STATUS1. Una vez leído, hay que escribir 1 en ese mismo bit para resetear su valor, de lo contrario, si el valor es 1 debido a un error, permanecerá en 1.

16.5 Comentarios

Permite detectar el error que pueda ser por instalación no correcta de las referencias de tensión o porque por instalación tienen las fases cruzadas (se ha visto más de una vez)

17. ADC_REDIRECT

17.1 Descripción

Is not an slow var, but a configuration parameter.

The ADE9000 provides a multiplexer that allows any ADC output to be redirected to any digital processing datapath. By default, each modulator is mapped to its corresponding datapath. For example, the IAP and IAN pins go into the IA modulator, which is mapped to the IA digital processing datapath. Write to the ADC_REDIRECT register to change the ADC to digital channel mapping. The redirection can be useful to simplify layout, depending on if the ADE9000 is on the top or bottom of the PCB, by redirecting

the IA ADC output to the IC digital datapath and the IC ADC output to the IA digital datapath. To redirect the IA and IC ADC outputs, write IA_DIN = 010 and IC_DIN = 000 in the ADC_REDIRECT register. Alternatively, the VA voltage channel output can be used for all three datapaths by writing VB_DIN = 101 and VC_DIN = 101 in the ADC_REDIRECT register.

17.2 Parámetros

El registro ADC_REDIRECT. Configurar cada uno de los canales de tension y corrente.

VC channel data can be selected from all channels. The bit descriptions for 000b through 110b match VC_DIN. When the value is equal to 111b, then:

- 000 IA ADC data.
- 001 IB ADC data.
- 010 IC ADC data.
- 011 IN ADC data.
- 100 VA ADC data.
- 101 VB ADC data.
- 110 VC ADC data.
- default ADC data.

17.3 Comentarios

Cambia el signo de la corriente de una fase. Necesario cuando se ha instalado maluna pinza amperim etrica y se tiene que cambiar en remoto.

18. xIGAIN xVGAIN

18.1 Descripción

Is not an slow var, but a configuration parameter.

There are many sources of gain error in an energy metering system. The current sensor, including current transformer burden resistors, may have some error. There is part to part gain error in the ADE9000 device itself, and the voltage reference may have some variation (see the data sheet for the device specifications). The ADE9000 provides a current gain calibration register so that each metering device has the same current channel scaling.

The xVGAIN registers can be used to calibrate the voltage channel of each phase. The xVGAIN register has the same scaling as the xIGAIN register. See the Current Channel Gain, xIGAIN section for the equation.

The current channel gain varies with xGAIN as shown in the following equation:

$$CurrentChannelGain = (xGAIN - 1) * 2^{27}$$

18.2 Parámetros

GAIN que se quiere aplicar a cada fase. xGAIN