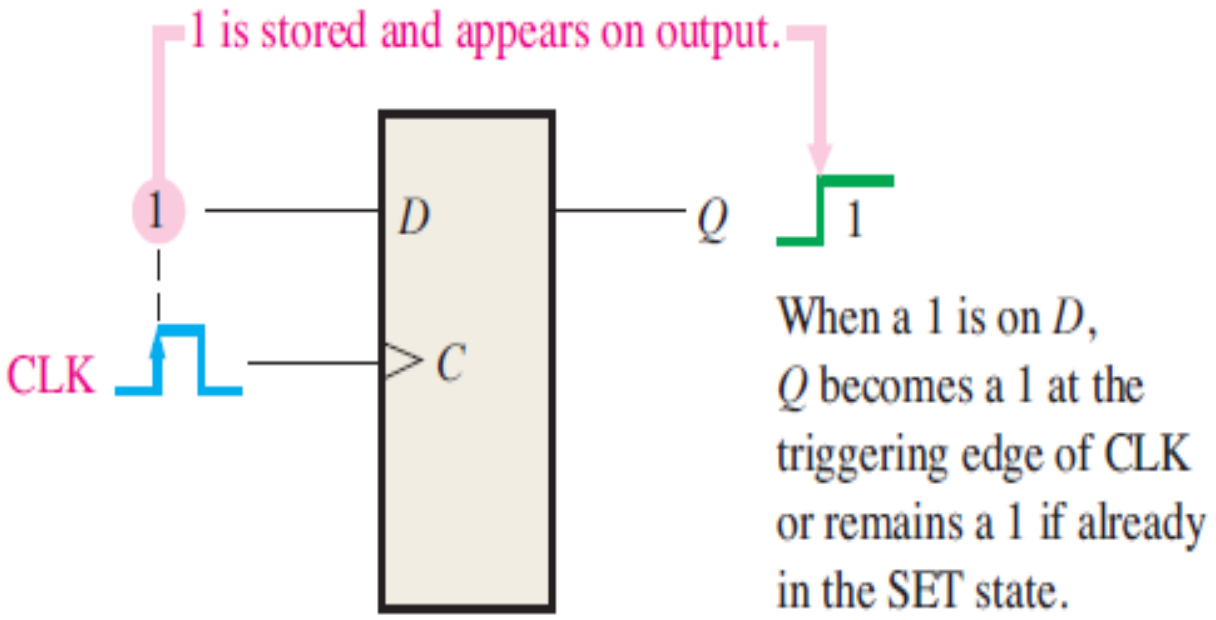
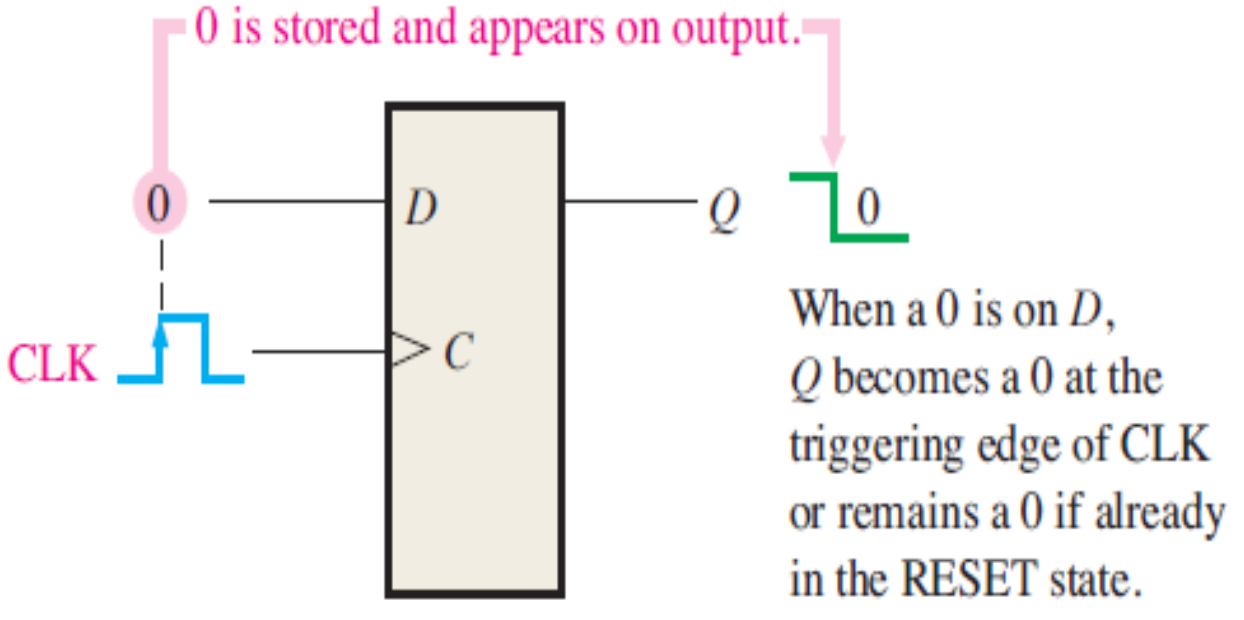
Lecture-3
Sequential Circuit Design
Shift Registers

Shift Registers

- Shift register is a digital circuit with two basic functions; data storage and data movement.
- Shift registers contains different arrangements of flip-flops.
- Each flip-flop in a shift register represents one bit of storage capacity.
- The number of flip-flops in a register determines its storage capacity.
- The shift operation of a register allows the movement of data from one stage to another stage or into or out of the register.



Concept of storing a 1

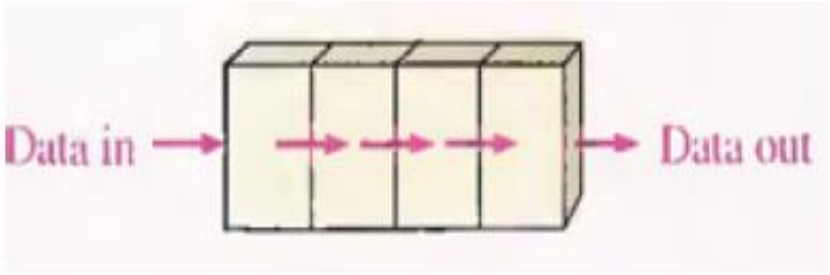


Concept of storing a 0

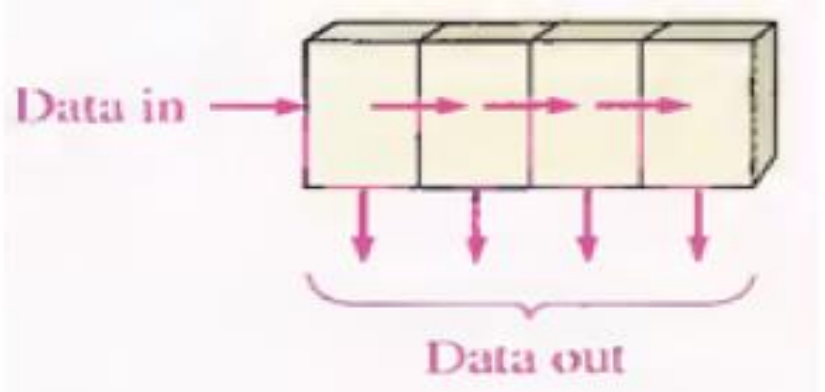
Shift Registers

The are four types of shift register based on their movement:

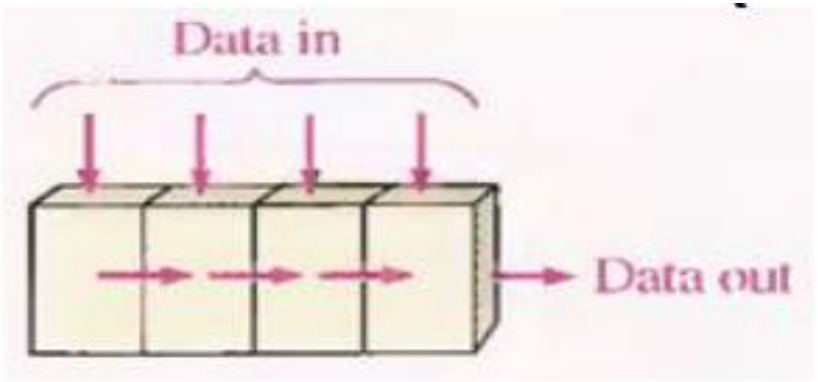
Serial In Serial Out (SISO)



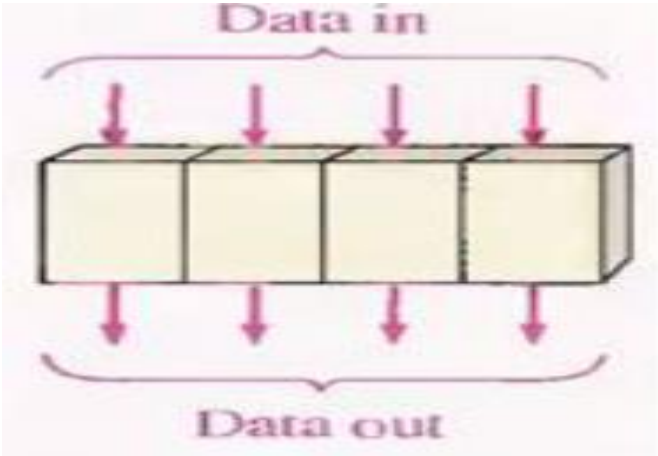
Serial In Parallel Out (SIPO)



Parallel In Serial Out (PISO)

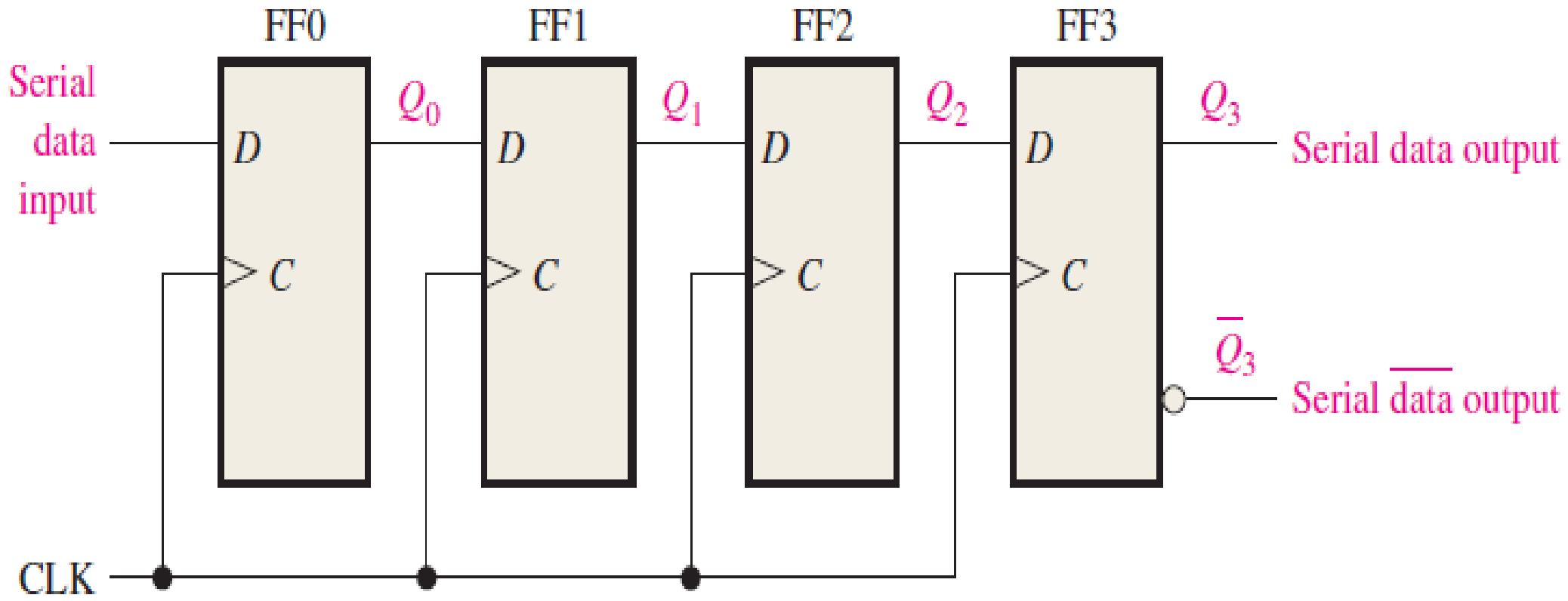


Parallel In Parallel Out (PIPO)



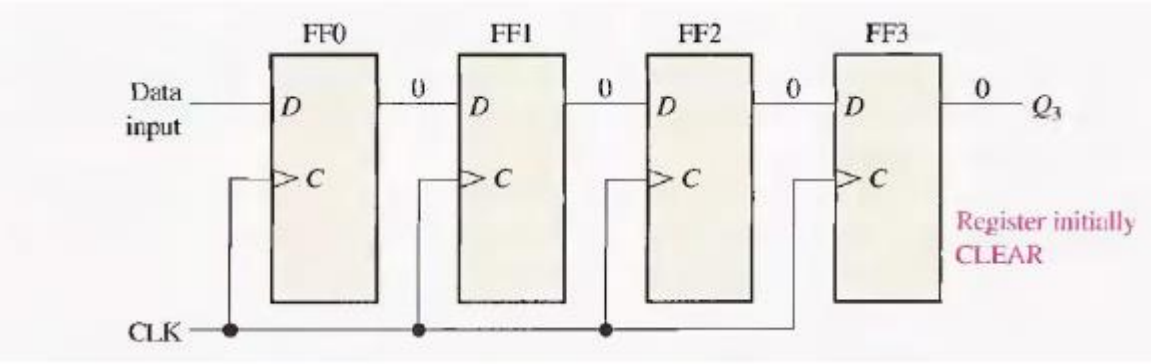
Serial In/ Serial Out Shift Registers

- The serial in/serial out shift registers accepts data serial, that is one bit at a time.
- It produces the stored information in its output also in serial form
- An N-bit flip-flop will take N clock pulses to store N-bit data completely.

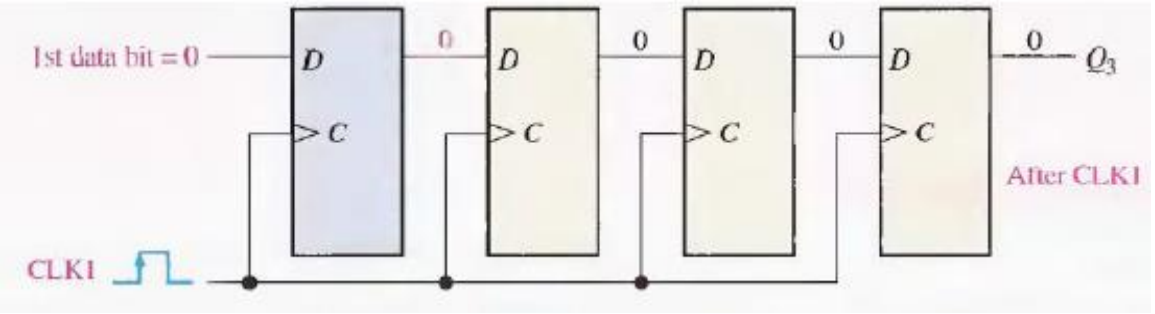


Serial In/ Serial Out Shift Registers

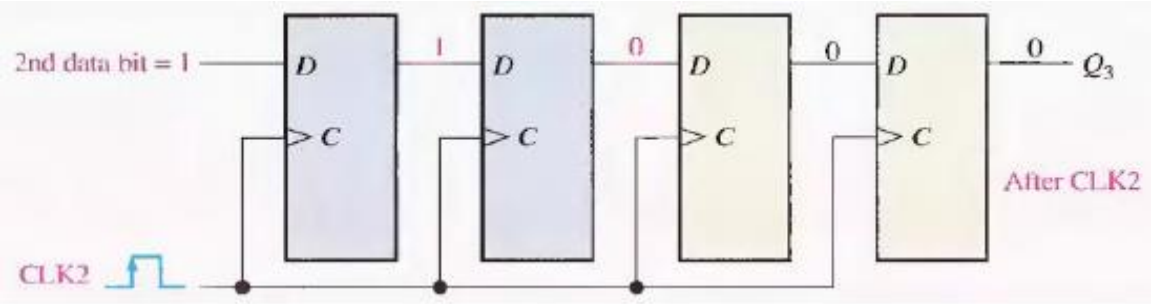
Four bits (1010) being entered serially into the shift register:



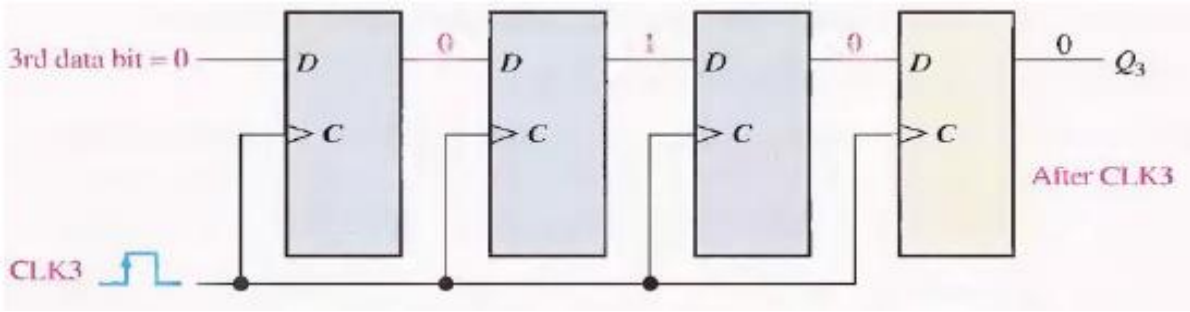
Initial State



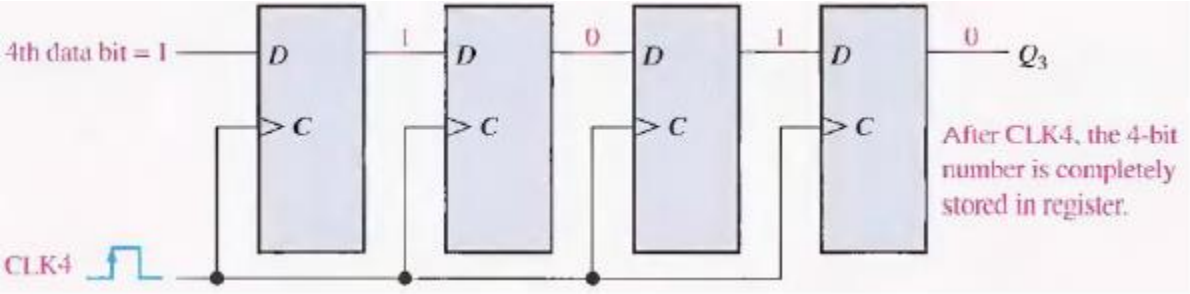
State after Clock Pulse 1



State after Clock Pulse 2



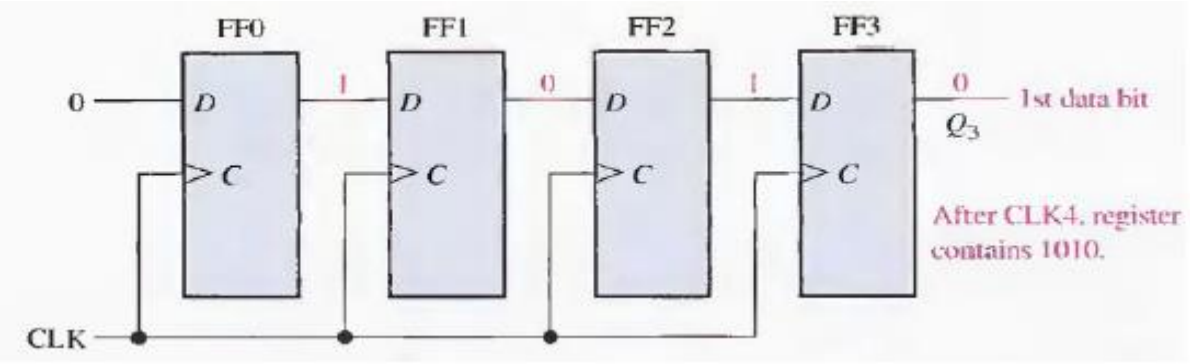
State after Clock Pulse 3



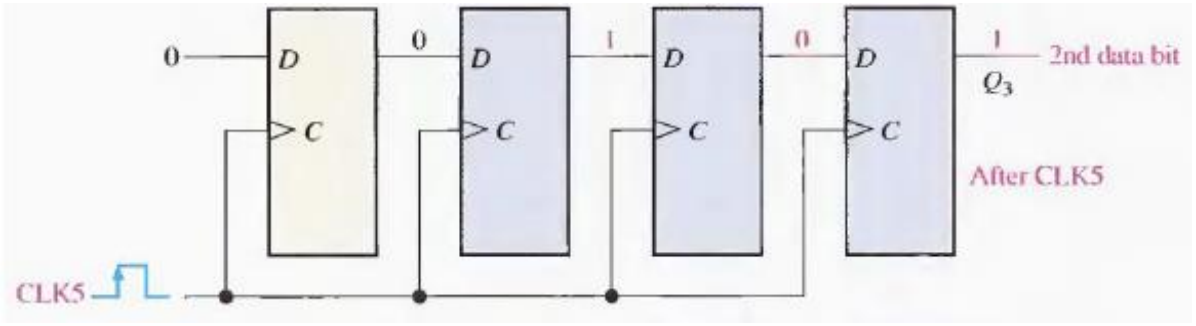
State after Clock Pulse 4

Serial In/ Serial Out Shift Registers

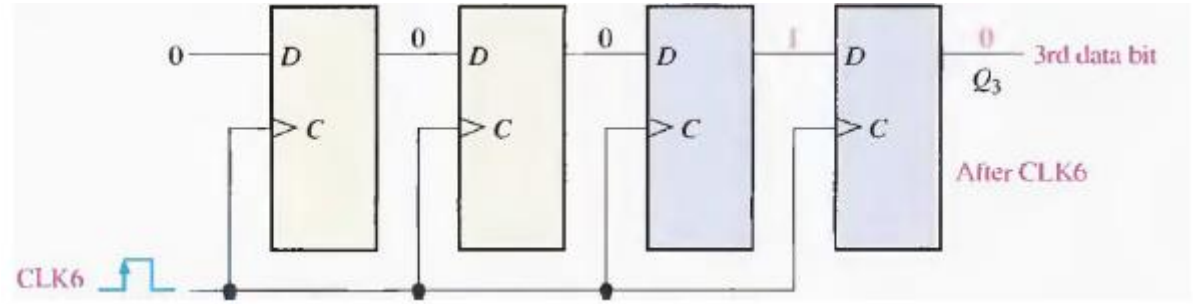
Four bits (1010) being serially shifted out of the register and replaced by zeros:



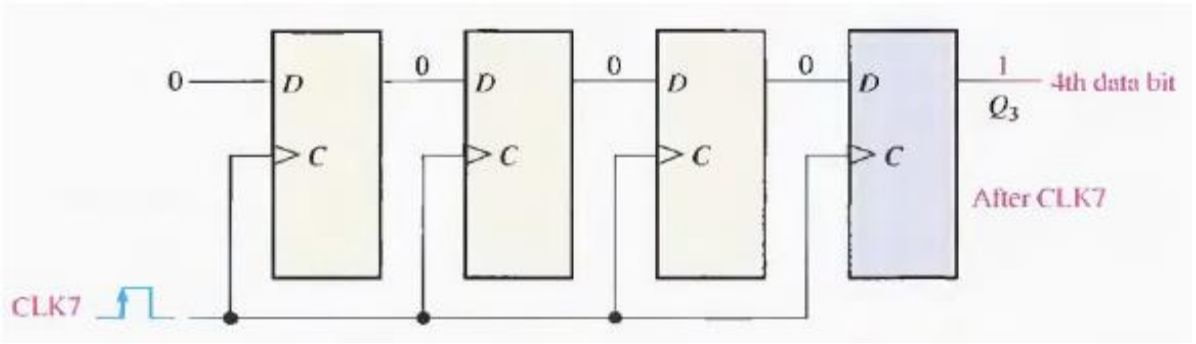
State after Clock Pulse 4



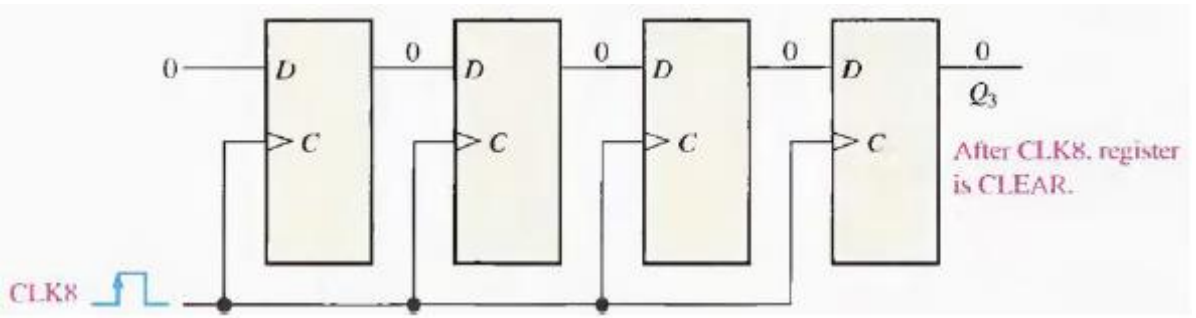
State after clock pulse 5



State after clock pulse 6

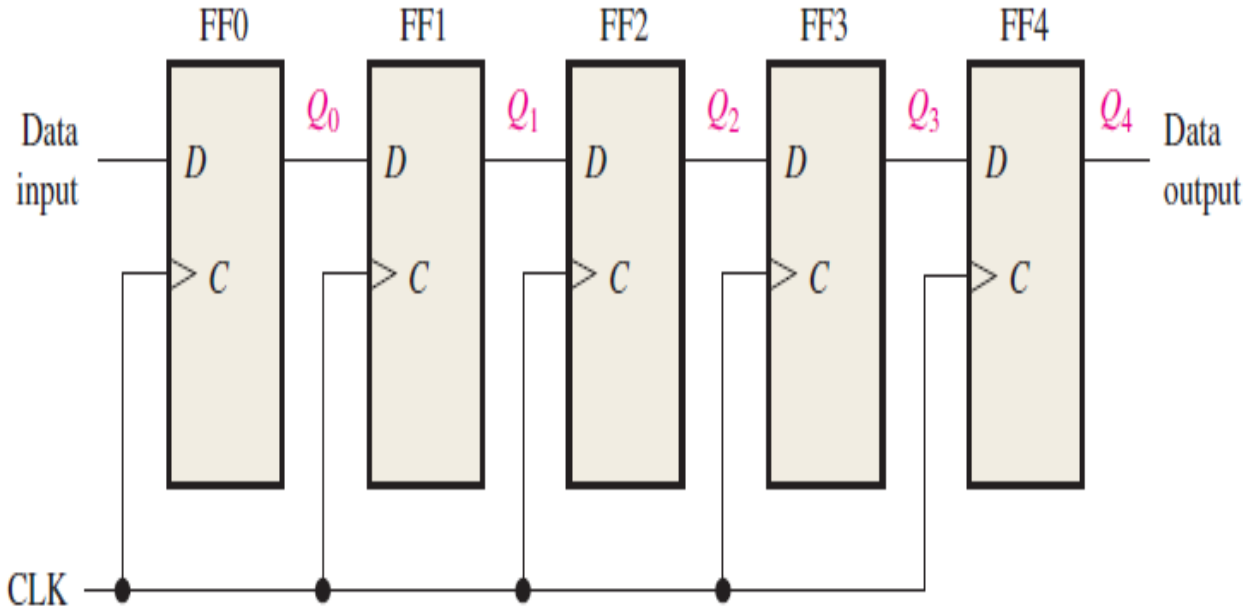


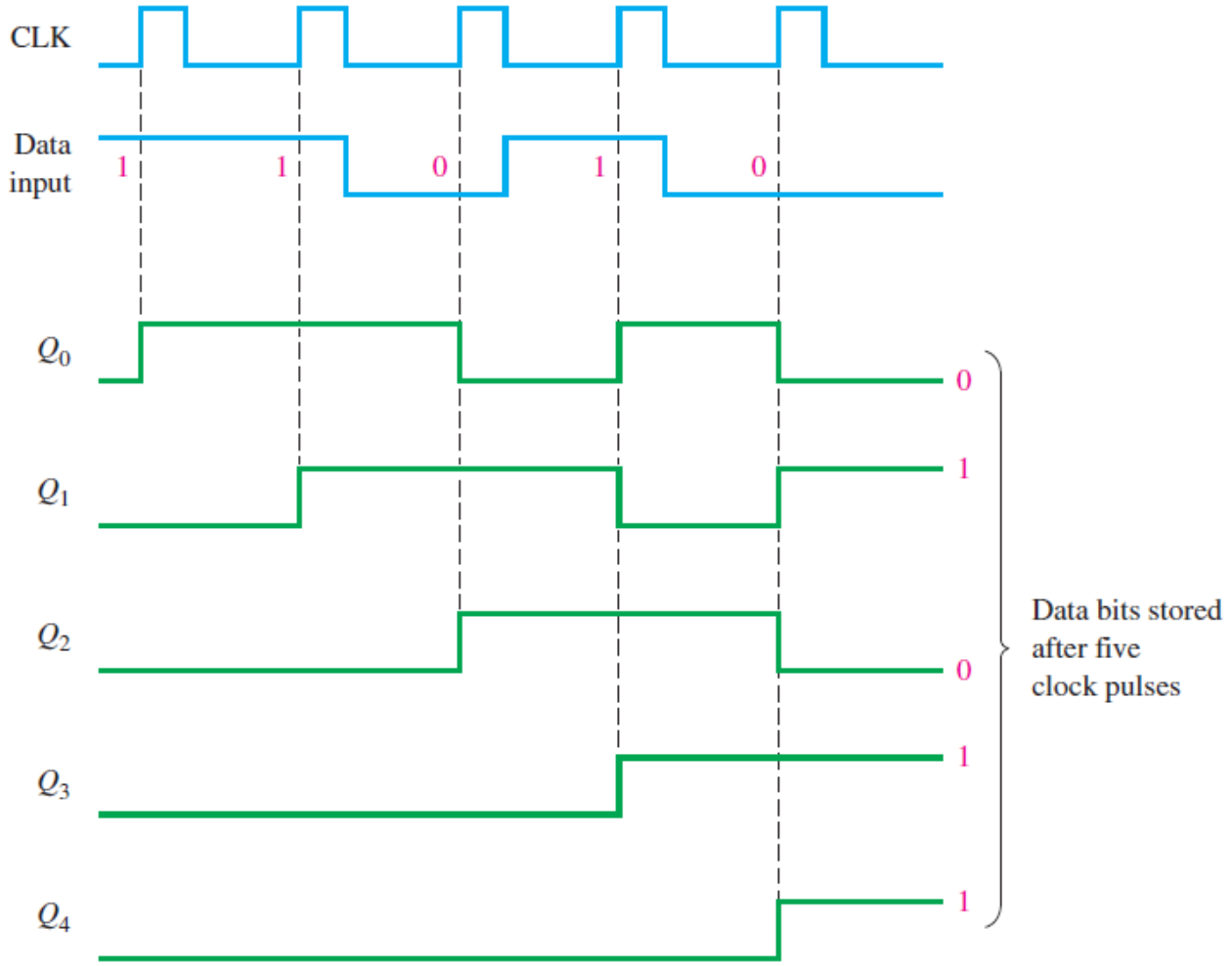
State after clock pulse 7



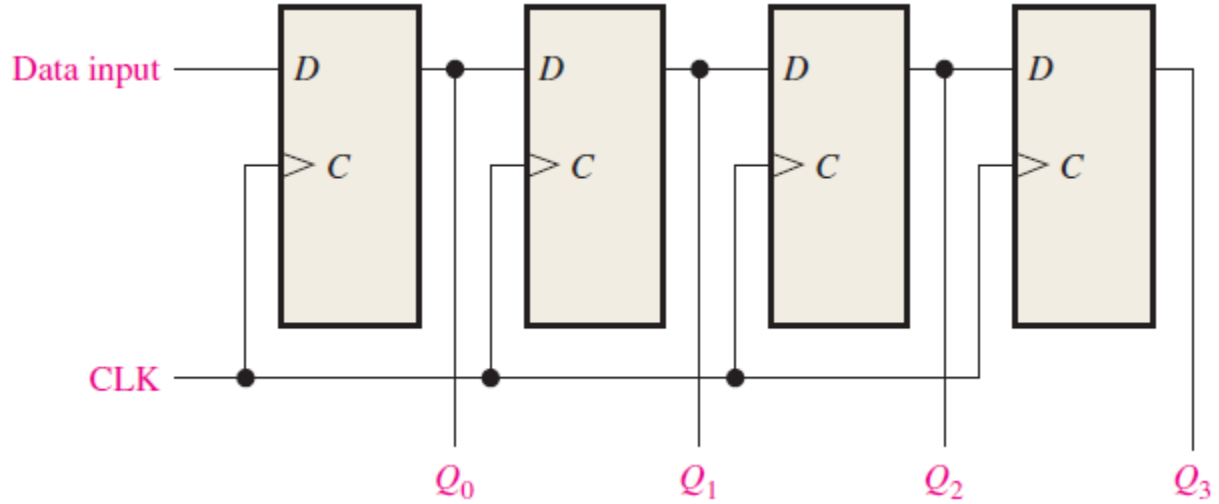
State after clock pulse 8

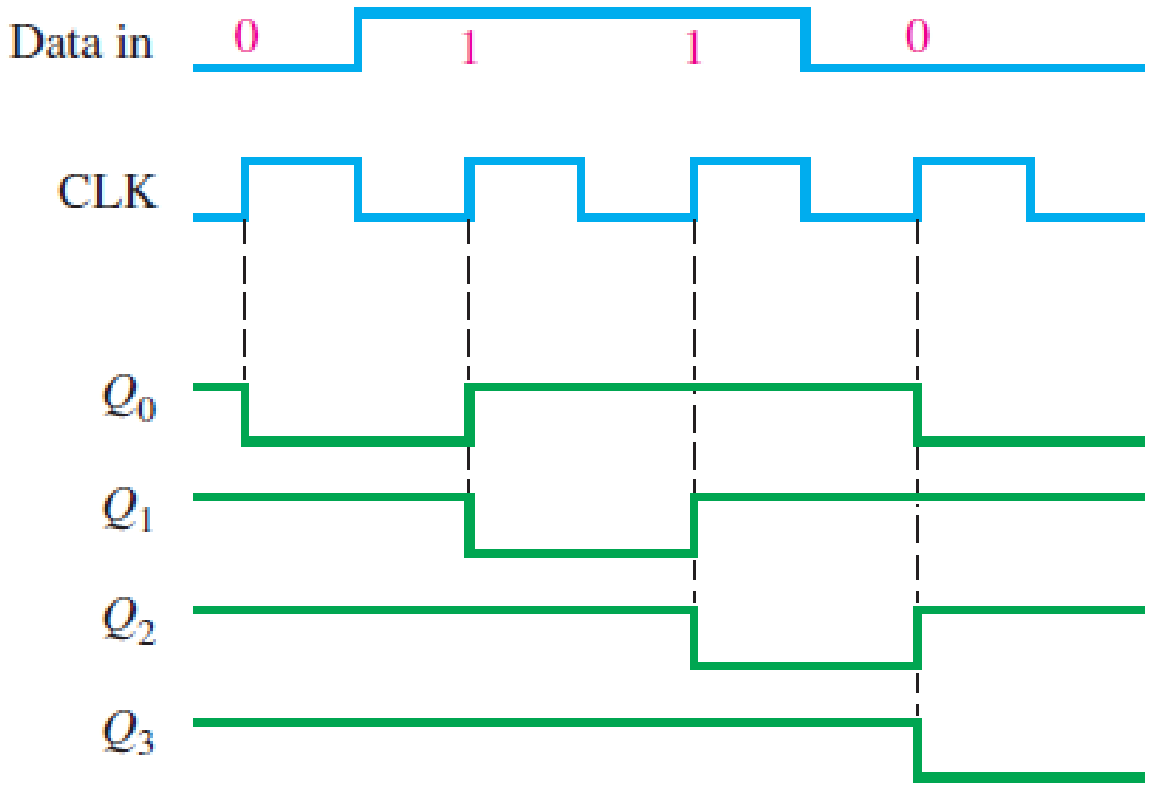
Serial In/ Serial Out Shift Registers

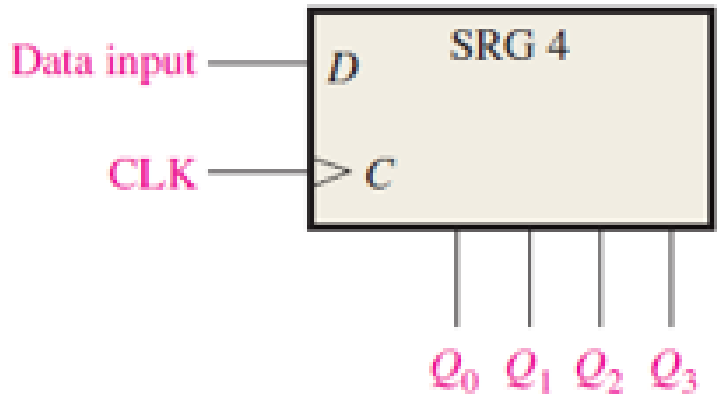




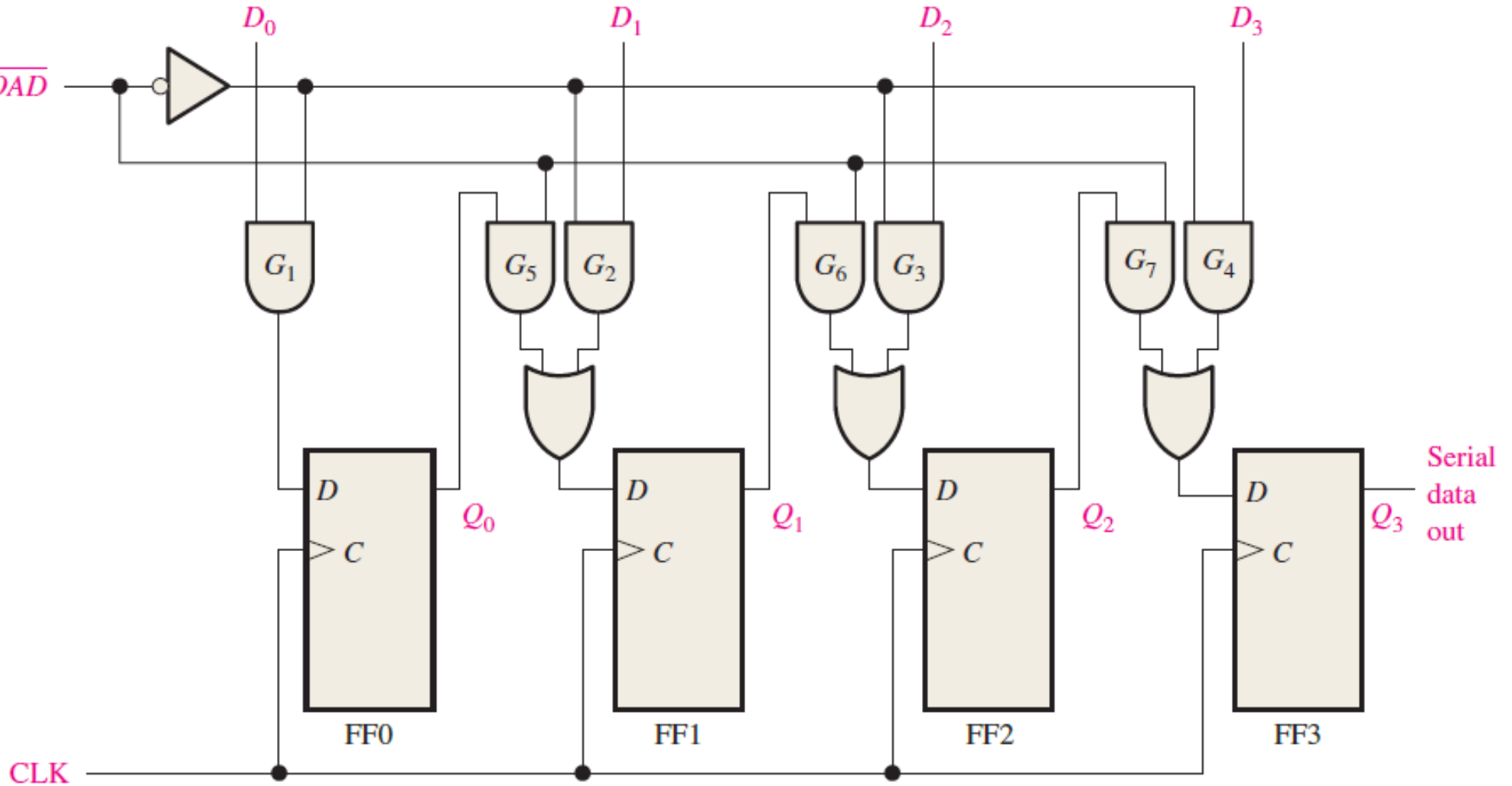
Serial In/ Parallel Out Shift Registers







Parallel In/ Serial Out Shift Registers

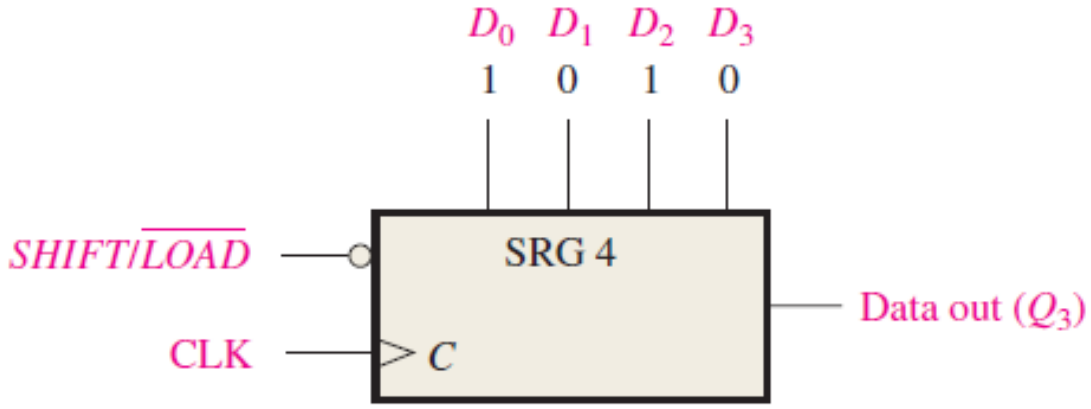


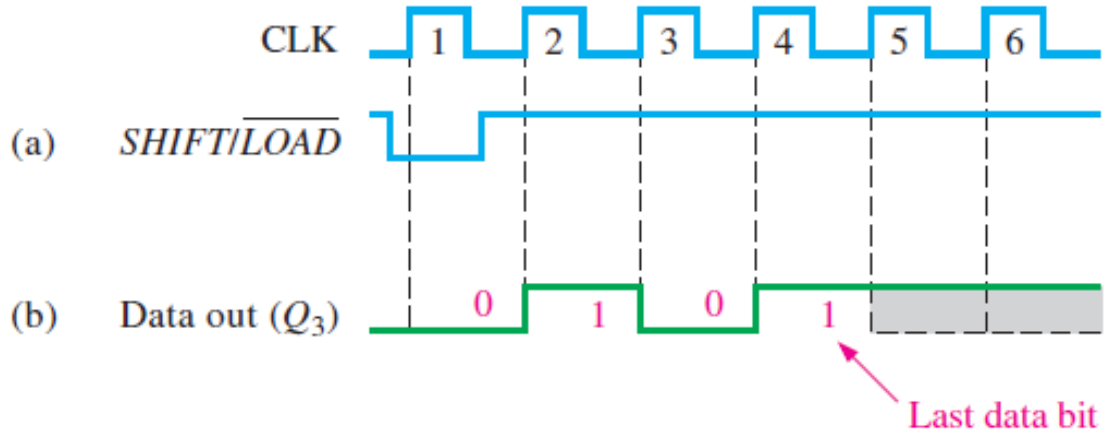
Shift/$\overline{\text{LOAD}}$=0, Load line gets activated

Shift/$\overline{\text{LOAD}}$=1, Shift line gets activated

Parallel In/ Serial Out Shift Registers

Show the data-output waveform for a 4-bit register with parallel input data and the clock and SHIFT/$\overline{\text{LOAD}}$ waveform.

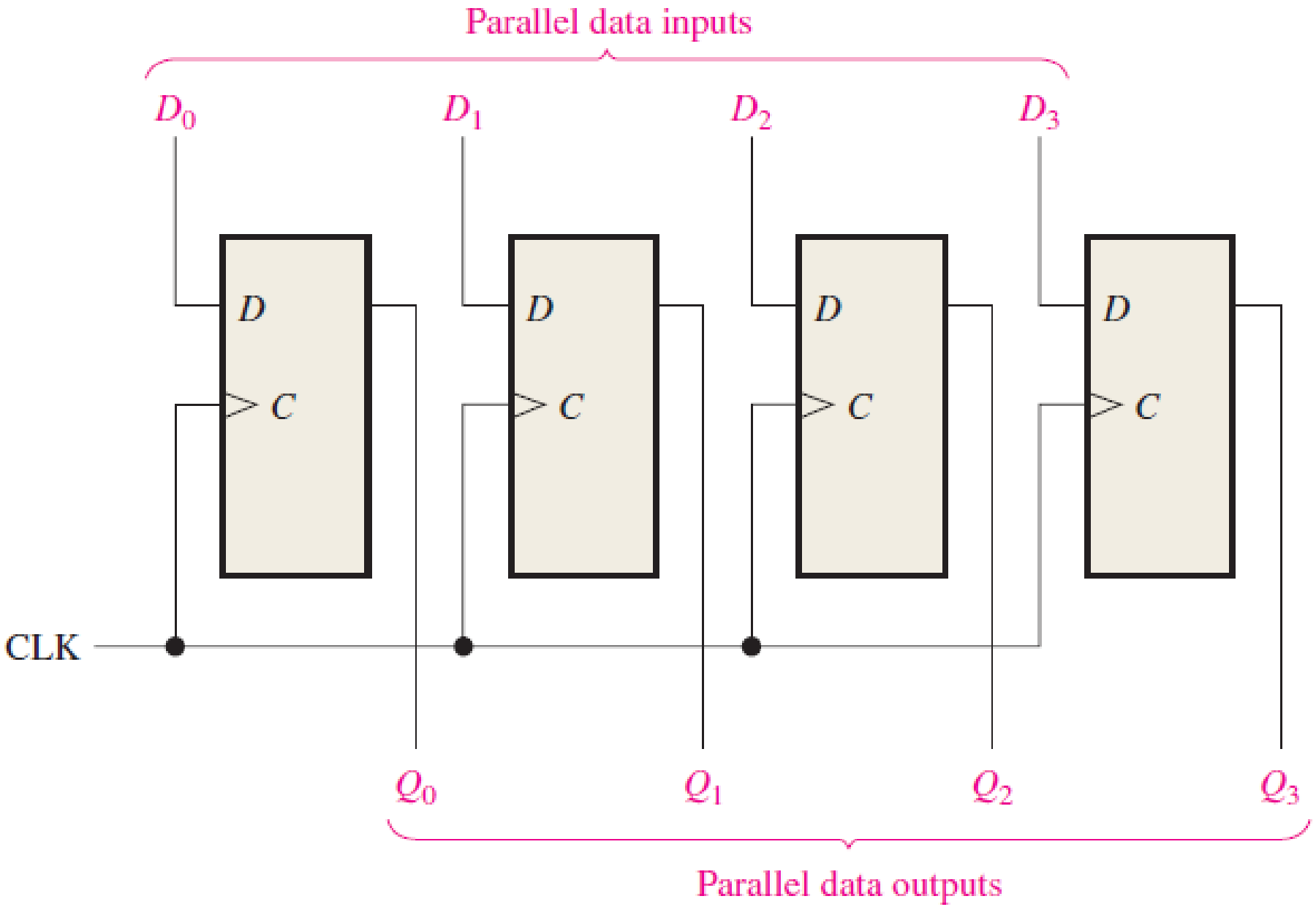




Solution:

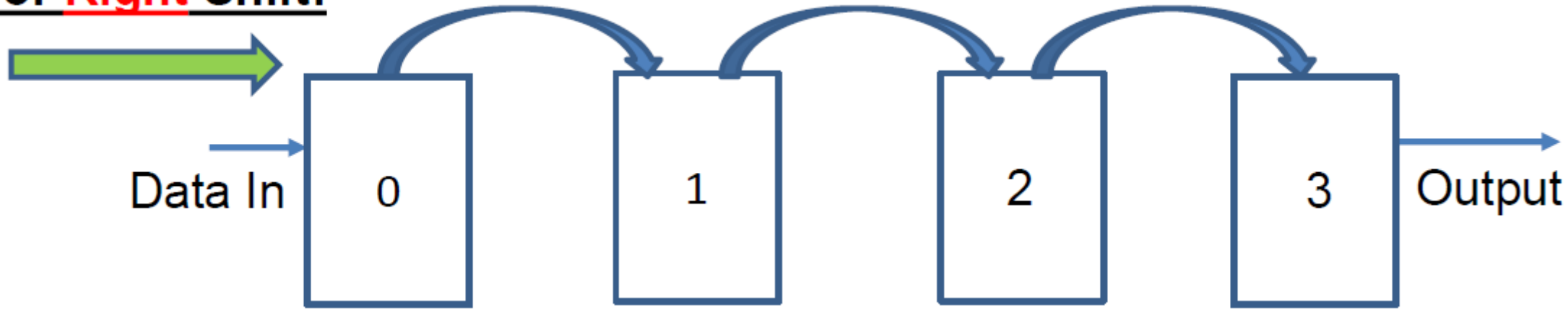
- On clock pulse 1, the parallel data ($D_0D_1D_2D_3 = 1010$) are loaded into the register making $Q_3 = 0$.
- On clock pulse 2, the 1 from Q_2 is shifted to Q_3.
- On clock pulse 3, the 0 is shifted on to Q_3.
- On clock pulse 4, the last bit 1 is shifted on to Q_3
- And on clock pulse 5, all data bits have been shifted out, and only 1 remains in the register (assuming D_0 input remains a 1)

Parallel In/ Parallel Out Shift Registers

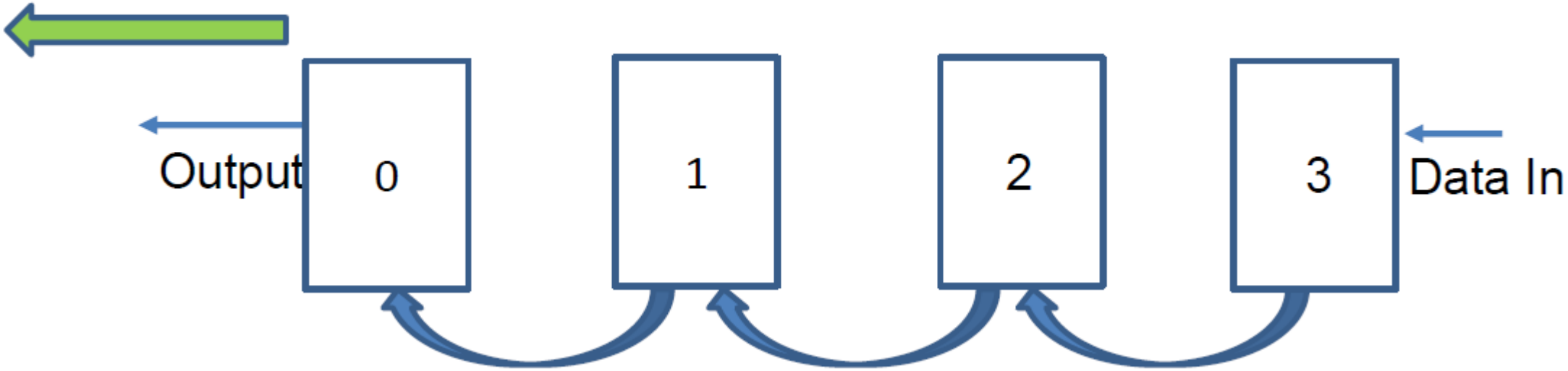


Right Left Shift Operation of SISO Shift Registers

For Right Shift:

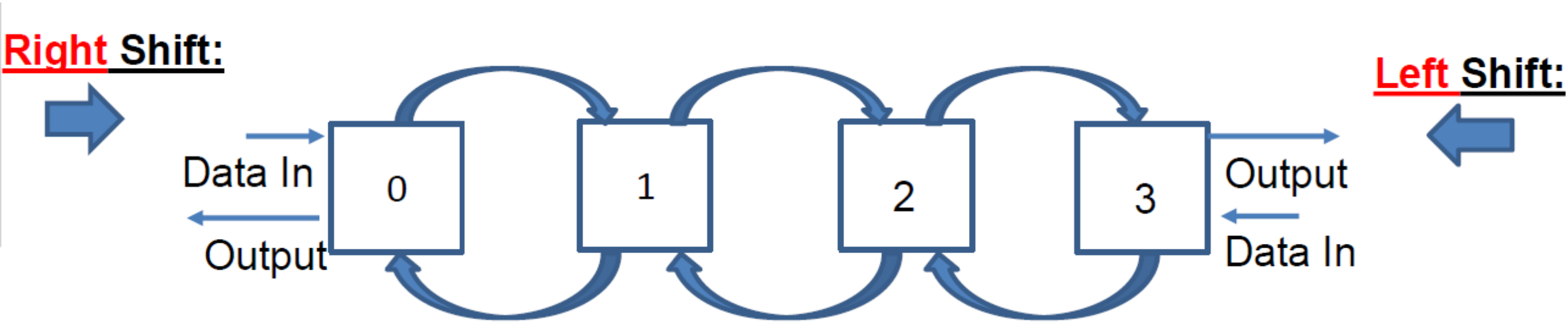


For Left Shift:

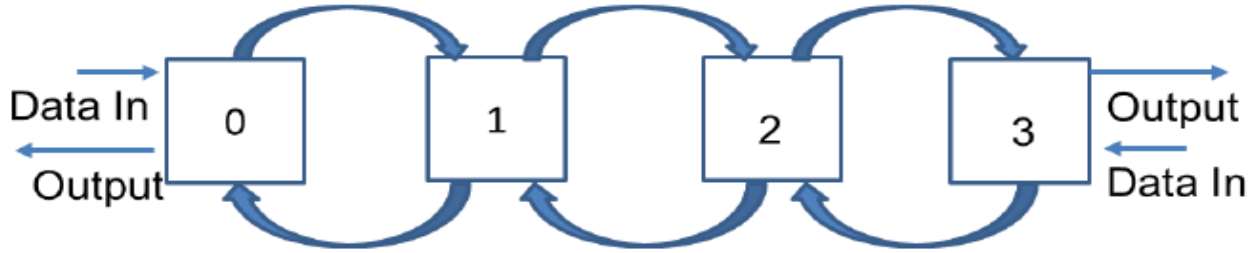


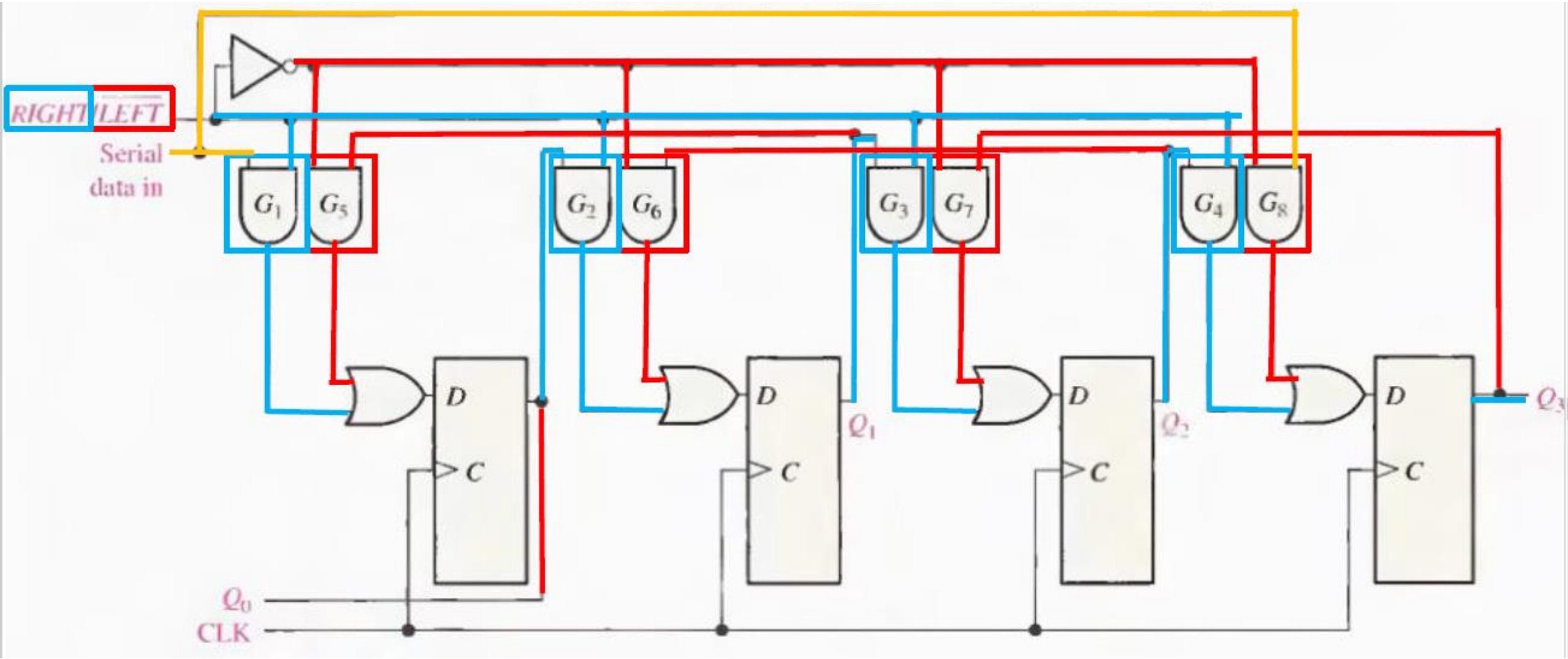
Bidirectional Shift Registers

- A bidirectional shift register is one in which data can be shifted either left or right.
- It can be implemented using gating logic.
- This is done with the help of a control input.



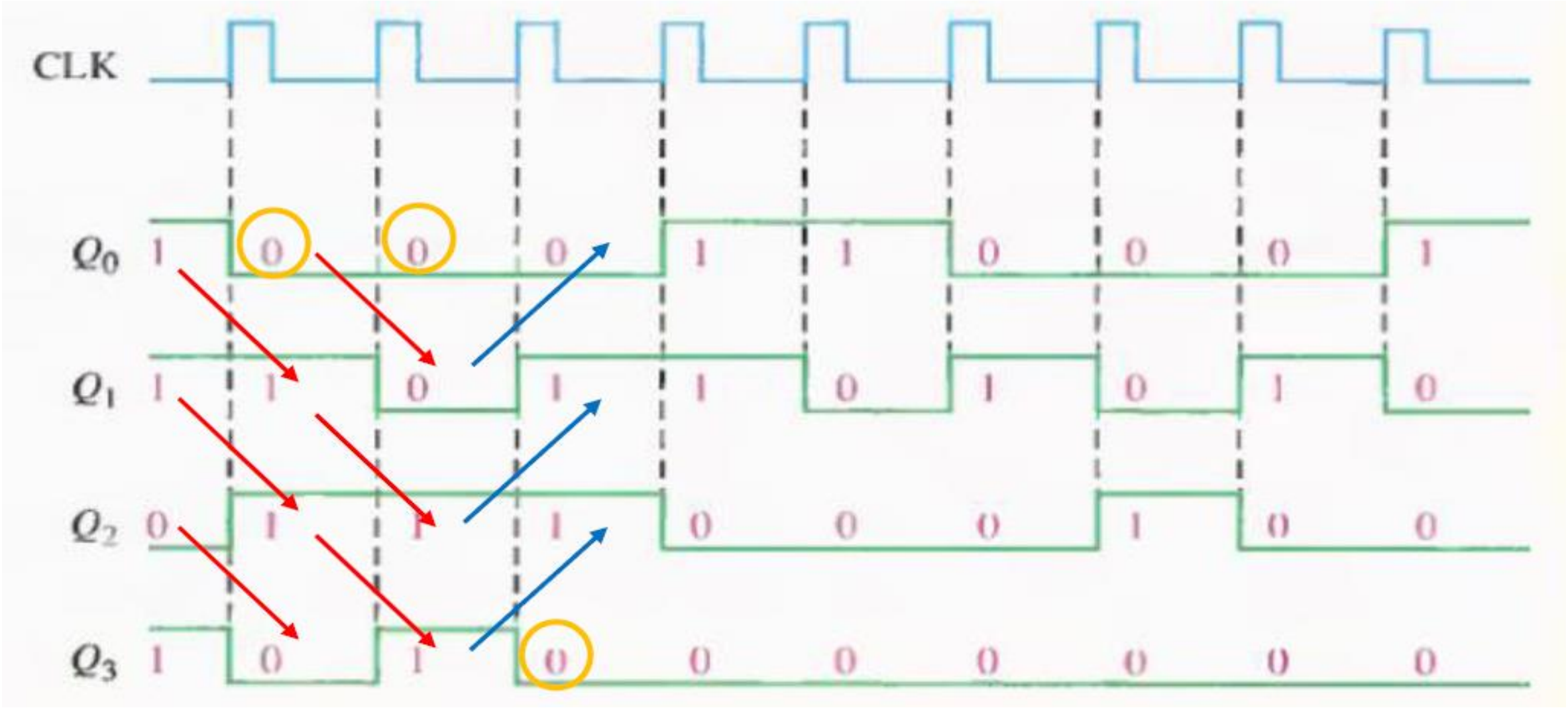
Bidirectional Shift Registers





Bidirectional Shift Registers

Determine the state of the shift register after each clock pulse for the given RIGHT/$\overline{\text{LEFT}}$ control input waveform. Assume $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 0$, and $Q_3 = 1$ and the serial data input line is LOW.



Shift Register Counters

A shift register counter is basically a shift register with the serial output connected back to the serial input to produce a special sequence. These devices are often classified as counters because they exhibit a specified sequence of states.

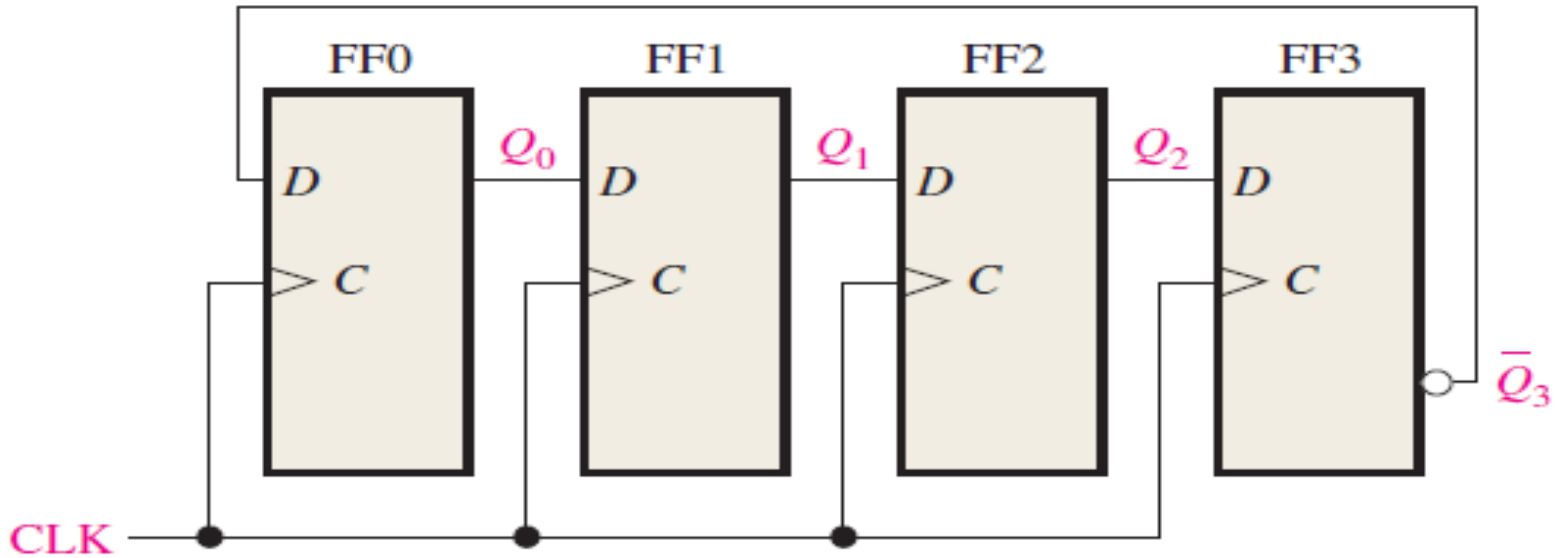
Johnson Counters

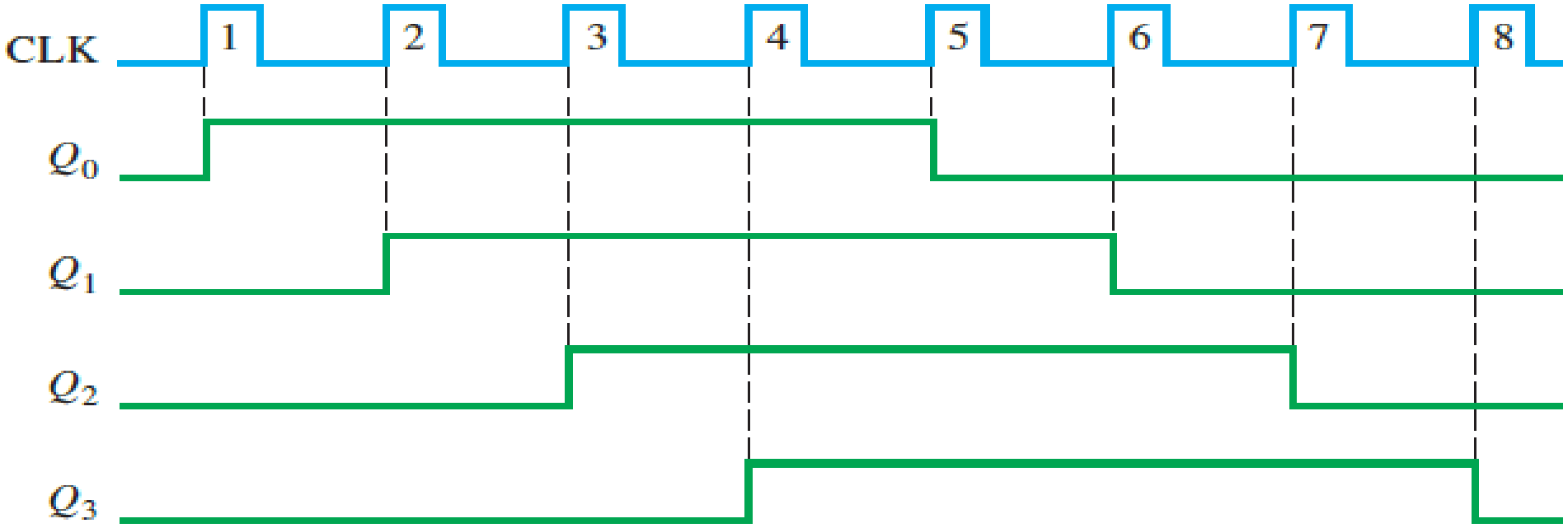
- In a Johnson counter, the complement of the output of the last flip-flop is connected back to the D input of the first flip-flop.
- This feedback produces a characteristic sequence of states.
- A Johnson counter has 2N states, if there are N flip-flops.
- That is a 4-bit sequence has 8 states and a 5-bit sequence has a total of 10 states.

Johnson Counters

Four-bit Johnson sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

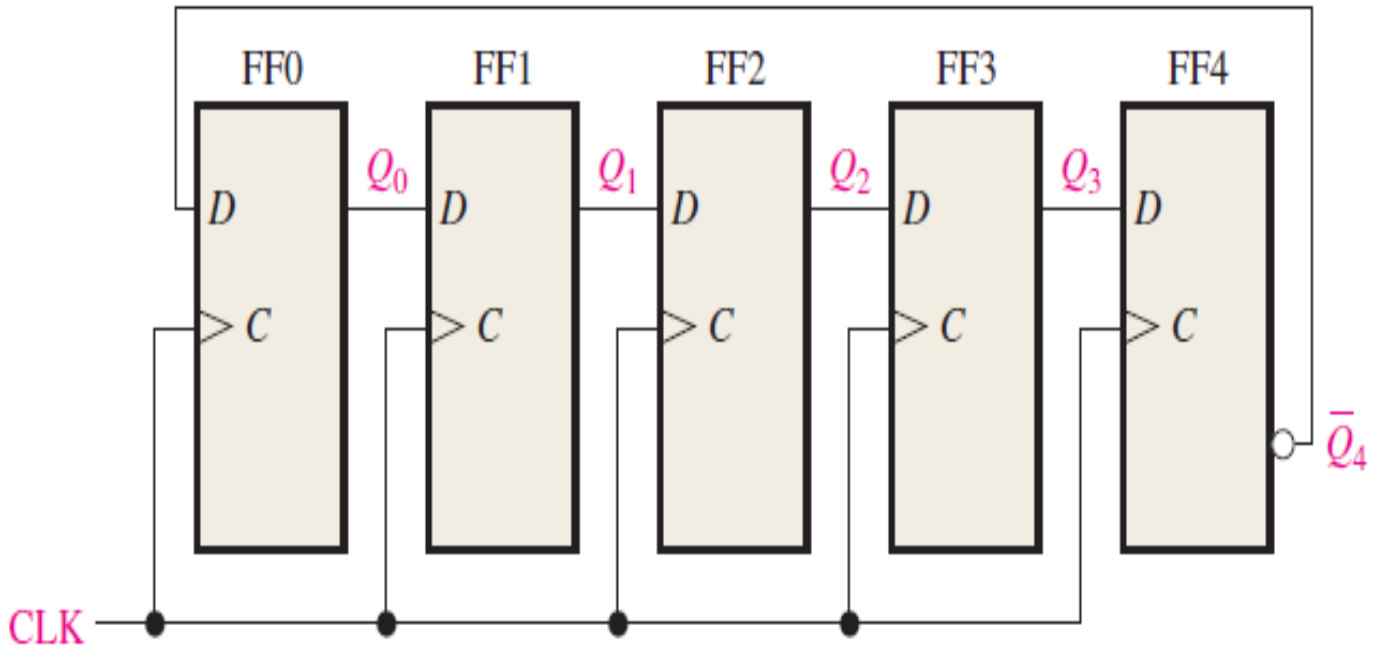


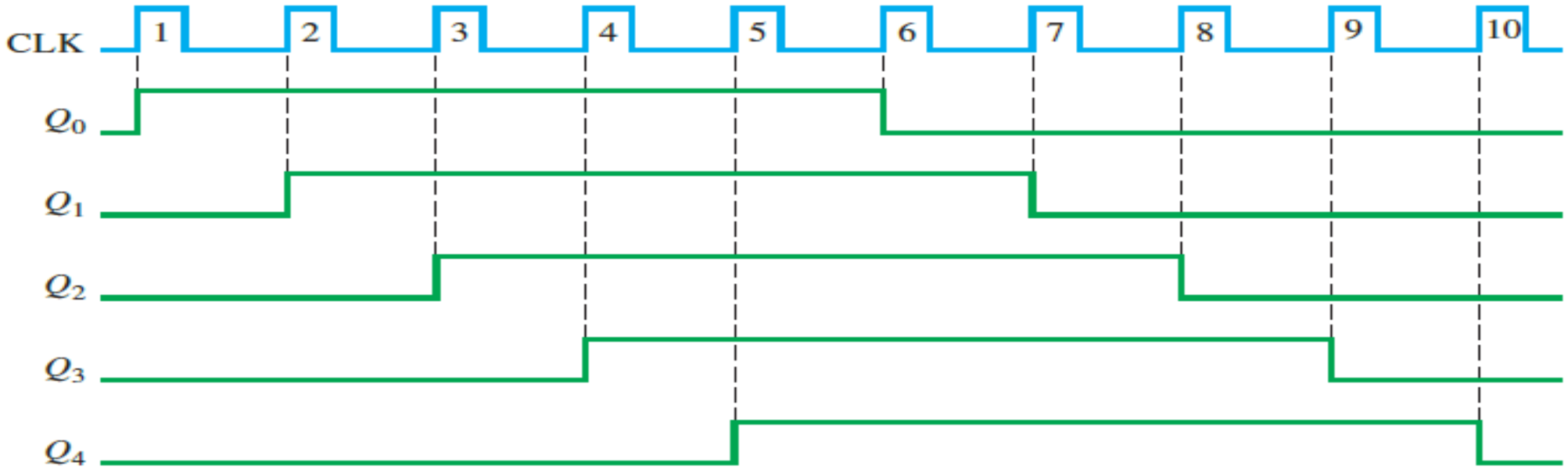


Johnson Counters

Five-bit Johnson sequence.

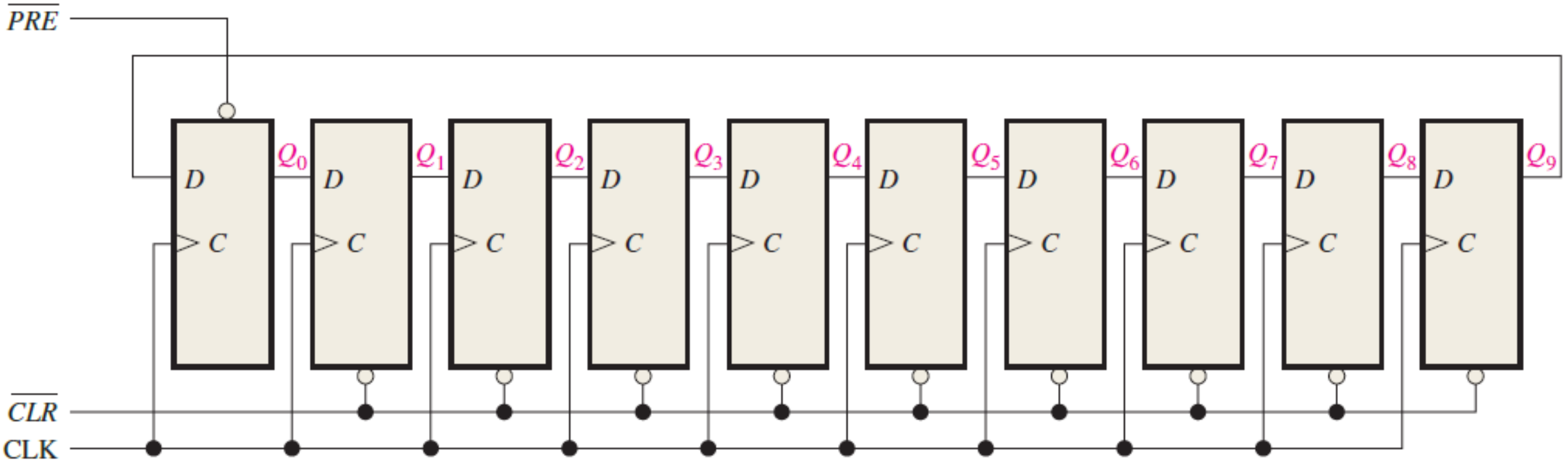
Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1





Ring Counters

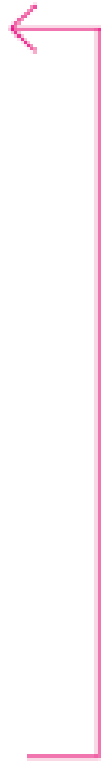
- The ring counter uses one flip-flop for one state in its sequence.
- It has an advantage that decoding gates are not required.
- In case of a 10-bit ring counter, there is an unique output for each decimal digit.



Ring Counters

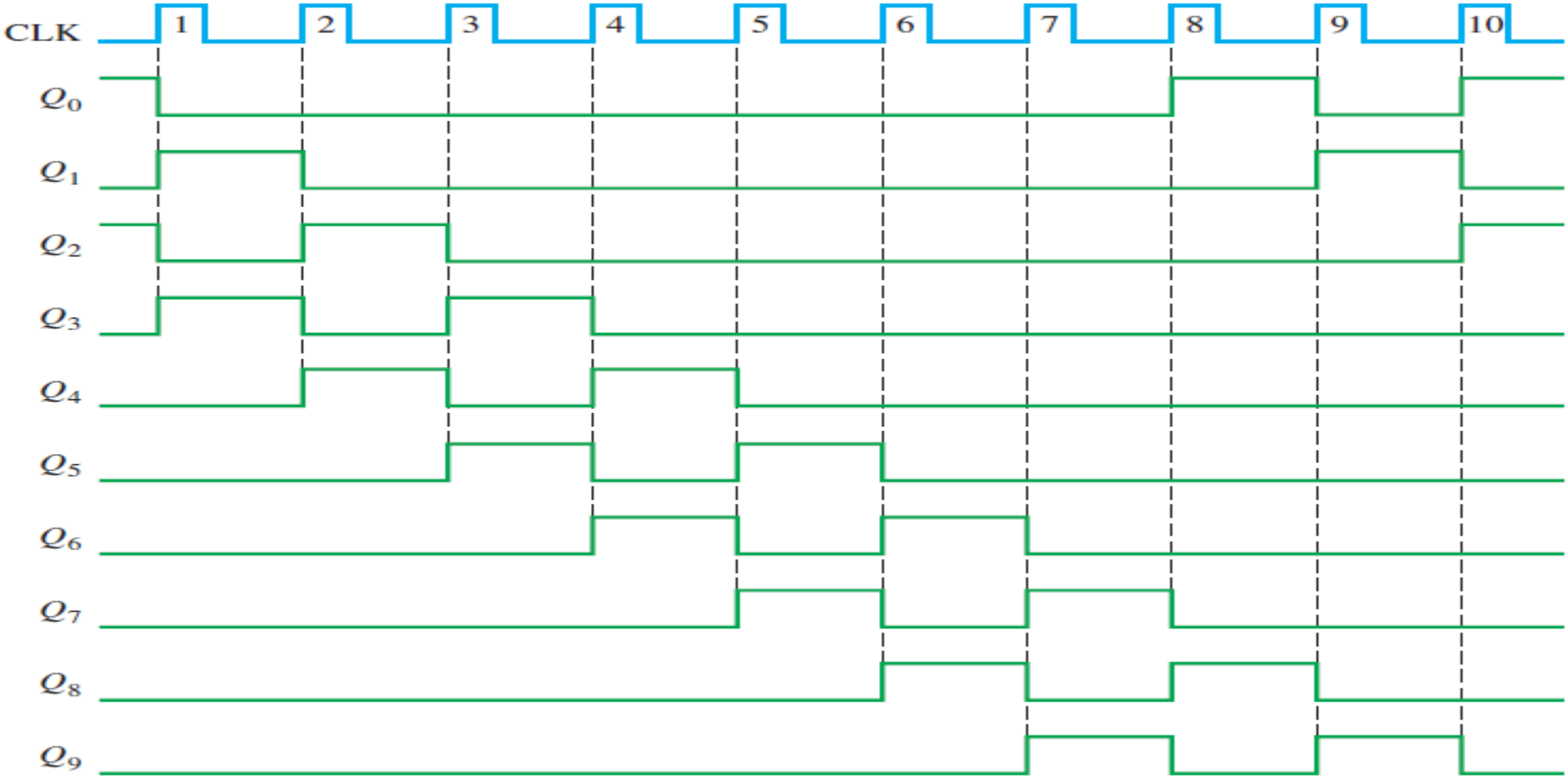
Ten-bit ring counter sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0
3	0	0	0	1	0	0	0	0	0	0
4	0	0	0	0	1	0	0	0	0	0
5	0	0	0	0	0	1	0	0	0	0
6	0	0	0	0	0	0	1	0	0	0
7	0	0	0	0	0	0	0	1	0	0
8	0	0	0	0	0	0	0	0	1	0
9	0	0	0	0	0	0	0	0	0	1



Ring Counters

If a 10-bit ring counter has an initial state of 1010000000, determine the waveform for each of the Q outputs.



References

1. Thomas L. Floyd, “Digital Fundamentals” 11th edition, Prentice Hall – Pearson Education.

Thank You