Lecture-4
Sequential Circuit Design
Memory and Storage 1

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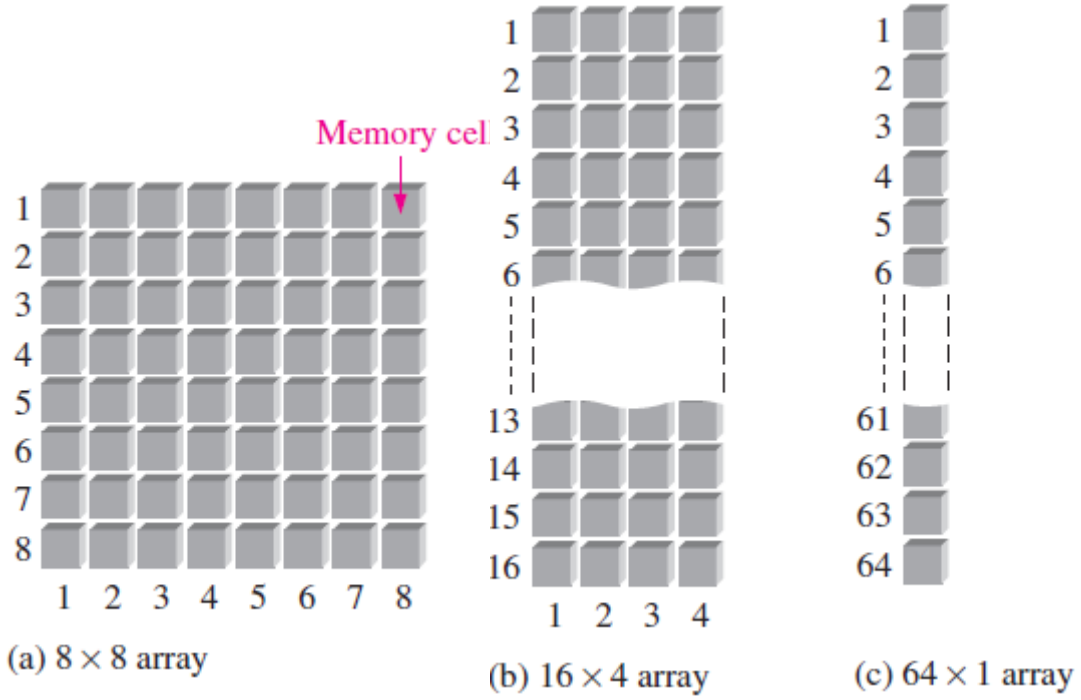
Basics of Semiconductor Memory

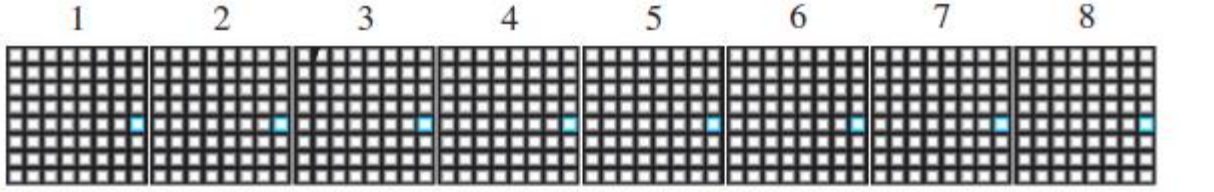
- The smallest unit of binary data is the bit.
- Data are handled in an 8-bit unit called byte.
- The byte can be split into two 4-bit unit that are called nibbles.
- A complete unit of information is called a word.
- For a 32-bit architecture, word size is 32 bit and for 64-bit architecture word size is 64 bit
- Each storage element in a memory can retain either a 1 or a 0 is called a cell.
- Memories are made up of array of cells.
- Each block in the memory array represents one storage cell.
- Its location can be identified by specifying a row and a column.



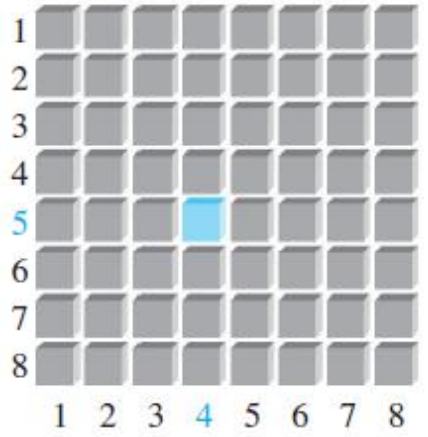
A 64-cell memory array organized in 3 different ways

Basics of Semiconductor Memory

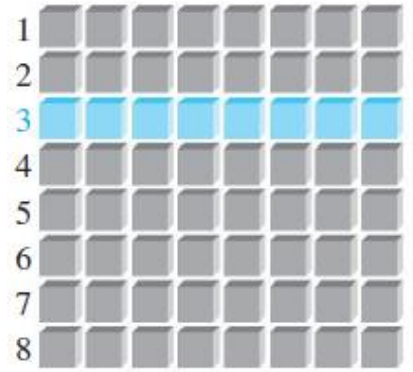
- The location of a unit of data in a memory array is called its address.
- The capacity of a memory is the total number of data units that can be stored.
- A bit in the memory as shown, can be located by the row and column.
- A byte in the memory as shown can be located by a row.
- The figure below shows a memory module of eight 8X8 bit array.
- And the address of a byte is stored in one cell of each array, that is row 5 and column 8 of each array.



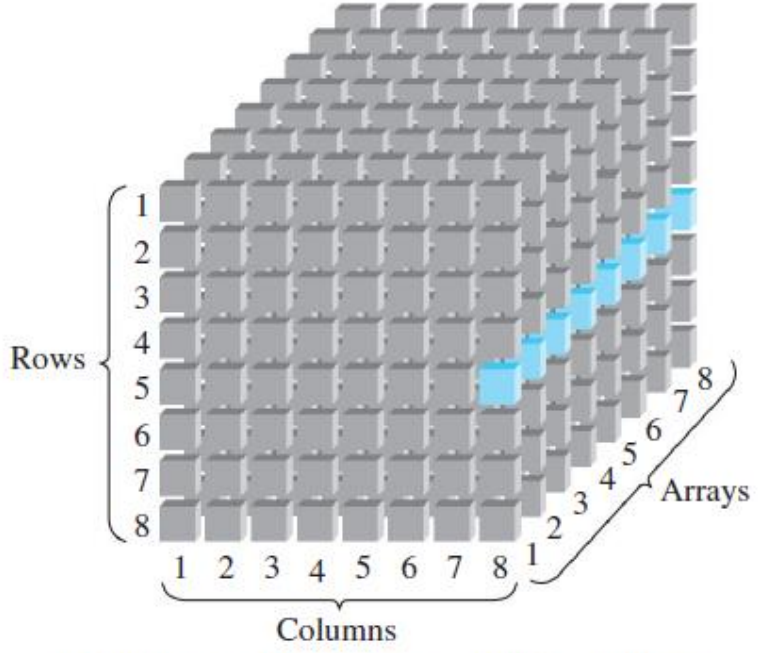
The 8 × 8 bit array expanded to a 64 × 8 bit array. This array forms a memory module.



The address of the blue bit is row 5, column 4.



The address of the blue byte is row 3.

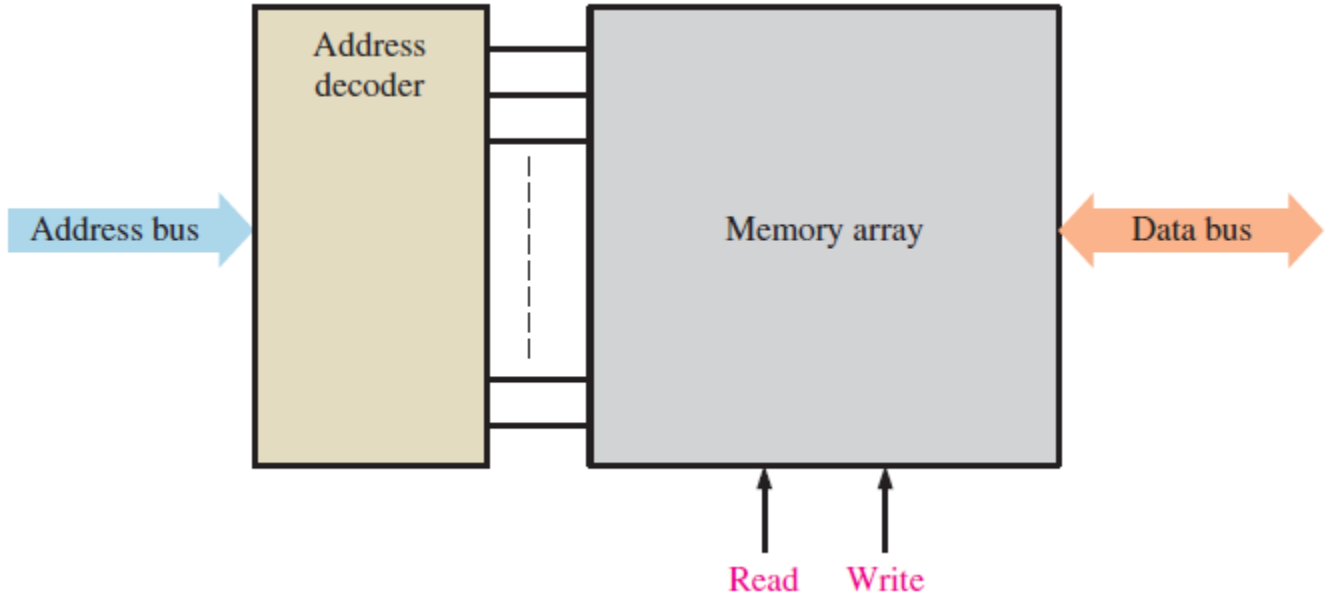


The address of the blue byte is row 5, column 8.

Basics of Semiconductor Memory

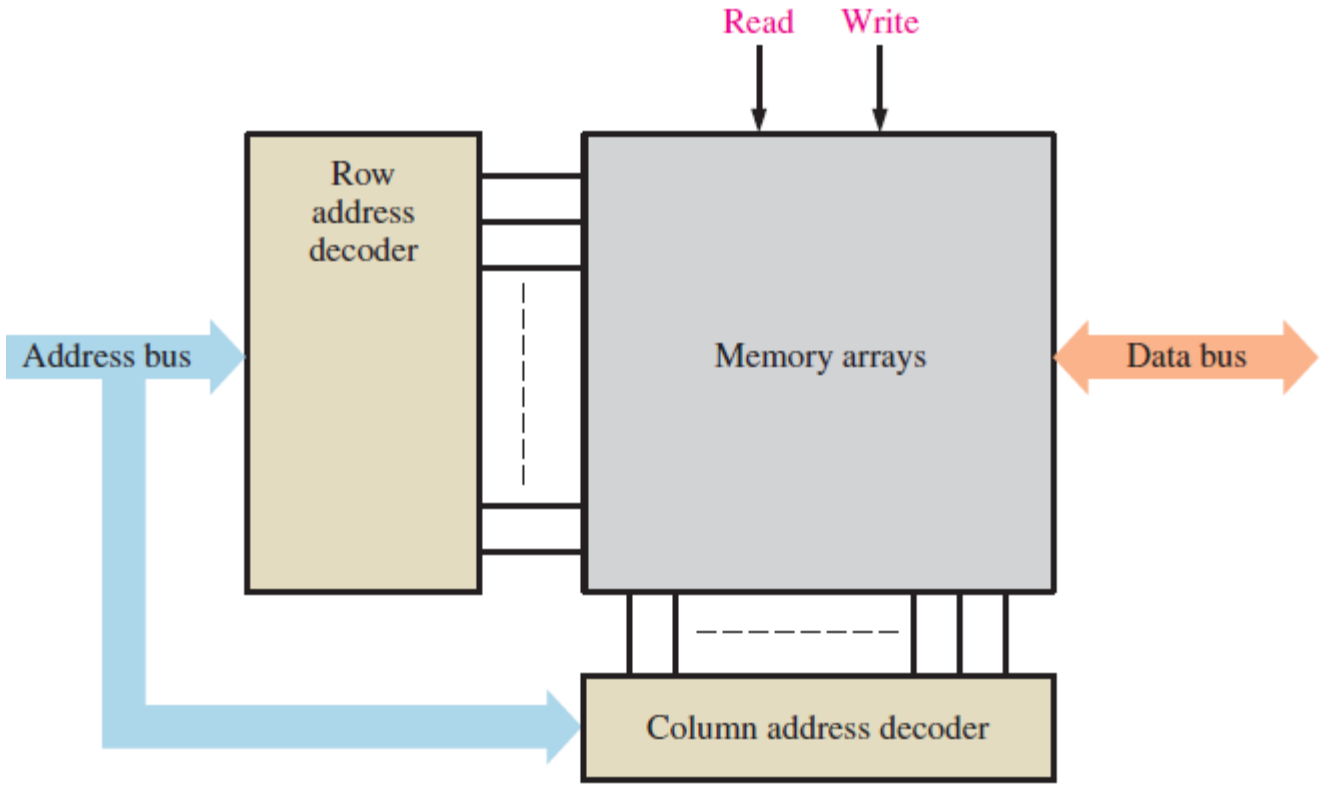
- The write operation puts data into a specified address in the memory.
- The read operation copies data out of a specified address in the memory.
- Data units go into the memory during write operation.
- Data units come of the memory during a read operation.
- The data go in and out of the memory on set of lines called data bus.
- The data bus is bidirectional, which mean that data can go in either direction.
- In case of byte-organized memories, data bus has at least eight lines so that all eight bits in a selected address are transferred in parallel.
- For a read or write operation, an address is selected by placing a binary code representing the desired address on a set of lines called the address bus.

Basics of Semiconductor Memory



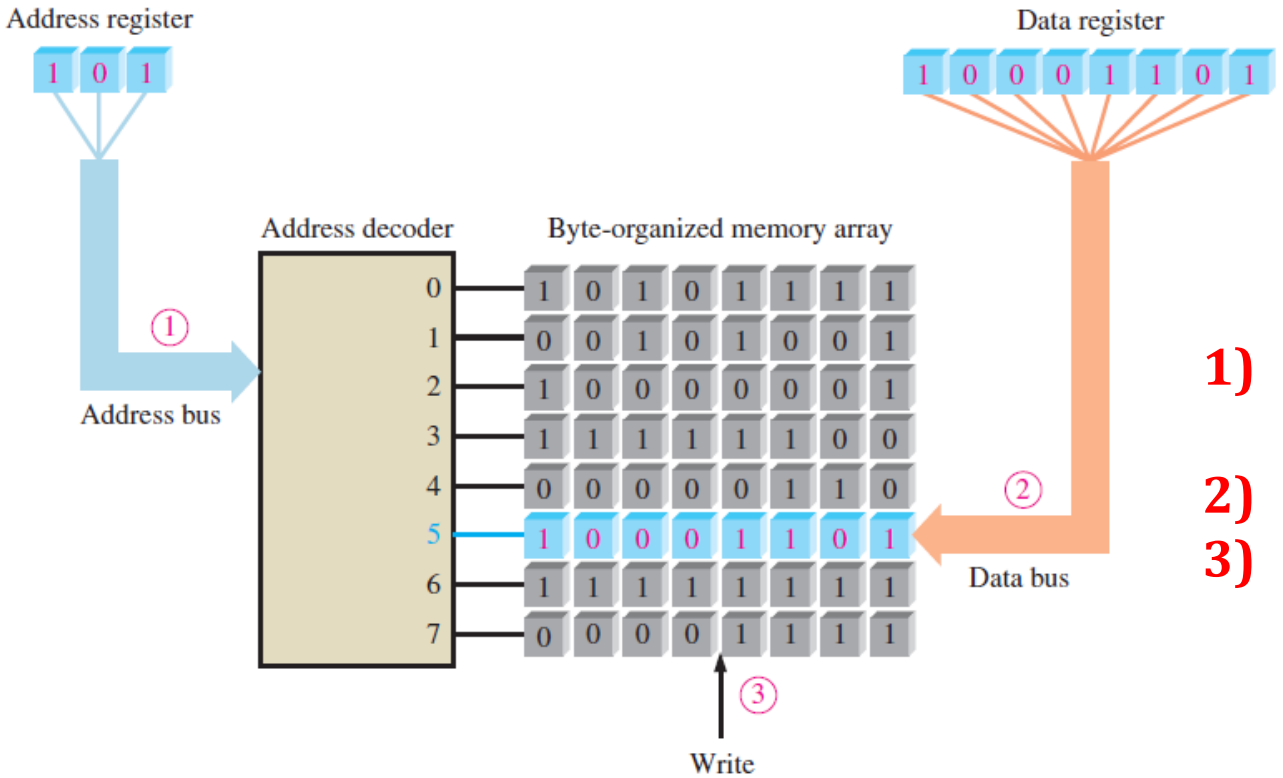
Block diagram of a single-array memory showing address bus, address decoded, bidirectional data bus and read/write inputs

Block diagram of a multiple-array memory showing address bus, address decoded, bidirectional data bus and read/write inputs



Write Operation

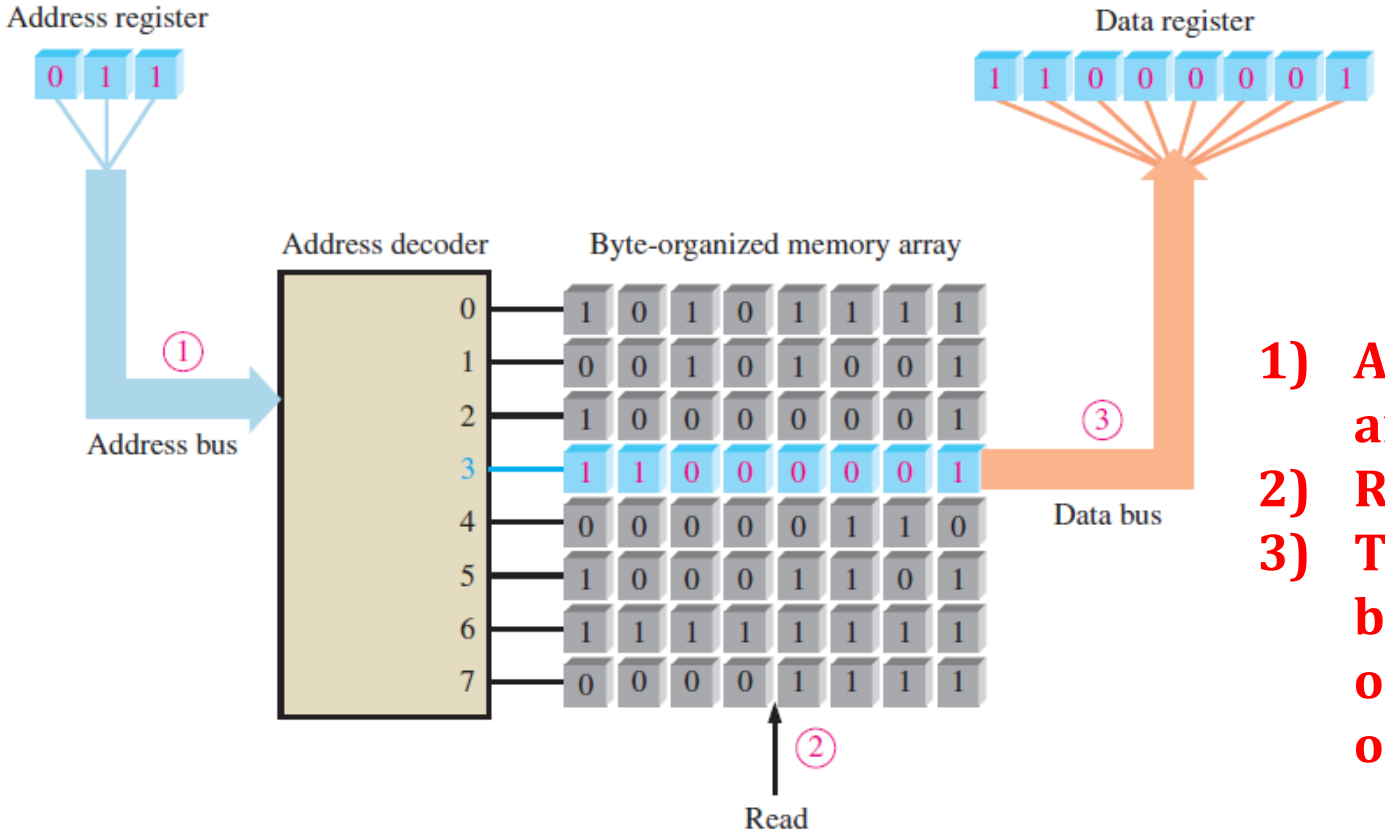
- To store a byte of data in the memory, a code held in the address register is placed on the address bus.
- Once the address code is on the bus, the address decoded decodes the address and selects the specified location in the memory.
- The memory then gets a write command, and the data byte in the data register is placed on the data bus and stored in the selected memory address, thus completing the write operation.
- When a new data byte is written into a memory address, the current data byte stored at that address is overwritten



1) **Address code 101 is placed on the address bus and address 5 is selected.**
2) **Data byte is placed on the data bus.**
3) **Write command causes the data byte to be stored in address 5, replacing previous data.**

Read Operation

- A code held in the address register is placed on the address bus.
- Once the address code is on the bus, the address decoder decodes the address and selects the specified location in the memory.
- Then memory then gets a read command and “copy” of the data byte is stored in the selected memory address is placed on the data bus and loaded into the data register, thus completing the read operation.
- When a data byte is read from a memory address, it also remains stored at that address. This is called nondestructive read.



1) **Address code 011 is placed on the address bus and address 3 is selected.**
2) **Read command is applied.**
3) **The content of address 3 is placed on the data bust and shifted into data register. The content of address 3 is not erased by the read operation.**

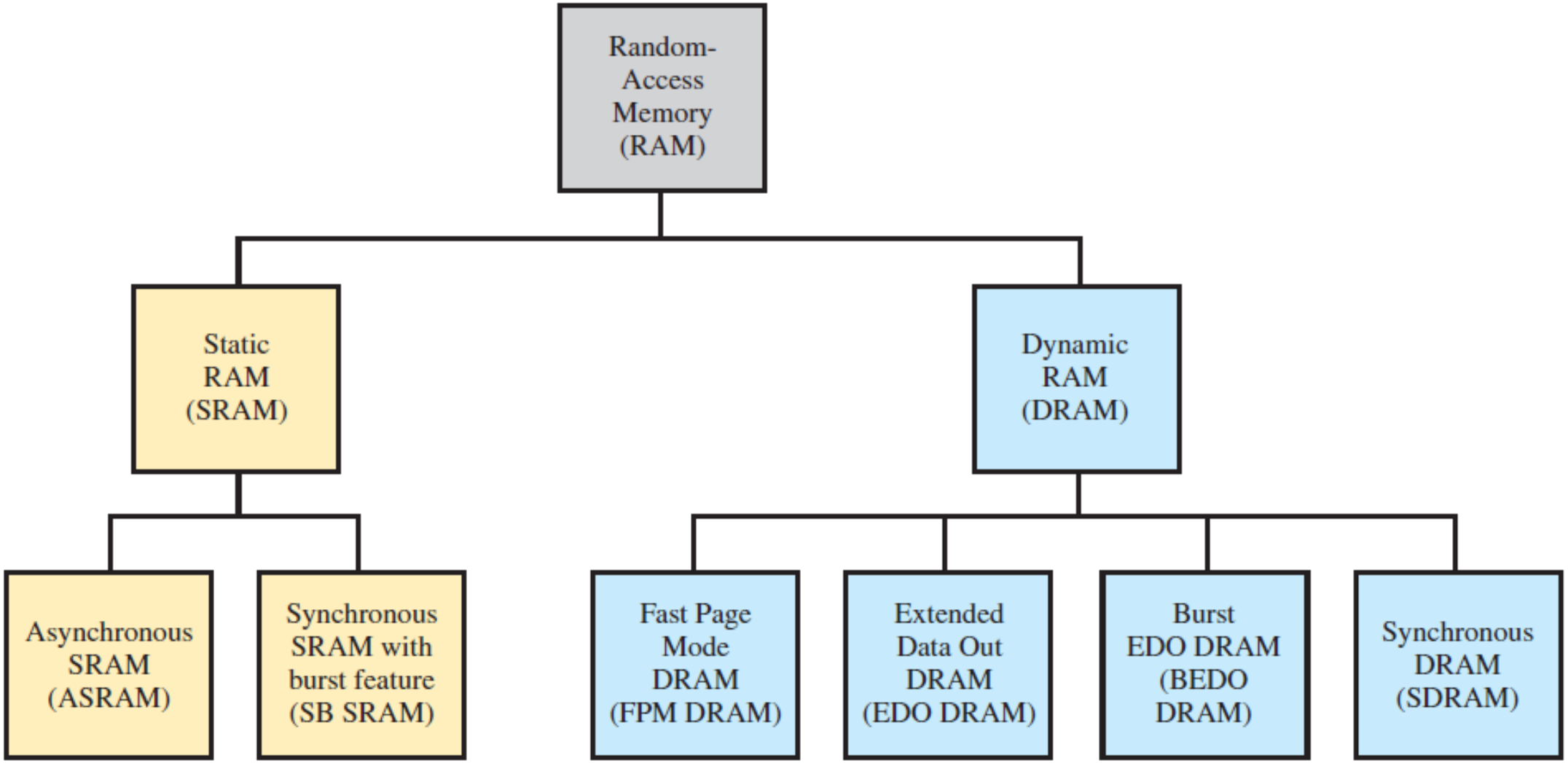
RAMs and ROMs

- The two major categories of semiconductor memories are the RAM and ROM
- RAM stands for Random Access Memory.
- It is a type of memory in which all addresses are accessible in equal amount of time and can be selected in any order for a read or write operation.
- Therefore it is called random accessed memory.
- All RAMs have both read and write capability.
- Because RAMs lose stored data when the power is turned off, they are called volatile memories.
- ROM stands for Read Only Memory.
- It is where data are stored permanently or semi-permanently.
- Data can be read from a ROM, but there is no write operation as in RAM.
- The ROM, like the RAM, is a random-access memory but the term RAM traditionally means Random-Access Read/Write Memory.
- Because ROMs retain stored data even if power is turned off, they are nonvolatile memory.

Random Access Memory (RAM)

- RAMs are read memories in which data can be written into or read from any selected address in any sequence
- When a data unit is written into a given address in the RAM, the data unit previously stored at that address is replaced by the new data unit.
- When a data unit is read from a given address in the RAM, the data unit remains stored and is not erased by the read operation.
- This non-destructive read operation can be viewed as copying the content of an address while leaving the content intact.
- A RAM is typically used for short-term data storage because it cannot retain stored data when power is turned off.
- There are basically two categories of RAMs: SRAM and DRAM
- SRAM stands for Static RAM
- DRAM stands for Dynamic RAM.
- Both the type of RAMs are volatile memories, so they will loose data once power is removed.

Random Access Memory (RAM)



The RAM Family

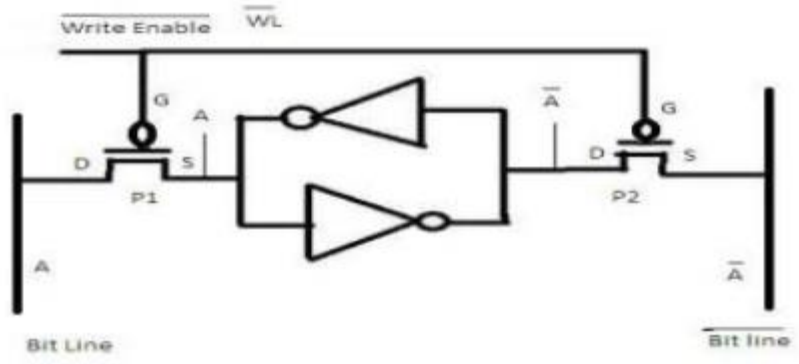
Random Access Memory (RAM)

Comparison between SRAM and DRAM:

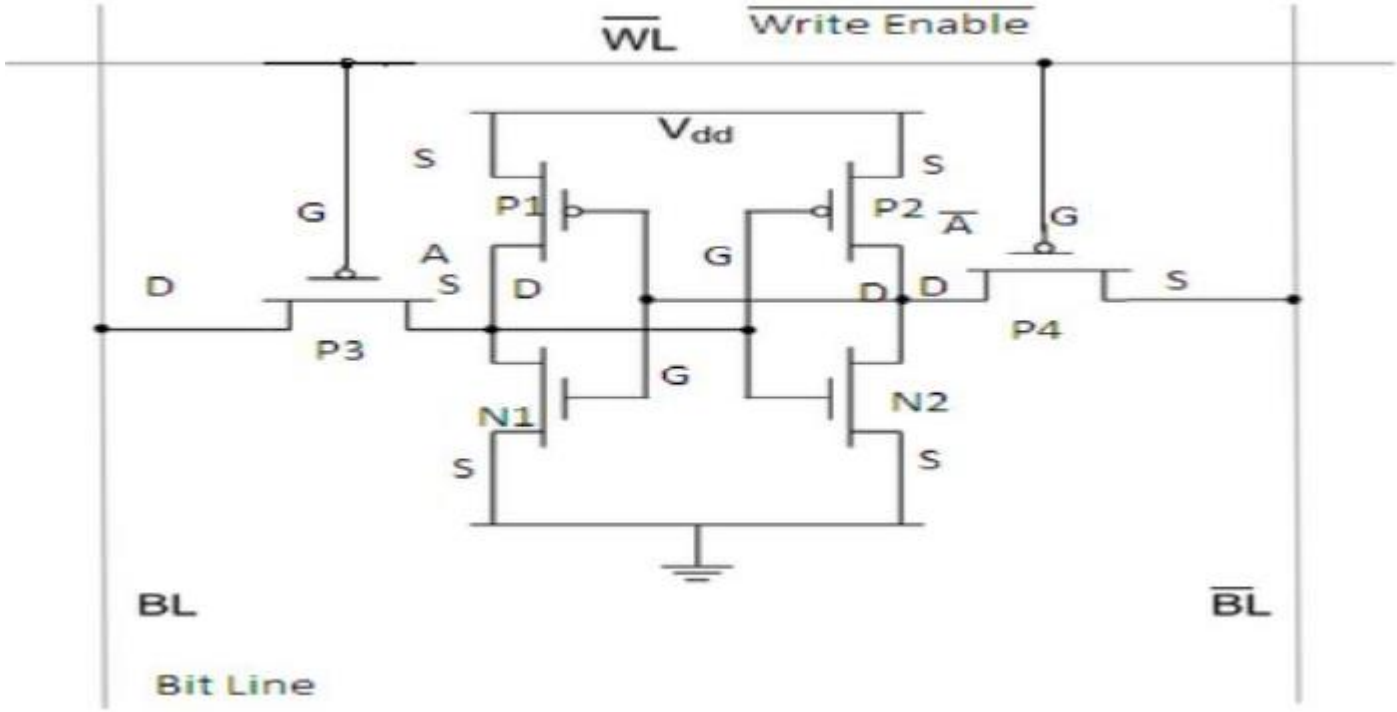
1. SRAM generally uses Latches as storage elements	1. DRAM generally uses capacitors as storage elements.
2. Therefore, can store data indefinitely as long as power is applied.	2. Therefore, cannot retain data very long without the capacitors being refreshed.
3. SRAMs are faster.	3. DRAMs are slower.
4. For a given physical size and cost SRAMs can store less data than	4. For a given physical size and cost DRAMs can store much more data.
5. SRAM cell is complex.	5. DRAM cell is much simpler.
6. For a given physical size, less number cells can be crammed in the space.	6. For a given physical size, a greater number of cells can be crammed in the space

Static Random-Access Memory (SRAM)

- All static RAM are characterized by latch memory cells.
- As long as dc power is applied to a static memory cell, it can retain a 1 or 0 indefinitely.
- If power is removed, the stored data bit is lost.
- Flip-flop storage cell are typically implemented in integrated circuits with several MOS transistors.



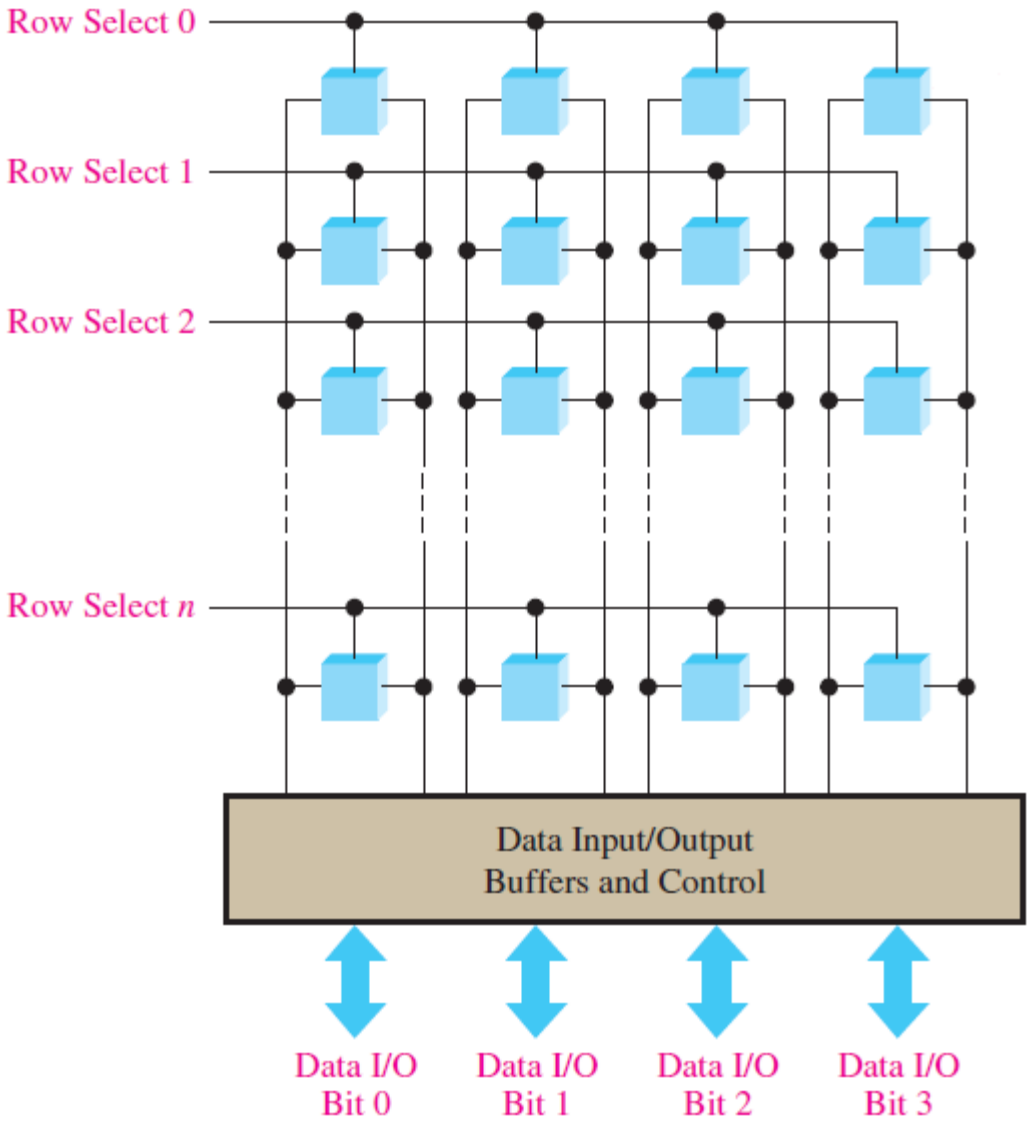
SRAM cell with inverter latch



A 6-T SRAM cell

Static Random-Access Memory (SRAM)

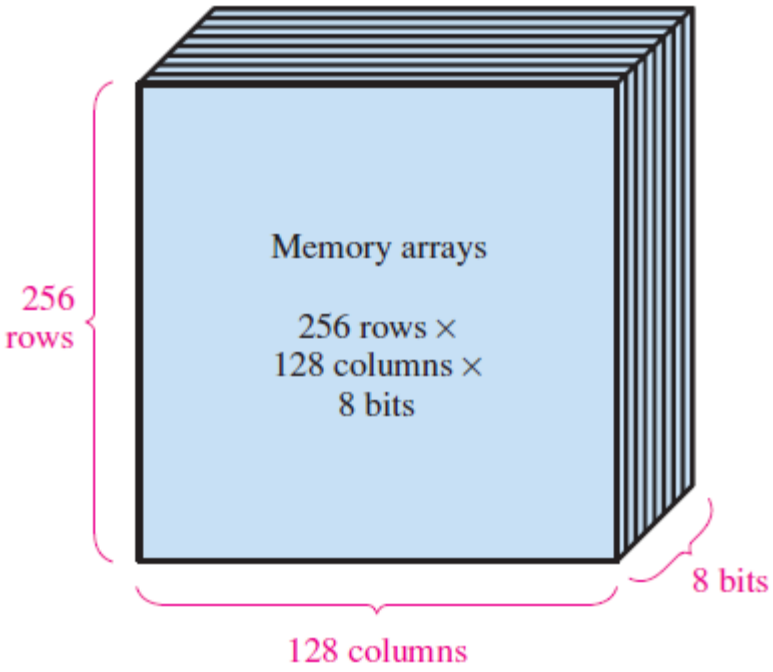
- The cell is selected by an active level on the bit select line.
- Data is written into the cell by placing it on the data in & data out lines.
- A data is read by taking it off data in & data out lines.
- To write a data unit, here nibble, into a given row of cells in the memory array, the corresponding ROW Select line is activated
- Then the four data bits are placed in the data I/O lines.
- The write line is then activated which stores each data bit in a selected cell of associated column.
- To read a data unit, the Read line is activated.
- This causes 4 data bits stored in the selected row to appear on the I/O lines



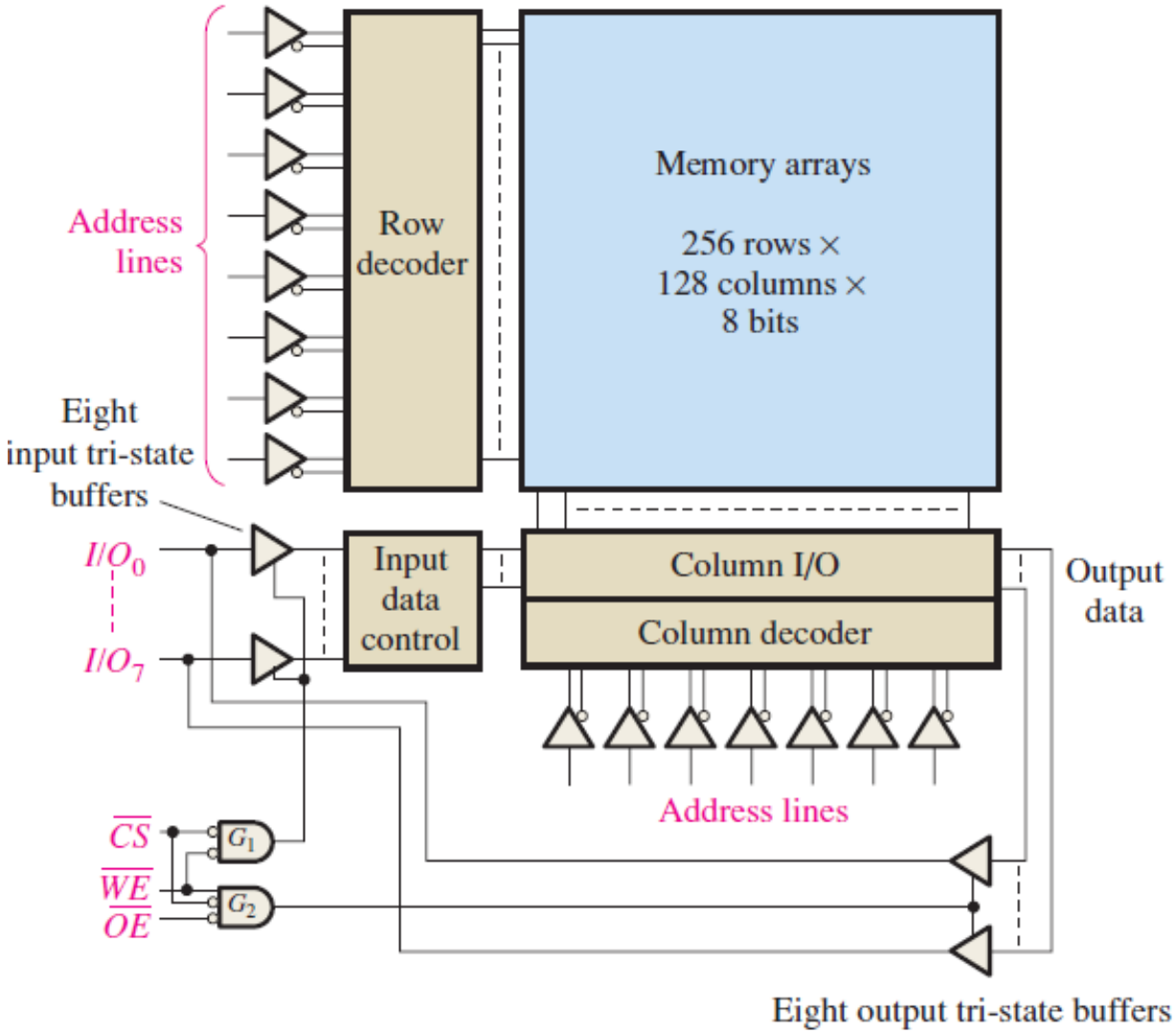
Basic SRAM array

Static Random-Access Memory (SRAM)

Basic organization of an asynchronous 32K X 8 SRAM



Memory array configuration



Memory Block Diagram

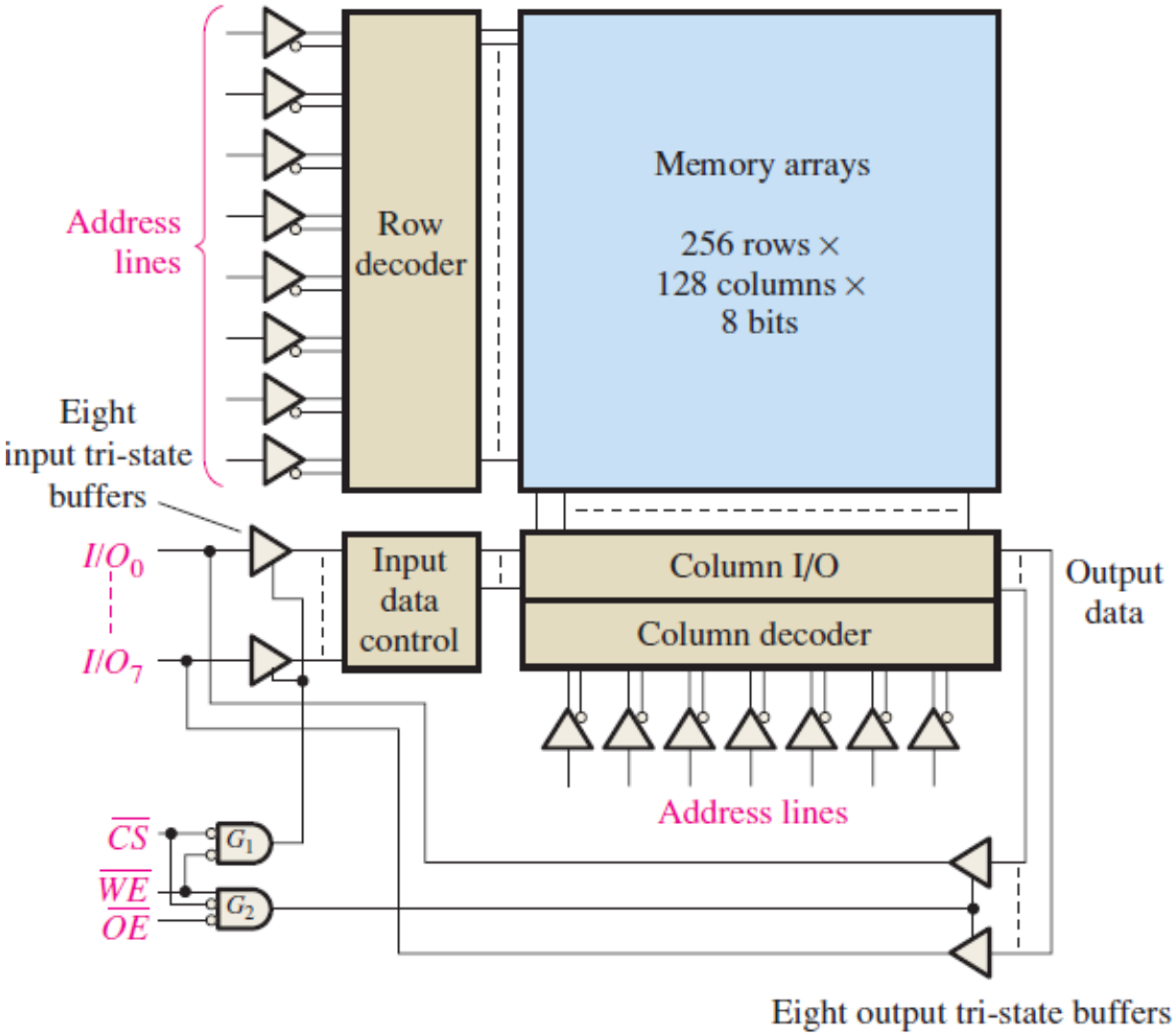
Static Random-Access Memory (SRAM)

Read Operation

- $\overline{CS} = 0, \overline{OE} = 0(LOW), \overline{WE} = 1(HIGH)$
- Input buffers are disabled by G1.
- Column output buffers are enabled by G2.
- Eight Data bits from the selected address sequence are routed through the column i/p to the data lines which are acting as data output lines.

Write Operation

- $\overline{CS} = 0, \overline{OE} = 1(HIGH), \overline{WE} = 0(LOW)$
- Input buffers are enabled by G1.
- Column output buffers are disabled by G2.
- Eight input data bits on the data lines are routed through the input data control and column I/O to the selected address and stored.



References

1. Thomas L. Floyd, “Digital Fundamentals” 11th edition, Prentice Hall – Pearson Education.

Thank You