Lecture -5
Sequential Circuit Design: Memory and Storage 2

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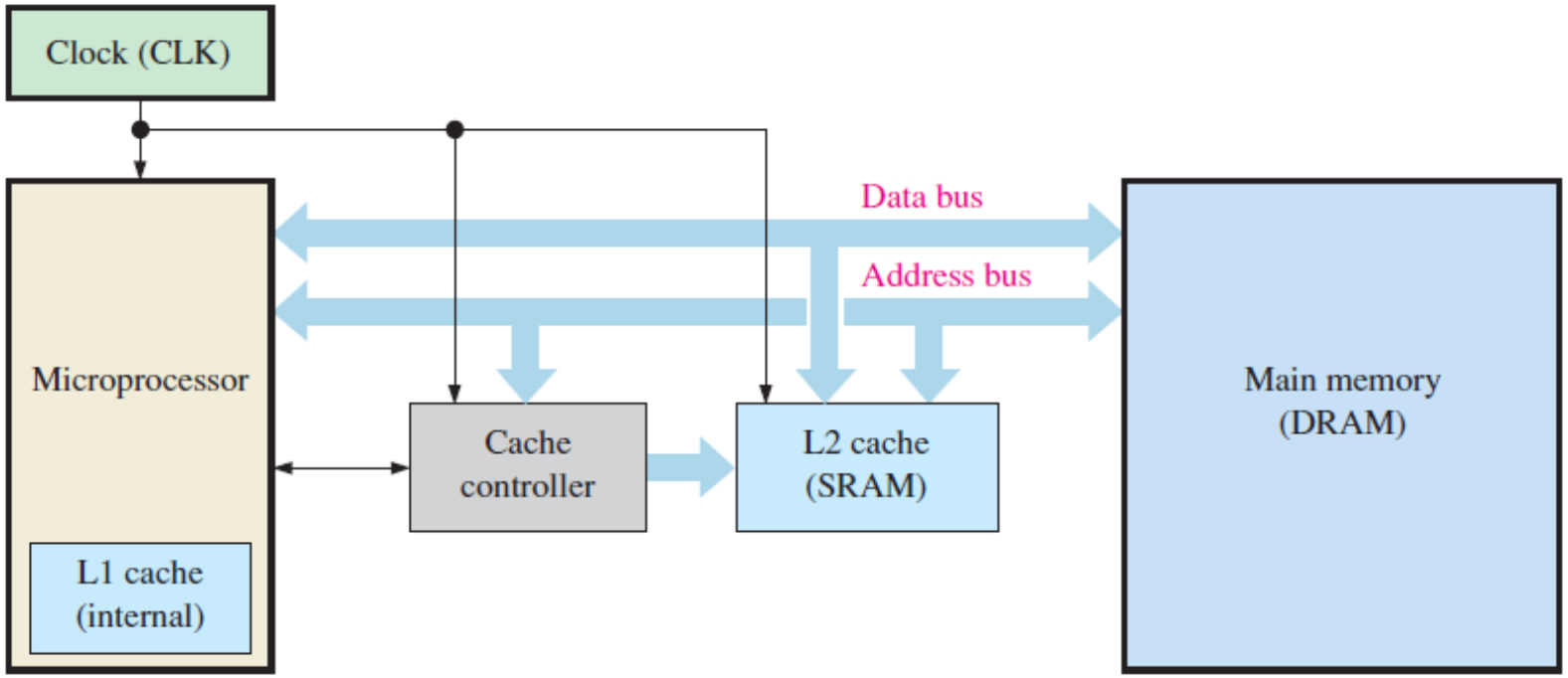
Cache Memory

- One of the major applications of SRAM is the cache memories in computers.
- Cache memory is a relatively small, high-speed memory that stores the most recently used instructions or data from the larger but slower main memory.
- Cache memory uses SRAM technology as it is faster.
- However, SRAM is faster but more expensive where as, DRAM is slower but cheaper.
- It is a cost-effective method of improving system performance without having to resort to the expense of making the overall memory faster.



Block Diagram of cache memory in a computer system

Cache Memory

- The operation of cache memory is analogous to the refrigerator at our home.
- We can get all what we need from the supermarket, however, we store the most necessary items in our refrigerator to save time.
- So every time we need something, we first look at our refrigerator, if it is there, we save a lot of time.
- Commonly there are two levels of cache: L1 and L2
- L1 is the first level cache and is usually integrated in the microprocessor.
- It has a very limited storage capacity.
- L1 is also known as primary cache.
- L2 cache is a separate memory chip or set of chips external to the processor.
- L2 cache usually has a larger storage capacity than L1 cache.
- L2 cache is also known as secondary cache.
- It should be noted that some systems also have higher level of cache L3 and L4

Dynamic Random-Access Memory

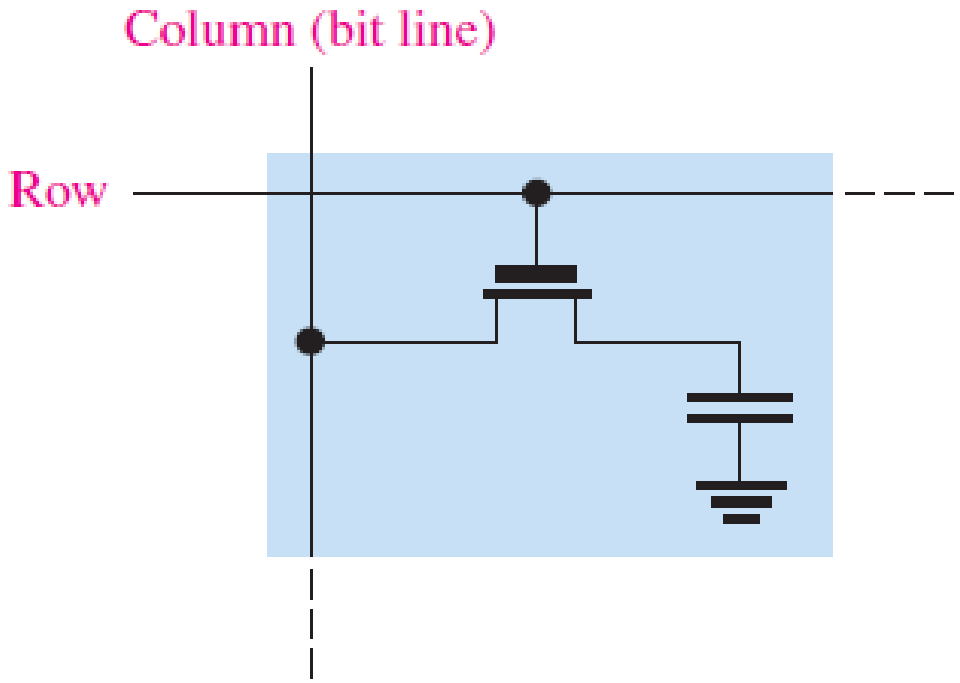
- Dynamic memory cells sore a data bit in a capacitor rather than a latch or flip-flop.
- Each cell consists of only one transistor and a capacitor.
- It is much simpler than the SRAM cell.
- It allows very large memory arrays to be constructed on a chip at a lower cost per bit than in a SRAM.

Disadvantages of DRAM

- The storage capacitors can not hold its charge over an extended period of time and lose the stored data bit unless its charge is refreshed periodically.
- To refresh it requires additional circuit and thus complicates the operation of DRAM

Dynamic Random-Access Memory

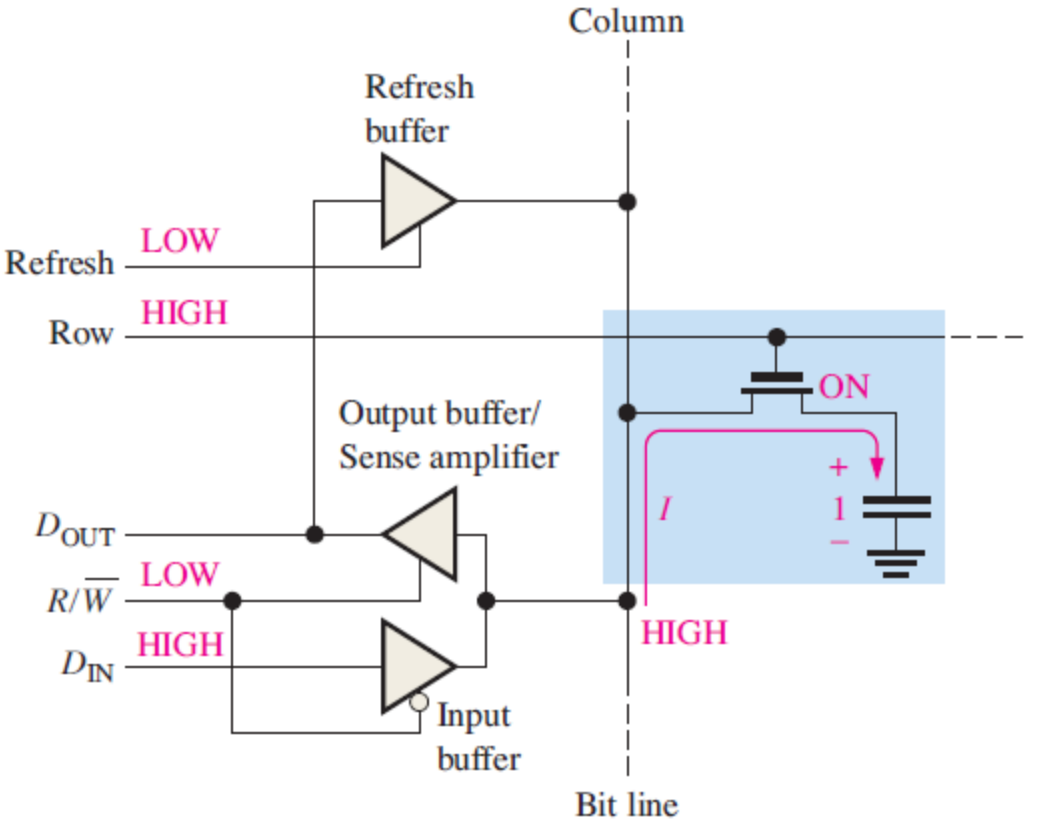
- The figure shows a DRAM cell.
- The transistor acts as a switch.
- The capacitor stores the charge.
- The row line is connected to the gate of the transistor.
- The column line is the bit line.
- When the transistor is on, the capacitor is connected to the bit line.
- Depending on the value of the capacitor and bit line the capacitor either charges or discharges.



Basic Operation of DRAM

Storing a 1 into the memory cell:

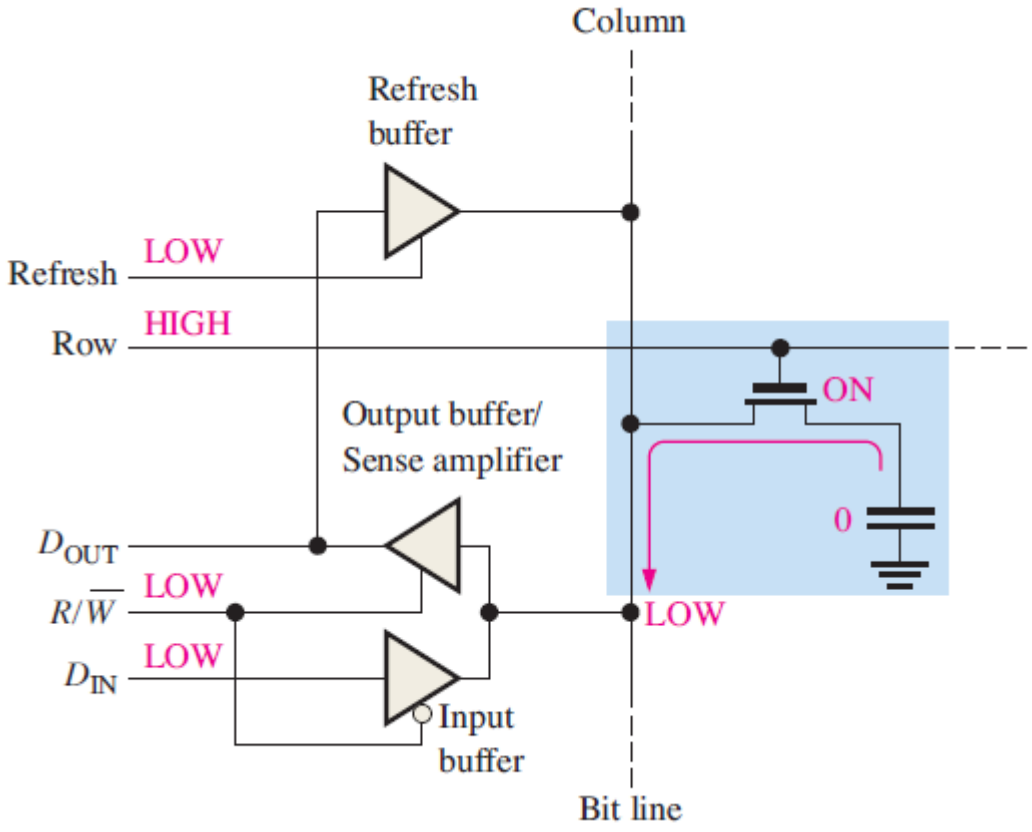
- A LOW on the R/$\overline{W}$ line enables the tri-state input buffer and disables the output buffer.
- For a 1 to be written D_{IN} is HIGH.
- The Row line is turned HIGH to turn on the transistor.
- Thus the bit line is connected to the capacitor.
- And the capacitor is charged to store 1.
- Then when the Row line is turned LOW the transistor is OFF.
- And the charge gets trapped in the capacitor.



Basic Operation of DRAM

Storing a 0 into the memory cell:

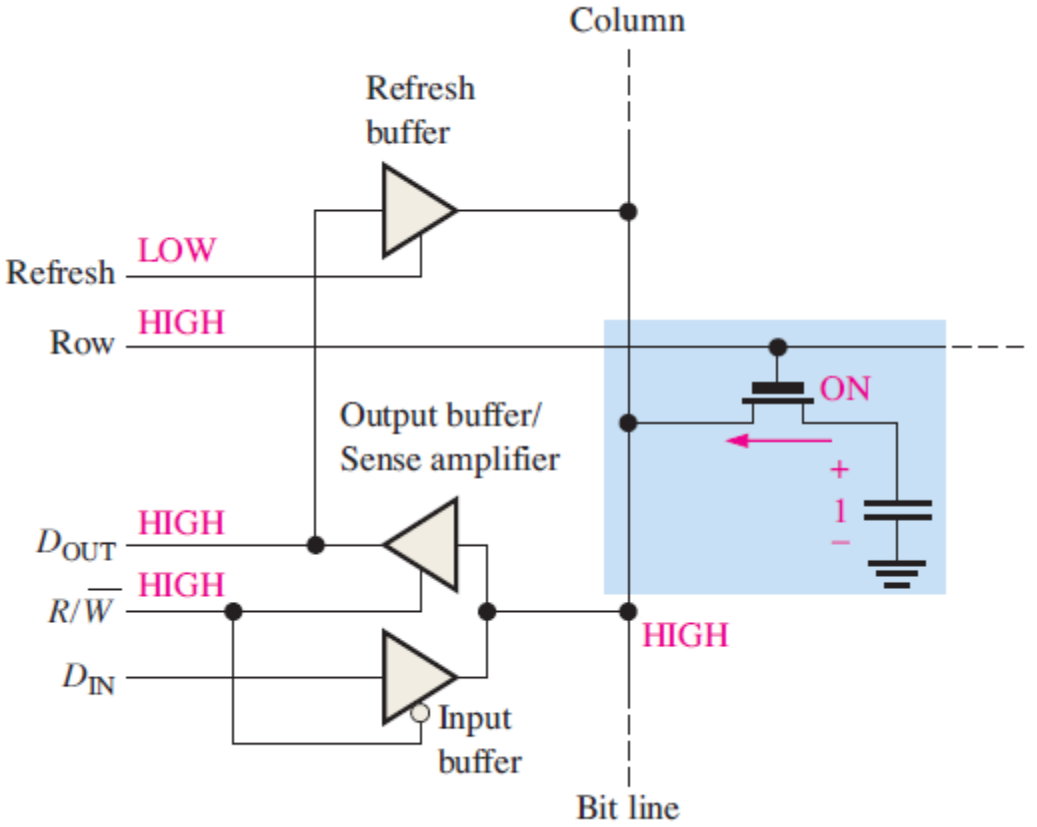
- A LOW on the R/$\overline{W}$ line enables the tri-state input buffer and disables the output buffer.
- For a 0 to be written D_{IN} is LOW.
- The Row line is turned HIGH to turn on the transistor.
- Thus the bit line is connected to the capacitor.
- If the capacitor is storing a 0 it remains uncharged or it discharges to 0.
- Then when the Row line is turned LOW the transistor is OFF.
- And the charge gets trapped in the capacitor.



Basic Operation of DRAM

Reading a 1 from the memory cell:

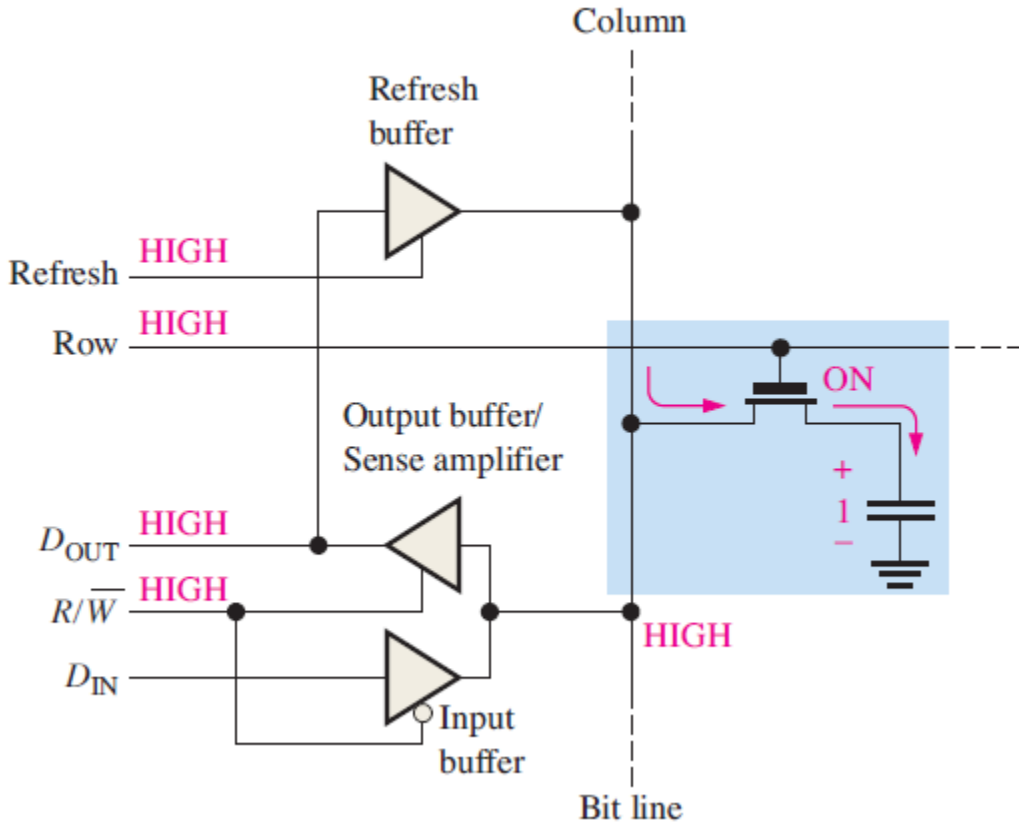
- A HIGH on the R/$\overline{W}$ line enables the tri-state output buffer and disables the input buffer.
- For a 0 to be written D_{IN} is LOW.
- The ROW line is turned HIGH to turn on the transistor.
- Thus the bit line is connected to the capacitor.
- The capacitor value appears on the input of the output buffer.
- The buffer relays the value to the data-output line.



Basic Operation of DRAM

Refreshing a stored 1:

- A HIGH on the R/$\overline{W}$ line enables the tri-state output buffer and disables the input buffer.
- The ROW line is turned HIGH to turn on the transistor.
- The Refresh line HIGH.
- Thus the bit line is connected to the capacitor.
- The output buffer is enabled, and the stored data is applied to the input of the refresh buffer, which is enabled by the HIGH on the refresh input.
- This produces a voltage on the bit line corresponding to the stored bit and thus replenishing the capacitor



References

1. Thomas L. Floyd, “Digital Fundamentals” 11th edition, Prentice Hall – Pearson Education.

Thank You