Lecture -1
Sequential Circuit Design: Latches and Flip-Flops

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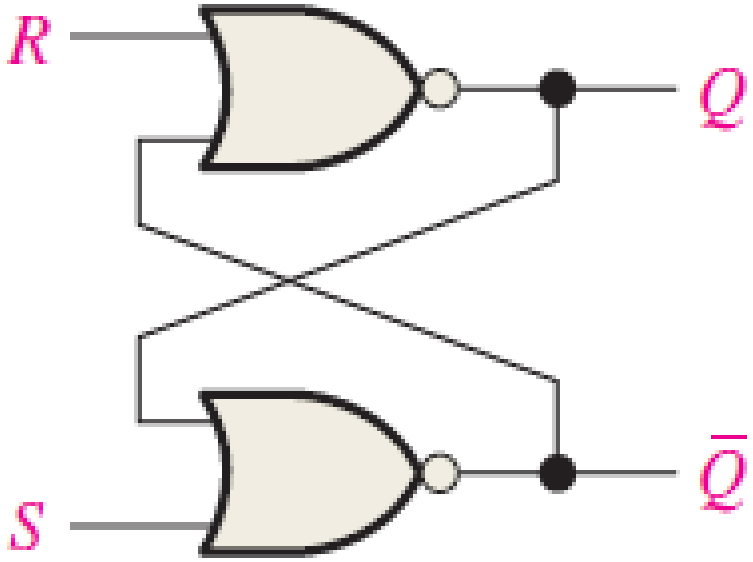
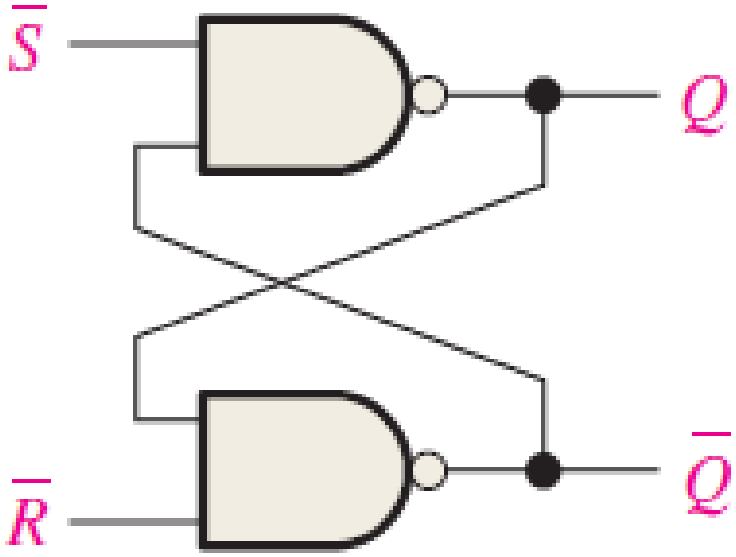
Latches

- A **latch** is a temporary storage device that has two stable states (bi-stable).
- It is a basic form of temporary storage device which can reside in either 1 or 0.
- The S-R (Set-Reset) latch is the most basic type.
- It can be constructed from two cross-coupled NOR gates or NAND gates.
- With NOR gates the latch responds to active-HIGH inputs.
- With NAND gates the latch responds to active-LOW inputs.

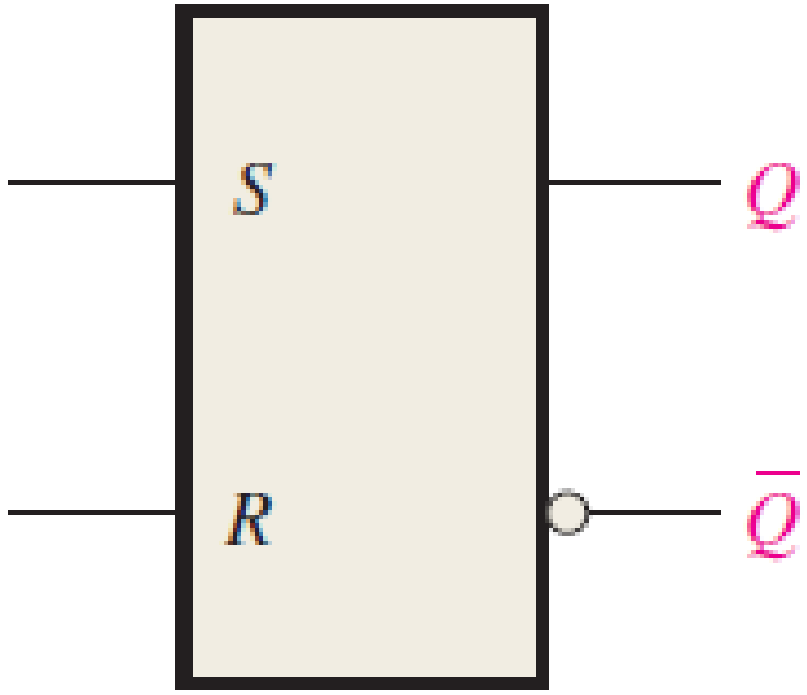


An Active-HIGH S-R Latch



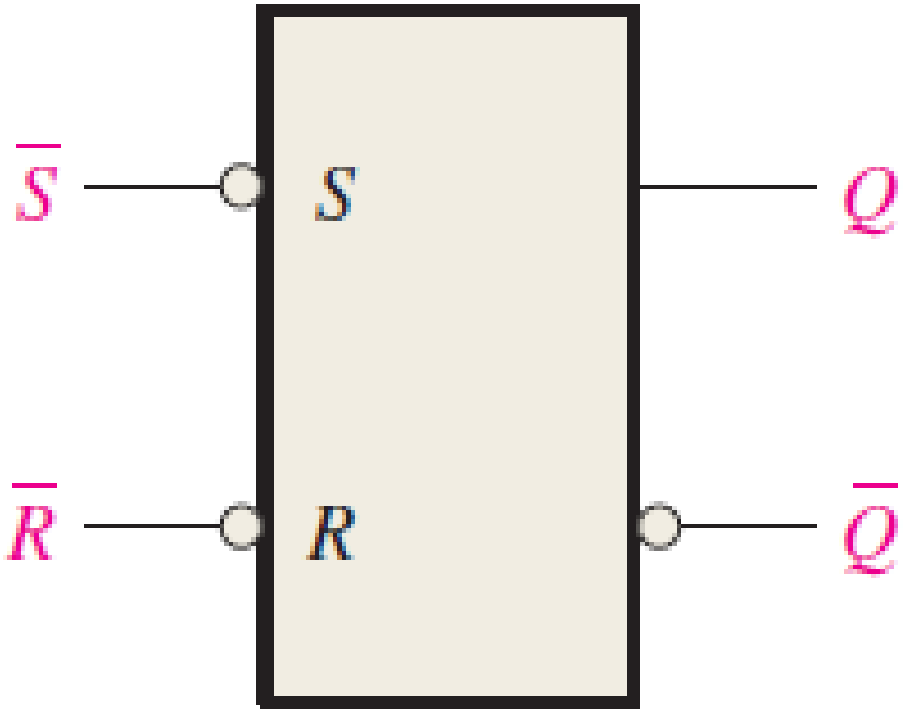
An Active-LOW S-R Latch

Latches



Block diagram of an Active-HIGH S-R Latch

- For an Active-HIGH S-R Latch there are no bubbles in the inputs.



Block diagram of an Active-LOW S-R Latch

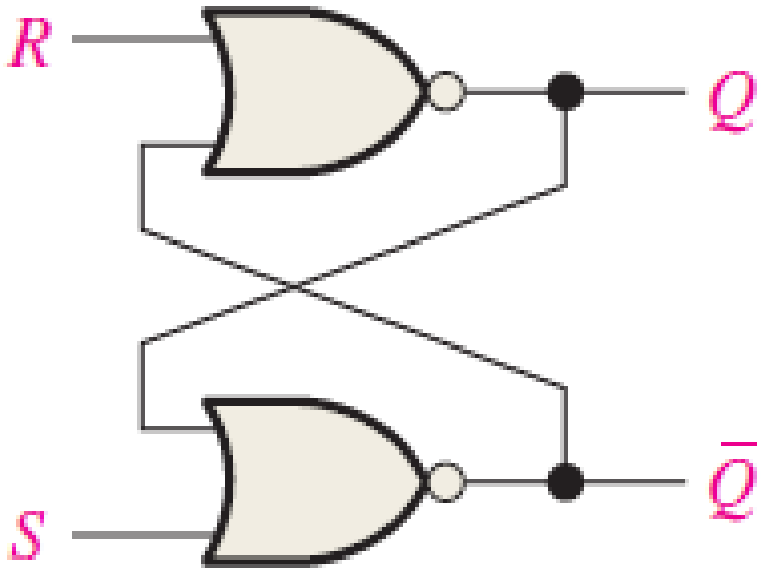
- For an Active-LOW S-R Latch there are bubbles in the inputs.

Latches

Operation of an Active-HIGH S-R Latch

STARTING CONDITION Q=0 AND $\overline{Q}$=1

- WHEN S=1, R=0, Q=0 AND $\overline{Q}$=1 (SET OPERATION)
  - $\overline{Q}$=0. AS $\overline{Q}$=0 AND R=0, Q=1.
- WHEN S=0, R=0, Q=1 AND $\overline{Q}$=0 (MEMORY OPERATION)
  - AS S=0 AND Q=1, $\overline{Q}$=0.
  - AS $\overline{Q}$=0 AND R=0, Q=1.
- WHEN S=0, R=1, Q=1 AND $\overline{Q}$=0 (RESET OPERATION)
  - AS R=1, Q=0.
  - AS Q=0 AND S=0, $\overline{Q}$=1
- When both inputs are 1, the operation is INVALID



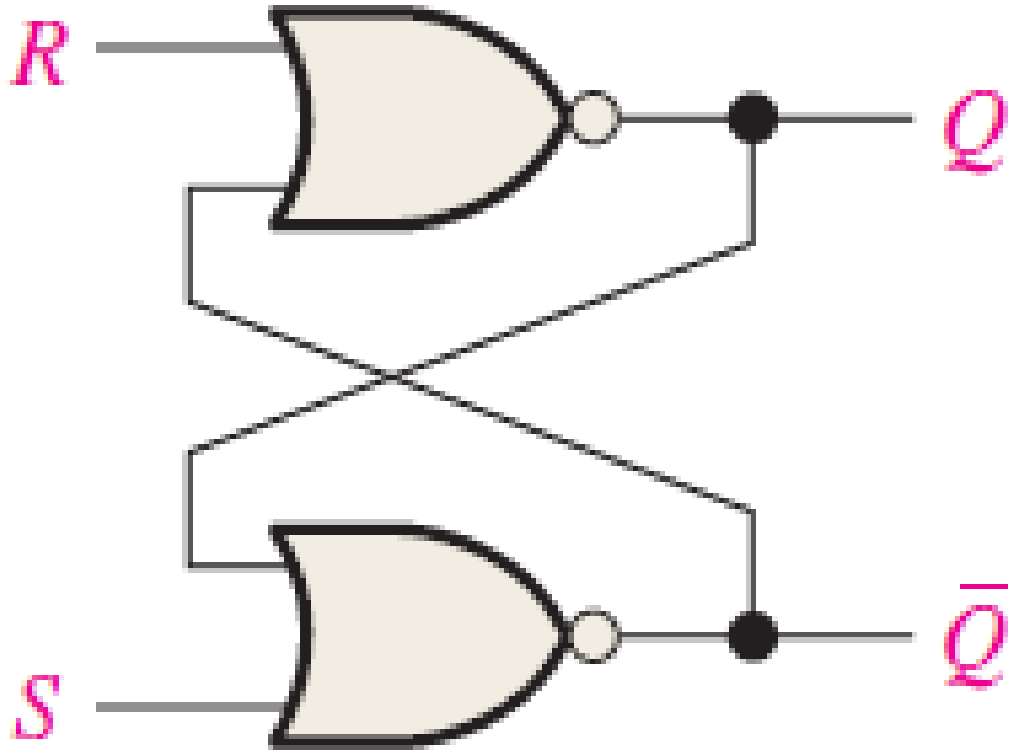
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Truth-table for NOR gate

Latches

Table of operation of an Active-HIGH S-R Latch

Input		Outputs		Comments
S	R	Q	$\bar{Q}$	
0	0	NC	NC	MEMORY
0	1	0	1	RESET
1	0	1	0	SET
1	1	--	--	INVALID

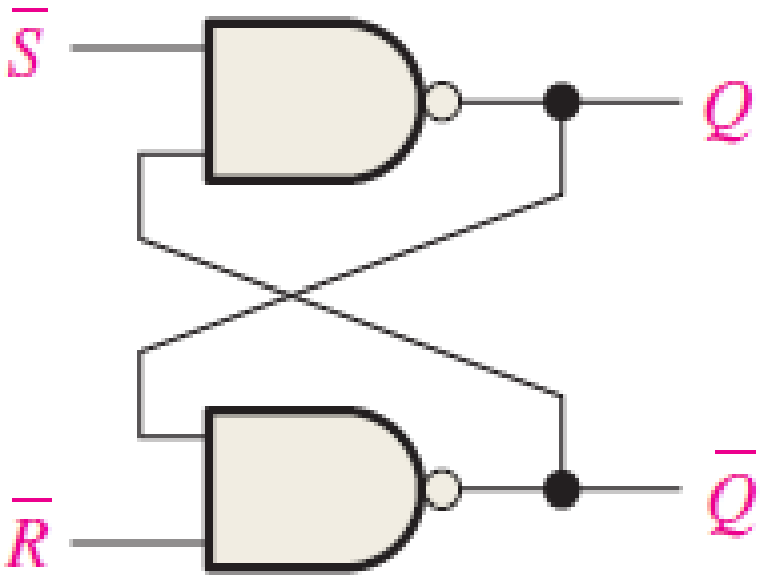


Latches

Operation of an Active-LOW S-R Latch

STARTING CONDITION Q=0 AND $\overline{Q}$=1

- WHEN S=0, R=1, Q=0 AND $\overline{Q}$=1 (SET OPERATION)
  - Q=1. AS Q=1 AND R=1, $\overline{Q}$=0.
- WHEN S=1, R=1, Q=1 AND $\overline{Q}$=0 (MEMORY OPERATION)
  - AS S=1 AND $\overline{Q}$=0, Q=1.
  - AS Q=1 AND R=1, $\overline{Q}$=0.
- WHEN S=1, R=0, Q=1 AND $\overline{Q}$=0 (RESET OPERATION)
  - AS R=0, $\overline{Q}$=1.
  - AS $\overline{Q}$=1 AND S=1, Q=0
- When both inputs are 0, the operation is INVALID



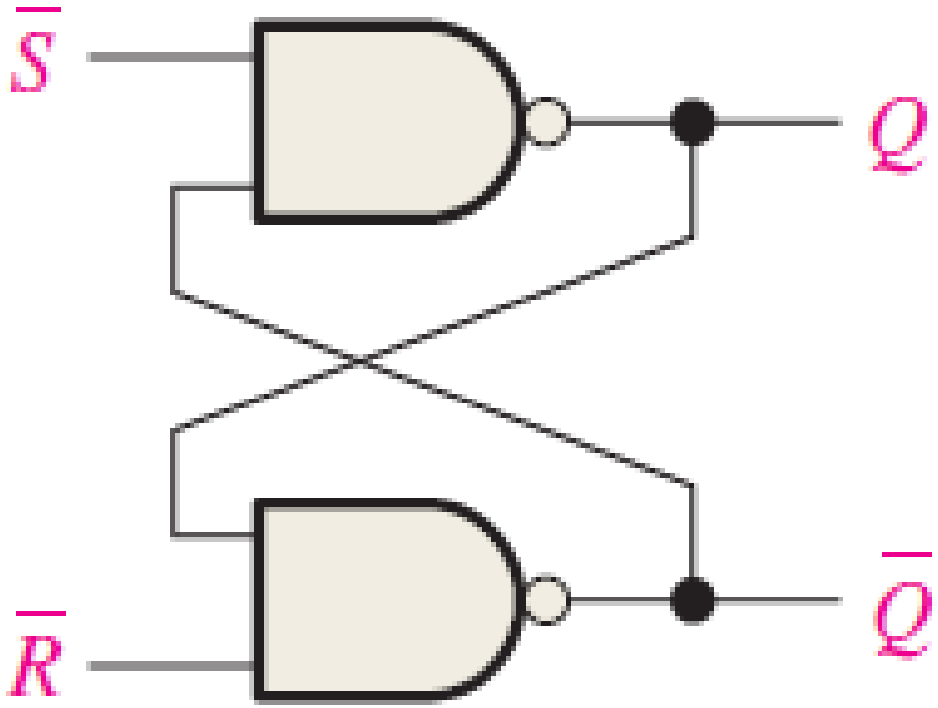
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Truth-table for NAND gate

Latches

Table of operation of an Active-LOW S-R Latch

Input		Outputs		Comments
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
1	1	NC	NC	MEMORY
1	0	0	1	RESET
0	1	1	0	SET
0	0	--	--	INVALID

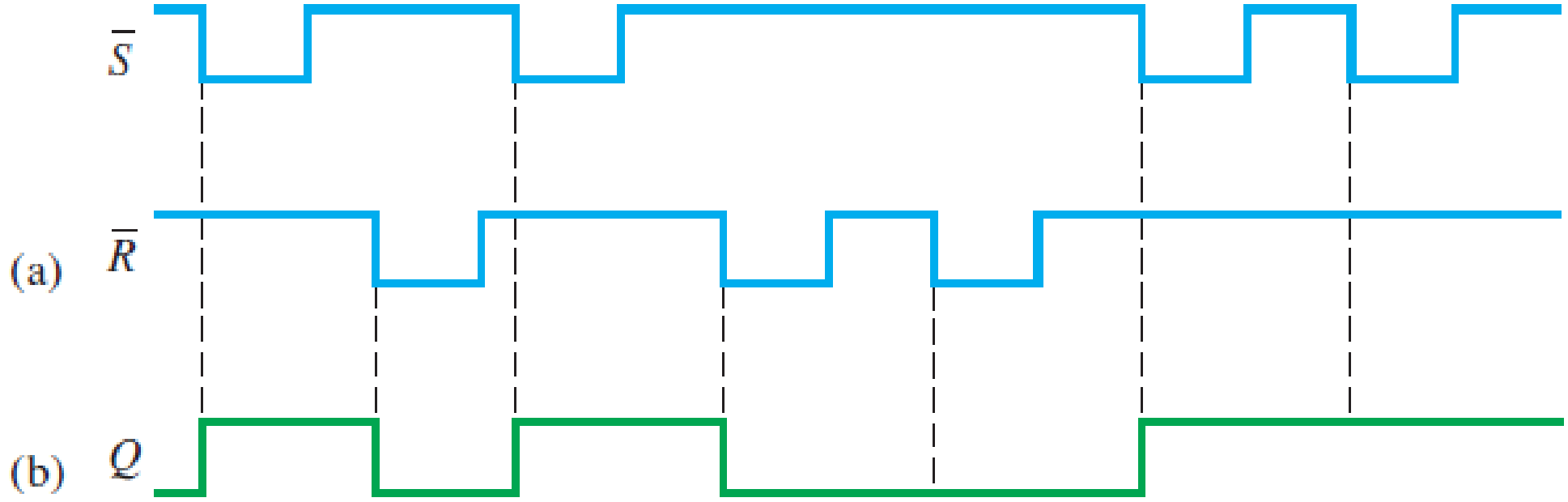


Latches

Exercise 1:

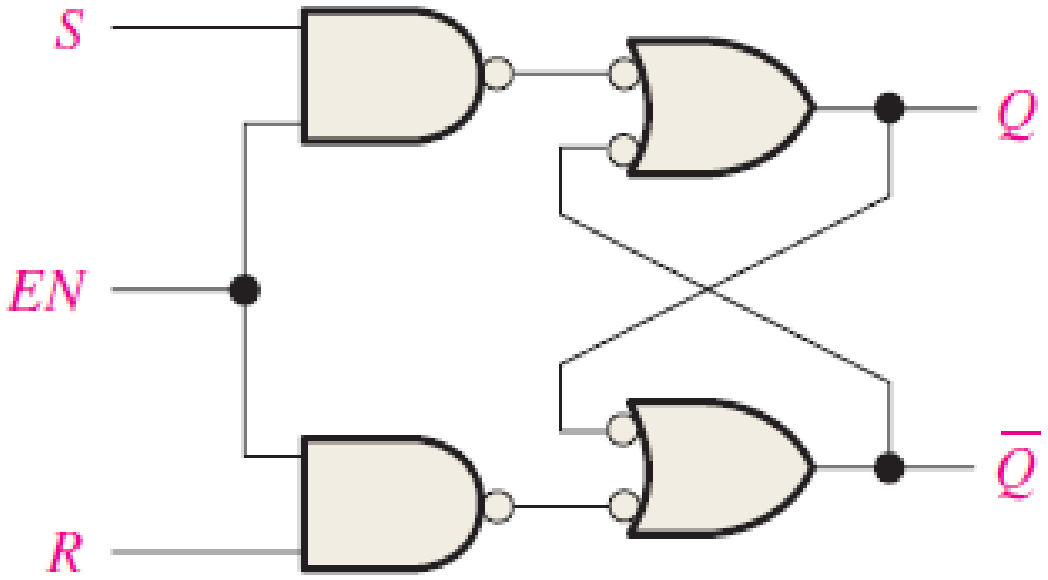
If the $\overline{S}$ and $\overline{R}$ waveforms in Figure 7–5(a) are applied to the inputs of the latch in Figure 7–4(b), determine the waveform that will be observed on the Q output. Assume that Q is initially LOW.

SOLUTION

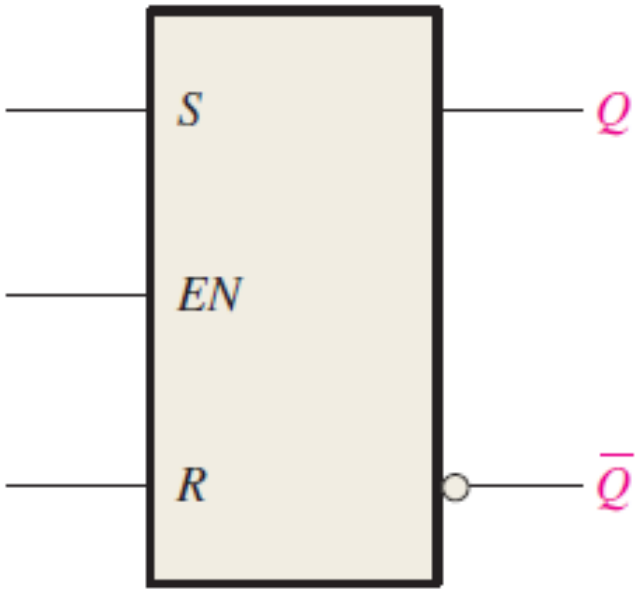


Gated S-R Latches

- A gated latch is a variation of basic latch.
- A gated latch has an extra input “ENABLE” (EN).
- The latch responds to S and R if and only if EN is HIGH.
- So the extra input brings more control over the operation.
- Gated Latches are level sensitive.



A gated S-R Latch

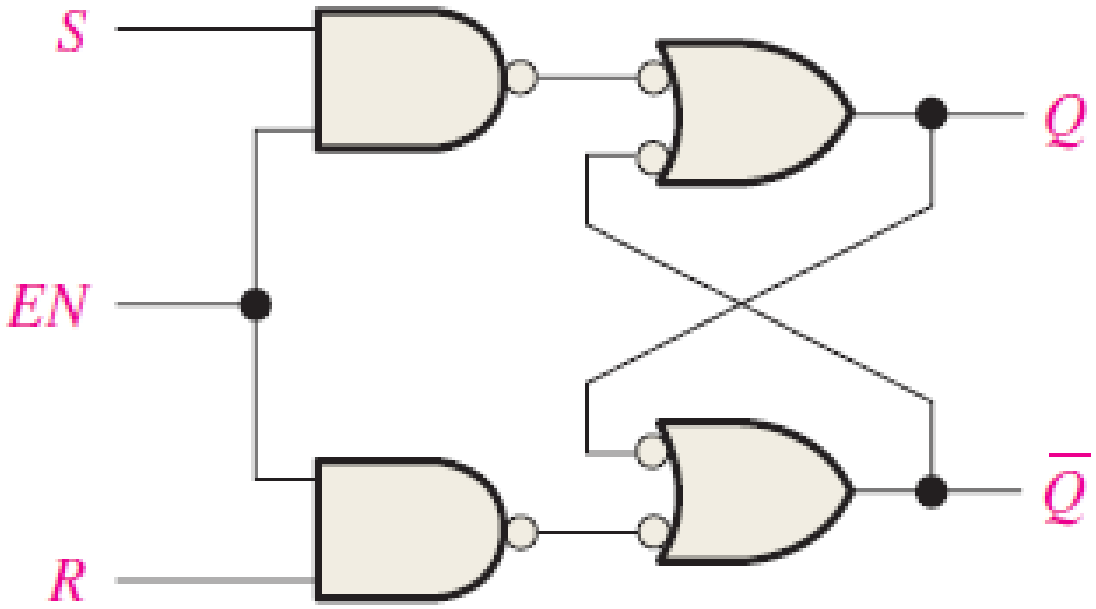


Block diagram of a gated S-R Latch

Gated S-R Latches

Input			Input		Outputs		Comments
S	R	E	$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
1	1	0	1	1	NC	NC	MEMORY
0	0	1	1	1	NC	NC	MEMORY
0	1	1	1	0	0	1	RESET
1	0	1	0	1	1	0	SET
1	1	1	0	0	--	--	INVALID

Table of operation for a gated S-R Latch



Logic Circuit of a gated S-R Latch

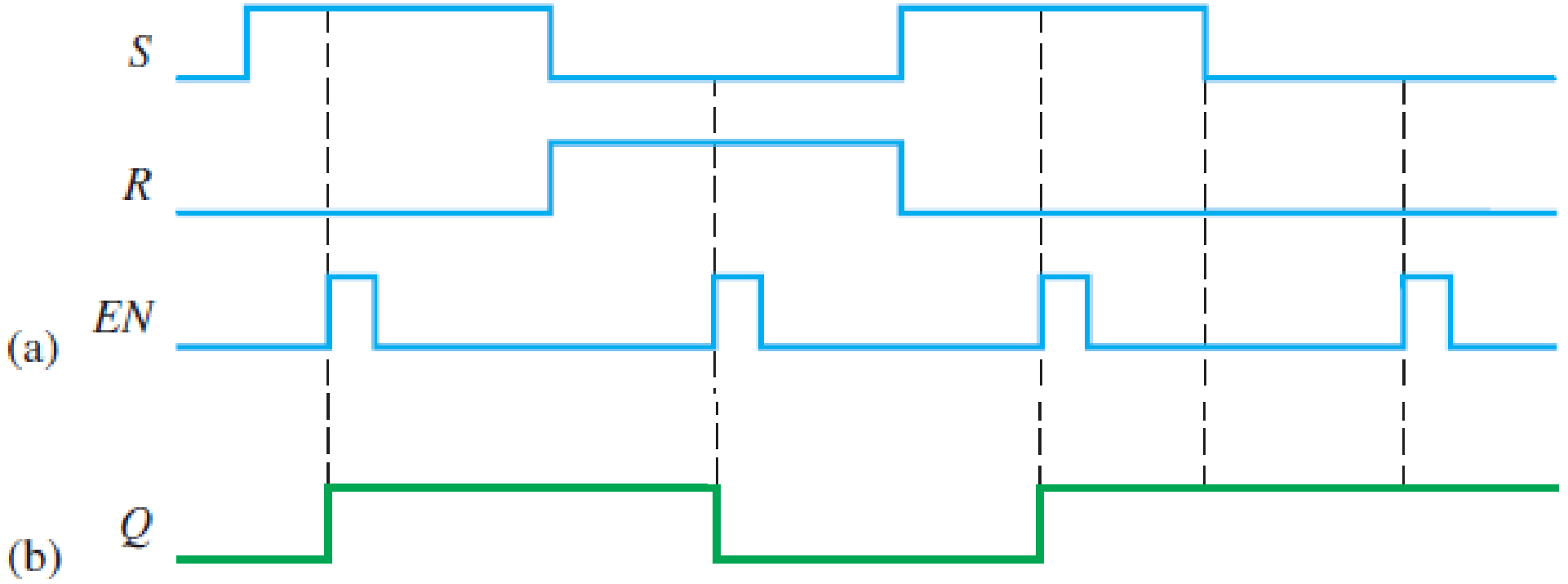
Truth table for a NAND gate

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Gated S-R Latches

Exercise 2:

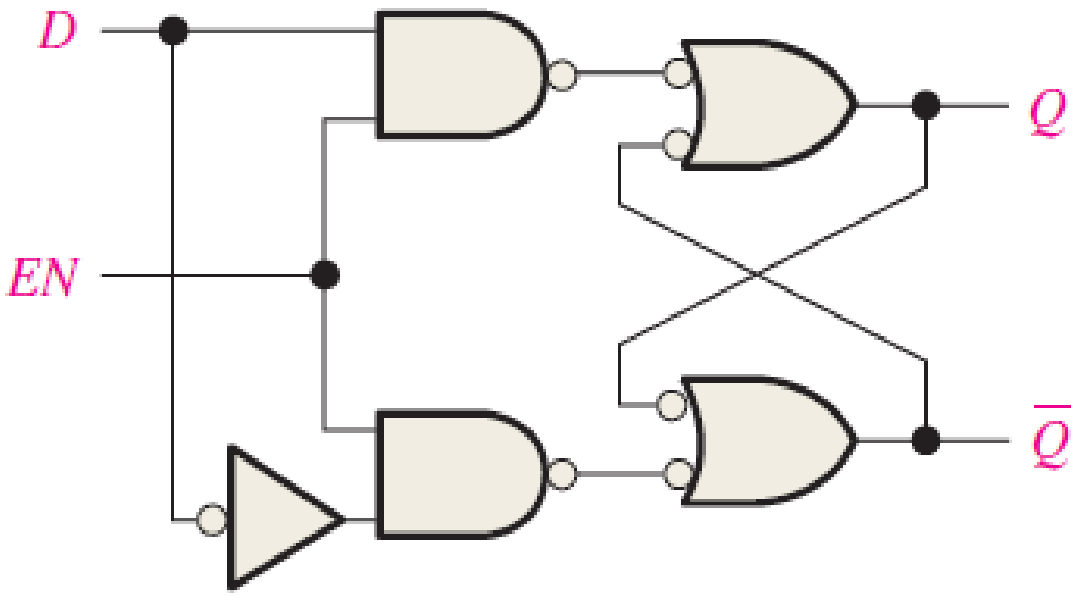
Determine the Q output waveform if the inputs shown in Figure 7–9(a) are applied to a gated S-R latch that is initially RESET.



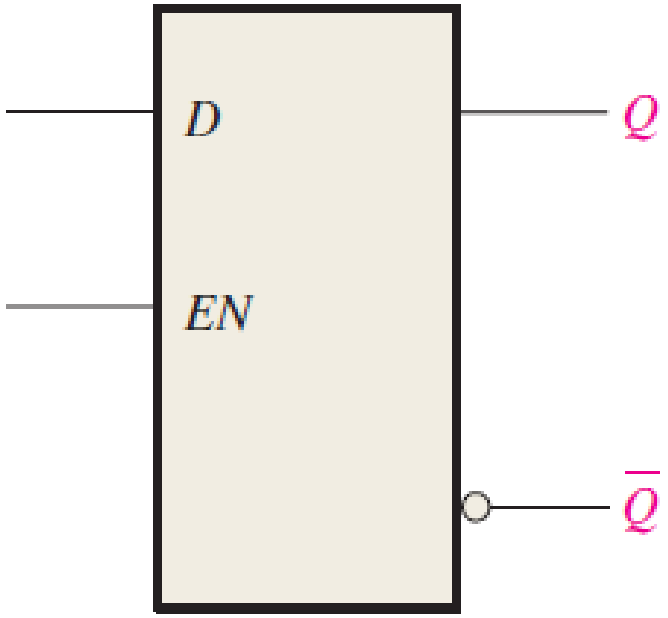
SOLUTION

Gated D Latches

- The D latch is another variant of latches
- It combines the S and R input into a single input D.
- When D and EN is HIGH, the latch is SET.
- When D is LOW and EN is HIGH, the latch is RESET.
- A simple rule is, when EN is HIGH, the Q follows the input D



A gated D-Latch

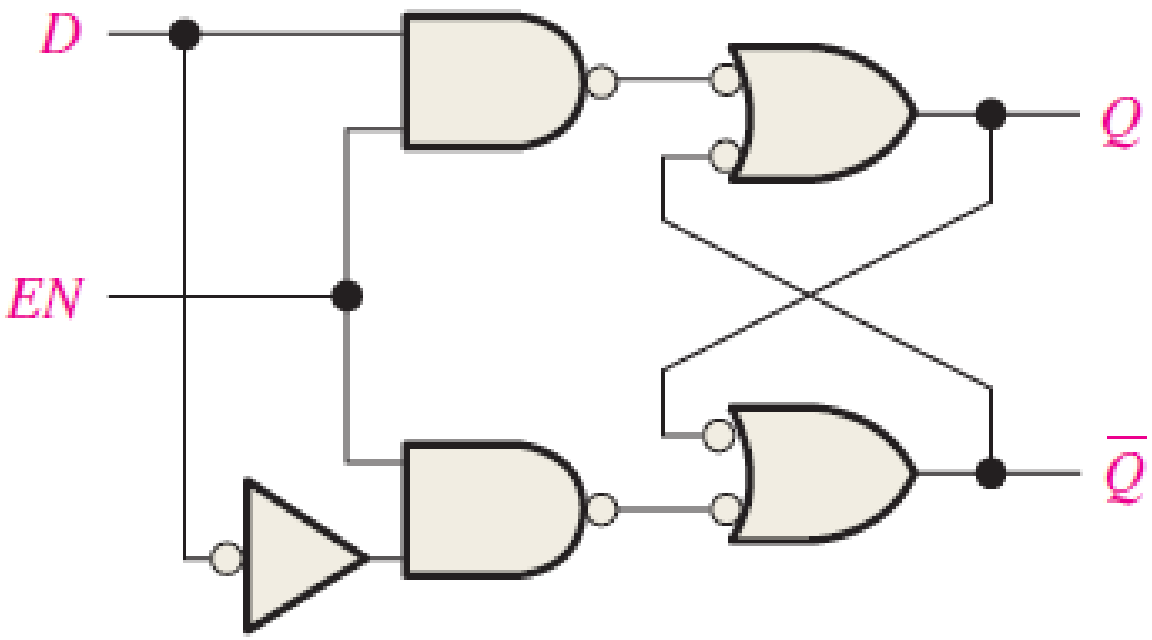


Block diagram of a gated D-Latch

Gated D Latches

Input		Outputs		Comments
D	EN	Q	$\overline{Q}$	
X	0	NC	NC	MEMORY
0	1	0	1	RESET
1	1	1	0	SET

Table of operation for Gated D-Latch

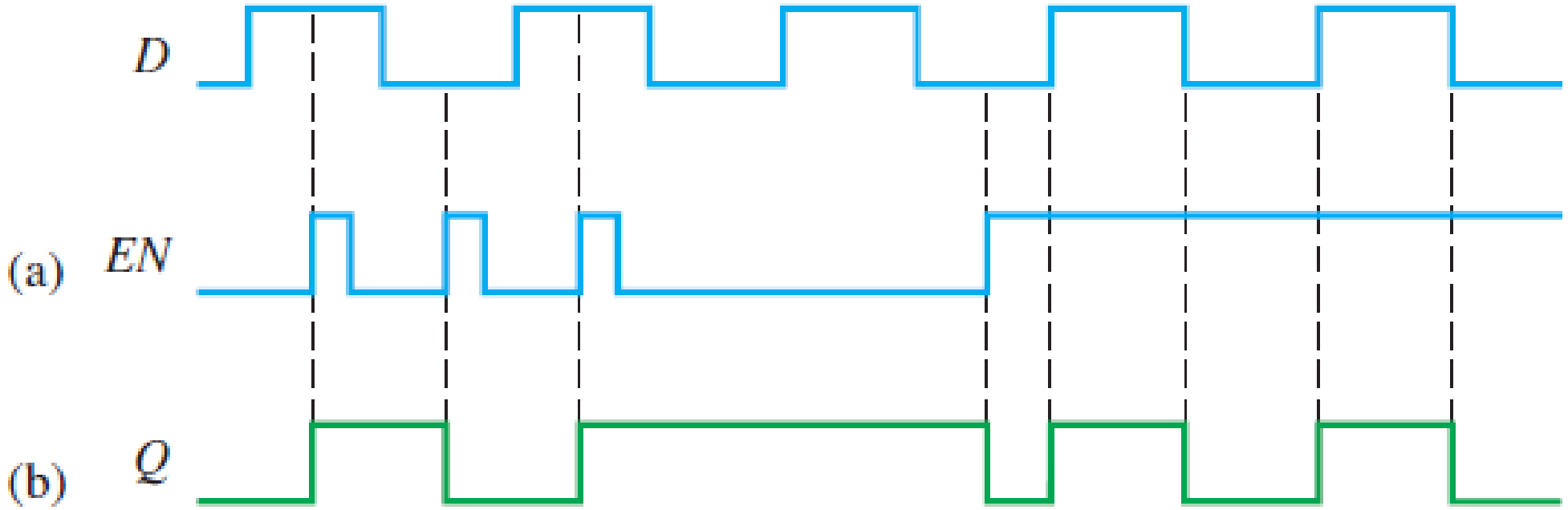


Logic Circuit of a Gated D-Latch

Gated D Latches

Exercise 3:

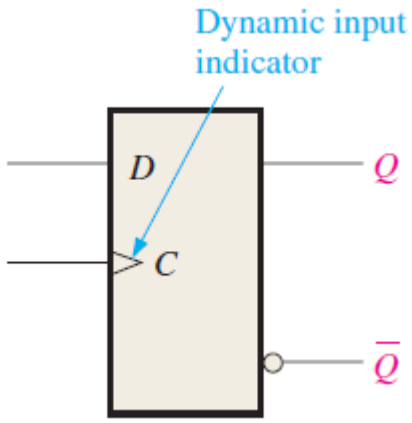
Determine the Q output waveform if the inputs shown in Figure 7–11(a) are applied to a gated D latch, which is initially RESET.



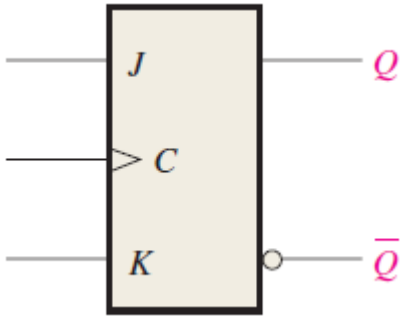
SOLUTION

Flip-Flops

- Flip-Flops are synchronous bi-stable devices, also know as bi-stable multi-vibrator.
- Synchronous means the output changes only at the triggering of a control input “Clock”.
- Compared to gated latches, flip-flops are edge triggered devices.
- Edge triggered means, the output only changes at “Rising Edge” or “Falling Edge” of a clock.
- A rising edge triggered device is also called a positive edge triggered device.
- A falling edge triggered device is also called a negative edge triggered device.

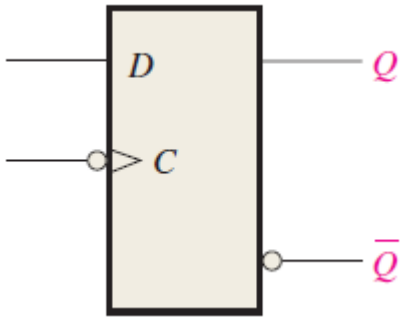


a) D Flip-Flop

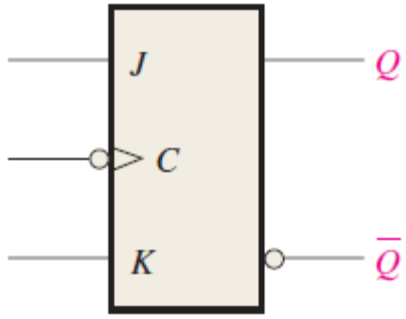


b) J-K Flip-Flop

Positive edge triggered Flip-Flops



a) D Flip-Flop

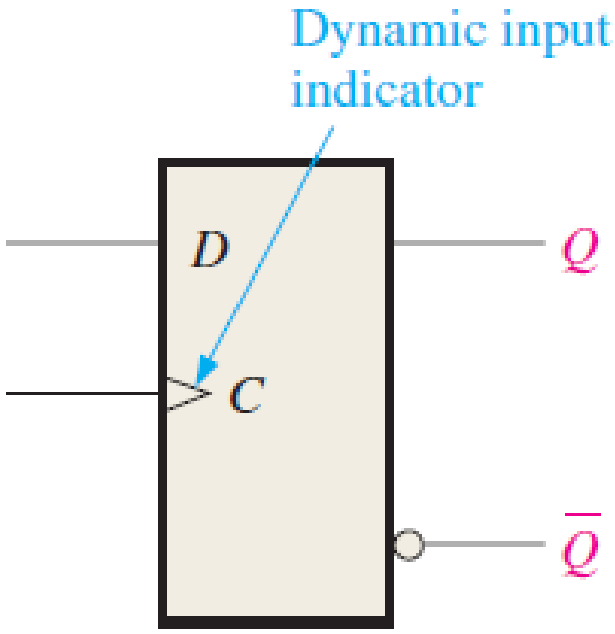


b) J-K Flip-Flop

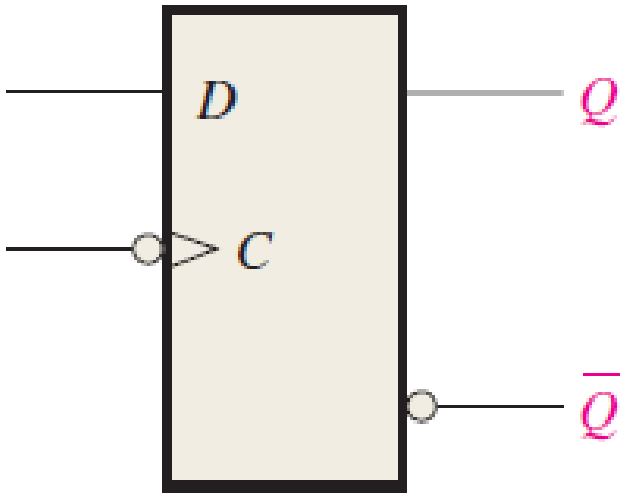
Negative edge triggered Flip-Flops

D Flip-Flops

- The D input is a synchronous input, as the input is only transferred at the triggering of a clock pulse (positive or negative).
- The operation is almost similar to that of a D latch.
- At a clock pulse, if D is HIGH, the flip-flop is SET, so $Q = 1$ and $\overline{Q} = 0$.
- At a clock pulse, if D is LOW, the flip-flop is SET, so $Q = 0$ and $\overline{Q} = 1$.



Positive edge triggered D-flip flop

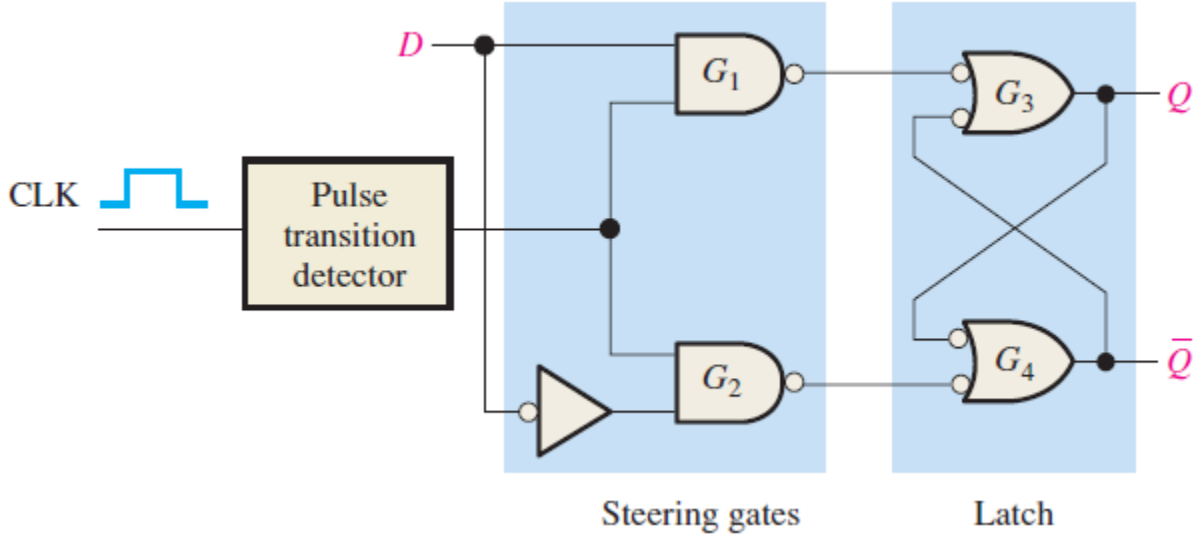


Negative edge triggered D-flip flop

D Flip-Flops

Inputs		Outputs		
D	CLK	Q	$\overline{Q}$	Comments
0	↑	0	1	RESET
1	↑	1	0	SET

a) Operation table of positive edge triggered D flip-flop



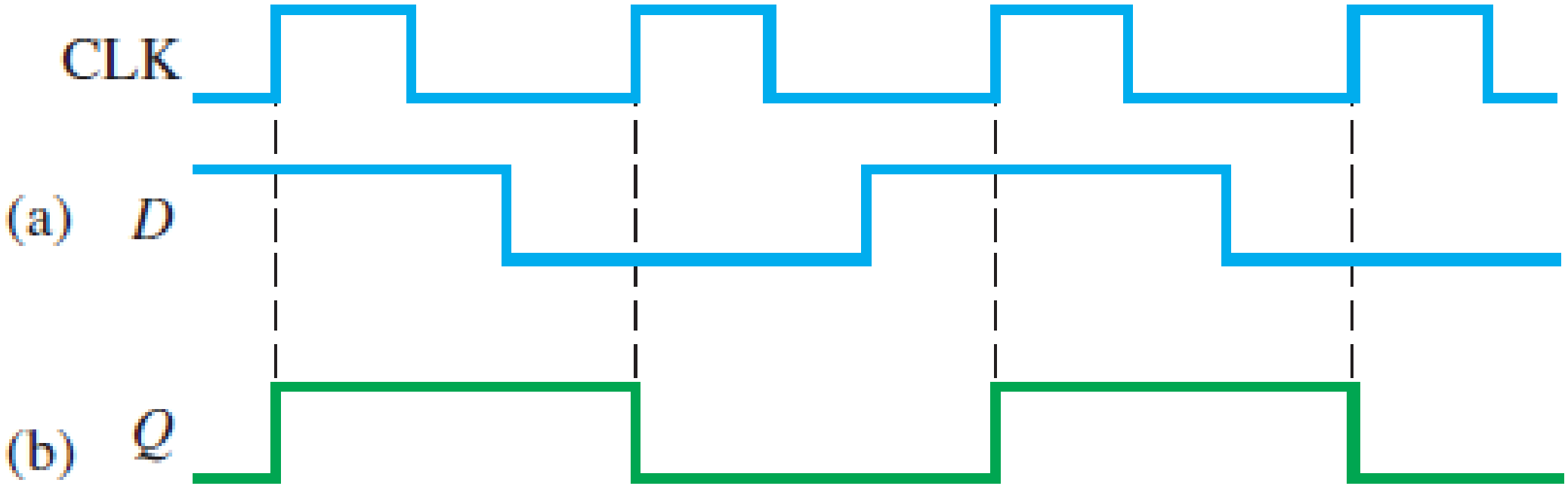
b) Positive edge triggered D flip-flop

- In the operation table, the arrow indicates the rising edge, and thus it is a positive edge triggered D flip-flop.
- Rising edge is indicated by an upward arrow, likewise, a falling edge is indicated by a downward value.
- The circuit diagram of a D flip-flop is also similar to a gated D Latch, except for an additional pulse transition detector.
- The pulse transition detector is used to produce the triggering edge.

D Flip-Flops

Exercise 4:

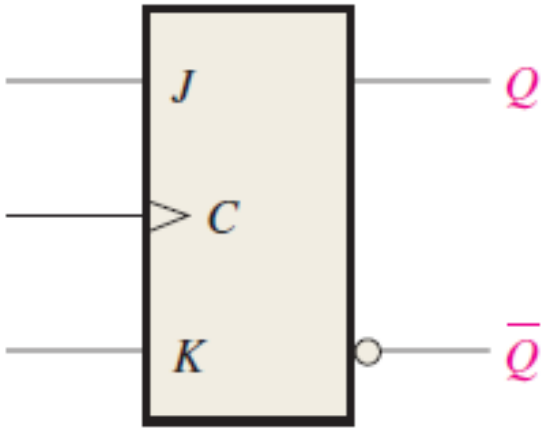
Given the waveforms in Figure 7–22(a) for the *D* input and the clock, determine the *Q* output waveform if the flip-flop starts out RESET.



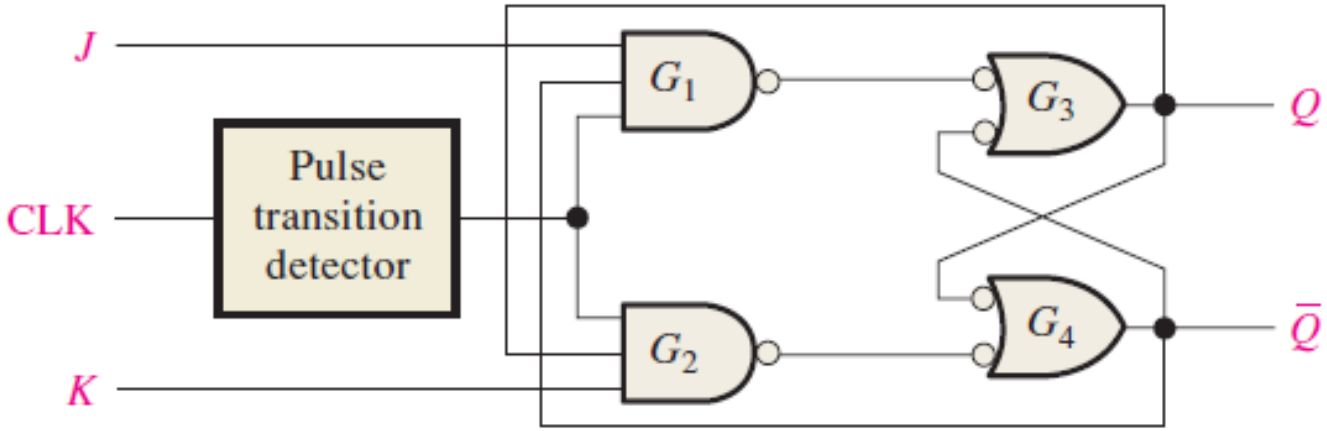
SOLUTION

JK Flip-Flops

- The JK Flip-Flop is a more versatile and widely used type of Flip-Flop.
- The J and K inputs are synchronous inputs.
- The JK flip-flop eradicates the problem of SR flip-flop.
- JK flip-flops does not have the invalid state.
- When both J and K are HIGH, a JK flip-flop performs the toggle operation.
- JK flip-flops are widely used to make counters.

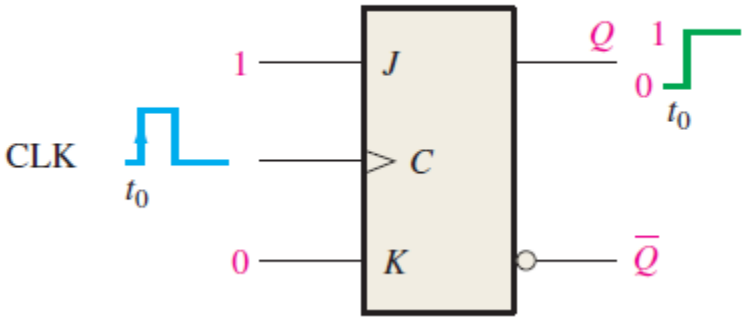


Block diagram of positive-edge triggered J-K flip-flop

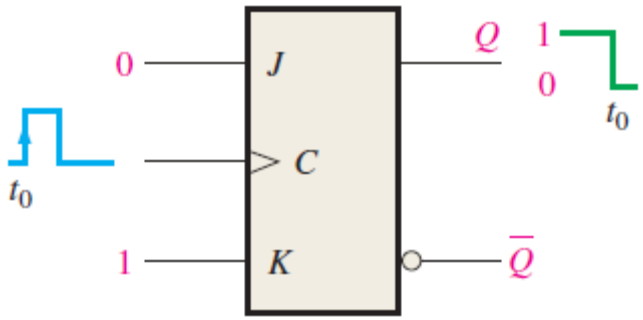


Logic circuit of positive-edge triggered J-K flip-flop

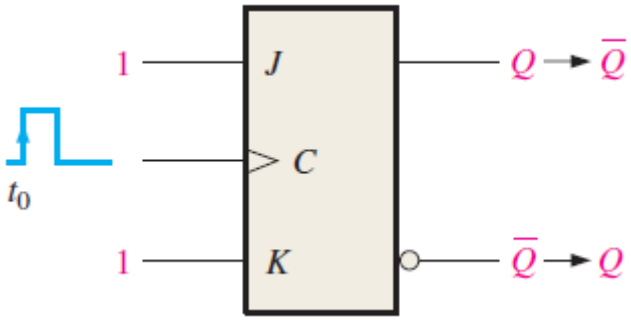
JK Flip-Flops



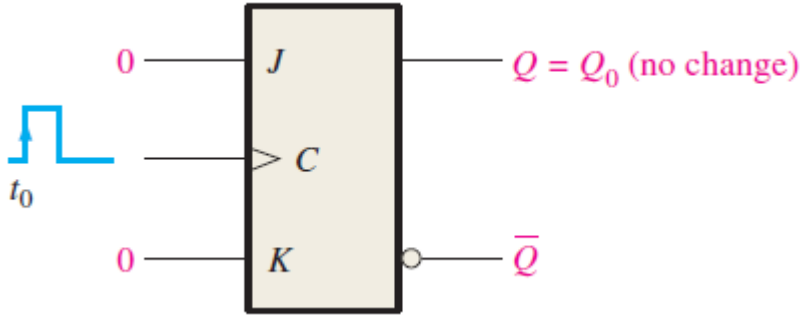
Set Operation



Reset Operation



Toggle Operation



Memory Operation

Input			Outputs		Comments
J	K	Clk	Q	$\bar{Q}$	
X	X	X	NC	NC	MEMORY
0	0	↑	NC	NC	MEMORY
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q_0}$	Q_0	TOGGLE

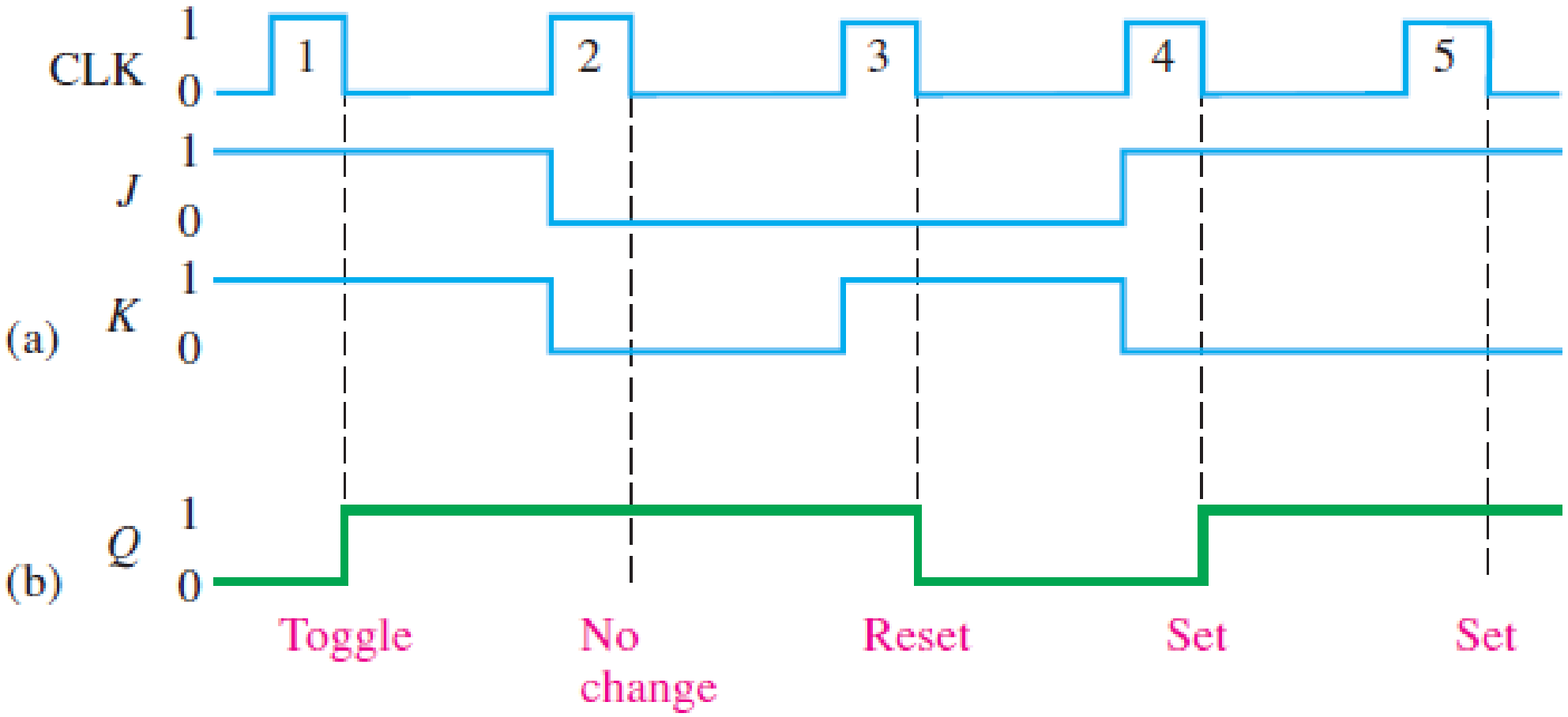
Characteristic table of positive-edge triggered J-K flip-flop

JK Flip-Flops

Exercise 5:

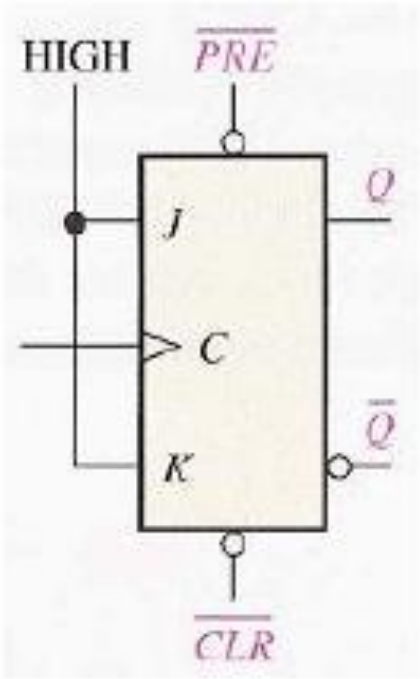
The waveforms in Figure 7–18(a) are applied to the J, K, and clock inputs as indicated. Determine the Q output, assuming that the flip-flop is initially RESET.

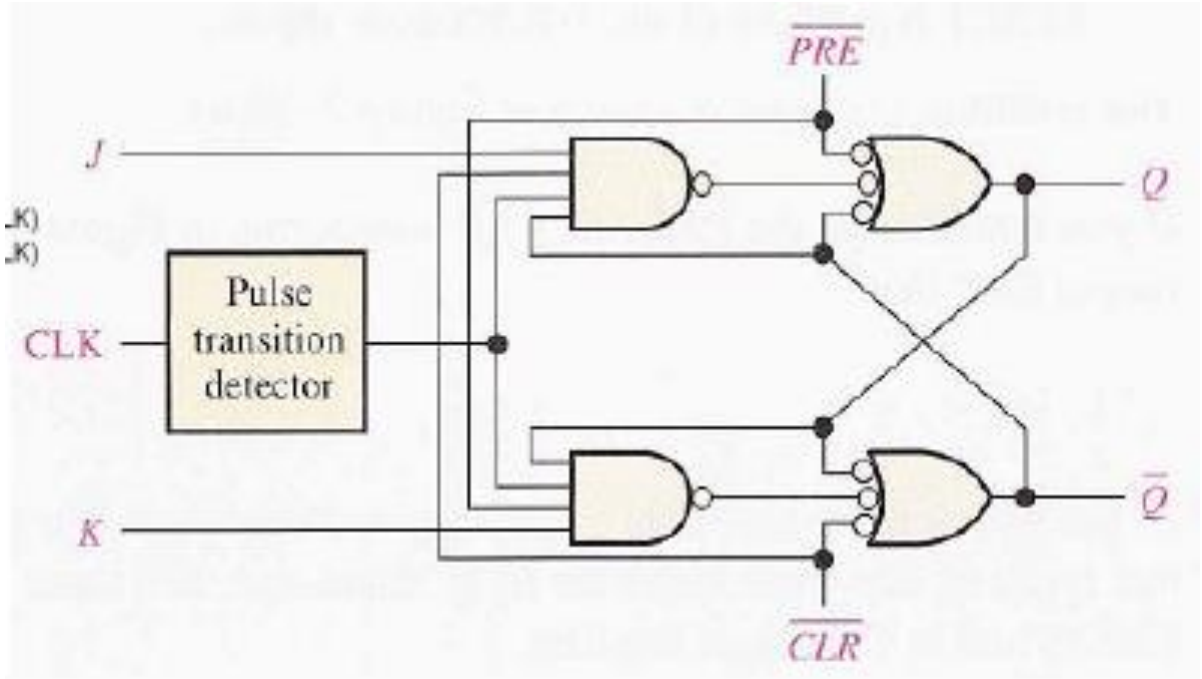
SOLUTION



JK Flip-Flops with Asynchronous Inputs

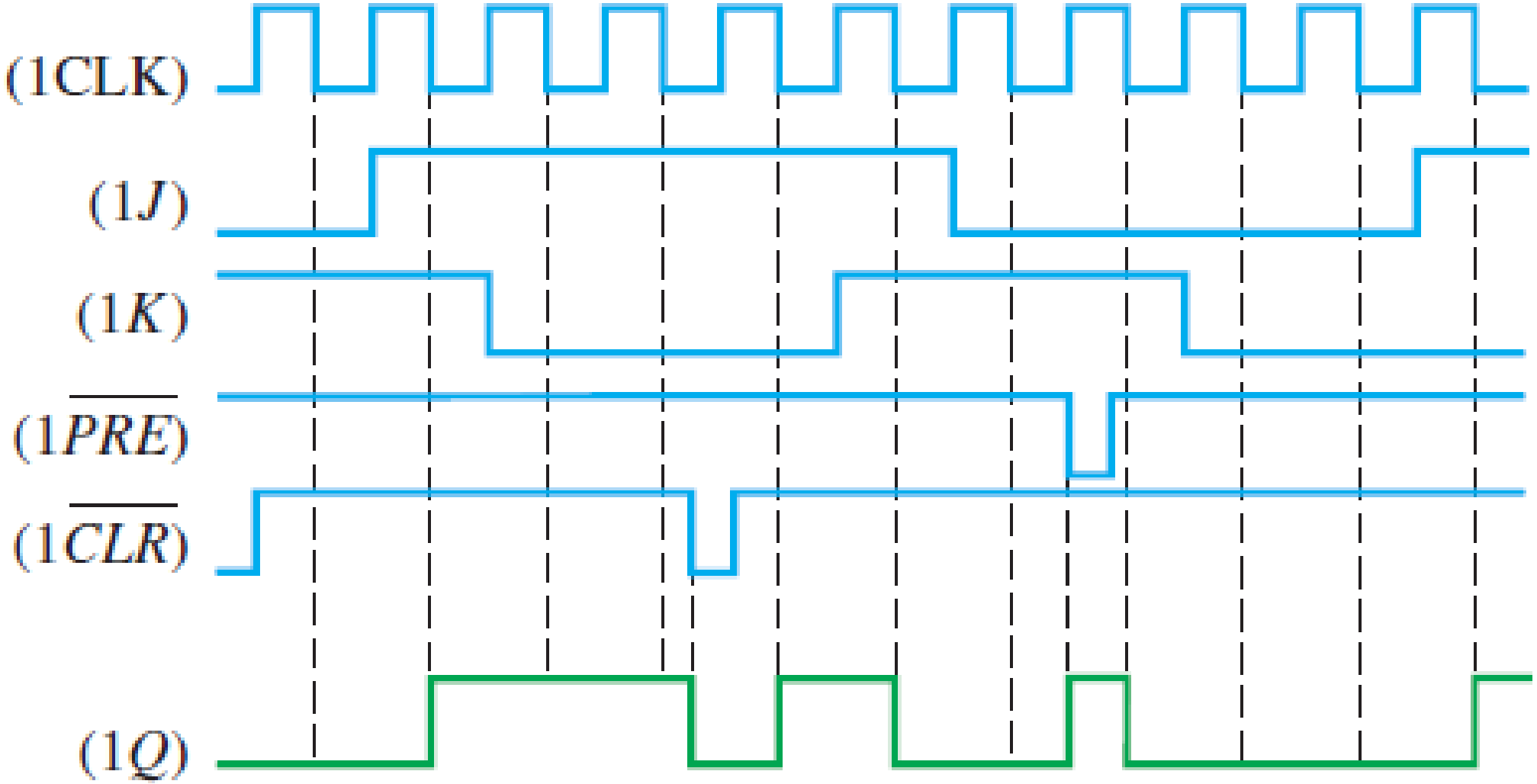
- Most flip-flops also have asynchronous inputs other than their synchronous inputs.
- The asynchronous inputs affect the output independent of the presence of clock edge.
- Two such inputs are Preset and Clear.
- Both are Active-LOW, that is, they affect the output when they are LOW.
- When Preset is LOW, it sets the flip-flop, irrespective of the synchronous inputs.
- When Clear is LOW, it resets the flip-flop, irrespective of the synchronous inputs.





JK Flip-Flops with Asynchronous Inputs

Exercise 6:

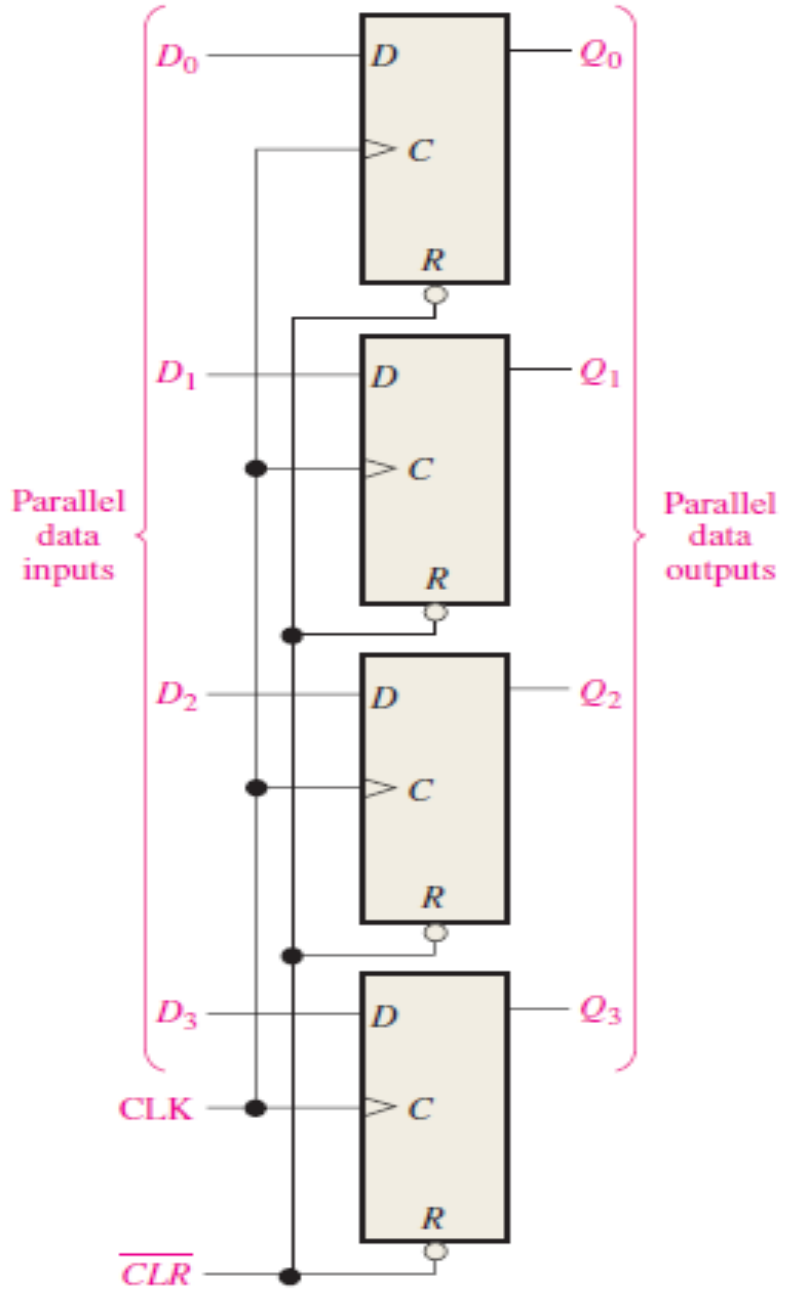


SOLUTION

Application of Flip-Flops

DATA STORAGE

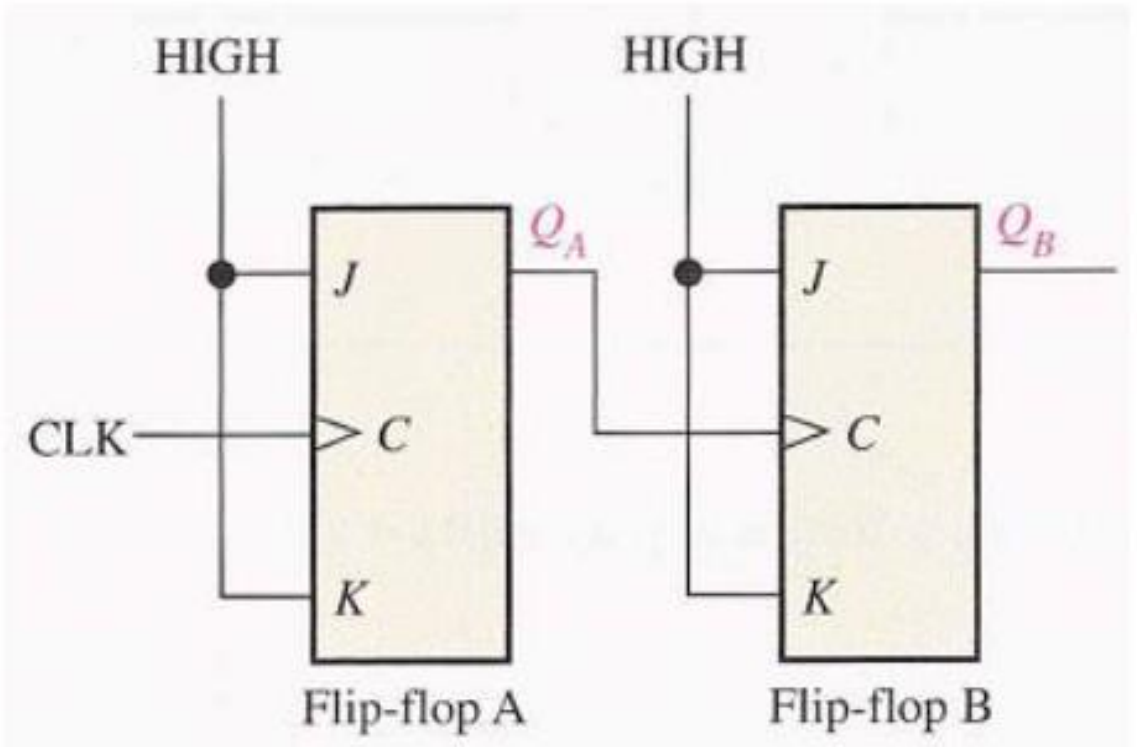
- D flip-flops can be used as parallel data storage devices.
- Multiple D flip-flops are connected in parallel.
- For a N-bit data, N no. of flip-flops are required.
- The data is stored at the triggering edge of the clock pulse.
- Figure shows a 4-bit positive edge triggered data storage device.
- The same clock is parallel connected to all the flip-flops.
- The input of the flip-flops are connected to the data bus.
- At every clock pulse, the data in the data bus gets stored in the flip-flops.
- The device also has common asynchronous Clear input.
- When the memory is needed to emptied, the Clear input is set to LOW.

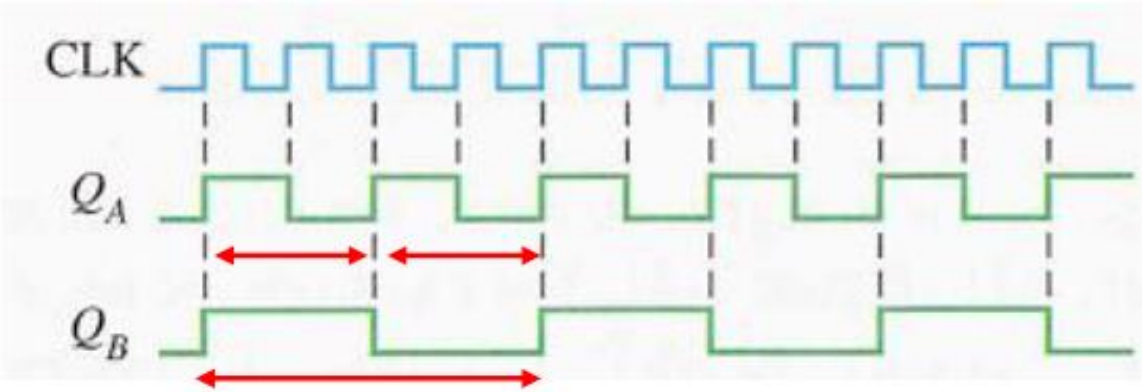


Application of Flip-Flops

FREQUENCY DIVISION

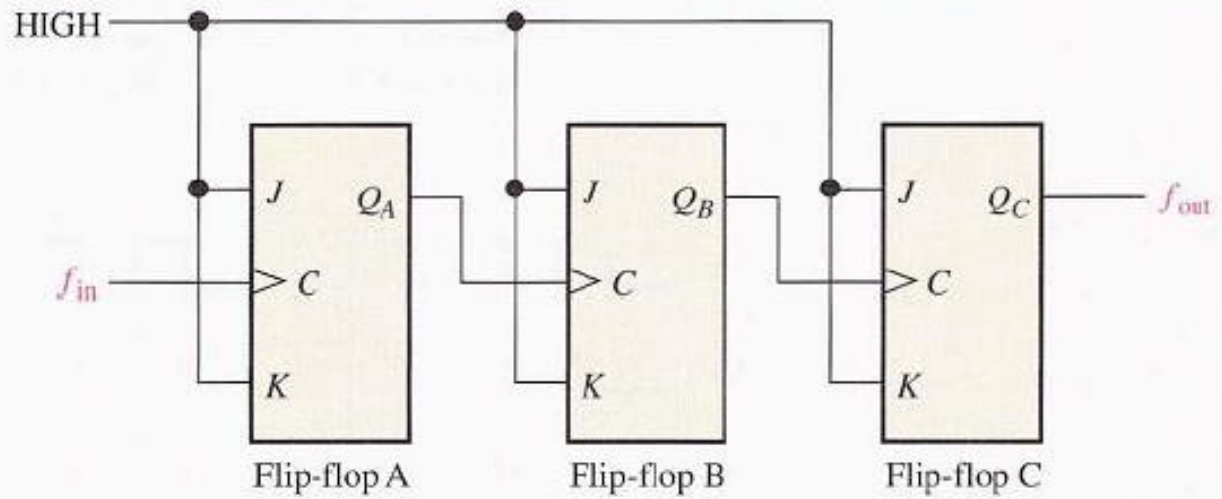
- JK flip-flops can be used to slow down clocks.
- It is also known as frequency division.
- The JK flip-flop is operated in the toggle mode.
- Each flip-flop divides the frequency by 2.
- There fore, N flip-flops can be connected in series to divide the frequency by 2^N.
- A benefit of using flip-flops for frequency division is that the duty cycle is exactly 50%.
- The figure shows the arrangement to divide the clock frequency by 4.

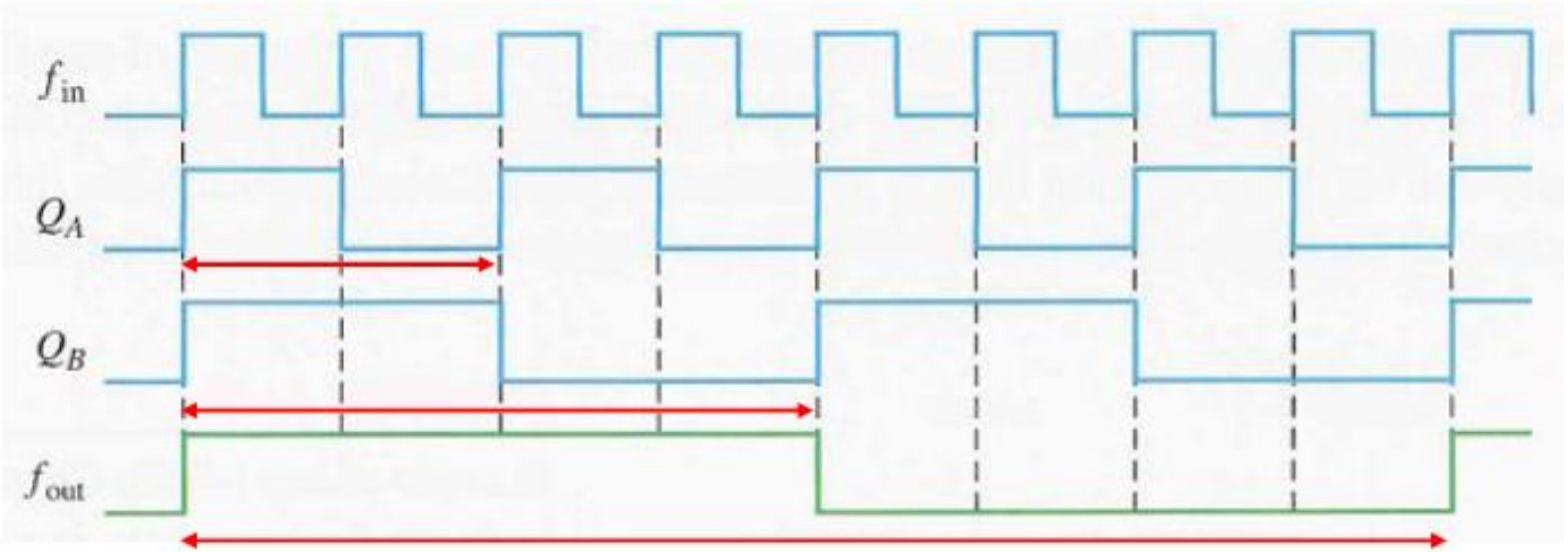




Application of Flip-Flops

Develop the f_{out} waveform for the circuit in Figure 7–39 when an 8 kHz square wave input is applied to the clock input of flip-flop A.

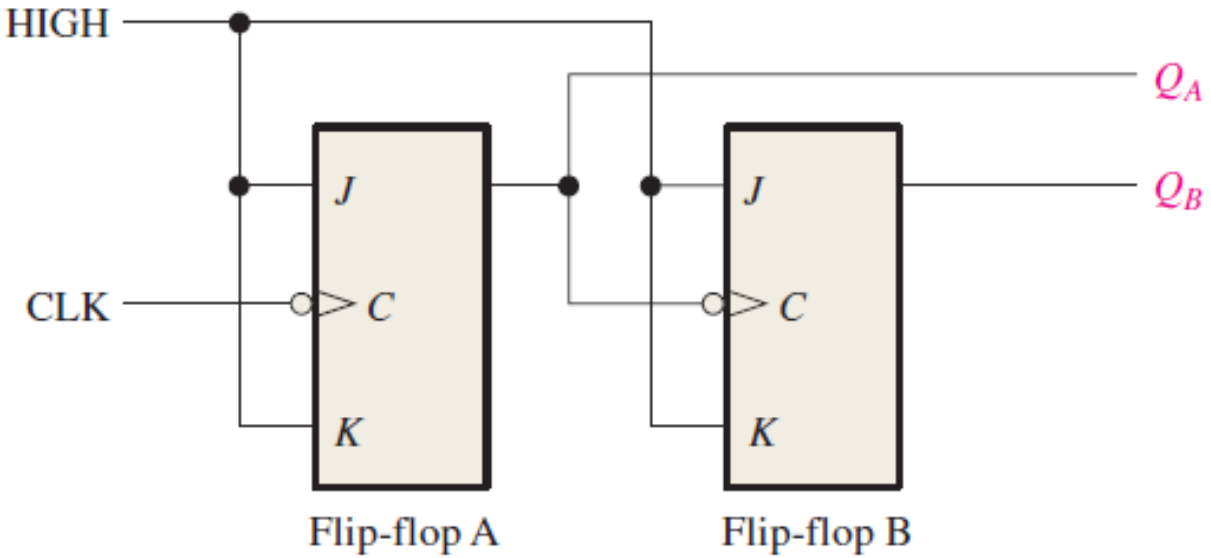


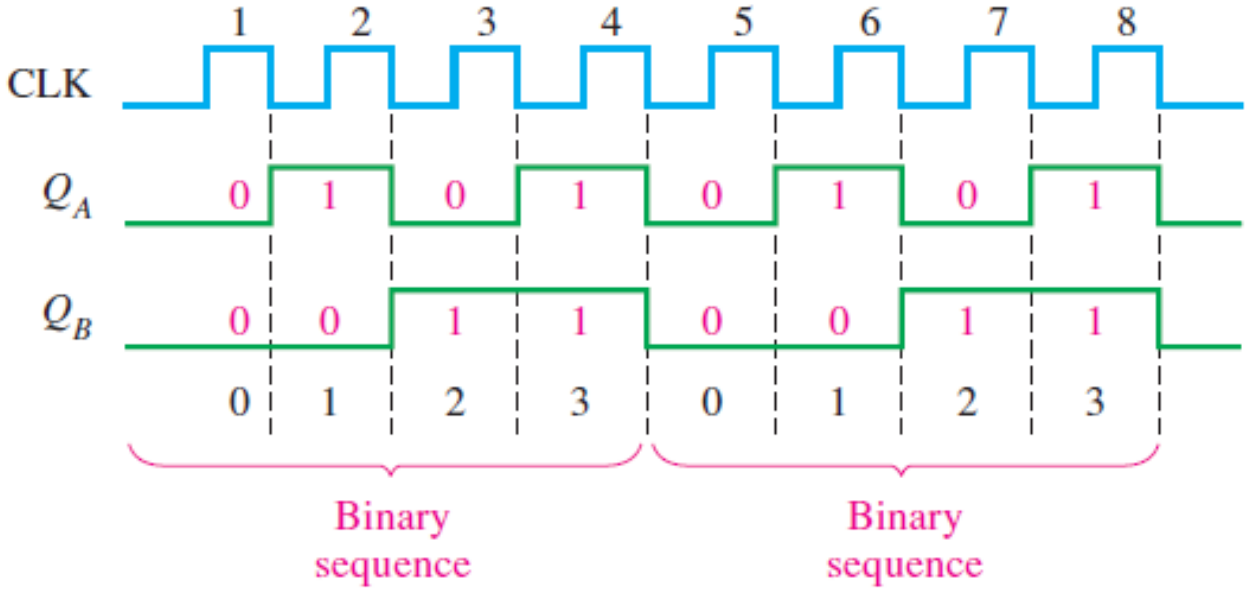


Application of Flip-Flops

COUNTING

- Flip-flops can also be used to make digital counters.
- JK flip-flops are used to make counters.
- JK flip-flop is operated in the toggle mode.
- N flip-flops are required for N-bit counters.
- Counters can be synchronous or asynchronous.





References

1. Thomas L. Floyd, “Digital Fundamentals” 11th edition, Prentice Hall – Pearson Education.

Thank You