Low Power VLSI Architecture for Reconfigurable FIR Filter

R. Loganya, S. Lavanya, S. Logasangeerani and M. Thiruveni

Abstract--- *This paper proposes an architectural approach to the design of low power VLSI for reconfigurable FIR filter. Depending on the magnitude of both the filter coefficients and inputs, the filter order can be dynamically changed. In other words, when the product of data sample and the coefficient is so small, as to reduce the effect of partial sum in FIR filter, the multiplication operation could be simply canceled. Generally, the amount of power consumption depends on the amount of operation, if dynamically cancelled off some of the multipliers; significant power savings could be achieved. However, switching activities on the multiplier lead to Dynamic Power Consumption. A Multiplier Control Signal Decision Window (MCSD) is used to solve the switching problem.*

Keywords--- *MCSD, Performance Degradation, Dynamic Power Consumption, Reconfigurable FIR Filter*

I. INTRODUCTION

DEMAND on Low power digital signal processing systems has become increased due to the tremendous growth in mobile computing. One of the most widely used operations performed in DSP is finite impulse response (FIR) filtering. The input-output relationship of the linear time invariant (LTI) FIR filter can be expressed as he following equation:

$$y(n)=\sum_{k=0}^{N-1} c_k x(n-k) \qquad (1)$$

Where N represents the length of FIR filter, c_k the kth coefficient, and x(n-k) the input data at time instant n-k . In many applications, in order to achieve high noise attenuation, FIR filters with large number of taps are necessary

II. EXISTING SYSTEM

In this section, we present already existing systems and how it consumes more power. It also describes about the previous power reduction techniques and it drawbacks.

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A. Introduction to Digital Filters

Digital filters are classified into one of two basic forms, according to how they respond to a unit impulse function: Finite impulse response or FIR filters express each output sample as a weighted sum of the last N input samples, where N is the order of the filter. FIR filters are normally non-recursive, which means they do not use any feedback and they are stable. A moving average filter is examples of FIR filters that are normally recursive (that use feedback).As FIR filter delays signals of all frequencies in an equal manner (because fir filter is linear phase as its coefficients are symmetrical)it found important in many applications. It is additionally straight advance to avoid overflow in an FIR filter. The main disadvantage is that they may require fundamentally more processing and memory resources than designed IIR variants. FIR filters are generally easier to design than IIR filters.

Infinite impulse response or IIR filters are the digital partner to analog filters. Such a filter contains internal state, and the output and the next internal state are determined by a linear combination of the previous inputs and outputs i.e., feedback is used in the case of IIR filter. In theory, the impulse response of such a filter never goes out completely, hence the name IIR, though in practice, this is not true. IIR filters normally require less computing resources than an FIR filter of similar performance. However, due to the feedback, high order IIR filters may have problems with instability, arithmetic overflow, and limit cycles, and require careful design to avoid such drawbacks. Also, since the phase shift is inherently a non-linear function of frequency, the time delay through such a filter is frequency-dependent, which can be a problem in many situations. Hence direct form FIR filter is used in most of the situations rather than an IIR filter.

B. Previous Power Reduction Techniques

In previous approaches of power reduction without changing the order of the filter, optimization of coefficient is concerned [1]-[3]. Here FIR filter structures are simplified to add and shift operations, and minimizing it is the need of hour at that time. However, one of the problems in those approaches is that in those methodologies is that once the filter architecture is chosen, the coefficients can't be changed. Consequently, those methods are not material to the FIR channel with programmable coefficients. Approximate signal processing strategies [4] are likewise utilized for the configuration of low power digital filters [5], [6]. However, the methodology in [5] experiences moderate filter order adjustment time because of its power calculations in the feedback component. Though in [6] arranging both the data samples and filter coefficients before the convolution operation has a desirable energy characteristic of FIR filter,

the overhead connected with the ongoing sorting of approaching input is very large. In Previous proposed Reconfigurable FIR filter for low power architectures, variable input word-length and filter taps, different coefficient word-lengths and dynamic reduced signal representation techniques are used. In those approaches, large overhead is caused to support reconfigurable schemes such as arbitrary nonzero digit assignment [7] or programmable shift [8].

III. PROPOSED SYSTEM

In this paper, we propose simple low power reconfigurable FIR filter architecture, where the filter order can be dynamically changed depending on the amplitude of both the filter coefficients and the inputs. The primary goal of this work is to reduce the dynamic power of the FIR filter, and the main results are as follows.

- A new reconfigurable FIR filter architecture with real-time input and coefficient monitoring circuits is presented. It can also be extended to adaptive or programmable coefficient FIR filter.
- We provide mathematical analysis of the power saving and filter performance degradation, area and delay on the proposed approach. The analysis is verified using experimental simulation results, and it can be used as a basis to design low power reconfigurable filters.

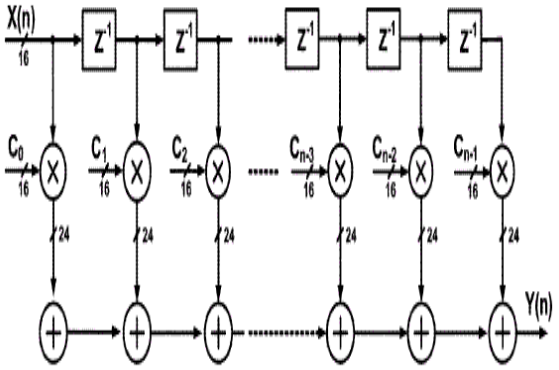

Figure 1: Architecture of Direct Form FIR Filter

The operation of original FIR filter is shown in Figure 1. FIR filtering process is based on convolution sum i.e., weighted summation of input sequences as given in (1). It consumes more power as all multiplication operation is performed. Power can be reduced dynamically by turning off some of the multipliers in traditional FIR filter.

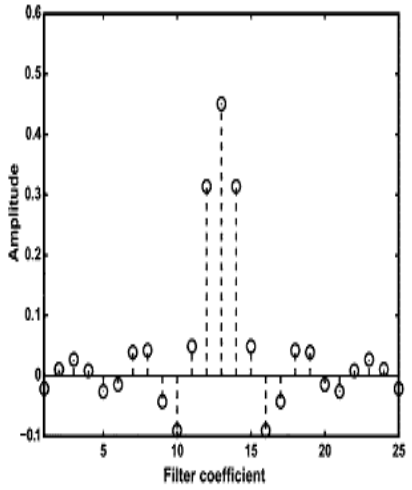

Figure 2: Amplitude of the 25-Tap Equi-Ripple Filter Coefficients

The coefficients of a typical 25-tap low-pass FIR filter are shown in Figure 2. The central coefficient has the largest value (the coefficient c12 has the largest value). The amplitude of the coefficients generally decreases as moving away from the center tap. The data input as well as the coefficient have large variations in amplitude. Therefore, the idea was that if the amplitudes of both the data input and filter coefficient are small, the multiplication of those two numbers will be obviously proportionately small. Thus, turning off such multiplier has negligible effect on the filter performance. For example, since two's complement data format is widely used in the DSP applications, if one or both of the multiplier input has negative value, multiplication of two small values gives rise to large switching activities, which is due to the series of 1's in the MSB part. By canceling the multiplication of two small numbers, reasonable power savings can be achieved with negligible filter performance degradation. In the fixed point arithmetic of FIR filter, full operand of the multiplier outputs is not generally used. In other words, as shown in Figure 1, when the bit-widths of data inputs and coefficients are 16, the multiplier generates 32-bit outputs. However, considering the circuit area of the following adders, the LSBs of multipliers outputs are usually truncated or rounded off, (e.g., 24 bits are used in Figure 1) which incurs quantization errors. When we turn off the multiplier in the FIR filter, if we can carefully select the input and coefficient amplitudes such that the multiplication of those two numbers is as small as the quantization error, filter performance degradation can be made negligible.

We need a threshold value to determine whether the input and the coefficient is small or not. When we determine threshold both performance and power savings should be balanced. We denote threshold value as x_{th} and c_{th}. When both input and the coefficient is small than this predefined threshold value, we cancel that particular multiplication operation.

IV. Architecture of Proposed Reconfigurable Fir Filter

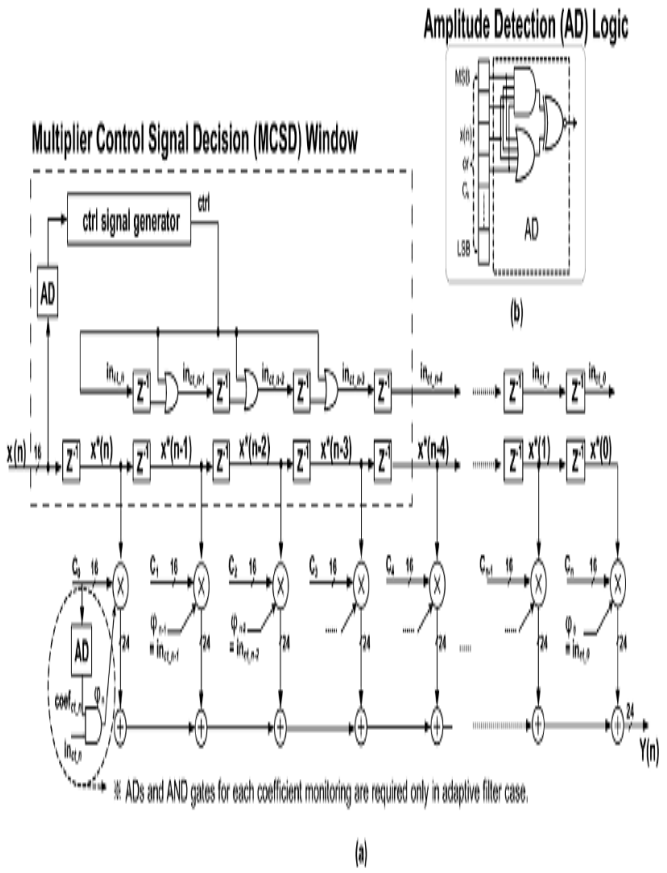

Figure 3(a): Proposed Reconfigurable FIR Filter Architecture (b): Amplitude Detection Logic

In this section, we present direct form (DF) architecture of the reconfigurable FIR filter, which is shown in Figure 3(a). In order to monitor the amplitudes of input samples and cancel the right multiplication operations, amplitude detector (AD) in Figure 3(b) is used. When the absolute value of input x(n) is smaller than the threshold , the output of AD is set to "1". The design of AD is dependent on the input threshold, where the fanin's of AND and OR gate are decided by xth. If xth and cth have to be changed adaptively due to designer's considerations, AD can be implemented by using simple comparator.

Dynamic power consumption of CMOS logic gates is a strong function of the switching activities on the internal node capacitances. In the proposed reconfigurable filter, if we turn off the multiplier by considering each of the input amplitude only, then, if the amplitude of input x(n) abruptly changes for every cycle, the multiplier will be turned on and off continuously, which causes considerable switching activities. Multiplier control signal decision window (MCSD) in Figure 3(a) is used to solve this switching problem. Using ctrl signal generator inside MCSD, the number of input samples consecutively smaller than xth are counted and the multipliers are turned off only when consecutive m input samples are smaller than xth. Here, m means the size of MCSD [in Figure 3(a), m is equal to 4]. As an input smaller than comes in and AD output is set to "1", the counter is counting up. When the counter reaches m, the ctrl signal changes to "1", which indicates that m consecutive small inputs are monitored and the multipliers are ready to turn off. One additional bit, in

Figure 3(a), is added and it is controlled by ctrl. This bit goes hand in hand with input data all the way in the following flip-flops to indicate that the input sample is smaller than xth and the multiplication can be canceled when the coefficient of the corresponding multiplier is also smaller than the threshold. Once the additional bit signal is set inside MCSD, the signal does not change outside MCSD and holds the amplitude information of the input. A delay component is added in front of the first tap for the synchronization between x*(n) and additional bit since one clock delay is needed due to the counter in MCSD. Additional Ads are required for monitoring the coefficient amplitudes in the case of adaptive filters. However, in the FIR filter with fixed or programmable coefficients, since we know the amplitude of coefficients ahead, extra AD modules for coefficient monitoring are not needed when the amplitudes of both input and coefficient are smaller than thresholds respectively, the multiplier is turned off by setting ϕ n to "1". Based on the simple circuit technique the multiplier can be easily turned off and the output is forced to "0" when the signal ϕ n is equal to one. The area overheads of the proposed reconfigurable filter are due to flip-flops for signals, AD and ctrl signal generator inside MCSD. Those overheads can be implemented using simple logic gates, and a single AD is needed for input comparing. Consequently, the overall circuit overhead for implementing reconfigurable filter is as small as a single multiplier.

V. Experimental Results

Simulation results of Reconfigurable FIR filter and its comparison with a Conventional FIR filter is shown in Table 1 below.Thus from the above simulation result it can be seen that power of the proposed Reconfigurable Fir Filter reduced drastically. The Figure 4 shows the comparison chart of Conventional FIR and Reconfigurable FIR filters in terms of power, area and delay.

Table 1: Comparison between Conventional and Reconfigurable FIR Filter

Parameter	Conventional Fir fiter	Reconfigurable Fir filter
POWER	21.28mW	12mW
DELAY	25.19 ns	27.28ns
AREA	193	210

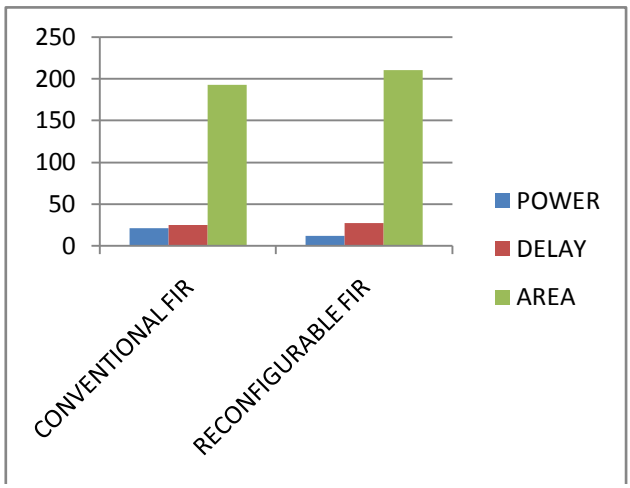

Figure 4: Comparison Charts of Conventional and Reconfigurable FIR Filter

VI. CONCLUSION

In the low power VLSI reconfigurable filter, the multiplier is turned off when the input data and coefficient are relatively low. The order of the filter is changed dynamically for power savings which results in a minor degradation in the system performance. In the application such as Digital Image Processing where the minor performance degradation may not affect the system output, this Reconfigurable filter can be used. When comparing the result of Conventional and Reconfigurable FIR filter, power is reduced drastically with small increase in area and delay. In this Reconfigurable FIR filter, Power is reduced by 43.6% with small increased area overhead of 8.8% and increased delay of 8.2%.So Reconfigurable FIR filter is well suited for Low Power Signal Processing Application where minute degradation in performance is acceptable. Our proposed approach can be extended to adaptive filter cases, where both data inputs and coefficients amplitude should be monitored simultaneously.

REFERENCES

[1] H. Samueli, "An improved search algorithm for the design of multiplier less FIR filter with powers-of-two coefficients," *IEEE Trans. Circuits Syst.*, vol. 36, no. 7, pp. 1044–1047, Jul. 1989.

[2] R. I. Hartley, "Sub expression sharing in filters using canonical signed digit multipliers," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.* vol. 43, no. 10, pp. 677–688, Oct. 1996.

[3] O. Gustafsson, "A difference based adder graph heuristic for multiple constant multiplication problems," in *Proc. IEEE Int. Symp. CircuitsSyst.*, 2007, pp. 1097–1100.

[4] S. H. Nawab, A. V. Oppenheim, A. P. Chandrakasan, J. M. Winograd, and J. T. Ludwig, "Approximate signal processing," *J. VLSI Signal Process.*, vol. 15, no. 1–2, pp. 177–200, Jan. 1997.

[5] J. Ludwig, H. Nawab, and A. P. Chandrakasan, "Low power digital filtering using approximate processing," *IEEE J. Solid-State Circuits*, vol. 31, no. 3, pp. 395–400, Mar. 1996.

[6] A. Sinha, A. Wang, and A. P. Chandrakasan, "Energy scalable system design," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 10, no. 2, pp.135–145, Apr. 2002.

[7] K.-H. Chen and T.-D. Chiueh, "A low-power digit-based reconfigurable FIR filter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53,no. 8, pp. 617–621, Dec. 2006.

[8] R. Mahesh and A. P. Vinod, "New reconfigurable architectures for implementing filters with low complexity," *IEEE Trans. Comput.-AidedDes. Integr. Circuits Syst.*, vol. 29, no. 2, pp. 275–288, Feb. 2010.

[9] Z. Yu, M.-L. Yu, K. Azadet, and A. N. Wilson, Jr, "A low power FIRfilter design technique using dynamic reduced signal representation,"in *Proc. Int. Symp. VLSI Tech., Syst., Appl.*, 2001, pp. 113–116.

[10] R. Mahesh and A. P. Vinod, "Coefficient decimation approach for realizing reconfigurable finite impulse response filters," in *Proc. IEEE Int.Symp. Circuits Syst.*, 2008, pp. 81–84.

[11] J. Park and K. Roy, "A low complexity reconfigurable DCT architecture to trade off image quality for power consumption," *J. Signal Process. Syst.*, vol. 53, no. 3, pp. 399–410, Dec. 2008.

[12] J. G. Proakis, *Digital Communications*, 3rd ed. New York: McGraw-Hill, 1995.

[13] Synopsys, Inc., Nanosim Reference Guide, 2007.

[14] S. Hwang, G. Han, S. Kang, and J. Kim, "New distributed arithmetic algorithm for low-power FIR filter implementation," *IEEE Signal Process. Lett.*, vol. 11, no. 5, pp. 463–466, May 2004.

[15] A. L. Garcia, *Probability, Statics, and Random Processes for Electrical Engineering*. Upper Saddle River, NJ: Pearson Education, 2009.