Analysis and Design of Low Power Dynamic Memory using FVD and SPD Methods

V. Agnes Christy and M. Navaneetha Velammal

Abstract--- *Dynamic gates are one of the critical circuits in RWD path of high speed memory. However these dynamic gates have poor noise immunity and their switching activity consume significant power. In this paper two dynamic domino circuits are proposed that reduce power consumption and delay at the output node. That is Footed node voltage domino method (FVD) and Switching Pulse domino method (SPD). These circuits prevent the leakage current and unwanted clock pulse during their high switching activity in precharge phase. Simulation is done by cadence virtuoso analog environment tool using 180nm technology and calculated power, delay, and speed of proposed circuit and compared results with existing domino method for power and clock frequency. This proposed domino method reduces power consumption and delay compare to standard and existing domino logic method. These circuits are placed in read out path of memory.*

Index Terms--- *Memory, Dynamic Gates, Domino Circuits, Switching Activity, Low Power Design*

I. INTRODUCTION

DYNAMIC domino logic circuits are widely used in processors and register files or memory. Dynamic circuits have more advantage than the Static circuit in memories. Static circuits require large number of transistor compare to dynamic circuits .Register files are also called as multi port memory that serves as temporary data storage in a microprocessor. The Arithmetic Logic Unit (ALU) is the heart of every microprocessor and determines its throughput. However, the High data activity associated with this unit results in high power. Memory stores a wide range of data, including the operands, intermediate results computed by an Arithmetic Logic Unit (ALU), information from the cache used by any execution units, and memory addresses of data accessed by the processor.

Domino logic circuit techniques are mostly applied in high-performance microprocessors due to the high speed and area of domino CMOS circuits as compared to static CMOS circuit's .Threshold voltage is more important in low power devices, reducing threshold voltage increase sub threshold leakage current and these dynamic domino gates are present in read path of memory. But Dynamic domino gates performance degrade with increasing the sub threshold leakage current and also the main drawback of dynamic logic circuits are more sensitive to noise in circuit compare to static circuits. Power dissipation of dynamic domino logic circuit has three part that is dynamic, leakage and short circuit power dissipation.

$$P_{TOTAL}=P_{LEAKAGE}+P_{SHORT\_CIRCUIT}+P_{DYNAMIC}\cdots (1)$$

$P_{DYNAMIC}$ is power consumed during charging and discharging of capacitance , $P_{LEAKAGE}$ is total leakage power of the domino circuit and $P_{SHORT\_CIRCUIT}$ is power dissipated when direct path between supply and gnd

$$P_{TOTAL}=V_{DD} * I_{LEAKAGE}+V_{DD} * I_{SC}+\sum_1^N \alpha_I C_I V_{DD} V_{SWING} F_{CLK}\cdots\cdots (2)$$

Where α_I is the switching activity at node I, V_{DD} is the supply voltage, V_{SWING} Voltage swing at node I , C_I is the effective switch capacitance per cycle at node I, $I_{LEAKAGE}$ is combination of sub threshold and gate oxide leakage current and I_{SC} is contention current that flows from evolution network and keeper transistor during evolution phase.

The domino logic with a new modified dynamic domino logic gates are compared and analysized. These modified methods are used for high performance and fast access of read in memory .The proposed method increases the performance and noise immunity of high performance devices.

The rest of the paper is arranged as follows, The Literature review is in second section II, then proposed system is described in III section, Result and Simulation result in section IV, the Simulations are done by cadence analog environment tool using gpdk 180 nm technology. Finally section V concludes the results of the proposed domino methods with the standard domino methods.

II. PREVIOUS WORK

The high performance memory designs are major concern of modern microprocessor. The architecture of memory has wide dynamic gate which employed in read write data path. Wide OR structure used in caches, match line of ternary constant addressable memories, comparators, De-mux, Multiplexer, and PLA. In order into improve the high performance of dynamic domino gate they were modified different domino logic method. The most popular method in dynamic domino logic gate is standard domino logic method as show as Fig: 1. Operation of the dynamic is divided into two phases that is precharge and evolution. In precharge phase Qp transistor is ON and Qe transistor is OFF then output is pulled to HIGH. Then evolution phase Qp transistor is OFF and Qe transistor is ON then output is pulled to LOW when there is a path in PDN to gnd. When the input is LOW the output is maintained HIGH in both operating node. When the

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input is HIGH the output depends on pull down network. These increases power consumption because of redundant switching.

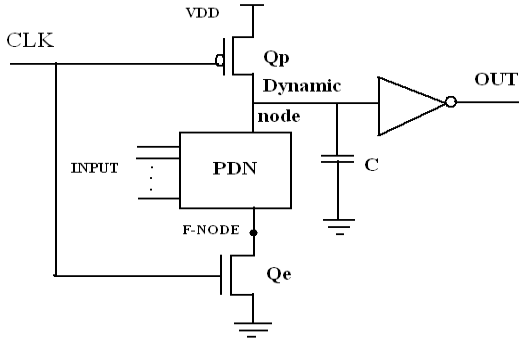

Fig.1: Standard Dynamic Domino method

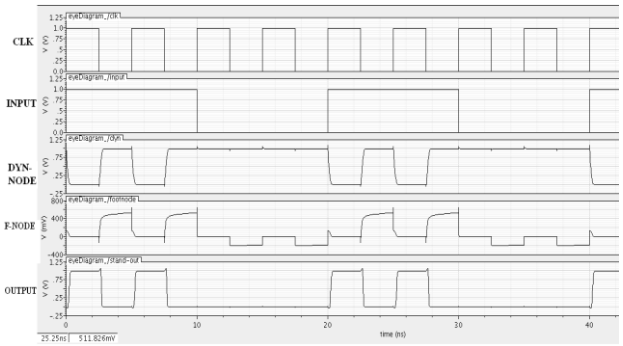

Fig. 2: Std Dynamic Domino Logic Node Characteristics

There are several technique proposed in the literature to address these issues .These dynamic domino methods has two categories, i) controlled keeper technique methods such as conditional keeper domino (CKD) method [4], High Speed domino (HPD) method [3], leakage current replica (LCR) method [6] and Static Switching Pulse Domino method [8]. ii) change of circuit topology of the footer transistor at pull down network side such as Diode Footed Domino [5] and Footed Voltage Domino methods [7].

A. High Speed Dynamic Domino Methods (HSD)

Dynamic domino logic gates require keeper transistor to overcome leakage current from evolution phase. High speed domino method as shown as Fig: 3 that circuit uses a Keeper circuit that improves noise immunity and current contention between keeper and evaluation phase. It increases the power consumption of standard dynamic domino logic circuits. This problem cause critical path to achieve better performance in dynamic node. There is a trade of between speed and performance hence the number of the keeper is limited.

B. Conditional Keeper Domino Method (CKD)

Conditional keeper domino method as shown as Fig:4. It has two added strong and weak PMOS keeper transistor which avoid unwanted discharge due to leakage current and pull down node current sharing during the evaluation period. In evolution phase weak keeper always ON the strong keeper turned ON after some delay period if dynamic node is charged by pull down network. The Main drawback is it increases external input noise at switching period.

C. Leakage Current Replica Domino Method (LCKD)

Fig: 5 shown as Leakage Current Replica Domino method which is used to overcome previous domino method noise by adding current mirror circuit in PMOS keeper circuit but this leakage current replica method require more power that affect circuit performance.

D. Static Switching Pulse Domino Methods (SSPD)

Static switching pulse domino circuit is shown in Fig: 6. The SSPD has two pull up transistors Q1 & Q2. These transistors are not turned ON simultaneously. Transistor Q1 is turned ON if dynamic node has been discharged or held low in previous cycle. SSPD has flexible turn on rise and fall delay. Q1 transistor is attached to conditional pulse generator (CPG) that provide clock pulse depends on the dynamic node charge. If dynamic node is not discharged means Q1 is OFF by conditional pulse generator.

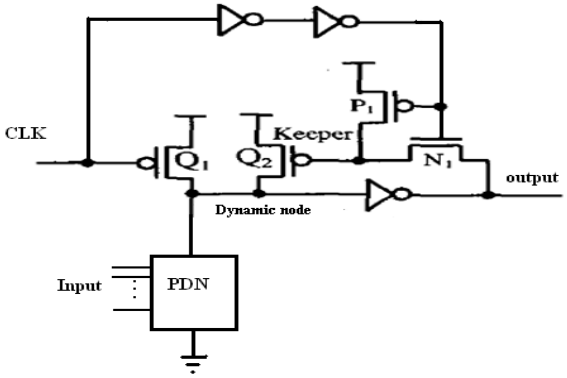

Fig. 3

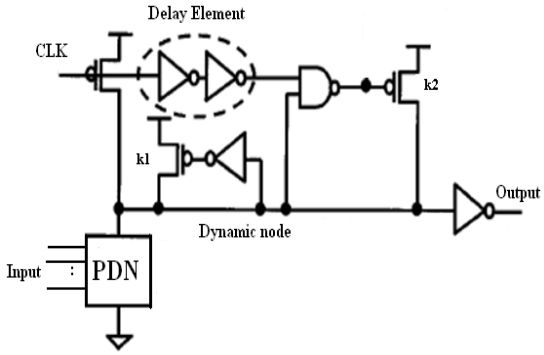

Fig. 4

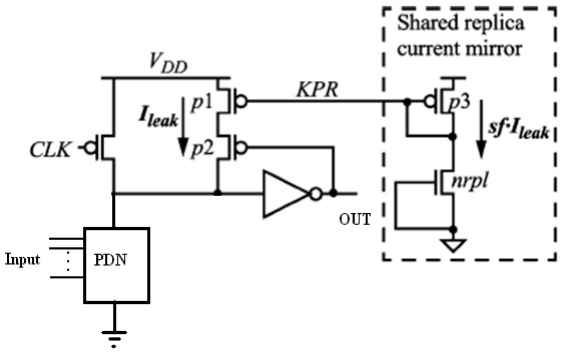

Fig. 5

This CPG generate two extra clock phases CCLKd and CCLKi where these two clock phases generate conditional delay to the CPG.This SSPD method reduce unwanted switching activities thereby reducing the power but main drawback of this method is complicated because of the presence of conditional pulse generator circuit that causes delay at signal performance.

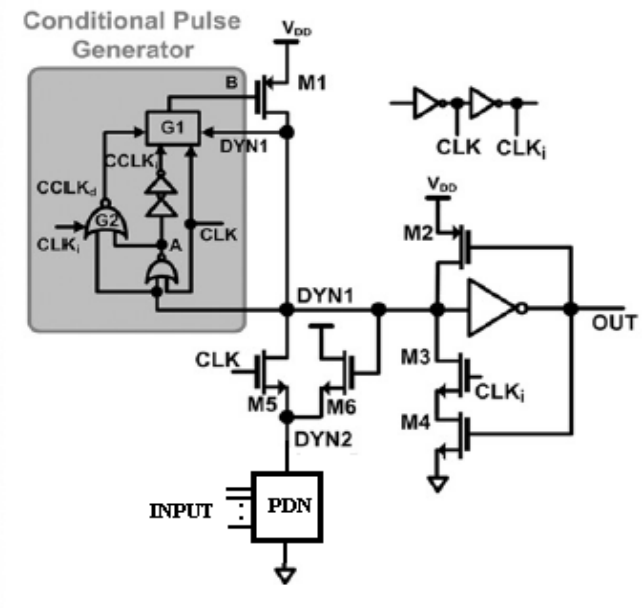

Fig. 6

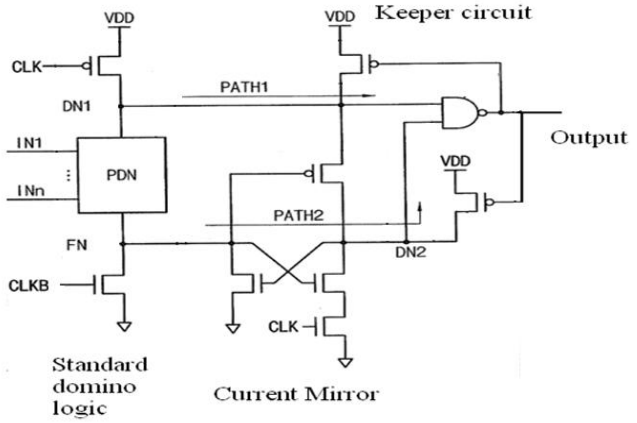

Fig. 7

E. Footed Voltage Feed Forward Domino Method (FVFD)

Footed Voltage Feed forward Domino method is shown in Fig: 7. In FVFD, the charge in the dynamic node capacitance is distributed to two nodes dynamic node 1 and footed node. During evolution phase charge sharing done by two parallel paths that is fast path and slow path. Slow path is connected to dynamic node 1 and the corresponding voltage drop is effectively utilized to evaluation phase. Fast path is connected to footed node that assist the primary evolution path. But main drawback is it consumed large switching power that affect the circuit performance and it also increase the leakage power.

III. PROPOSED SYSTEM

Dynamic domino logic circuits are designed for low power consumption in high performance devices .but high data switching activity leads to large power consumption and delay in memories. Footed node Voltage Domino method and Switching Pulse domino methods are proposed to overcome these problems in memories.

A. Switching Pulse Domino Method (SPD)

Circuit diagram of Switching Pulse Domino method shown in Fig: 8.and its selected node characteristics shown in Fig: 9. In SPD method Conditional pulse generator (CPG) is implemented at the precharge transistor. CPG has the inputs clock, delayed inverter clock and feedback output signal which generate conditional pulse G to the precharge transistor Q1 and control the function of Q1. Operation of this circuit is explained by considering input logic when input is LOW dynamic node value is high the output is static invert out that is LOW. When input is HIGH it performs two operations.

- In precharge period, CPG is LOW that turned ON precharge transistor and dynamic node is charged to vdd. Input pulldown transistor is ON output is HIGH
- In evolution period, CPG is HIGH dynamic node discharged to ground so the output is inverted output value that is HIGH.

B. Footed Node Voltage Domino Method (FVD)

Circuit diagram of Footed node Voltage Domino method shown in Fig: 10 and its selected node characteristics shown in Fig: 11. Charge sharing is main function of high performance memories. This charge charging done by two different ways that is dynamic path and footed path. FVD method has two dynamic node dyn1 & dyn2 and two footed node. Dynamic node has large capacitance so it has to limits swing voltage at both precharge and evolution phase. Dynamic node 2 is separated through footed node 1 that has rail to rail swing voltage, it reduce the switching power consumption. Operation of the circuit is considered by two ways.

- During evolution phase, dynamic node 1 path which has high parasitic capacitance and voltage discharged through pull down network. Output is evaluated through high skewed NAND gate.
- During precharge phase, clock signal is LOW precharge transistor is turned ON while footed node discharged by pulldown network. That discharge voltage given to next phase evolution.

FVD has keeper transistor & pull up keeper. Q1 &Q3 are precharge transistors for two dynamic node 1 and dynamic node 2.this circuit achieve better noise immunity compare to other domino logic circuits.

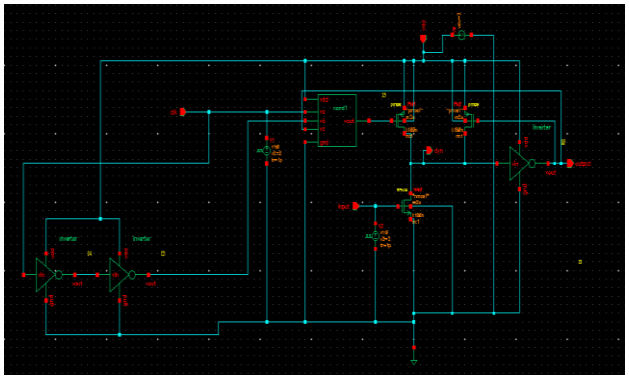

Fig. 8: Shows Switching Pulse Domino Method

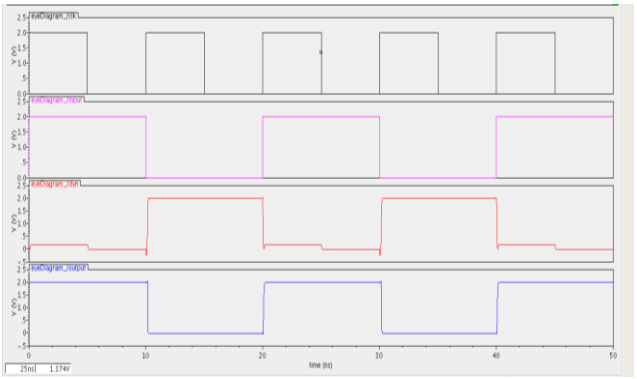

Fig. 9: SPD Selected Node Characteristics

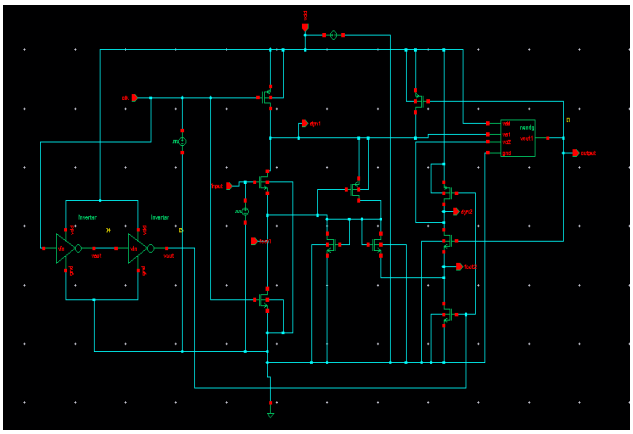

Fig. 10: Shows Footed Node Voltage Domino Method

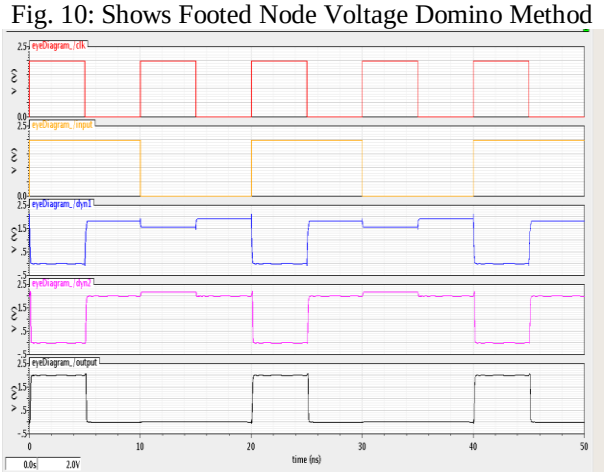

Fig. 11: FVD Selected Node Characteristics

IV. Simulation Result

The proposed circuits are simulated cadence virtuoso analog environment tool using 180 nm technologies. The supply voltage in the simulation is 2 V and clock frequency 20 GHz with clock period 10 ns. Rise and Fall time of clock rate is set equal to 1ps. Delay is determined from input to output node. Power consumption is determined when input is high voltage and standby power is measured when input of the circuit is low.

Comparison of power consumption of FVD and SPD domino circuits with Standard Dynamic Domino logic methods is tabulated in Table 1. In this comparison clock frequency, input frequency and load capacitance were set to 20GHz, 5GHz and 100 ff.

Table: 1 Comparison of Power Saving with Different Domino Logic in 180 nm (VDD=2V, Clock Frequency=10GHz and Input=5GHz)

Dynamic Domino methods	Power consumption (%)
Standard Dynamic Domino method	45.93
SPD	7.71
FVD	37.81

Comparison of power consumption with previous domino logic and proposed logic is shown in Fig: 12. As a result at higher load capacitance, SPD and FVD circuit save high power consumption as compared to standard dynamic domino method. Our proposed circuit have better power delay product as compare to other domino circuits are shown in Fig: 13

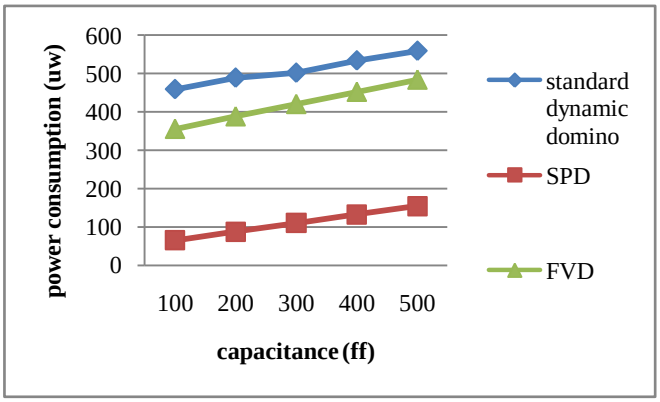

Fig. 12: Power Consumption vs Capacitance

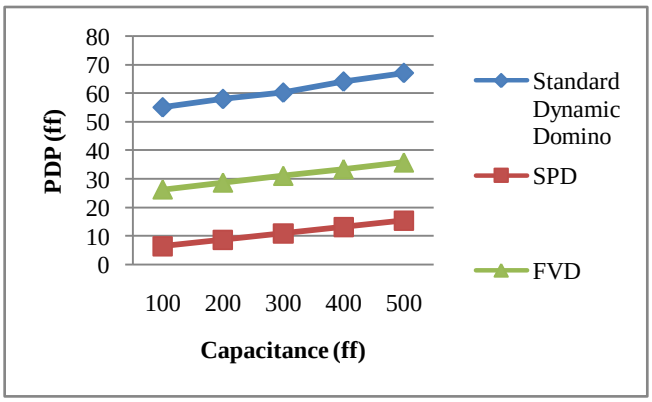

Fig. 13: Power Delay Product vs Capacitance

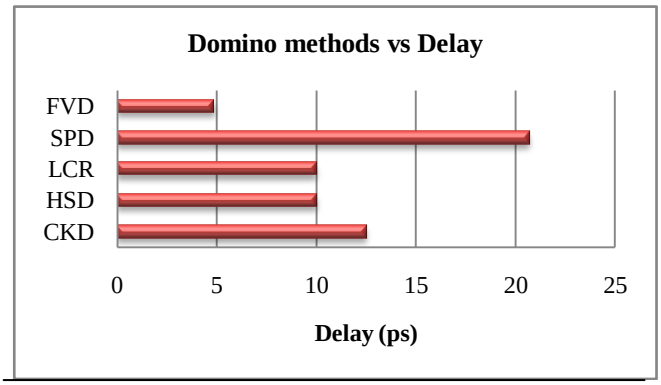

Fig. 14: Domino Methods vs Delay

In Fig: 14 Domino methods vs Delay is represented. SPD circuit suffers little delay penalty as compared with other Domino methods. Fig: 15 shows speed analysis between SPD, FVD and other Domino methods. Our proposed circuit has higher speed performance compare to other domino logic methods.

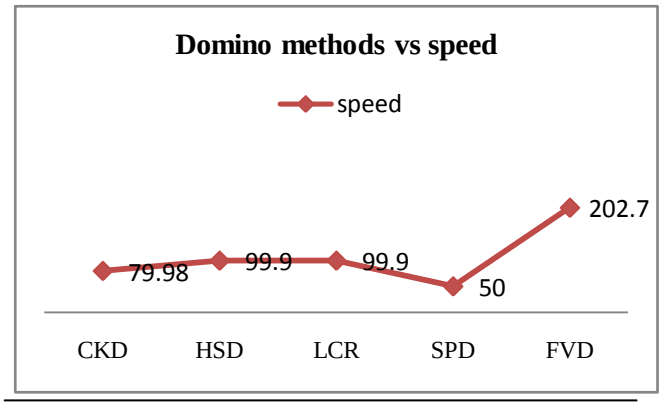

Fig. 15: Domino Methods vs Speed

V. CONCLUSION

In this paper, FVD and SPD methods are designed and simulated. FVD, SPD and other domino methods are simulated in cadence analog virtuoso tool using 180nm technologies. Performance of FVD and SPD logic circuits are compared with standard domino and other dynamic domino methods. Result shows the maximum power saving and improved speed in FVD and SPD methods.

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