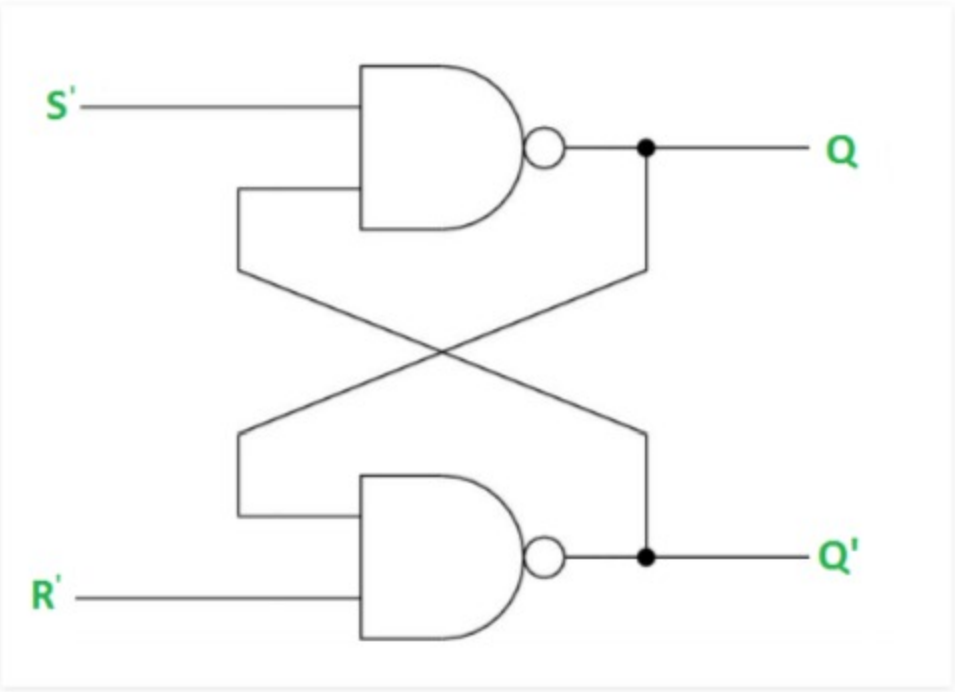
Latches in Digital Logic

Latches are basic storage elements that operate with signal levels (rather than signal transitions). Latches controlled by a clock transition are flip-flops. Latches are level-sensitive devices. Latches are useful for the design of the asynchronous sequential circuit.

SR (Set-Reset) Latch – SR Latch is a circuit with:
(i) 2 cross-coupled NOR gate or 2 cross-coupled NAND gate.
(ii) 2 input S for SET and R for RESET.
(iii) 2 output Q, Q'.

Q	Q'	STATE
1	0	Set
0	1	Reset

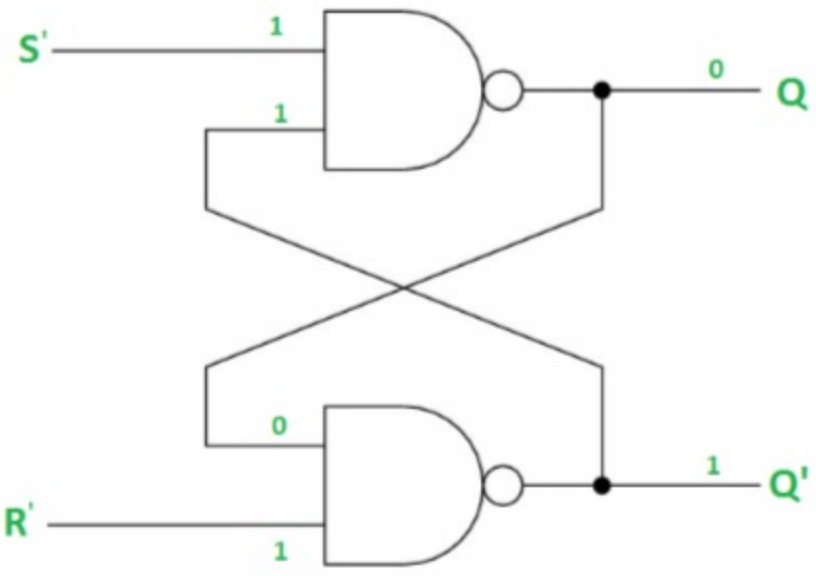
Under normal conditions, both the input remains 0. The following is the RS Latch with NAND gates:

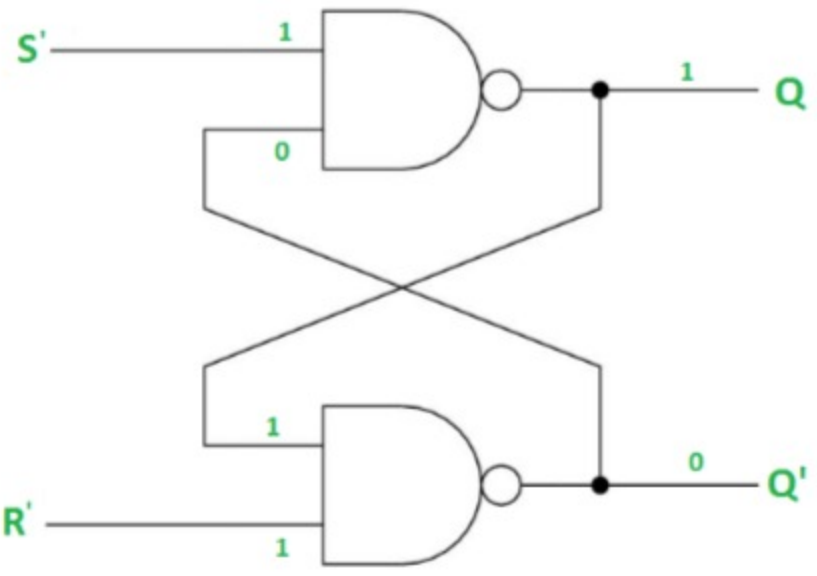


Case-1: S'=R'=1 (S=R=0) –

If Q = 1, Q and R' inputs for 2nd NAND gate are both 1.

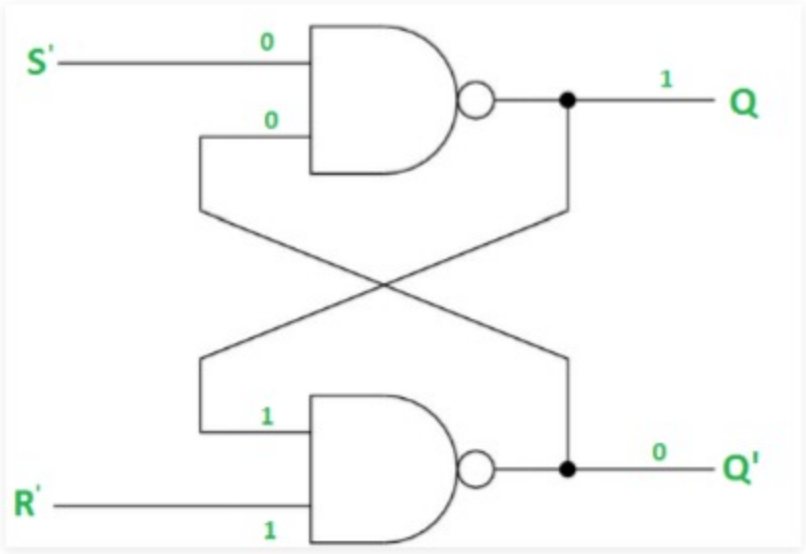
If Q = 0, Q and R' inputs for 2nd NAND gate are 0 and 1 respectively.





Case-2: S'=0, R'=1 (S=1, R=0) –

As S'=0, the output of 1st NAND gate, Q = 1(**SET state**). In 2nd NAND gate, as Q and R' inputs are 1, Q'=0.



Case-3: S'= 1, R'= 0 (S=0, R=1) –

As R'=0, the output of 2nd NAND gate, Q' = 1. In 1st NAND gate, as Q and S' inputs are 1, Q=0(**RESET state**).