Daffodil International University

Department of Computer Science & Engineering

Lab Manual

Course Code: **CSE 224**

Course Title: **Digital Electronics Lab**

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Session-1: Characteristics of AND, OR and NOT gates

Intended Learning Outcome:
To verify the input and output relationships/characteristics of 2-input AND, OR and 1-input NOT gates.

Required Instruments and ICs:

1. AT-700 Portable Analog/Digital Laboratory
   (or AT-800 Modular Lab, AT-701 Personal Lab)
2. 7404(NOT), 7408(AND), 7432(OR)

Circuit Diagram:

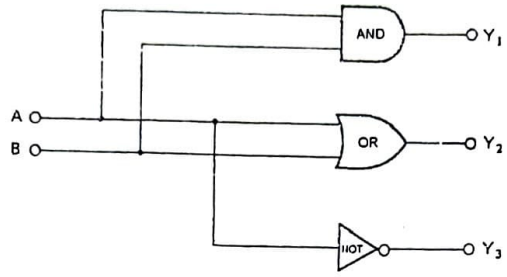
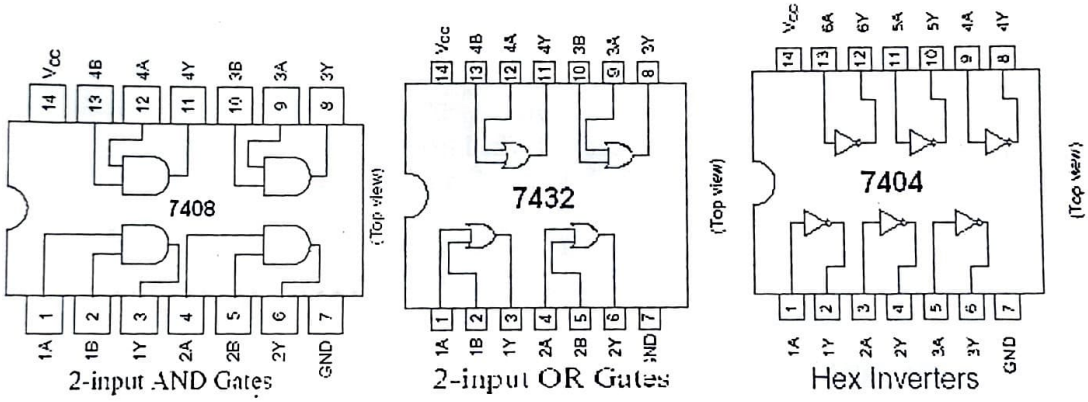


Fig 1–1



Procedure:

Step 1: Find out correctly the input and output pin numbers of each gate.
Step 2: Install the components of Fig 1-1 onto the breadboard of AT-700 and check properly the connections. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".
Step 3: Connect the Data switches "0" and "1" to point A and B of fig. 1-1 respectively. Then connect 8 bit LED Display's "0", "1" and "2" to the output of point Y1, Y2 and Y3 of Fig. 1-1 respectively. The connection diagram is as follows.

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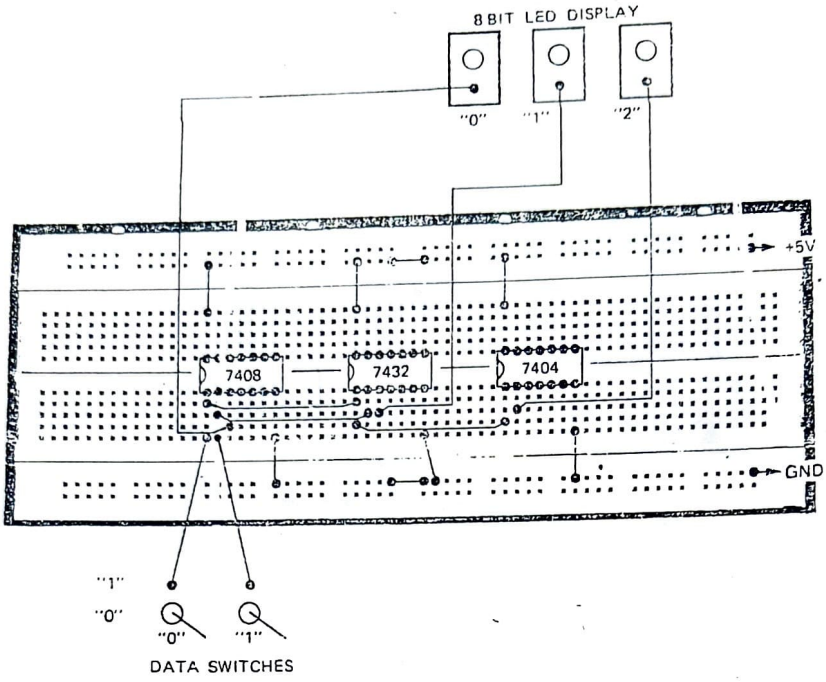

Fig 1–2

Step 4: Change Data Switches "0" and "1" between "0" and "1" position and observe the situation of 8 bit LED Display "0", "1" and "2". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition.

Step 5: Record the results that you have observed into the truth table as follows.

Truth Table 1-3

A	B	Y_1	Y_2	Y_3
0	0	0	0	1
0	1	0	1	1
1	0	0	1	0
1	1	1	1	0

Discussion & Conclusion:

The things that you should be careful while doing the experiment.

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Session-2: Characteristics of NAND and NOR gates

Intended Learning Outcome:
To verify the input and output relationships/characteristics of 2-input NAND and NOR gates.

Required Instruments and ICs:

1. AT-700 Portable Analog/Digital Laboratory
   (or AT-800 Modular Lab, AT-701 Personal Lab)
2. 7400(NAND), 7402(NOR)

Circuit Diagram:

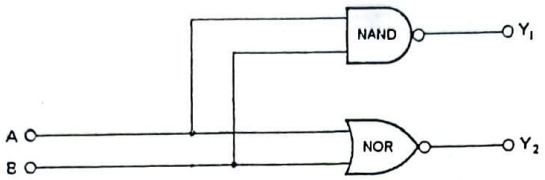
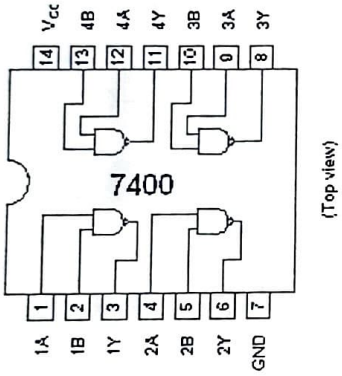
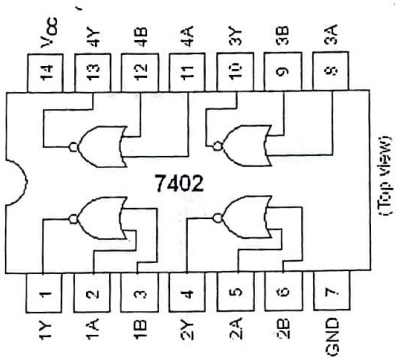


Fig 2–1





Procedure:

Step 1: Find out correctly the input and output pin numbers of each gate.
Step 2: Install the components of Fig 2-1 onto the breadboard of AT-700 and properly check the connections. Remember to connect IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".
Step 3: Connect the Data switches "0" and "1" to point A and B of fig. 2-1 respectively. Then connect 8 bit LED Display's "0" and "1" to the output of point Y1 and Y2 of Fig. 2-1 respectively. The connection diagram is as follows.

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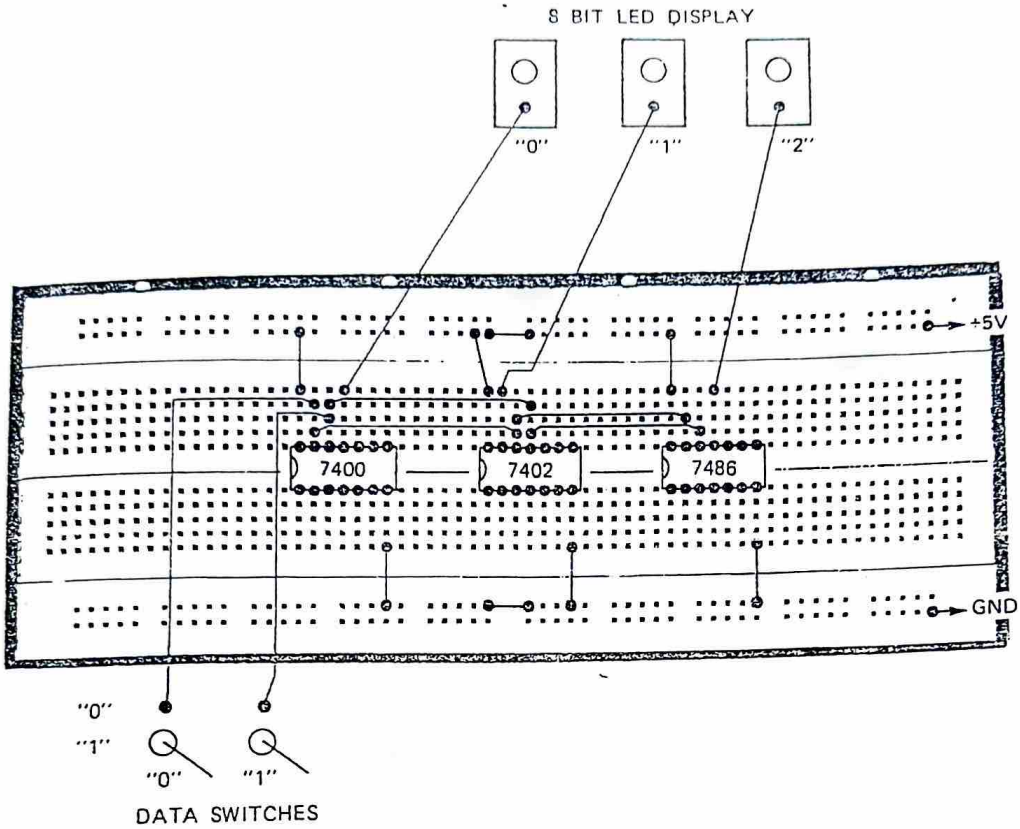

Fig 2–1

Step 4: Change Data Switches "0" and "1" between "0" and "1" position and observe the situation of 8 bit LED Display "0" and "1". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition.

Step 5: Record the results that you have observed into the truth table as follows.

Truth Table 2-2

A	B	Y_1	Y_2
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	0

Discussion & Conclusion:

The things that you should be careful while doing the experiment.

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Session-3: Verification of DeMorgan's Theorem

Intended Learning Outcome:
To verify that A.B = A + B and A+B = A . B by constructing truth tables for both sides of each of these two equations that describe DeMorgan's Theorem.

Required Instruments and ICs:

1. AT-700 Portable Analog/Digital Laboratory
   (or AT-800 Modular Lab, AT-701 Personal Lab)
2. 7404(NOT), 7408(AND), 7432(OR), 7400(NAND), 7402(NOR)

Circuit Diagram:

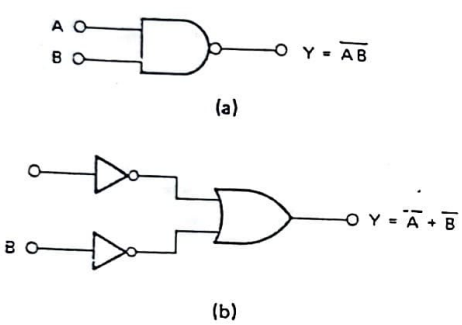

Fig 4–1

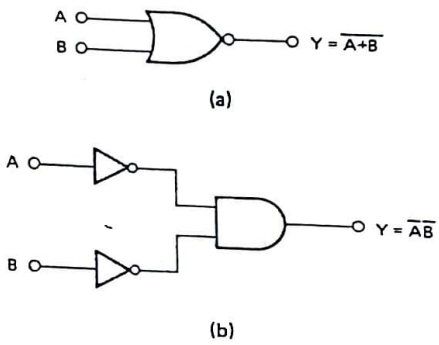

Fig 5–1

Procedure:

Step 1: Install the components of Fig 4-1 onto the breadboard as in Fig 4-2.

Step 2: Connect the Data switches "0" and "1" to point A and B and output "Y" to LED Display "0" of fig. 4-1(a). Connect the Data switches "2" and "3" to point A and B and output "Y" to LED Display "1" of fig. 4-1(b). Refer to Fig 4-2.

Step 3: Change Data Switches "0" and "1" between "0" and "1" position and observe the situation of 8 bit LED Display "0". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition. Record the results into the first empty column of Truth Table 4-3.

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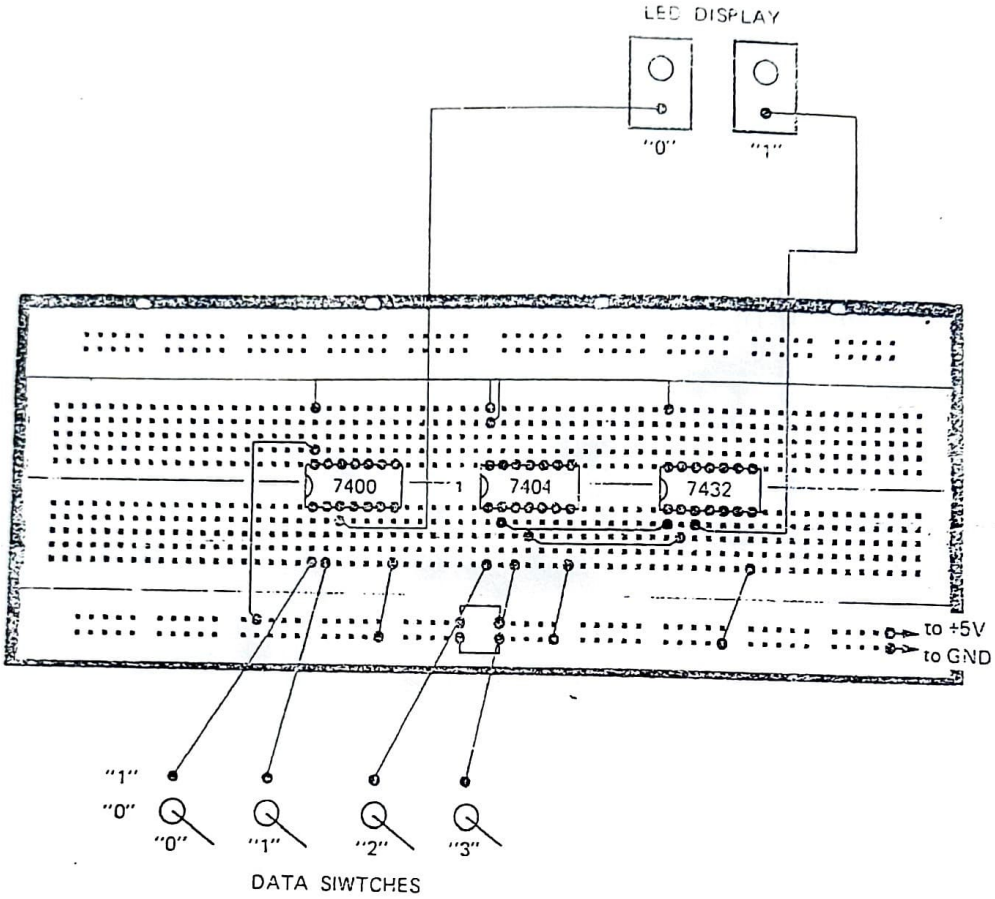

Fig 4–2

Truth Table 4-3

A	B	$Y = \overline{AB}$	$Y = \overline{A}+\overline{B}$
0	0		
0	1		
1	0		
1	1		

Step 4: Change both of the Data Switches "2" and "3" between "0" and "1" position and observe the situation of 8 bit LED Display "1". Record the results into the final empty column of Truth Table 4-3. The results of the last two columns must be identical.

Step 5: Install the components of Fig 5-1 onto the breadboard as shown in Fig. 5-2.

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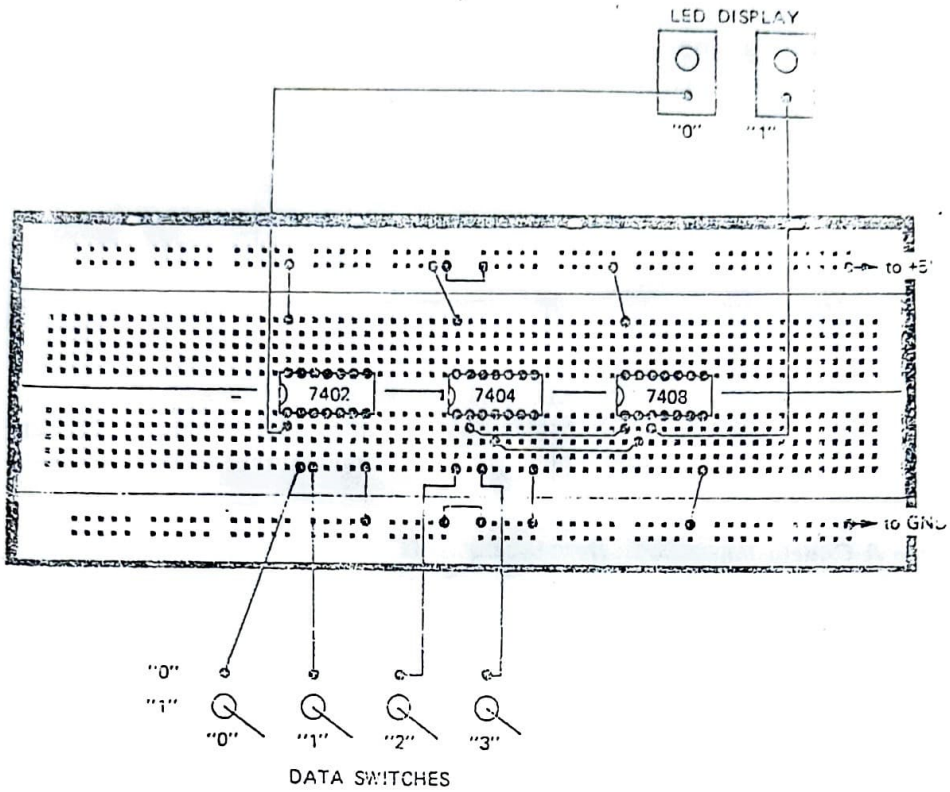

Fig 5–2

Step 6: Connect the Data switches "0" and "1" to point A and B and output "Y" to LED Display "0" of fig. 5-1(a). Connect the Data switches "2" and "3" to point A and B and output "Y" to LED Display "1" of fig. 5-1(b). Refer to Fig. 5-2.

Step 7: Change Data Switches "0" and "1" between "0" and "1" position and observe the situation of LED Display "0". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition. Record the results into the first empty column of Truth Table 5-3.

Truth Table 5-3

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A	B	$Y = \overline{A+B}$	$Y = \overline{A}\,\overline{B}$
0	0		
0	1		
1	0		
1	1		

Step 8: Change both of the Data Switches "2" and "3" between "0" and "1" position and observe the situation of 8 bit LED Display "1". Record the results into the final empty column of Truth Table 5-3. The results of the last two columns must be identical.

Discussion & Conclusion:
(On the basis of experimental results)

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Session-4: XOR, XNOR gates, parity generator and parity checker circuits

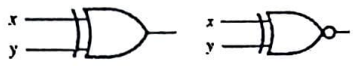
Intended Learning Outcome:

To verify the input-output relationships of XOR, XNOR gates by constructing their truth tables and implement them in parity generator and checker circuits for a 3-bit message.

Equipment Required:

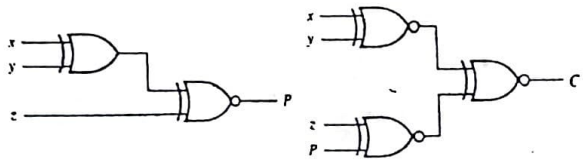
1. AT-700 portable laboratory
2. 7486(XOR), 7481(XNOR)

Circuit Diagram:



XOR gate XNOR gate

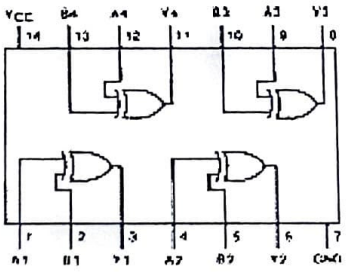
Fig 3-1



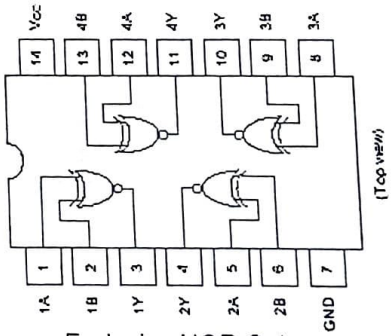
(a) 3-bit odd parity generator (b) 4-bit odd parity checker

Odd parity generator and checker circuits for a 3-bit message

Fig 3-2



Exclusive OR gates



Exclusive-NOR Gates

Procedure:

Step 1: Install the components of Fig 3-1 onto the breadboard of AT-700 and properly link the connections. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

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Step 2: Connect the Data switches "0" and "1" to point x and y of fig. 3-1 respectively. Then connect 8 bit LED Display's "0", and "1" to the outputs of the XOR and XNOR gates of Fig. 3-1 respectively.

Step 3: Change Data Switches "0" and "1" between "0" and "1" position and observe the situation of 8 bit LED Display "0" and "1". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition.

Step 4: Record the results that you have observed in the following truth table.

Truth Table 3-1

x	y	XOR	XNOR
0	0		
0	1		
1	0		
1	1		

Step 5: Install the components of Fig 3-2(a) onto the breadboard of AT-700 and properly link the connections. The parity generator circuit can also be implemented by the parity checker circuit of Fig. 3-2(b) with the *p* input permanently held at logic "0". Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

Step 6: Connect the Data switches "0", "1" and "2" to point x, y and z of fig. 3-1 respectively. Then connect 8 bit LED Display's "0" to point *p* of Fig. 3-2(a).

Step 7: Change Data Switches "0", "1" and "2" between "0" and "1" position and observe the situation of 8 bit LED Display "0". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition.

Step 8: Record the results that you have observed in the following truth table.

Truth Table 3-2

Odd parity generation

Three-bit message			Parity bit generated
x	y	z	p
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Step 9: Install the components of Fig 3-2(b) onto the breadboard of AT-700 and properly link the connections. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

Step 10: Connect the Data switches "0", "1", "2" and "3" to point x, y, z and p of fig. 3-2(b) respectively. Then connect 8 bit LED Display's "0" to point *C* of Fig. 3-2(b).

Step 11: Change Data Switches "0", "1", "2" and "3" between "0" and "1" position and observe the situation of 8 bit LED Display "0". The LED is light that indicates the output is

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in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition.

Step 12: Record the results that you have observed in the following truth table.

Truth Table 3-3

Odd parity checker

Four bits received				Parity error check
x	y	z	p	c
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Discussion & Conclusion:

(On the basis of experimental results)

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Session-5: Design and implementation of Full-adder and Half-adder Circuits using basic logic gates

Intended Learning Outcome:

Design and implementation of a Half-adder circuit using basic logic gates and cascade such two circuits to implement a Full-adder circuit.

Equipment Required:

1. AT-700 portable laboratory
2. 7408(AND), 7432(OR), 7486(XOR)

Circuit Diagram:

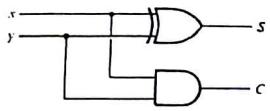


FIG. Half-adder Circuit

Truth table

x	y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

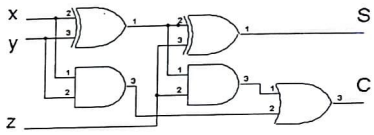
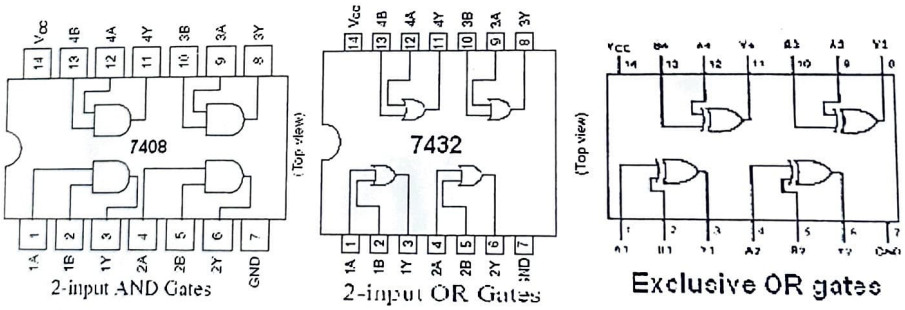


FIG. Full-adder circuit

Truth table

x	y	z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Procedure:

Half-adder Circuit

Step 1: Install the components for the Half-adder circuit onto the breadboard of AT-700 and properly link the connections.

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Step 2: Connect the Data switches "0", and "1" to point x and y of the circuit respectively. Then connect 8 bit LED Display's "0" and "1" to the points C and S respectively.
Step 3: Change Data Switches "0", and "1" between "0" and "1" position and observe the situation of 8 bit LED Display "0" and "1". Verify that the circuit realizes a Half-adder by constructing its truth table and comparing it to the one given in the figure.

Full-adder Circuit

Step 1: Install the components for the Full-adder circuit onto the breadboard of AT-700 and properly link the connections.
Step 2: Connect the Data switches "0", "1", and "2" to points x, y and z of the circuit respectively. Then connect 8 bit LED Display's "0" and "1" to the points C and S respectively.
Step 3: Change Data Switches "0", "1" and "2" between "0" and "1" position and observe the situation of 8 bit LED Display "0" and "1". Verify that the circuit realizes a Full-adder by constructing its truth table and comparing it to the one given in the figure.

Discussion & Conclusion:
(On the basis of experimental results)

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Session No-6: Design and implementation of Decoder and Encoder circuits using logic gates

Intended Learning Outcome:

This experiment is intended for the Implementation of a 2-to-4 decoder and a 4-to-2 encoder circuits using logic gates.

Equipment Required:

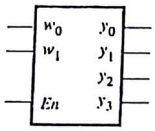
1. AT-700 portable laboratory
2. 7404(NOT), 7408(AND), 7432(OR)

Circuit Diagram:

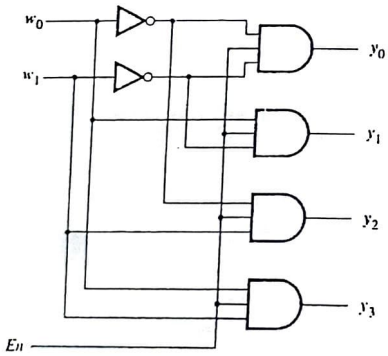
Truth table

En	w_1	w_0	y_0	y_1	y_2	y_3
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1
0	x	x	0	0	0	0

(a)



(b) Graphical symbol



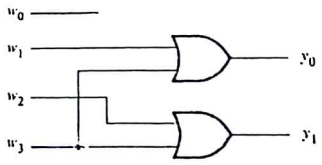
(c) Logic circuit

Fig. 8-1: a 2-to-4 Decoder circuit

Truth table

w_3	w_2	w_1	w_0	y_1	y_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

(a)



(b) Circuit

Fig. 8-2: a 4-to-2 Encoder circuit

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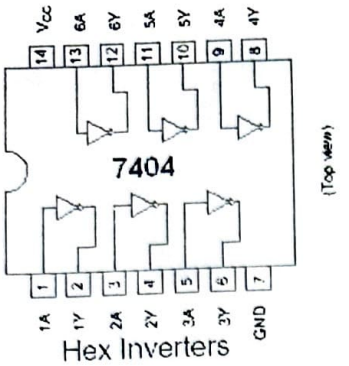

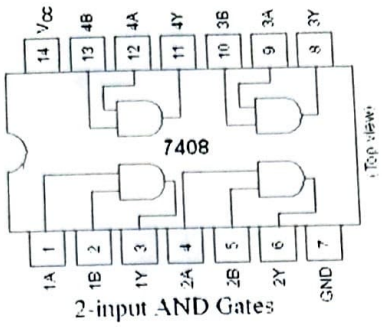

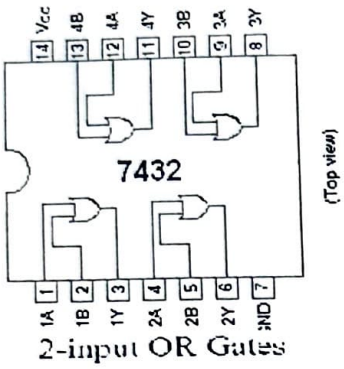

Procedure:Step 1: Install the components of Fig 8-1(c) onto the breadboard of AT-700 and properly link the connections. Use two 2-input AND gates to implement a 3-input AND gate. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

Step 2: Connect the Data switches "0", "1" and "2" to points *En, w0* and *w1* of fig. 8-1(c) respectively. Then connect 8 bit LED Display's "0", "1", "2" and "3" to the points Y0, Y1, Y2 and Y3 of Fig. 8-1(c) respectively.
Step 3: Change Data Switches "0", "1" and "2" between "0" and "1" position and observe the situation of 8 bit LED Display "0", "1", "2" and "3". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition. Reconstruct and verify the truth table of Fig. 8-1(c).

Step 4: Install the components of Fig 8-2(b) onto the breadboard of AT-700 and properly link the connections. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

Step 5: Connect the Data switches "0", "1", "2" and "3" to points *w0, w1, w2* and *w3* of fig. 8-2(b) respectively. Then connect 8 bit LED Display's "0" and "1" to the points Y0 and Y1 of Fig. 8-2(b) respectively.
Step 6: Change Data Switches "0", "1", "2" and "3" between "0" and "1" position and observe the situation of 8 bit LED Display "0" and "1". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition. Reconstruct and verify the truth table of Fig. 8-2(a).

Discussion & Conclusion:(On the basis of experimental results)

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Session-7: Design and implementation of Multiplexers

Intended Learning Outcome:

Design and implementation of a 2/1 Multiplexer using logic gates and hence design a 4/1 Multiplexer using 2/1 Multiplexer.

Equipment Required:

1. AT-700 portable laboratory
2. 7404(NOT), 7408(AND), 7432(OR)

Circuit Diagram:

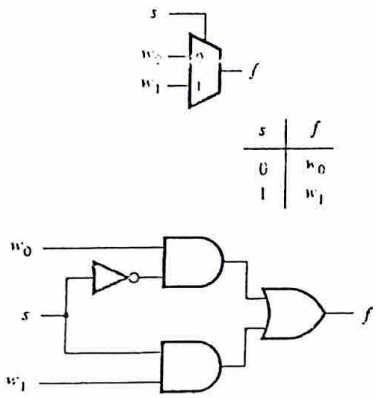


Fig. 10-1: A 2/1 MUX circuit

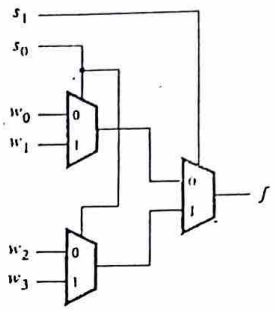
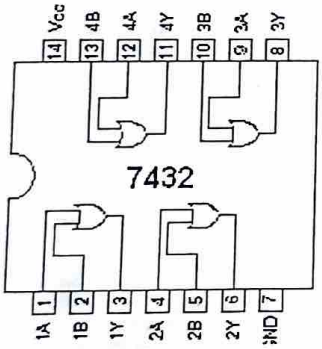
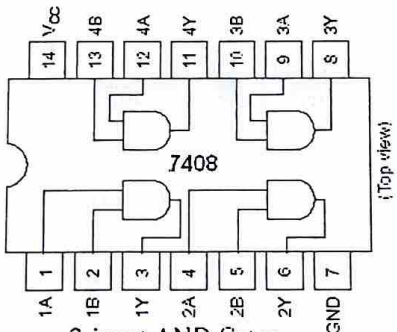


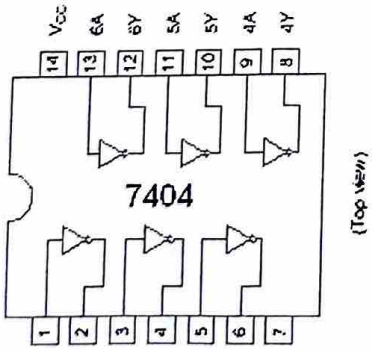
Fig. 10-2: A 4/1 MUX using 2/1 MUX



2-input OR Gates



2-input AND Gates



Hex Inverters

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Procedure:

Step 1: Install the components of Fig 10-1 onto the breadboard of AT-700 and properly link the connections. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".
Step 2: Connect the Data switches "0", "1" and "2" to points *s*, *w0* and *w1* fig. 10-1 respectively. Then connect 8 bit LED Display's "0", to the point *f* of Fig. 10-1.
Step 3: Change Data Switches "0", "1" and "2" between "0" and "1" position and observe the situation of 8 bit LED Display "0". Verify that the output follows the correct inputs as selected by the selector input *s*.
Step 4: Install the components of Fig 10-2 onto the breadboard of AT-700 and properly link the connections. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".
Step 5: Connect the Data switches to the inputs *s0, s1, w0, ... w3* fig. 10-2. Then connect 8 bit LED Display's "0", to the point *f* of Fig. 10-2.
Step 6: Change Data Switches between "0" and "1" position and observe the situation of 8 bit LED Display "0". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that he output is in the logic 0 condition. Verify that the output follows the correct inputs as selected by the selector inputs *s0* and *s1*.

Discussion & Conclusion:
(On the basis of experimental results)

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Session-8: Realization of SR latch using integrated circuit NAND and NOR gates

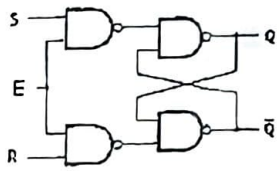
Intended Learning Outcome:

To construct SR latch circuits using NAND and NOR gate ICs separately and verify the input-output relations for both circuits.

Equipment Required:

1. AT-700 portable laboratory
2. 7400(NAND), 7402(NOR)

Circuit Diagram:



Truth Table 4-1

E	S	R	Q(t + 1)
0	x	x	Q(t) (No change)
1	0	0	Q(t) (No change)
1	0	1	0
1	1	0	1
1	1	1	x

Fig. 4-1: SR latch using NAND gates

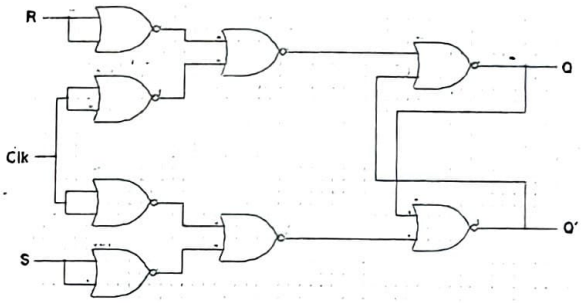
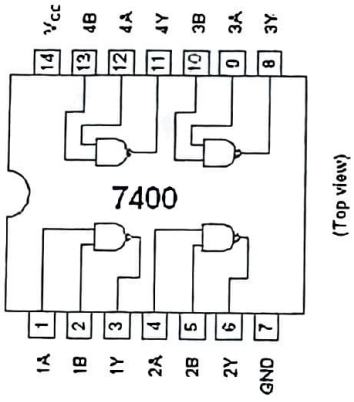
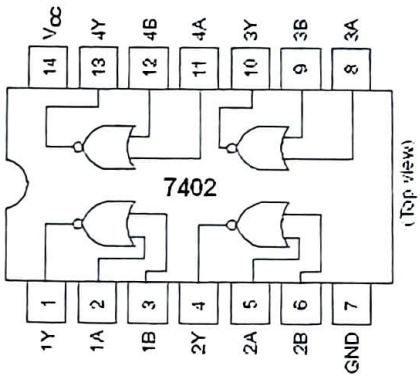


Fig 4-2: SR latch using NOR gates





Procedure:

Step 1: Install the components of Fig 4-1 onto the breadboard of AT-700 and properly link the connections. Remember to connect each IC's pin 14 to "+5V" of DC power supply of AT-700 and pin 7 to "GND".

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Step 2: Connect the Data switches "0", "1" and "2" to point E, S and R of fig. 4-1 respectively. Then connect 8 bit LED Display's "0", and "1" to the outputs Q and Q' of Fig. 4-1 respectively.

Step 3: Change Data Switches "0","1" and "2" between "0" and "1" position and observe the situation of 8 bit LED Display "0" and "1". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition.

Step 4: Record the results that you have observed in the following truth table.

Table 4

E	S	R	Q(t+1)
0	0/1	0/1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Step 5: Repeat **Step 1** to **Step 4** for the circuit of Fig 4-2.

Discussion & Conclusion:
(On the basis of experimental results)

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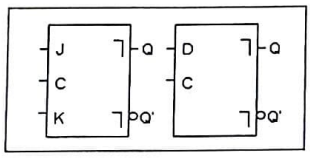
Session 9 &10: Characteristic verification of JK and D flip-flops

Intended Learning Outcome:
Familiarization with the operational characteristics of integrated circuit JK and D flip-flops.

Equipment Required:

1. AT-700 portable laboratory
2. 7476 (JK), 7474 (D)

Diagrams:



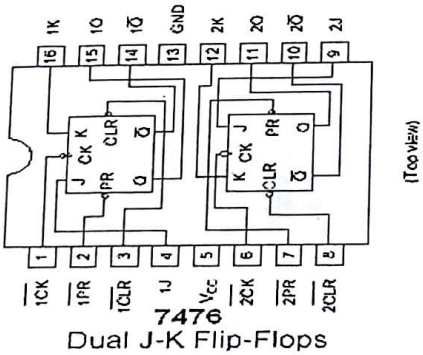
Symbols for JK and D flip-flops

Truth Table: D flip-flop

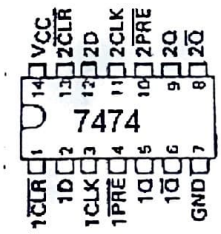
Inputs		Outputs		
D	C	Q	Q'	Comments
0	↑	0	1	RESET
1	↑	1	0	SET

Truth Table: JK flip-flop

Inputs			Outputs		
J	K	C	Q	Q'	Comments
0	0	↑	Q	Q'	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	Q'	Q	Toggle



Dual J-K Flip-Flops



Dual D Flip Flop

Procedure:

Step 1: Install the D flip-flop IC onto the breadboard of AT-700.
Step 2: Connect the Data switch "0" to D input and the Pulse "⊓" to Clk input of the flip-flop. If the flip-flop has Preset and Clear pins, deactivate them with proper logic- "0" or "1". Then connect 8 bit LED Display's "0", "1" to the output Q, Q' of the flip flop.
Step 3: Change Data Switches "0" between "0" and "1" position and press the Pulse switch "⊓" and observe the situation of 8 bit LED Display "0" and "1". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition.
Step 4: Record the results that you have observed in the following truth table.

Inputs		Outputs	
D	Clk	Q	Q'
0	↑		
1	↑		

Step 5: Install the JK flip-flop IC onto the breadboard of AT-700.
Step 6: Connect the Data switch "0", "1" to J, K inputs and the Pulse "⊓" to Clk input of the flip-flop. If the flip-flop has Preset and Clear pins, deactivate them with proper logic- "0" or "1". Then connect 8 bit LED Display's "0", "1" to the output Q, Q' of the flip flop.
Step 7: Change Data Switches "0", "1" between "0" and "1" position and press the Pulse switch ⊓ and observe the situation of 8 bit LED Display "0" and "1". The LED is light that indicates the output is in the logic 1 condition. When LED is dark, it indicates that the output is in the logic 0 condition.
Step 8: Record the results that you have observed in the following truth table.

Inputs			Outputs	
J	K	Clk	Q	Q'
0	0	↓		
0	1	↓		
1	0	↓		
1	1	↓		

Discussion & Conclusion:
(On the basis of experimental results)

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Session 11: Design and Implementation of parallel adder and subtractor using 7483

Expected Skills:

a. To realize IC7483 as the parallel adder / Subtractor.

Tools Required:

1. Digital Laboratory (or AT-800 Modular Lab, AT-701 Personal Lab)
2 IC 7483, IC 7404

Truth Table for Adder

A3	A2	A1	A0	B3	B2	B1	B0	C4(V)	S3(V)	S2(V)	S1(V)	S0(V)
0	0	0	1	0	0	1	0	0	0	0	1	1
0	1	0	1	1	0	1	1	1	1	0	0	0
1	0	1	0	1	0	1	0	1	0	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	1	1	0	0	1	1	0	1	0	1	0

Truth Table for Subtractor

A3	A2	A1	A0	B3	B2	B1	B0	C4(V)	S3(V)	S2(V)	S1(V)	S0(V)
0	0	1	0	0	0	0	1	1	0	0	0	1
0	1	0	1	0	0	1	1	1	0	0	1	0
0	0	1	1	0	1	0	1	0	1	1	1	0
1	0	1	0	0	1	1	0	1	0	1	0	0
1	0	0	0	1	1	1	1	0	1	0	0	1

Circuit Diagram:

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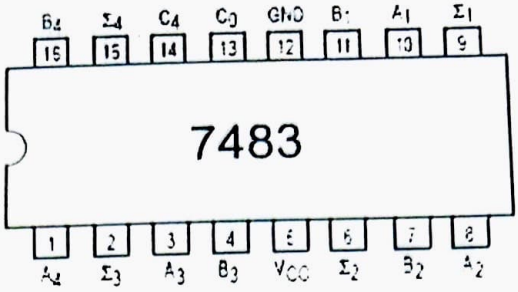
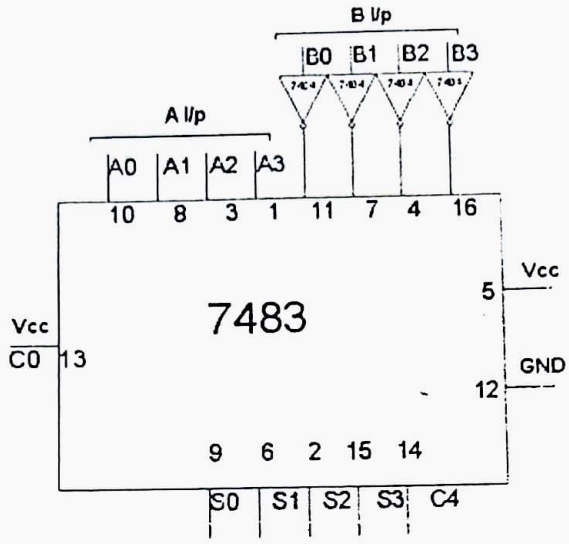
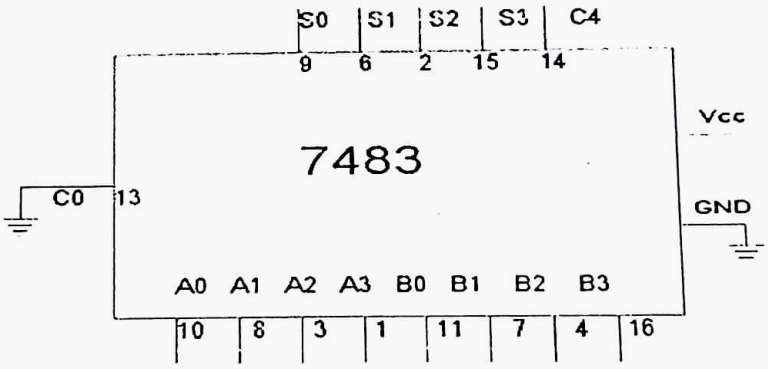
Pin Detail: -



Subtractor:



Adder: -



Procedure: -

Step-1. Apply the inputs to A0 to A3 and B0 to B3.

Step-2. Connect C0 to the Ground.

Step-3. Check the output sum on the S0 to S3 and also C4.

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Step-4. For subtraction connect C0 to Vcc, Apply the B input through NOT gate, which gives the complement of B.

Step-5. The truth table of adder and Subtractor are noted down.

Conclusion:
(On the basis of experimental results)

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Session 12: Design and implementation of BCD to Excess 3 AND Excess 3 to BCD.

Expected Skills:

a. To verify BCD to excess –3 code conversion using NAND gates. To study and verify the truth table of excess-3 to BCD code converter

Tools Required:

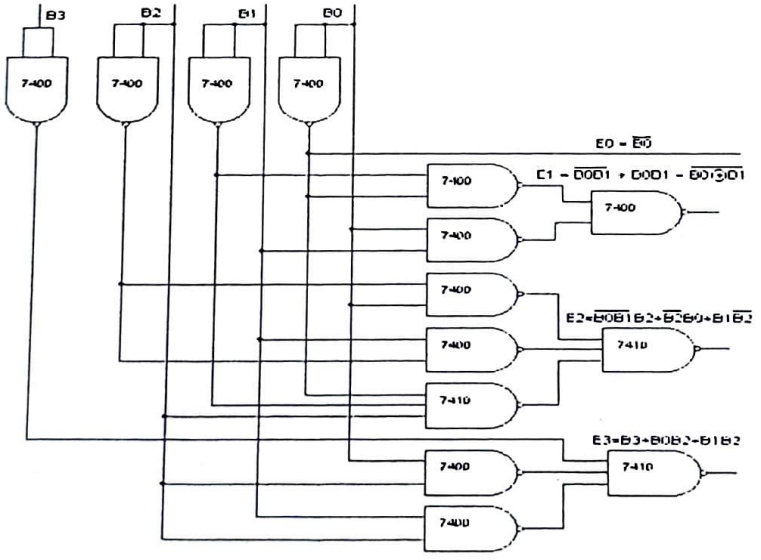
1. Digital Laboratory (or AT-800 Modular Lab, AT-701 Personal Lab)
2. IC 7400, IC 7404

Truth Table & Circuit Diagram:

Truth Table For Code Conversion: -

Inputs				Outputs			
B3	B2	B1	B0	E3 (v)	E2 (v)	E1 (v)	E0 (v)
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

BCD To Excess-3



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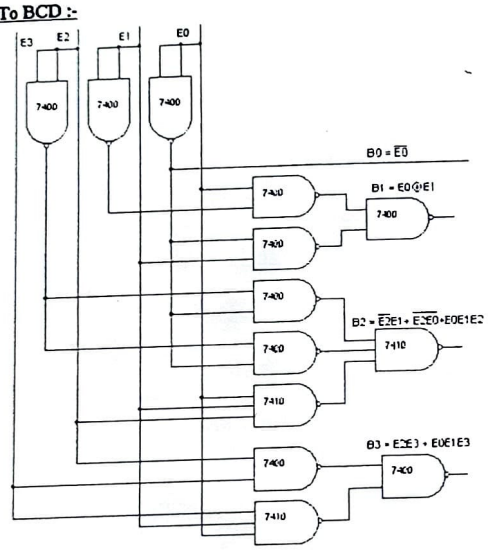
Truth Table For Code Conversion: -

Inputs				Outputs			
E3	E2	E1	E0	B3 (v)	B2 (v)	B1 (v)	B0(v)
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

Excess-3 To BCD :-



Procedure: - (BCD Excess 3 and Vice Versa)

Step-1: Make the connections as shown in the fig.

Step-2. Pin [14] of all IC'S are connected to +5V and pin [7] to the ground.

Step-3. The inputs are applied at E3, E2, E1, and E0 and the corresponding outputs at B3, B2, B1, and B0 are taken for excess – 3 to BCD.

Step-4. B3, B2, B1, and B0 are the inputs and the corresponding outputs are E3, E2, E1 and E0 for BCD to excess – 3.

Step-5. Repeat the same procedure for other combinations of inputs.

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Step-6. Truth table is written.

Conclusion:
(On the basis of experimental results)

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Session 13: Design and implementation of Flip-Flop circuit.

Expected Skills:

a. **Truth table verification of Flip-Flops:**
   - **(i) JK Master Slave**
   - **(ii) D- Type**
   - **(iii) T- Type.**

Tools Required:

1. Digital Laboratory (or AT-800 Modular Lab, AT-701 Personal Lab)
2. IC 7410, IC 7400

Truth Table & Circuit Diagram:

Truth Table:- (Master Slave JK Flip-Flop)

Preset	Clear	J	K	Clock	Qn+1	$\overline{Qn+1}$	
0	1	X	X	X	1	0	Set
1	0	X	X	X	0	1	Reset
1	1	0	0	⎍	Qn	$\overline{Qn}$	No Change
1	1	0	1	⎍	0	1	Reset
1	1	1	0	⎍	1	0	Set
1	1	1	1	⎍	$\overline{Qn}$	Qn	Toggle

D Flip-Flop:-

Preset	Clear	D	Clock	Qn+1	$\overline{Qn+1}$
1	1	0	⎍	0	1
1	1	1	⎍	1	0

T Flip-Flop:-

Preset	Clear	T	Clock	Qn+1	$\overline{Qn+1}$
1	1	0	⎍	Qn	$\overline{Qn}$
1	1	1	⎍	$\overline{Qn}$	Qn

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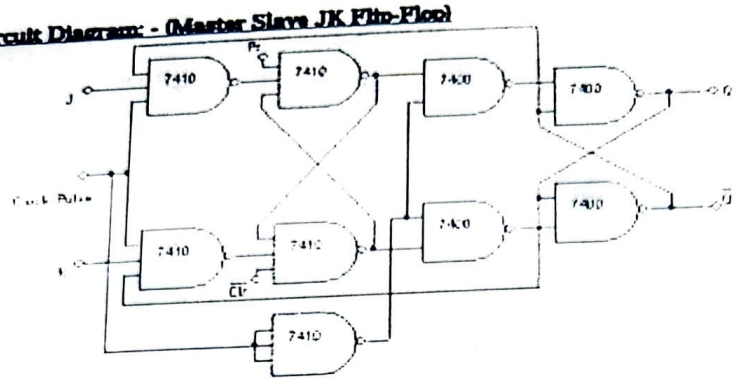
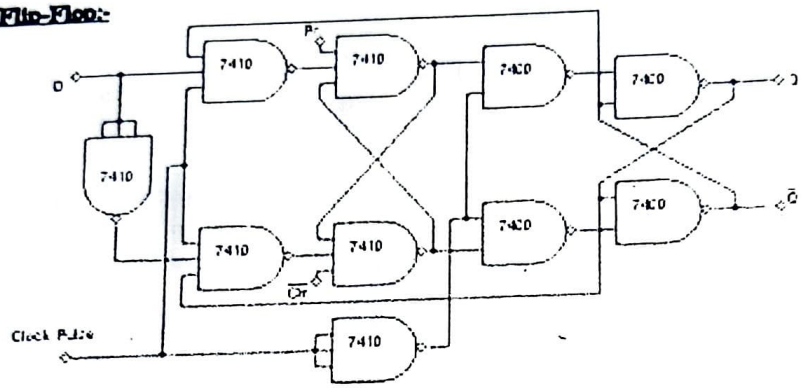
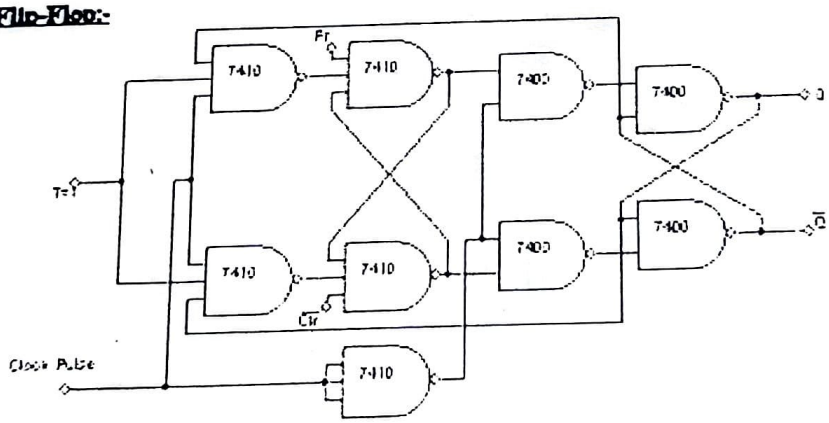
Circuit Diagram: - (Master Slave JK Flip-Flop)



D Flip-Flop:-



T Flip-Flop:-



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Procedure: -
Step-1. Connections are made as per circuit diagram.

Step-2. The truth table is verified for various combinations of inputs.

Conclusion:
(On the basis of experimental results)

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Session 14: Design and testing of Ring counter/ Johnson counter.

Expected Skills:

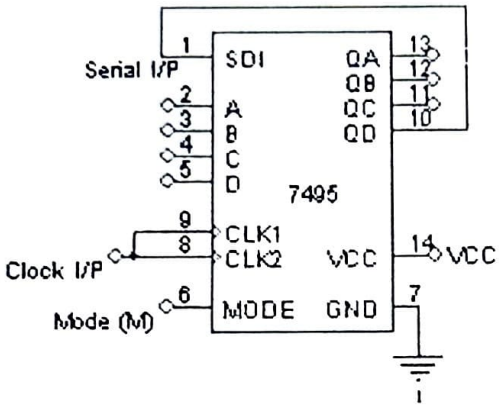
a. Design and testing of Ring counter/ Johnson counter.

Tools Required:

1. Digital Laboratory (or AT-800 Modular Lab, AT-701 Personal Lab)
2. IC 7495, IC 7404

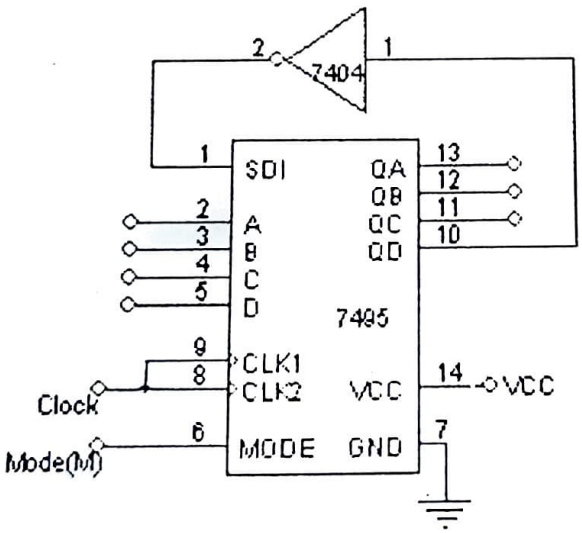
Truth Table & Circuit Diagram:

Circuit Diagram: - Ring Counter



Mode	Clock	QA	QB	QC	QD
1	1	1	0	0	0
0	2	0	1	0	0
0	3	0	0	1	0
0	4	0	0	0	1
0	5	1	0	0	0
0	6	repeats			

Johnson Counter:-



Mode	Clock	QA	QB	QC	QD
1	1	1	0	0	0
0	2	1	1	0	0
0	3	1	1	1	0
0	4	1	1	1	1
0	5	0	1	1	1
0	6	0	0	1	1
0	7	0	0	0	1
0	8	0	0	0	0
0	9	1	0	0	0
0	10	repeats			

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Procedure: -

Step-1. Connections are made as per the circuit diagram.

Step-2. Apply the data 1000 at A, B, C and D respectively.

Step-3. Keeping the mode M = 1, apply one clock pulse.

Step-4. Now the mode M is made 0 and clock pulses are applied one by one and the truth table is verified.

Step-5. Above procedure is repeated for Johnson counters also.

Conclusion:

(On the basis of experimental results)

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