Silicon Nanotube FET-Based Bio-Plausible Tripartite Synapse With Neuromodulation Capability

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***Abstract*— Realizing biomimetic synapses on hardware is crucial for enabling realistic learning and memory processes akin to the human brain in neuromorphic computing systems. The overall energy efficiency can be increased significantly, and adaptive learning and context-aware decision-making can be enabled in these systems by replicating both the plasticity and the neuromodulation capability of the biological synapses. Although several emerging nonvolatile memories exhibit synaptic plasticity, an ultrascaled bio-plausible hardware synapse with neuromodulation capability is still elusive. To this end, in this work, for the first time, we propose a highly scalable nanotube (NT) FET-based tripartite synapse that exhibits both plasticity and neuromodulation capability simultaneously. While the proposed synaptic element exploits the lateral band-to-band-tunneling (L-BTBT) gate-induced drain leakage (GIDL) mechanism for mimicking plasticity, its core gate facilitates precise modulation of the postsynaptic current (PSC) similar to the neuromodulation by astrocytes. We show that the proposed synaptic element exhibits a large dynamic range (DR), a high degree of neuromodulation, and ultralow programming energy, making it suitable for online learning.**

***Index Terms*— Nanotube (NT) FETs, gate-induced drain leakage (GIDL), lateral band-to-band tunneling (L-BTBT).**

I. Introduction

THE unprecedented growth in the field of artificial intelligence (AI) and machine learning (ML), specifically the recent surge in the development of large language models (LLMs), has necessitated the development of highly energy-efficient computing platforms that can process and store billions of model parameters [1] efficiently. However, the performance of the traditional digital computing platforms, such as general-purpose CPUs or GPUs, with decoupled processing and memory units owing to their von Neumann architecture [2], is limited by the frequent energy-hungry data transfer between the ALU and memory block and the saturating Moore's law. Therefore, alternate computing paradigms such as brain-inspired or neuromorphic computing, approximate computing, adiabatic reversible computing, and so on, have been extensively explored for AI/ML accelerators. Neuromorphic computing, owing to its massive parallelism and ultrahigh energy efficiency, is considered the most promising alternative. Furthermore, neuromorphic computing primitives utilize an extensive network of synaptic devices to connect a vast array of neurons [2]. Several emerging nonvolatile memory devices, such as resistive (R) RAMs, phase change memory (PCM), magnetic (M) RAMs, and so on, have been proposed to emulate the synaptic behavior on hardware. However, these synaptic elements exhibit an oversimplified, nonbio-plausible two-terminal architecture where the synaptic plasticity is solely governed by the spatiotemporal input spiking pattern of the pre- and postsynaptic neurons. On the other hand, the recent advancements in the field of neuroscience have revealed that information processing inside the brain is not limited to the neuronal circuitry (consisting of only neurons and synapses) but is carried out in an expanded neuron-glia network [3], [4], [5], [6]. In the mammalian brain, the glial cell known as astrocyte [3], [4] not only performs the typical "bipartite" information exchange between the pre- and postsynaptic neurons but also acts like a neuromodulator and regulates the synaptic activity between them as shown in Fig. 1. These astrocytes play a key role in neuronal programming by achieving a high order of synaptic plasticity with enhanced precision and enable the "tripartite" information exchange [5]. Precise tunability is crucial to ensure accurate modulation of neural activity, which is essential for complex cognitive functions like learning, memory, and decision-making. It also allows for dynamic and adaptive control of brain circuits, enabling precise response to the sensory inputs while maintaining functional balance between excitatory and inhibitory processes to prevent disorders such as epilepsy or neurodegenerative diseases [3]. Since neuromorphic computing involves taking inspiration from the signaling and information processing mechanisms within the brain and trying to emulate it on hardware, astrocyte functionality must be emulated within synaptic elements to realize true potential of neuromorphic hardware which can dynamically adjust to changes in input or task demands, similar to how the brain learns and adapts in real-time, enhancing flexibility and robustness of AI systems.

However, most prior hardware synaptic implementations are bipartite in nature, with only a few implementations

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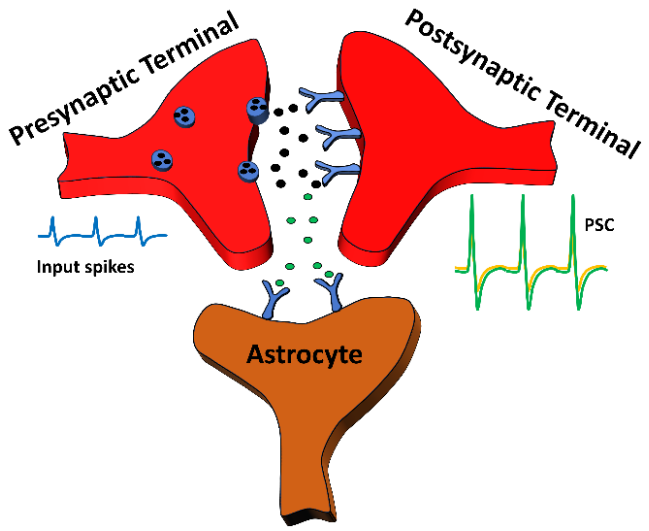


Fig. 1. Schematic of the biological tripartite synapse connecting the pre- and postsynaptic neurons with the astrocyte as the neuromodulator.

addressing the tripartite synapses. For instance, a 2D-heterostructure-based gate-tunable synaptic transistor (called synaptic barrister) [7] and a 2-D WSe_2 and WO_3-based mem-transistor [8] were proposed recently to emulate a tripartite synapse. Moreover, a junctionless (JL) transistor with Si-doped HfO_2 as the ferroelectric layer [9] and a thin-film transistor (TFT) with ferroelectric capacitor connected to the gate electrode [10] were also used to demonstrate a synaptic element with neuromodulation capability. However, these tripartite synapse implementations [7], [8], [9], [10] exhibit a large footprint, low endurance, high operating voltage, and large spatial and temporal variation owing to their immature fabrication technology, which limits their widespread application in online training accelerators.

Considering the urgent need for highly scalable astrocyte functionality-embedded hardware synaptic implementations for online training accelerators, in this work, for the first time, we explore the potential of nanotube (NT) JL field-effect transistor NT JL FET (NT JLFET) as a tripartite synaptic element. Utilizing experimentally calibrated TCAD simulations, we show that the proposed NT JLFET-based synaptic element exhibits a high degree of plasticity with large dynamic range (DR), exploiting the otherwise undesirable lateral band-to-band-tunneling (L-BTBT) gate-induced drain leakage (GIDL) mechanism, with ultrafast (∼ns) program/erase pulses at significantly lower operating voltages (and energy) even at ultra-scaled device dimensions. Furthermore, the astrocyte functionality (neuromodulation) can be emulated using the core gate of the NT JLFET, and the maximum and minimum achievable synaptic conductance can be precisely tuned and further modulated by a factor of $\sim 10^2$ and $\sim 10^4$, respectively, with the aid of the core gate voltage. Furthermore, we have also provided comprehensive design guidelines for further increasing the DR and synaptic plasticity in the proposed tripartite synapse.

II. Device Structure and Simulation Framework

The 3-D structure and 2-D cross-sectional view of the proposed NT JLFET-based tripartite synapse are shown in Fig. 2, and its structural parameters are reported in Table I. The NT JLFET is essentially a vertical nanowire FET with a shell gate that wraps around the uniformly doped ($N_D = 10^{19}$ cm^{-3}) silicon film in the channel region and an additional core gate that spans from the channel region to the drain region [11]. While the diameter of the core gate (d_{core}) inside the channel region is 20 nm, the thickness of the core gate in the drain region, where the core gate overlaps with the drain region (t_{gcd}), is kept intentionally small to reduce the gate-to-drain Miller capacitance (c_{gd}), which may degrade the dynamic performance.

Furthermore, silicon NTs have already been experimentally demonstrated using high-precision plasma-treated nanosphere lithography and reactive ion etching (RIE) [12]. NT JLFETs with a core gate may be fabricated using similar process steps as NT MOSFETs [13], [14], [15]. The proposed NT JLFET-based tripartite synapse may be fabricated on a silicon-on-insulator (SOI) substrate, comprising a handle substrate, a buried insulator, and a silicon device layer, using the process

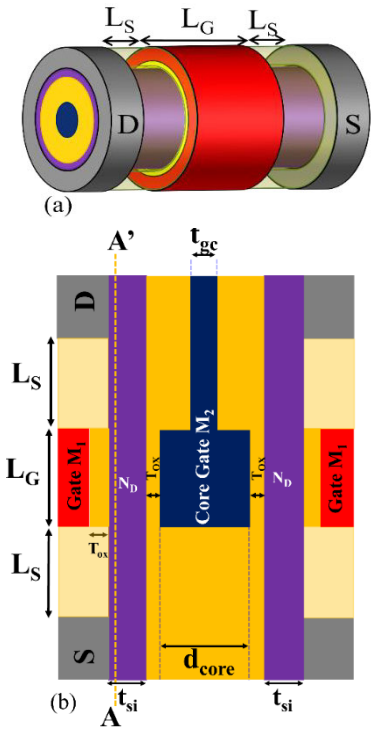


Fig. 2. (a) 3-D view and (b) 2-D cross-sectional view of the proposed NT JLFET-based tripartite synapse.

TABLE I
Structural Parameters

Parameters	Values
Silicon film Doping (N_D)	$N_D = 10^{19}$ cm^{-3}
Core Gate diameter (d_{core})	20 nm
Gate Contact Thickness (T_{gc})	5 nm
Silicon Film thickness (t_{si})	10 nm
Gate length (L_G)	20 nm
Spacer length (L_S)	25 nm
Spacer thickness (t_{sp})	5nm
Effective oxide (SiO_2) thickness (T_{OX})	1 nm
work function (outer shell gate M_1 / core gate M_2)	5.2 eV / 4.5 eV

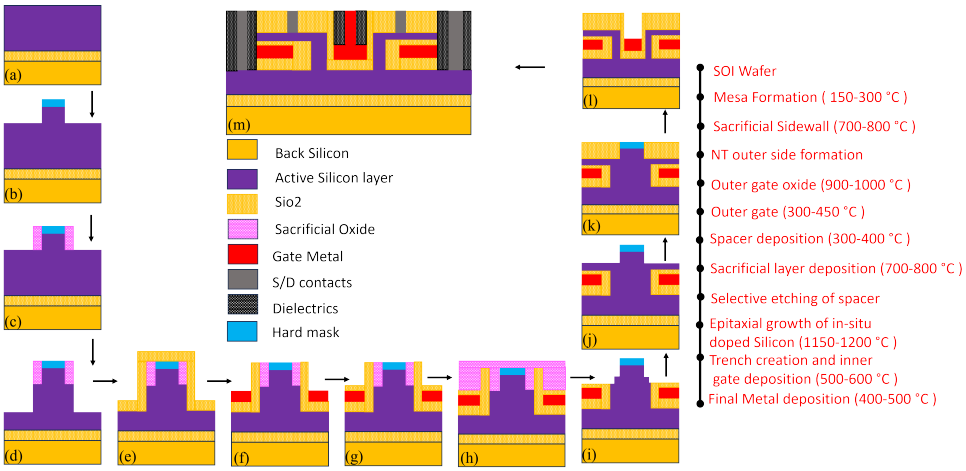


Fig. 3. Suggested fabrication flow for realizing NT JLFETs.

flow suggested in Fig. 3. A hard mask, such as silicon nitride, can be deposited on the SOI layer to define the cylindrical structure. Using photolithography and RIE, the hard mask can be patterned and etched into the cylindrical shape. The exposed silicon can then be vertically etched to create a mesa structure with the desired cylindrical geometry as shown in Fig. 3(b). Tight process control of this etching step is needed for creating a mesa island with high yield, since it defines the overall diameter of the inner gate, and this process may introduce variability through line edge roughness (LER) of the photoresist, directly translating to fluctuations in the silicon film thickness. Next, a sacrificial dielectric layer, such as silicon dioxide, can be deposited and etched back around the mesa to define the outer geometry of the NT as shown in Fig. 3(c) and (d). A gate dielectric layer and the outer shell gate electrode material can then be subsequently deposited, and excess material can be removed through planarization and etching, forming the outer gate structure as shown in Fig. 3(e)–(i). An epitaxial silicon layer can be grown to realize the source and drain regions as shown in Fig. 3(j). Since epitaxial silicon growth is typically a high-temperature process (∼1150 °C–1200 °C), it can potentially lead to degradation (and even melting) of the outer shell gate metal (deposited before the epitaxial growth). Therefore, it restricts the choice of materials available for realizing the outer shell gate-stack. However, for realizing efficient volume depletion, the outer shell gate of the NT JLFET should have a high work function (≥5.1 eV), and metals with high work function, such as palladium and platinum, can withstand the elevated temperatures required for epitaxial growth without reaching their melting points (>1500 °C). Also, since the epitaxial growth process creates the active layer of the proposed tripartite synapse, stringent process control is required over temperature fluctuations (which dictate doping uniformity), gas flow dynamics (which dictate growth uniformity), and growth chamber environment (which may introduce batch-to-batch inconsistency and crystallographic defects). The inner portion of the cylindrical silicon layer can then be etched to create a hollow tube while maintaining a concentric geometry. A dielectric layer can be deposited inside the hollow cylinder to serve as the inner gate dielectric. The trench can be filled with a conductive material to form the inner core gate, and sidewall spacers can be added around the inner core gate to electrically isolate it from surrounding regions. Finally, trenches can be etched to provide access to the inner core and outer shell gates, as well as the source and drain regions, as shown in Fig. 3(m). Also, gate sidewall spacers are crucial during the fabrication of NT FETs [13], [14], [15], [16], and we have used SiO_2 spacers in this work.

For analyzing the synaptic properties of the proposed NT JLFETs, 3-D device simulations were carried out using the Sentaurus TCAD release Version S-2021.06 [17]. To capture field- and doping-dependent mobility degradation, the Lombardi mobility model and the Philips unified mobility model were included. The Auger recombination model and Fermi–Dirac statistics were also invoked. Since the silicon film is heavily doped (10^{-19} cm^{-3}), the Slotboom bandgap narrowing model and the doping-dependent Shockley–Read–Hall (SRH) recombination model (which reduces the carrier lifetimes to $\sim 10^{-7}$ s corresponding to a silicon film doping of 10^{-19} cm^{-3}) were also included. Furthermore, the non-local BTBT model was activated to consider the L-BTBT GIDL mechanism, which is dominant in JLFETs [11]. Since quantum confinement effects are insignificant for silicon thickness ≥7 nm [18], quantization effects were not considered. Furthermore, the simulation setup was calibrated by reproducing the experimental results for nanowire JLFETs with three different nanowire widths [19] and the results for NT JLFET for a gate length of 15 nm, as shown in Fig. 4. The values of the tunneling mass of electrons $m_e = 0.4\ m_0$ and holes $m_h = 0.65\ m_0$ and the effective density of states for holes $g_v = 0.66$ and electrons $g_c = 2.1$ were tuned to reproduce the experimental data. It may be noted that the main objective of this work is to demonstrate the potential of NT JLFETs as tripartite synaptic element rather than showing the exact values of currents although the TCAD simulation framework utilized in this work is well established [22], [23],

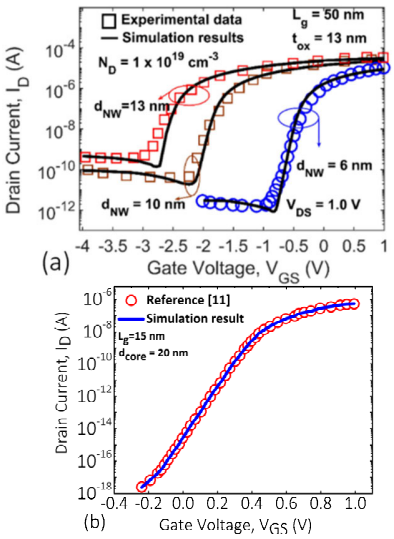


Fig. 4. Calibration of the simulation setup by reproducing the experimental results of (a) NW JLFETs [19] and (b) NT JLFETs [11].

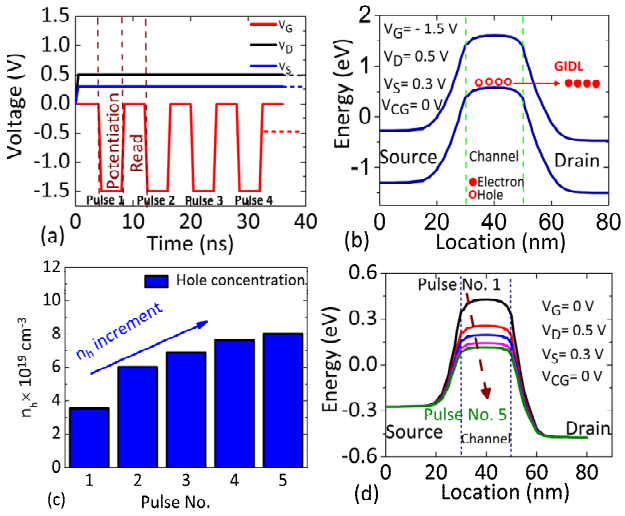


Fig. 5. (a) Voltage waveform utilized for potentiation and read operation. (b) Energy band profile of the proposed NT JLFET-based synapse at a cutline taken 1 nm below the Si–SiO_2 interface during the potentiation operation, clearly indicating L-BTBT GIDL leading to accumulation of holes in the channel region. (c) Maximum hole concentration ($n_h \times 10^{19}$ cm^{-3}) in the channel region of the NT JLFET-based synapse with the number of potentiation pulses. (d) Conduction band energy profiles during the read operation after several consecutive potentiation pulses.

[24], [25], [26], [27], [28] and also validated by accurately reproducing the experimental characteristics of an ultrascaled V-groove JLFET with a channel length of 3 nm and channel thickness of 1 nm in [20].

III. Results and Discussion

The gate-all-around architecture in nanowire FETs not only leads to an efficient control of the channel charge and an enhanced electrostatic integrity but also results in a significant band bending even in the OFF-state ($V_{GS} = 0$ V) which results in considerable proximity of the valence band of the channel region and the conduction band of the drain region [21], [22], [23], [24], [25], [26], [27], [28]. This band overlap results in the dominant L-BTBT GIDL mechanism in nanowire FETs, which leads to hole accumulation in the channel region and induces floating body effects including triggering of a parasitic BJT in the OFF-state [21], [22], [23], [24], [25], [26], [27], [28]. Since L-BTBT GIDL originates due to an efficient gate control [21], [22], [23], [24], [25], [26], [27], [28], the introduction of a core gate in the nanowire MOSFETs to realize NT MOSFETs with even better electrostatic integrity increases the L-BTBT GIDL further [16]. L-BTBT is induced at the channel-drain interface underneath the outer shell gate as well as the inner core gate surface in NT MOSFETs [16]. As a result, the hole accumulation-induced floating body effects, such as the parasitic BJT action, are more dominant in the NT MOSFETs [16]. However, the introduction of a core gate with a high work function in NT JLFETs depletes the channel region at the channel–drain interface underneath the core gate surface, leading to a larger tunneling width for L-BTBT and a larger effective base width of the parasitic BJT, diminishing the current gain and the consequent floating-body effects [11]. Therefore, the core gate can be used as an effective tool to modulate the L-BTBT GIDL in NT FETs (diminishing the parasitic BJT action in NT JLFETs [11] while leading to the dominant floating-body effects in NT MOSFETs [16]).

In this work, we exploit a core gate with a midgap work function in NT JLFETs and use the independent core gate voltage-based modulation of the L-BTBT GIDL-induced floating-body effects in NT JLFETs to emulate two different types of synaptic elements: 1) a bipartite synapse without any neuromodulation capability and 2) a tripartite synapse with astrocyte-mimetic neuromodulation.

A. NT JLFET as a Bipartite Synaptic Element

We first propose an NT JLFET with a grounded core gate, that is, core gate voltage, $V_{CG} = 0$ V, which mimics the bipartite synaptic functionality, facilitating information exchange between the pre- and postsynaptic neurons without astrocyte-like neuromodulation. To realize bio-plausible synaptic plasticity, including long-term potentiation (LTP) and long-term depression (LTD) in the NT JLFET-based bipartite synapse, we exploit the outer shell gate-induced L-BTBT GIDL, which results in the generation and accumulation of holes in the channel region (yielding potentiation) and their recombination with majority electrons (leading to depression).

The LTP is performed by applying an identical train of negative pulses to the outer shell gate (V_G) with a pulsewidth of 4 ns and amplitude of −1.5 V, as illustrated in Fig. 5(a) while keeping the drain (V_D) and source (V_S) electrodes pinned to 0.5 and 0.3 V, respectively. Application of a negative outer shell gate voltage ($V_{GS} \leq 0$ V) triggers L-BTBT GIDL along the channel–drain interface underneath the shell gate surface, leading to the generation of holes and their accumulation in the channel of NT JLFETs, as shown in Figs. 5(b) and 6(a). Each subsequent negative voltage pulse applied at the outer shell gate further increases the band bending and reduces the tunneling width between the valence band of the channel region and the conduction band of the drain region, leading

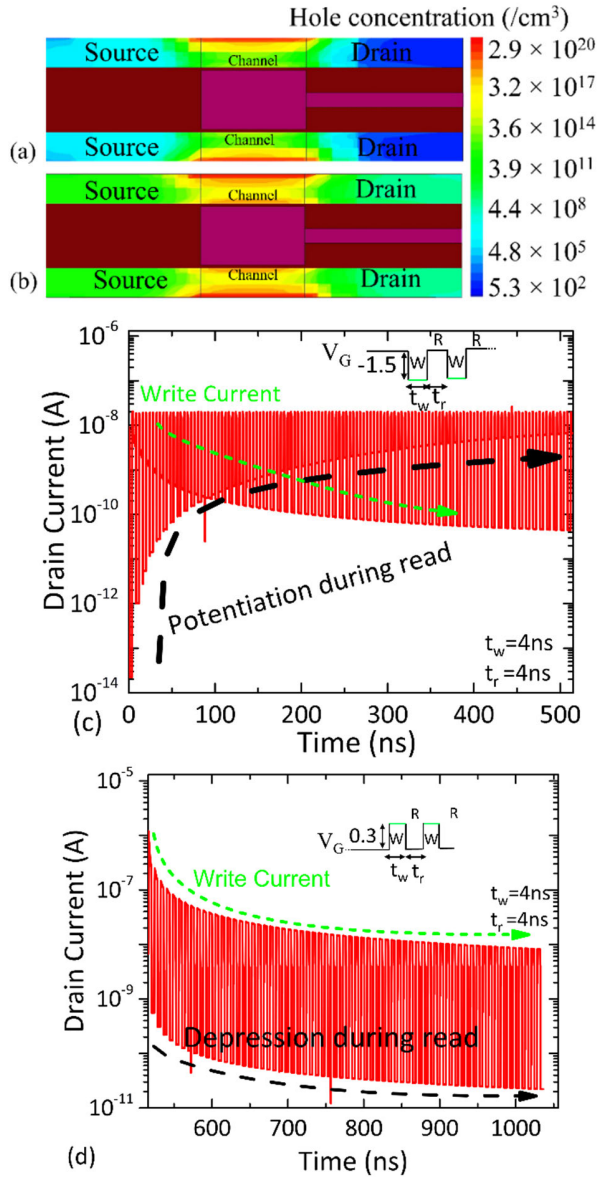


Fig. 6. Hole density contour plot of the proposed NT JLFET-based synapse after (a) first and (b) fifth potentiation pulses, clearly indicating the gradual increase in the hole accumulation in the channel region with potentiation pulses. Transient drain current response of the proposed NT JLFET-based synapse after applying (c) consecutive potentiation pulses followed by read operations and (d) consecutive depression pulses followed by read operations (I_{DR}, I_{WP}, and I_{WD} denote the drain current during read, potentiation, and depression operation). The voltage waveforms on the outer shell gate electrode are shown in (c) and (d).

to an increased generation and accumulation of holes in the channel region, as shown in Fig. 5(c).

The drain current during the read process, I_{DR}, which represents the postsynaptic current (PSC), is measured after each write pulse (negative outer shell gate pulse) using a read pulse with $V_G = 0$ V at $V_D = 0.5$ V and $V_S = 0.3$ V. The gradual increase in the hole accumulation in the channel region with each write pulse [Fig. 6(b)] induces a lowering of the source-channel barrier height during the read operation [Fig. 5(d)] and results in a higher read current (PSC) as evident from Fig. 6(c).

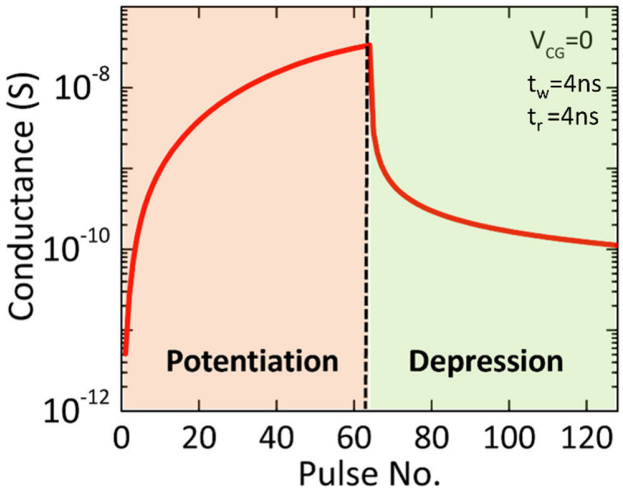


Fig. 7. Variation in the conductance state (synaptic weight) of the proposed NT JLFET-based bipartite synapse (with core gate voltage $V_{CG} = 0$ V) during the read operation with consecutive potentiation and depression pulses.

Similarly, LTD is performed utilizing a train of positive outer gate pulses with a magnitude of 0.3 V and a pulsewidth of 4 ns, which uncover the majority of electrons in the channel region underneath the outer shell gate surface, leading to dynamic recombination of the accumulated holes. The application of each subsequent positive pulse at the outer shell gate introduces more electrons to the channel region, which results in larger recombination of the accumulated holes and a reduction in the accumulated hole concentration, diminishing the floating-body effects. This gradual removal of holes from the channel region results in increasing the source–channel barrier height and reducing the drain current during the read process (I_{DR}) after each positive pulse, as shown in Fig. 6(d). Therefore, the LTP and LTD operations in the proposed NT JLFET are analogous to the biological synapses, and the conductance of the NT JLFET during the read process, as shown in Fig. 7, can effectively emulate the connection strength or the synaptic weight, which dictates the magnitude of the PSC.

B. NT JLFET as a Tripartite Synaptic Element

In addition to the bipartite synaptic functionality, we show that the NT JLFET, with the aid of the independent core gate, can also exhibit neuromodulation similar to the astrocyte, emulating the tripartite behavior with adaptive synaptic tunability. While synaptic potentiation and depression for the proposed NT JLFET-based tripartite synapse are performed by applying negative voltage pulses and positive voltage pulses, respectively, on the outer shell gate, similar to the bipartite case, the application of core gate voltage leads to neuromodulation of the conductance of the NT JLFET (synaptic weight). Fig. 8(a) shows the conductance of the proposed NT JLFET-based tripartite synapse with a number of potentiation/depression pulses for different core gate voltages. As can be observed from Fig. 8(a), while a negative core gate voltage suppresses the PSC and decreases the conductance measured during

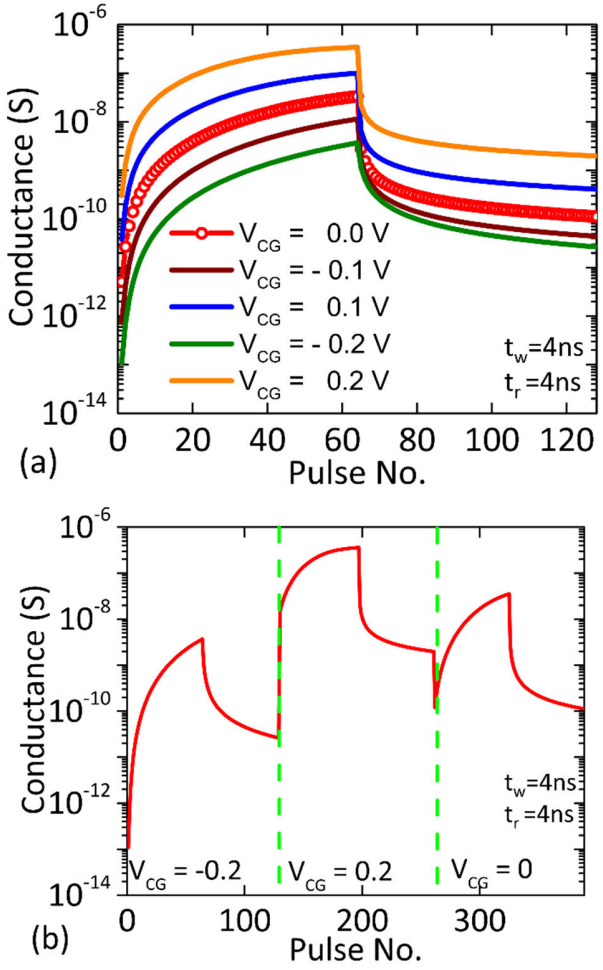


Fig. 8. (a) Modulation of the conductance state (synaptic weight) of the proposed NT JLFET-based tripartite synapse during the read operation after consecutive potentiation and depression pulses with the aid of the core gate voltage (mimicking astrocyte neuromodulation). (b) Large number of continuous conductance states (synaptic weights) realized within the proposed NT JLFET-based tripartite synapse in real time by continuously adjusting the core gate voltage during the potentiation/depression operation.

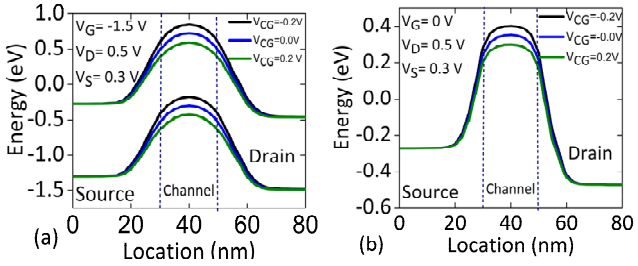


Fig. 9. (a) Energy band profiles of the proposed NT JLFET-based tripartite synapse taken at a cutline 1 nm above the Si–SiO_2 interface of the core gate after application of the potentiation pulse for different core gate (neuromodulator) voltages. (b) Conduction band energy profile of the proposed NT JLFET-based tripartite synapse during the read operation for different core gate (neuromodulator) voltages.

the read process, application of a positive core gate voltage enhances the PSC, leading to increased device conductance during the read operation.

The impact of the core gate voltage on the PSC and the conductance during the read operation of the proposed NT JLFET-based tripartite synapse can be understood from Fig. 9. The application of a negative core gate voltage leads to the depletion of the channel region at the channel–drain interface underneath the core gate surface leading to a larger tunneling width suppressing the L-BTBT and the consequent hole accumulation in the channel region as shown in Fig. 9(a). Furthermore, it also results in an increased effective base width of the parasitic BJT, leading to a reduced current gain, further diminishing the floating-body effects [11]. Therefore, owing to the reduced hole accumulation and suppressed parasitic BJT action, the source–channel barrier height of the NT JLFET increases during the read operation, as shown in Fig. 9(b), leading to the reduced PSC and decreased conductance. On the other hand, application of a positive core gate voltage results in an enhanced L-BTBT-induced parasitic BJT action, leading to an increased conductance during the read operation.

Furthermore, we can tune the maximum conductance value ($G_{\max}$) in the range of 0.34 μS–3.7 nS and the minimum conductance value ($G_{\min}$) in the range of 0.3 nS–0.109 pS by using an appropriate core gate voltage (V_{CG}) between 0.2 and −0.2 V. Therefore, the proposed NT JLFET-based tripartite synapse not only exhibits a significantly high DR of conductance (DR = $G_{\max}/G_{\min}$), but the conductance range can be further tuned (by orders of magnitude) with the aid of the core gate voltage. Moreover, a large number of continuous conductance states (synaptic weights) can be realized in the proposed NT JLFET-based tripartite synapse in real time by continuously adjusting the core gate voltage during the potentiation/depression operation. For instance, as shown in Fig. 8(b), multiple continuous conductance states can be realized by changing the core gate voltage from −0.2 to 0.2 to 0 V. Furthermore, the worst case switching energy for the proposed NT JLFET-based tripartite synapse was found to be ultralow (1.19 aJ). Therefore, the core gate can be utilized as an effective tool for precise synaptic tunability in the proposed tripartite synapse while enabling ultraenergy-efficient neuromorphic computing.

C. Retention, Sensitivity, and Thermal Stability

The neuromodulation of the synaptic conductance (potentiation and depression operations) in the proposed NT JLFET-based tripartite synapse is attributed to the gradual modulation of the L-BTBT-generated hole concentration in the floating-channel region with the help of an independent core gate, which is susceptible to dynamic recombination within the channel, resulting in a short retention. Therefore, it becomes imperative to analyze the retention behavior of the proposed tripartite synaptic element. To this end, we have evaluated the retention of the proposed NT JLFET-based tripartite synapse as: 1) a binary memory element (with two extreme conductance states representing two memory states) as shown in Fig. 10(a) and 2) an analog synaptic element with 6-bit precision as shown in Fig. 10(b). As shown in Fig. 10(a), the binary state retention is measured by programming the memory cell to its extreme conductance states (represented by I_{D0} and I_{D1}) and then continuously monitoring the conductance states through read pulses [8]. Although

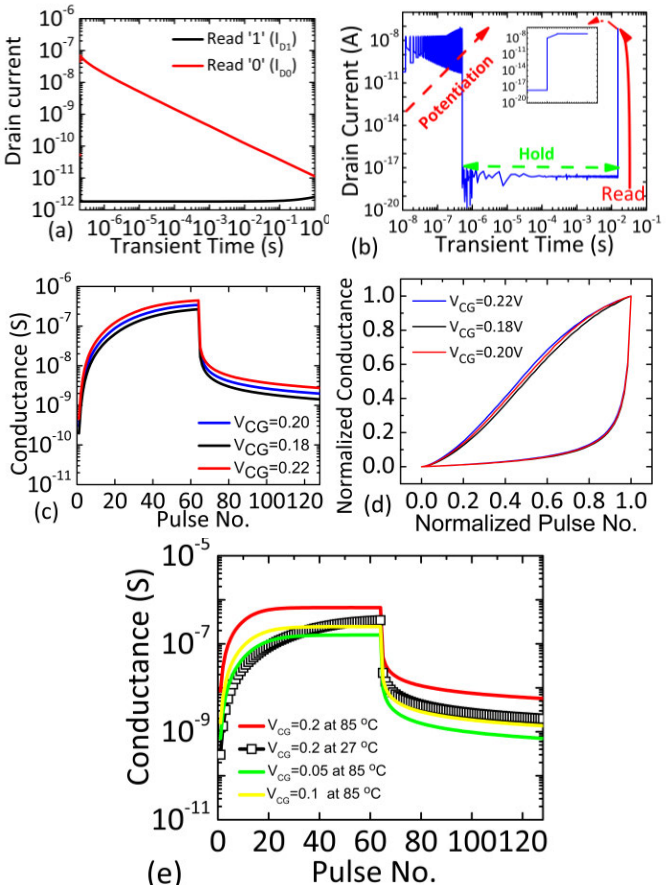


Fig. 10. (a) Binary state retention, (b) synaptic-state retention of the proposed NT JLFET-based tripartite synapse, (c) variation in the conductance state with respect to ±10% V_{CG} variation in the proposed NT JLFET-based tripartite synapse, and (d) variation in normalized conductance values with normalized pulse number with respect to ±10% V_{CG} variation. (e) Thermal variation in the conductance state.

I_{D1} degrades with time owing to recombination, I_{D1} and I_{D0} are distinguishable and exhibit a separation of more than an order of magnitude even after 1 s.

Moreover, due to the limited literature available on synaptic-state retention, we propose a method to systematically evaluate and quantify the retention of the proposed tripartite element as an analog synapse. Since the recombination rate is proportional to the accumulated hole concentration, the worst synaptic-state retention time is obtained for the largest hole concentration corresponding to the extreme ($2^n - 1$ for n-bit precision) programmed state. To measure the synaptic-state retention time, we first program the proposed synaptic element to the extreme programmed state [$(2^n - 1)$th state for n-bit precision] and then keep it in the hold mode ($V_D = V_S = 0.5$ V and $V_{CG} = V_G = -0.1$ V) and monitor the read current. We then define the synaptic-state retention time as the hold time required for reduction of the read current corresponding to the extreme programmed state [$(2^n - 1)$th state for n-bit precision] to the read current corresponding to the penultimate $(2^n - 2)$th programmed state. The proposed synaptic element exhibits a worst case synaptic-state retention time of 15 ms for 6-bit precision as shown in Fig. 10(b).

Furthermore, we have analyzed the sensitivity of the neuromodulation capability to the core gate voltage fluctuations by performing potentiation and depression operations while varying the core gate voltage by ±10% around the reference value ($V_{CG} = 0.2$ V), as shown in Fig. 10(c). While an increase in the core gate voltage by 10% leads to a simultaneous increment in both the maximum and minimum synaptic conductance values, G_{max} and G_{min} from 0.34 μS and 0.3 nS to 0.44 μS and 0.45 nS, respectively, a reduction in the core gate voltage by 10% decreases the G_{max} and G_{min} values from 0.34 μS and 0.3 nS to 0.266 μS and 0.19 nS, respectively. Although a change in the core gate voltage leads to a slight change in the synaptic conductance states, the overall accuracy of online learning algorithms depends on the normalized synaptic conductance values and the nonlinearity of the weight update process rather than the absolute values, which remain the same. Therefore, the proposed NT JLFET-based tripartite synapse exhibits a robust performance even in the presence of core gate voltage fluctuations.

Moreover, we have also analyzed the thermal stability of the proposed NT JLFET-based tripartite synaptic element as shown in Fig. 10(e). An increase in the operating temperature to 85 °C leads to a larger change in the synaptic conductance state with the application of potentiation or depression pulses (as opposed to gradual changes at 27 °C), ultimately resulting in saturation of the conductance state to the extreme values for the same core-gate voltage. Therefore, the synaptic conductance characteristics saturate at their extreme values for a lower number of potentiation or depression pulses, introducing significant nonlinearity in the synaptic behavior, which may result in degradation in accuracy for online learning. To mitigate this temperature-induced nonlinearity in the synaptic behavior, a temperature-adaptive core gate voltage V_{CG} tuning scheme can be utilized (similar to the dynamic voltage scaling used in modern processors). Specifically, reducing V_{CG} to 0.1 V at 85 °C can compensate for the temperature-induced increase in the nonlinearity.

D. Neuromodulated Plasticity for Online Learning

The neuromodulation of the synaptic conductance in the proposed NT JLFET-based tripartite synapse is attributed to the gradual modulation of the L-BTBT-generated hole concentration in the floating-channel region with the help of an independent core gate. Therefore, the working mechanism of the proposed NT JLFET-based tripartite synapse is analogous to the capacitor-less 1T-DRAM cells, which encode memory states as accumulation or absence of holes within their floating body [29]. While conventional memory devices such as Flash, RRAMs, PCMs, and so on, exhibit limited endurance ($<10^6$ cycles), BTBT-generated hole accumulation-based capacitor-less 1T-DRAMs offer superior endurance exceeding 10^{15} cycles [30]. Since the proposed NT JLFET-based tripartite synapse works on the same mechanism, it is expected to show an ultrahigh endurance, and coupled with its run-time neuromodulation property, such a synaptic element is particularly relevant for applications involving online learning and adaptive edge computing, where weights must be continuously updated in real-time based on feedback signals, necessitating frequent write operations.

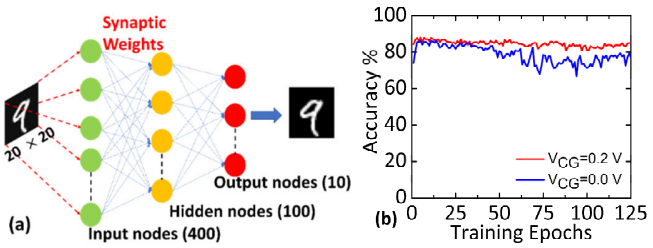


Fig. 11. (a) MLP network utilized for image recognition and (b) training accuracy versus epochs.

TABLE II
PARAMETERS UTILIZED FOR THE MLP NETWORK

Parameters	Values
Number of Layers	3
No. of hidden layers	1
Optimizer	Adam
Epoch size	125
Bias	0
Learning rate for the weights from input to hidden (α_1) and hidden to output layer (α_2)	0.04 and 0.02
Weights	Mapped on NT JLFET-based synaptic element

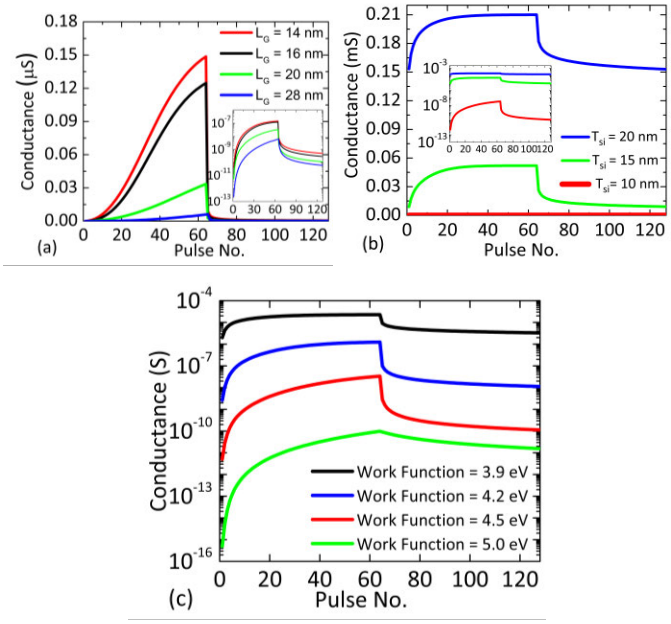


Fig. 12. Impact of (a) gate length (L_G), (b) silicon film thickness (T_{si}) [the insets show the plots on log scale], and (c) work function of the core gate on the synaptic conductance during potentiation and depression operation.

Therefore, to explore the potential of the proposed NT JLFET-based bipartite and tripartite synaptic elements for online learning, we employed the proposed bipartite and tripartite synaptic elements as weights in a multilayer perceptron (MLP) network to classify the MNIST handwritten dataset [31] utilizing the NeuroSim framework [32]. The MLP network comprises an input layer, one hidden layer, and an output layer as shown in Fig. 11(a). The model parameters utilized for performance benchmarking are listed in Table II. We calculated the nonlinearity parameter for potentiation and depression operations utilizing the normalized synaptic conductance modulation behavior of the bipartite and tripartite synaptic elements shown in Figs. 7 and 8. While the NT JLFET-based bi-partite synaptic element exhibits a nonlinearity value of −1.5695 in potentiation (NL_LTP) and −10.5211 in depression (NL_LTD), the proposed tripartite synaptic element based on NT JLFETs exhibits a significantly reduced nonlinearity value of 0.0228 in potentiation (NL_LTP) and −8.4163 in depression (NL_LTD) when the core gate voltage (V_{CG}) is 0.2 V. The MLP network with the proposed NT JLFET-based bipartite and tripartite synaptic elements exhibits a recognition accuracy of 77.23% and 85.11%, respectively, as shown in Fig. 11(b). Therefore, the proposed tripartite synaptic element can be effectively utilized to improve the nonlinearity factor and the accuracy by ∼10% for online learning applications.

Furthermore, for tasks such as image classification using the MLP network, each training iteration (comprising forward propagation, backpropagation, and weight updates) requires a transient retention time of ∼200 ns per layer [33]. Therefore, the synaptic-state retention time of the proposed tripartite synapse is sufficient to support the temporal requirements of online learning even in the presence of dynamic recombination. Moreover, after the training phase, the optimized weights can be offloaded to a nonvolatile memory with large retention for inference deployment.

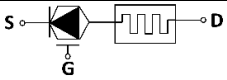
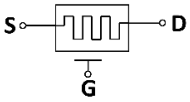
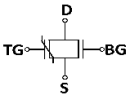
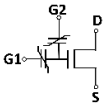
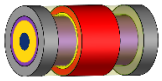
E. Integration With Hardware Neurons/Activation Circuits

Hardware neurons and activation function implementations often operate across diverse design paradigms ranging from weak inversion to strong inversion regimes and span a broad spectrum of input current levels (∼from nA to μA) [34], [35], [36], [37], [38]. Such a diverse range of input current levels poses a significant challenge for their integration with the conventional bipartite synapses, which lack the adaptive tunability required for seamless interfacing. Furthermore, owing to the mismatch between the range of synaptic currents and the operating regime of the neuronal/activation circuit, many of these implementations utilize trans-impedance amplifiers (TIAs) [35], [38] to convert the accumulated synaptic input currents to a voltage output. Designing TIAs for such low input currents is particularly challenging since they suffer from high noise sensitivity, limited gain, and increased power consumption. These constraints hinder seamless integration of existing neuronal/activation circuit designs with a wide variety of bi-partite synaptic elements. On the other hand, the neuromodulation capability of the proposed tripartite synapses facilitates dynamic (run time) current modulation, enabling the synaptic current to match the operational regime of the neuronal/activation circuits without extensive redesign, facilitating seamless integration and compatibility with a wide range of neuron architectures and activation function circuits.

F. Performance Benchmarking

We have benchmarked the performance of the proposed NT JLFET-based tripartite synapse with the recently reported

TABLE III
PERFORMANCE BENCHMARKING

	SYNAPTIC BARRISTOR [7]	MULTI-GATE MEMRISTIVE SYNAPSE [8]	DG SOI-Fe-JLFET [9]	DG-FeTFT [10]	Our Work
Cell Structure					
Retention Behaviour	~1000 s	~100 s	Non-Volatile	Non-Volatile	~1 s
Operating Voltage	- 40 V	- 40 V	-5.5 V	2 to 5 V	- 1.5 V
Max. PSC current (I_{max})	~ 0.185 µA (30 Potentiation Cycles)	~ 0.004 µA (50 Potentiation Cycles)	~ 0.24 µA (50 Potentiation Cycles)	~8 µA (30 Potentiation Cycles)	~0.35 µA (64 Potentiation Cycles)
PSC ratio (at fixed voltage) (I_{max}/I_{min})	19	6.25	8	8	1.12×10^3
Programing Time	~ ms	~ ms	~ µs	~ µs	~ ns
Endurance	10^3	---	$\sim 2\times10^3$	---	$\geq 10^{15}$#
CMOS Compatible	No	No	Yes	Yes	Yes
Footprint and Gate length (L_G)	A* > 30 µm^2 L_G* > 15 µm	A* > 30 µm^2 L_G* > 15 µm	A = 1.2µm^2 L_G* > 400 nm	A = 400 µm^2 L_G = 10 µm	A = 0.002 µm^2 L_G = 20 nm
Symmetric pulse in Potentiation and Depression	Yes	No	Yes	Yes	Yes

*Based on optical images #Based on projection of capacitorless DRAMs [30]

tripartite synapses in terms of performance metrics such as retention behavior, operating voltage, maximum PSC, PSC ratio, programming time, endurance, CMOS compatibility, footprint, gate lengths, and symmetric behavior with respect to pulses, as shown in Table III. The proposed NT JLFET-based tripartite synaptic element is not only CMOS-compatible and highly scalable but also exhibits the highest PSC ratio while operating at a significantly lower voltage when compared to the other tripartite synapses [7], [8], [9]. Although the synaptic barrister- [7], DG-SOI-Fe-JLFET- [9], and DG FeTFT-based [10] tripartite synapses are also CMOS-compatible, they require higher pulse widths (in the range of ms and μs) during potentiation and depression, apart from a large-area footprint.

G. Device Design Guidelines

Since the L-BTBT GIDL-induced floating-body effects in NT JLFETs depend heavily on the gate length (L_G), silicon film thickness (T_{si}), and the work function of the gate electrode [26], [27], [28], it becomes imperative to analyze the impact of these parameters on the performance of the proposed NT JLFET-based tripartite synapse and propose design guidelines to further improve the performance. Gate length scaling not only leads to an increased lateral electric field enhancing the L-BTBT but also results in a reduced effective base width (channel length) of the parasitic BJT [26], [27], [28]. This leads to a significant increase in the hole accumulation and current gain of the parasitic BJT, which leads to a considerable reduction in the source–channel barrier height during the read operation. Therefore, the maximum conductance of the proposed tripartite synapse increases from 5.9 nS to 0.14 μS when L_G is reduced from 28 to 14 nm, as shown in Fig. 12(a).

Moreover, increasing the silicon film thickness (T_{si}) leads to a reduction in the electrostatic integrity, increasing the influence of the drain voltage on the channel electrostatics. The consequent drain-induced barrier thinning (DIBT) reduces the tunneling width, increasing the L-BTBT, which results in a larger read current. Therefore, the maximum conductance of the proposed tripartite synapse increases from 33 nS to 210 μS when T_{si} is increased from 10 to 20 nm [Fig. 12(b)].

Although a higher work function of the core gate electrode boosts L-BTBT and triggers the parasitic BJT action, leading to a large hole accumulation in the channel region, it also increases the threshold voltage, leading to a significant reduction in the read current. Therefore, the maximum conductance of the proposed tripartite synapse decreases from 22 μS to 7.7 pS when the work function of the core gate electrode is increased from 3.9 to 5 eV, as shown in Fig. 12(c).

IV. Conclusion

In this work, for the first time, we have demonstrated the feasibility of a highly scalable and ultraenergy-efficient tripartite synapse with a large DR and ultrafast synaptic potentiation and depression even at ultrascaled dimensions, utilizing the core gate in an NT JLFET to efficiently mimic the neuromodulation process of astrocytes. Although experimental realization of the proposed NT JLFET-based tripartite synapse with high yield requires comprehensive process control strategies primarily focusing on the epitaxial growth stage (governed by temperature, chamber gas flow dynamics, and seed selection) and the mesa island etch step, our promising results may provide the incentive for its process flow exploration.

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