KARNATAK LAW SOCIETY'S

GOGTE INSTITUTE OF TECHNOLOGY

UDYAMBAG, BELAGAVI-590008

(An Autonomous Institution under Visvesvaraya Technological University, Belagavi)

(APPROVED BY AICTE, NEW DELHI)

Course Activity Report on

Digital clock using counters implementation and design

Submitted in the partial fulfillment for the academic requirement of

3rd Semester B.E.

In

Digital Electronics Course

Electronics and Communication Engineering

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CERTIFICATE

Certified that the course activity entitled **Digital clock using counters implementation and design** is a bonafide work carried out by

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in partial fulfillment for the award of **Bachelor of Engineering** in Electronics and Communication Engineering in 3rd semester of the Visvesvaraya Technological University,

Belagavi during the year 2021- 2022.

It is certified that all corrections/suggestions indicated have been incorporated in the report. The activity report has been approved as it satisfies the academic requirements in respect of course activity prescribed for the said Degree.

ABSTRACT

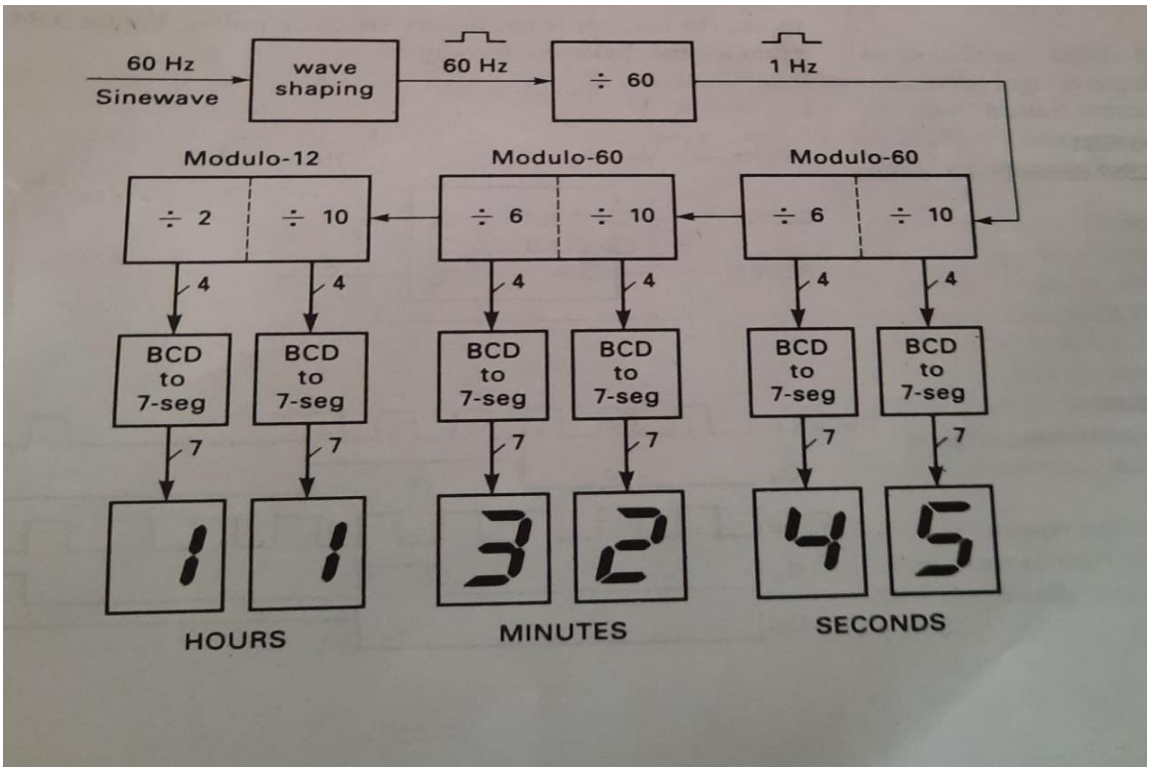
The aim of the project is to design a Digital Clock that displays the time digitally, in contrast to an analog clock, where the time is indicated by the positions of rotating hands. With the help of wave shaping circuits, counters and decoders, a digital clock to display time in hours, minutes and seconds can be constructed. Digital clock has a counter that receives a clock signal from any source and increases the number according to the clock signal. The main clock signal having 1 Hertz frequency is given to the decade counter which provides binary output to the decoder driver. This driver decodes the binary input to decimal and sends it to the seven-segment display. The counter triggers the counter next to it when it resets. The remaining counters work in a similar fashion by receiving a clock signal from the previous counter and giving a clock signal to the next counter when it resets. Seven-segment display is a very common and efficient option for displaying a decimal value. The project focuses on building a digital clock with simple gates, flip-flops and counters with sequential logic.

INTRODUCTION

A digital clock is a type of clock that displays the time digitally (i. e. in numerals or other symbols), as opposed to an analog clock, where the time is indicated by the positions of rotating hands. The times derived by analog clocks come from either a pendulum or a spring. Pendulums are unusable on moving platforms, such as a ship, and springs unwind more and more slowly as they release stored up tension. The use of sweep hands allowed these mechanical time bases to be presented in a mechanically driven display. With the perfecting of multivibrator chips, electrical circuits could be built that could accurately keep time under a wide range of conditions. As the time base had switched from mechanical to electrical, the time display had to follow suit. Display devices called 7 segment displays were designed to allow the time to be shown numerically.

DESIGN AND IMPLEMENTATION OF DIGITAL CLOCK USING COUNTERS

Counters have numerous applications in digital systems. A common application, one that illustrates the use of different modulo-n counters, is a 12-hour digital clock. Starting with a 60Hz sine wave from the input power line and using a series of wave shaping circuits, counters and d encoders, a clock system can be designed. The system block diagram of digital clock is as shown below. The clock timing frequency is derived from the 60Hz sine wave shaped into a square wave (by clipping the sine wave and presenting the result to a Schmitt trigger gate). The output from the wave shaping circuit is a 60Hz square wave suitable for a timing reference input to some counters.



COUNTERS

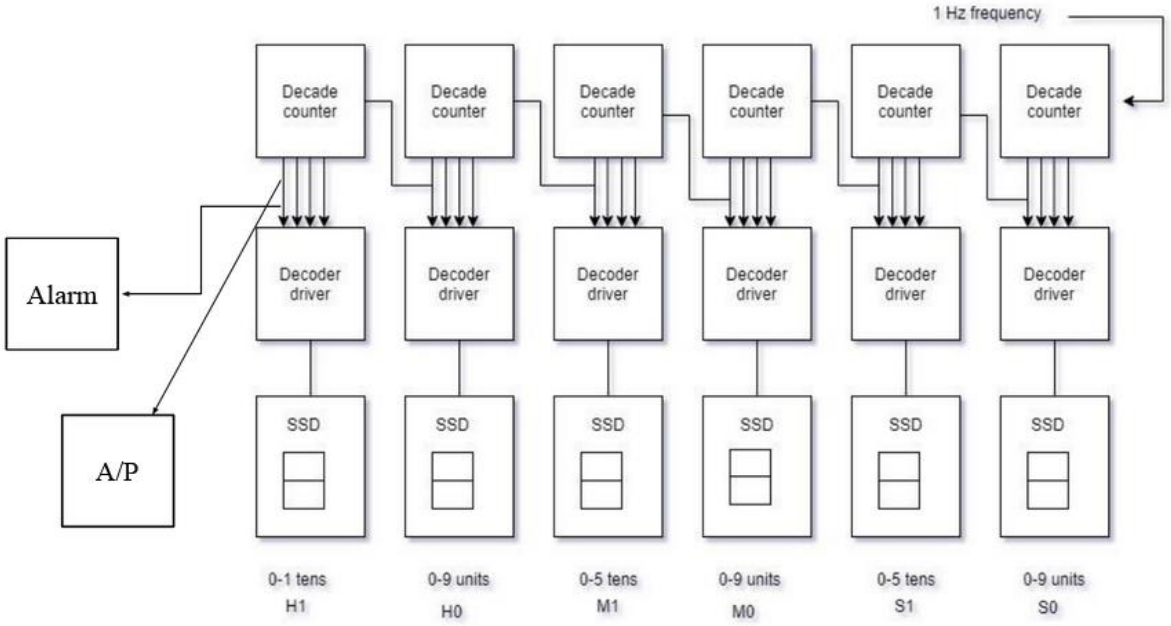
A divide-by-60 counter reduces the 60 Hz to 1 Hz, one count for each second. The second divide-by-60 counter produces a count for each minute, and the third counter produces a count for each hour. Since 24 hours make up a day, broken into two part (AM and PM), the final counter must be a divide by 12. We need two decade counters each time level: seconds, minutes, hours, and days. Each decade counter output must be decoded for presentation to a display.

A 74LS57 is used as a divide-by-60 counter to convert the 60 Hz square wave to 1 Hz square wave. The device is selected because it matches exactly with the needed function. It is an eight-pin device that requires an Icc of 17 mA. Internally, the chip contains three counters: a divide by 6 (QA output), a divide by 5 (Q. output), and a divide by 2 (Qc output). The Qa output is internally connected to the input of the divide by-2 counter. By connecting the Q, output to the B clock input we get a divide by 60 in one eight-pin IC.

The detailed logic and timing for the 74LS57 are shown in Figures 5.81 and 5.82 The 74LS57 provides a simple divide-by-60 function. The timing diagram shows how the Q, output divides the A clock by 6, and when the Q, output is connected to the B clock input, the C counter output divides the input by 60. The Q, output of the 75L557 IC goes low once for every 6 clock inputs. Output Qgoes high once every 5 times that Q. goes low and then Qc goes low once every 5 times that goes low. The result is that Qe goes low once for every 60 input clock pulses.

The seconds and minutes counters must use something other than the 74LS57. Access to the individual flip-flop outputs, for the purpose of decoding, is necessary. The SN74LS162 contains a decade counter that performs a divide-by-10 function. By using gates external to the counter any terminal count (less than 10) can be obtained. In the example we need a divide-by-6 function. By using the 74162, configured as shown in Figure 5.83, we can obtain a divide-by-6 function. The counter outputs are decoded by a single two-input NAND gate to detect when the terminal count of 5 (six events, 0-5) is reached. If the terminal count (TC) signal is coupled back to the active-low clear input, the counter is reset every six clock pulses. Figure illustrates the timing diagram for the divide-by-6 counter.

BLOCK DIAGRAM



COMPONENTS USED

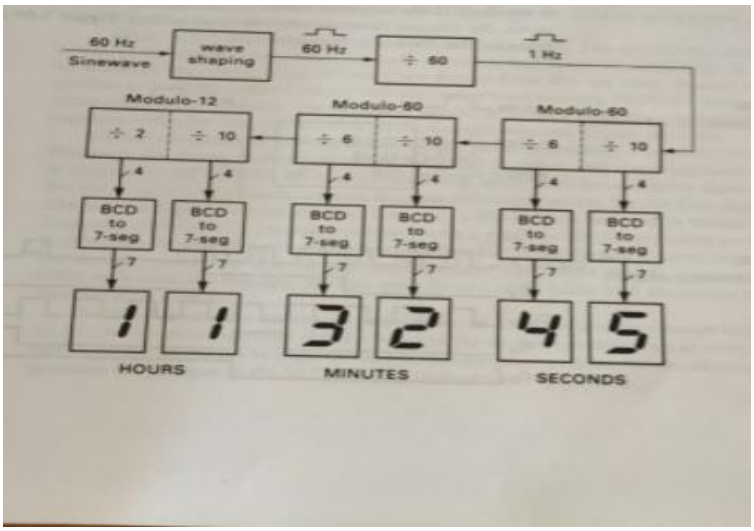
- 555 Timer
- Decade counter (IC 7490)
- Decoder (IC 7447)
- Seven Segment Display
- DIP Switch
- Magnitude Comparator

WORKING

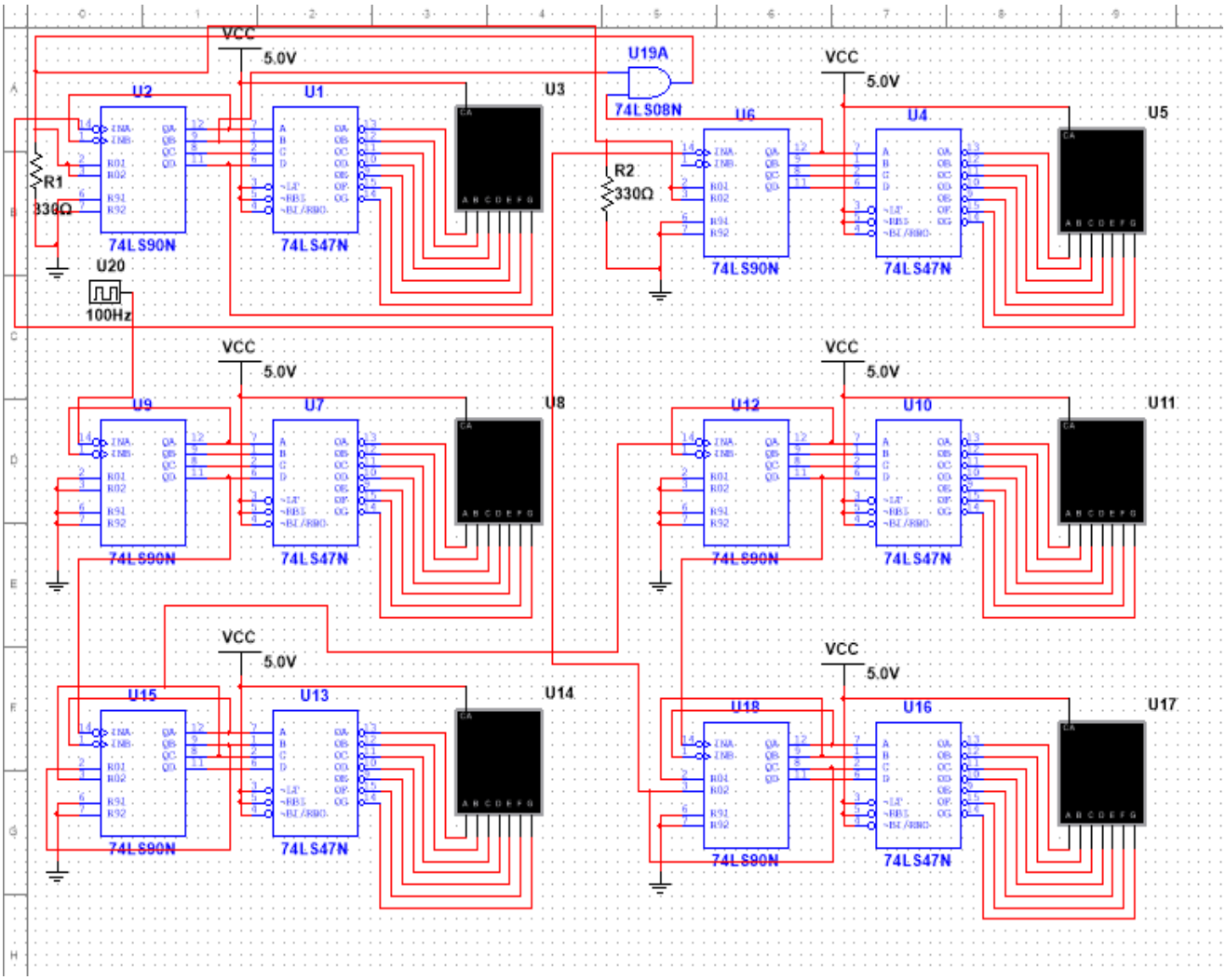
Using two SN74LS162 chips provides the divide-by-10 and divide-by-6 counters needed for the seconds and minutes. A digital clock logic diagram is shown in Figure 5.85. The decade and divide-by-6 counters are used to count time seconds, minutes, and hours External logic is required to initialize the correct time of day. Once that is done the "set time" button would be pushed to load the correct values into the respective counters SN74247 integrated circuits are used to translate the BCD and parual BCD data from the counters to seven segment codes for distribution to a series of seven-segment display modules.

A binary counter with feedback could be used to produce a modulo-12 counter. However, the hours display consists of two BCD decoders and seven-segment displays. A single four-bit modulo-12 counter could not drive both hour display digits. Instead, we use a modulo-12 hours counter that has a decade counter for the first digit (LSD). The second digit, however, is either 0 or 1, so a flip-flop can be used. A modulo-2 (flip flop) and a modulo-10 (decade) counter forms a modulo-20 counter when no feedback is provided. By providing feedback from the flip-flop to the decade counter, we can cause the decade counter to reset at the correct count. The hours decade counter resets to 0001 each time the flip-flop changes state from 1 to 0. Table 5.13 illustrates the hours counter state changes.

The flip-flop sets the terminal count output, RCO, of the decade counter and remains set for two more hours, then the flip-flop and the decade counter reset to start the mod ulo-12 count all over. The logic needed for the feedback to clear the decade counter and generate the D input to the MSD flip-flop.



CIRCUIT DIAGRAM



CONCLUSION

- Thus, this is how our main system has been built up.
- More and more knowledge involving the whole system has been gained with time and through more research.
- We have completed this project successfully and have successfully made a 12 hour digital clock with an alarm and a A.M./P.M. display.

Now-a-days different pattern of digital clocks are available in market. Most of them are of very high price and low quality. Many of those cannot provide the time accurately for longer period as those are designed with timer IC's like 555 timer. Again, some digital clocks loss their data whenever the power supply shuts down. But our designed multipurpose digital clock is accurate because of its Real Time Clock module that keeps track of the system time and update. The DS1307 has a built-in power sense circuit that detects power failures and automatically switches to the 3V Li Cell battery supply which is incorporated with the RTC. Most of the digital clock in the market does not cover all the time functions whether our designed digital clock covers all the time options and we will also incorporate the alarm option in next version. However, the Temperature displaying is an additional feature of our smart digital clock. It is possible to develop this system with only USD 7. So this version of digital clock is really a cheap, precise and well featured device for the present market.