Register Access Controller for Amazilia Design Review

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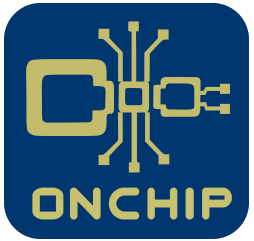
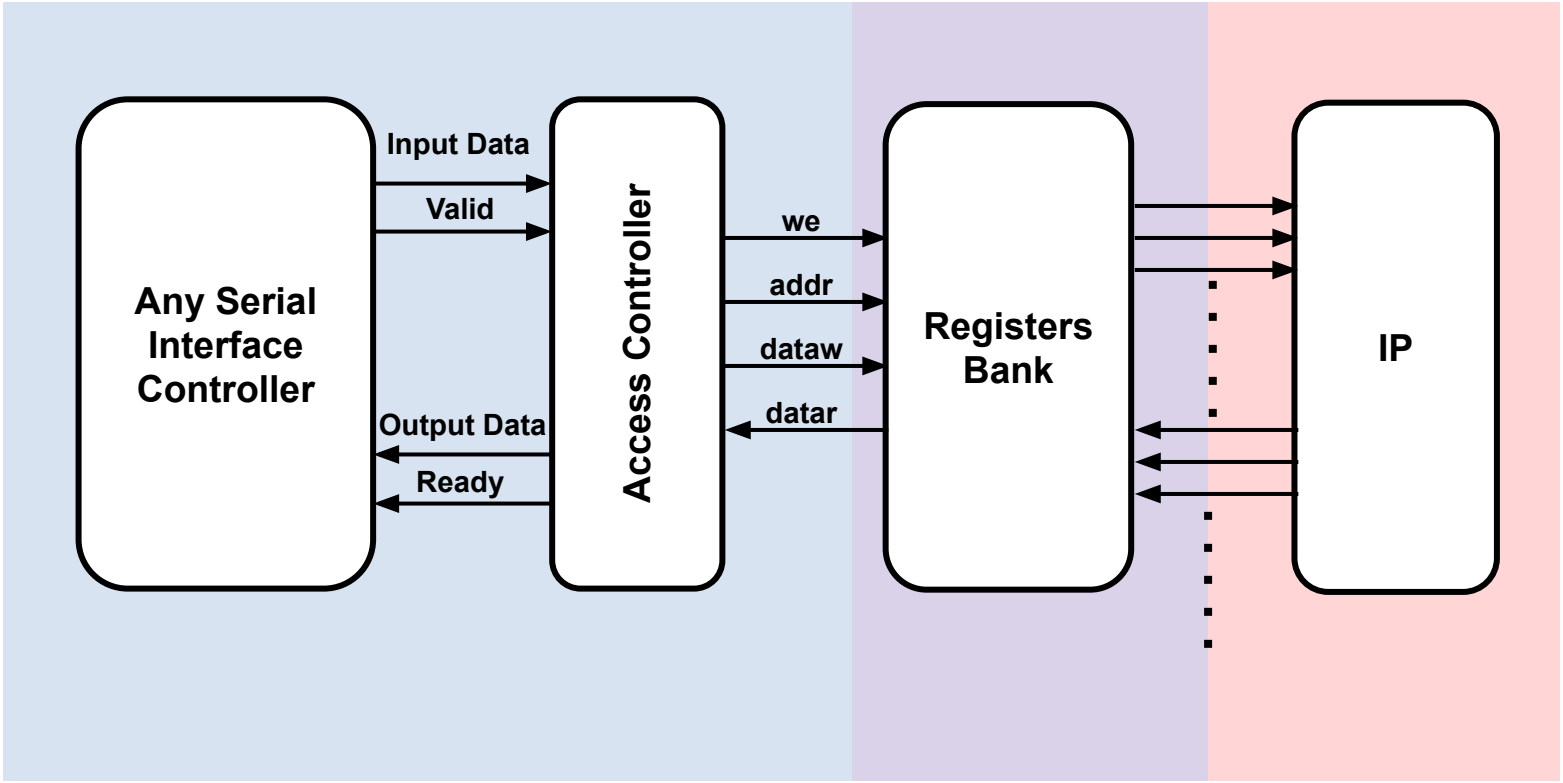


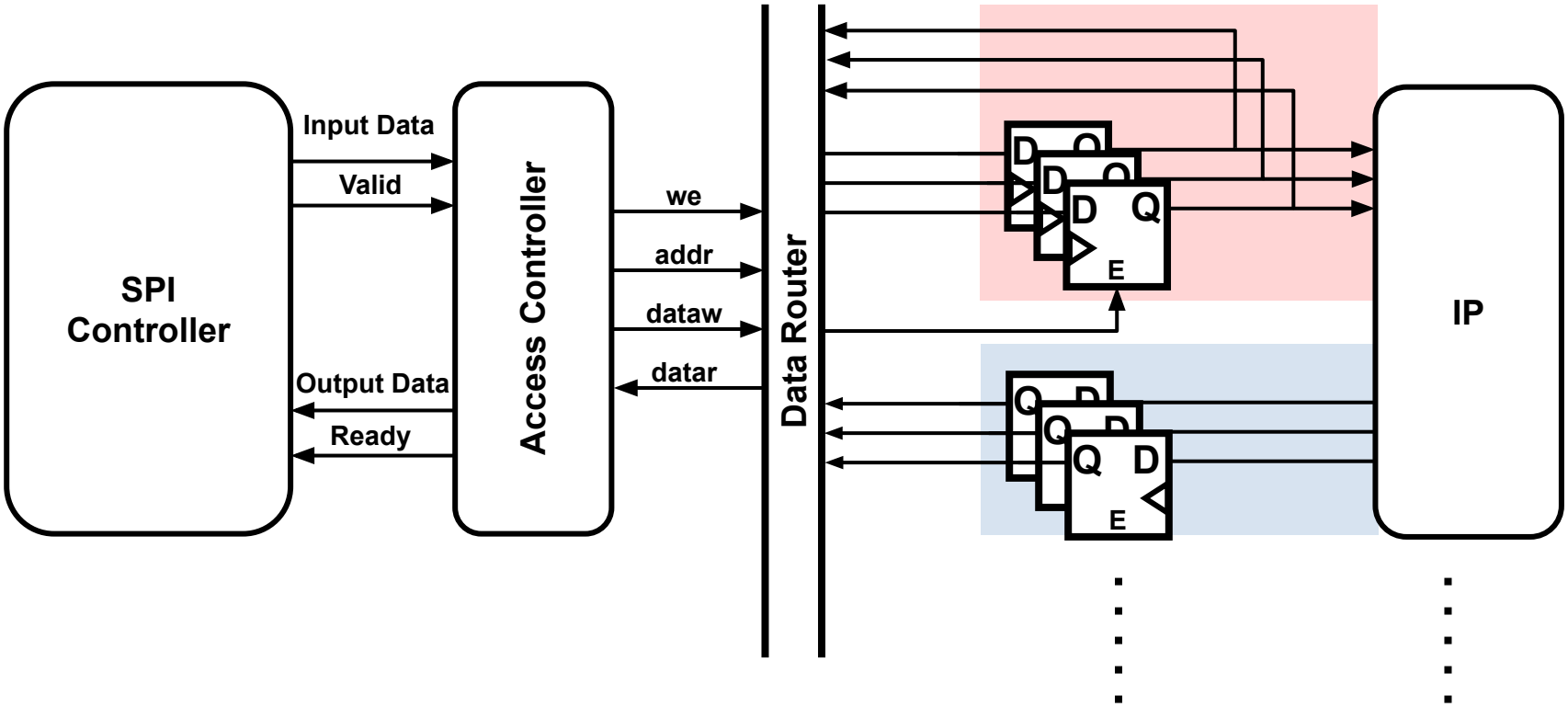
Outline

- Introduction to the architecture
- SPI controller review
- Access controller review
- Register bank review
- Synthesis results

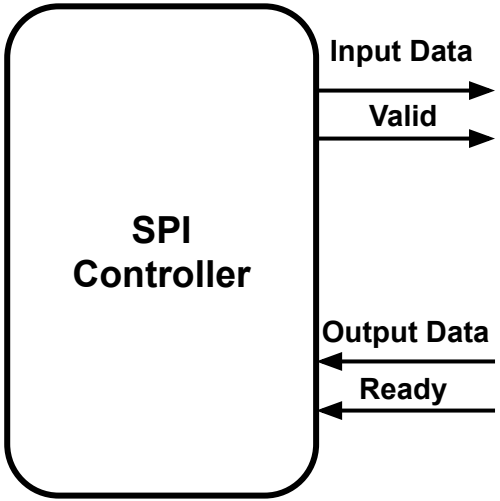
Implemented Architecture



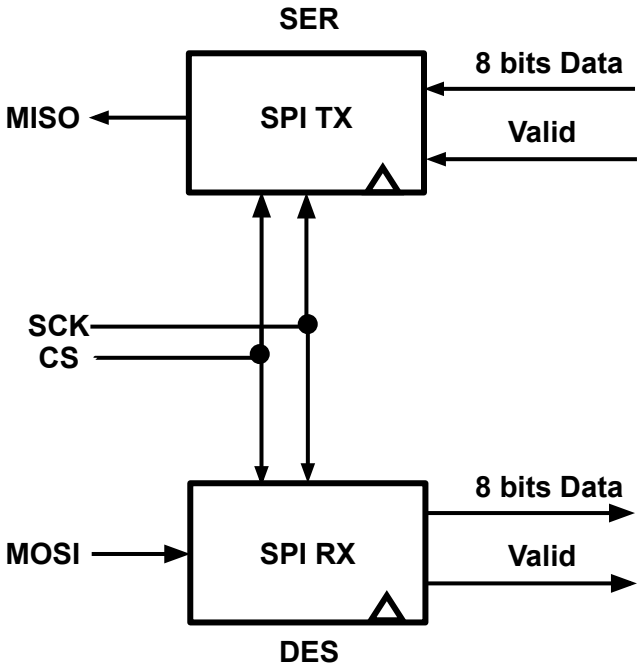
Amazilia Implementation



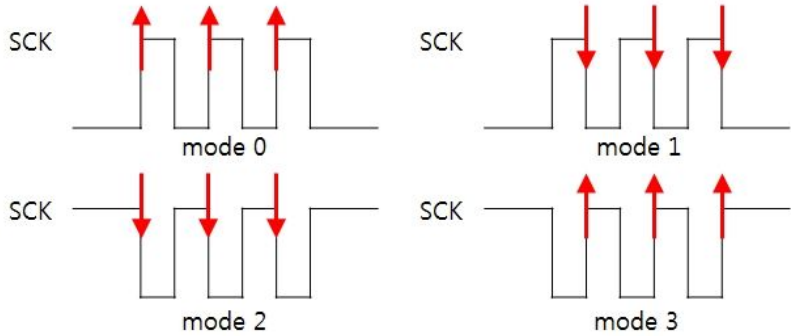
Serial Interface Controller



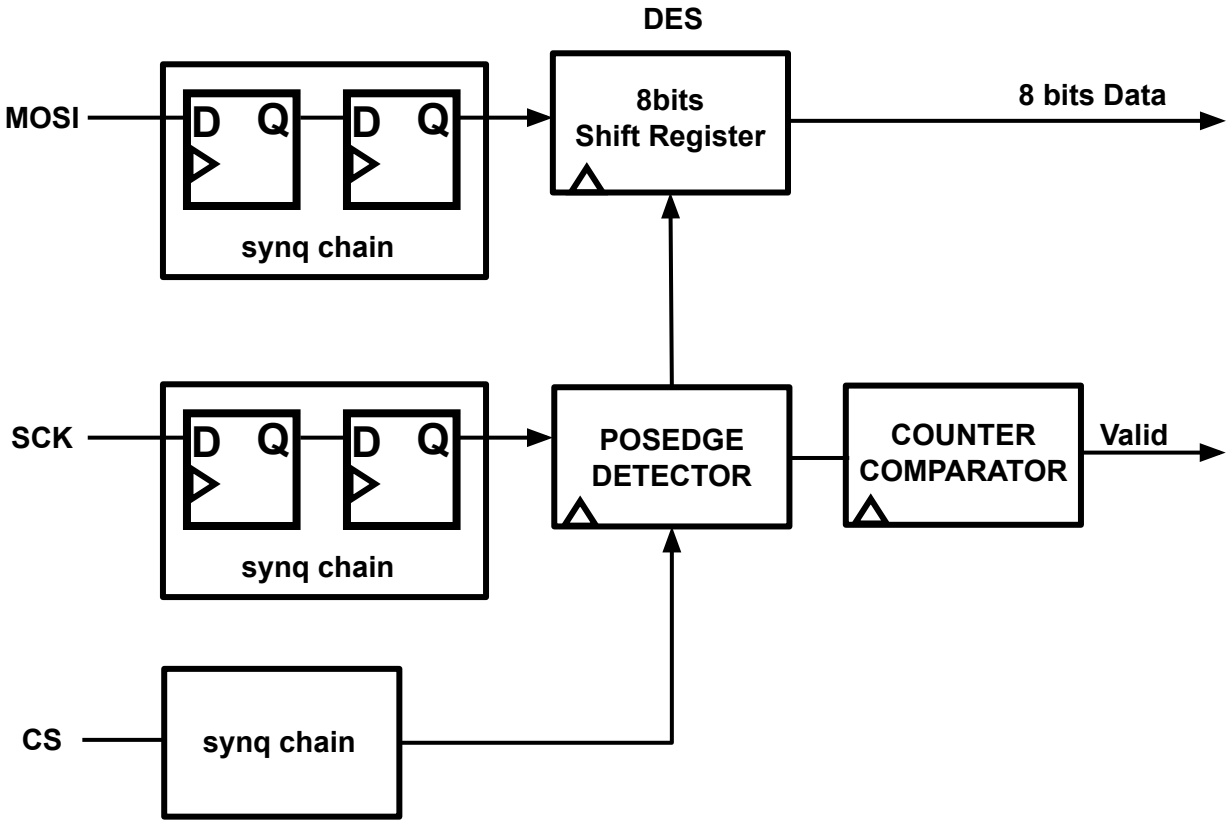
Full Duplex SPI Mode 0 Controller



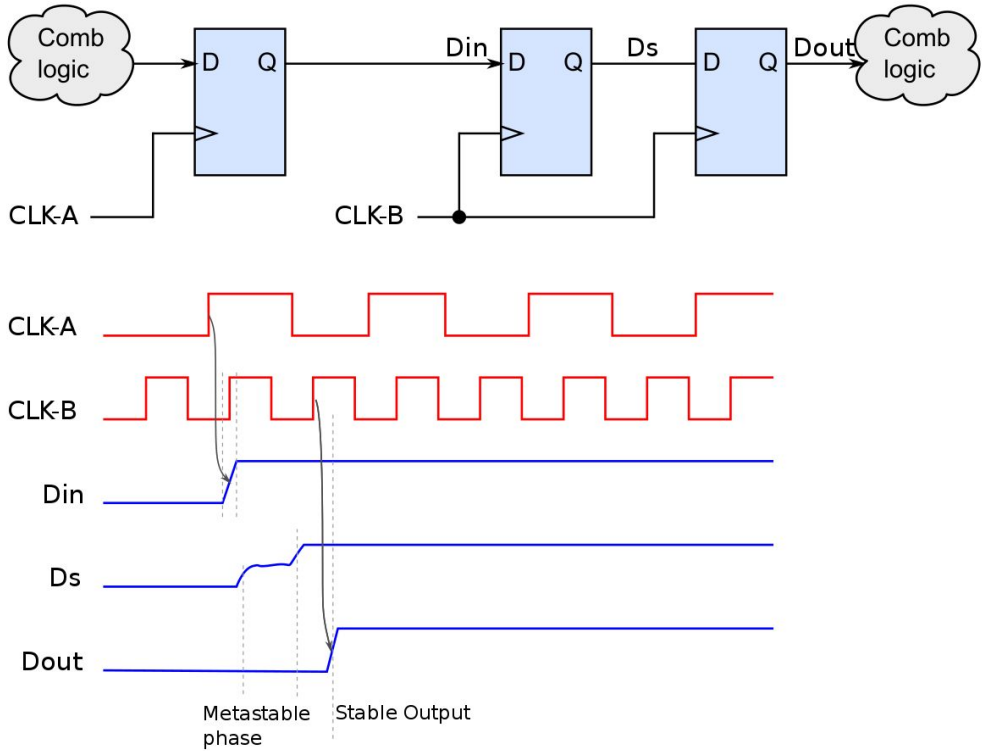
SPI MODES



Serial Interface Controller RX



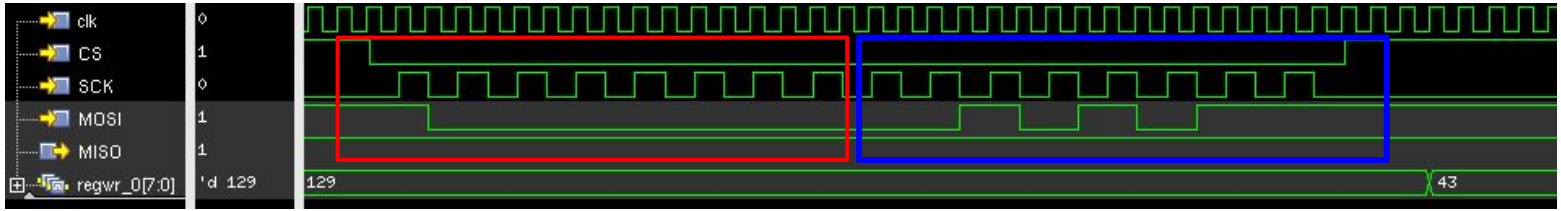
Clock sync



Tomado de :
https://commons.wikimedia.org/wiki/File:Metastability_D-Flipflops.svg#/media/File:Metastability_D-Flipflops.svg

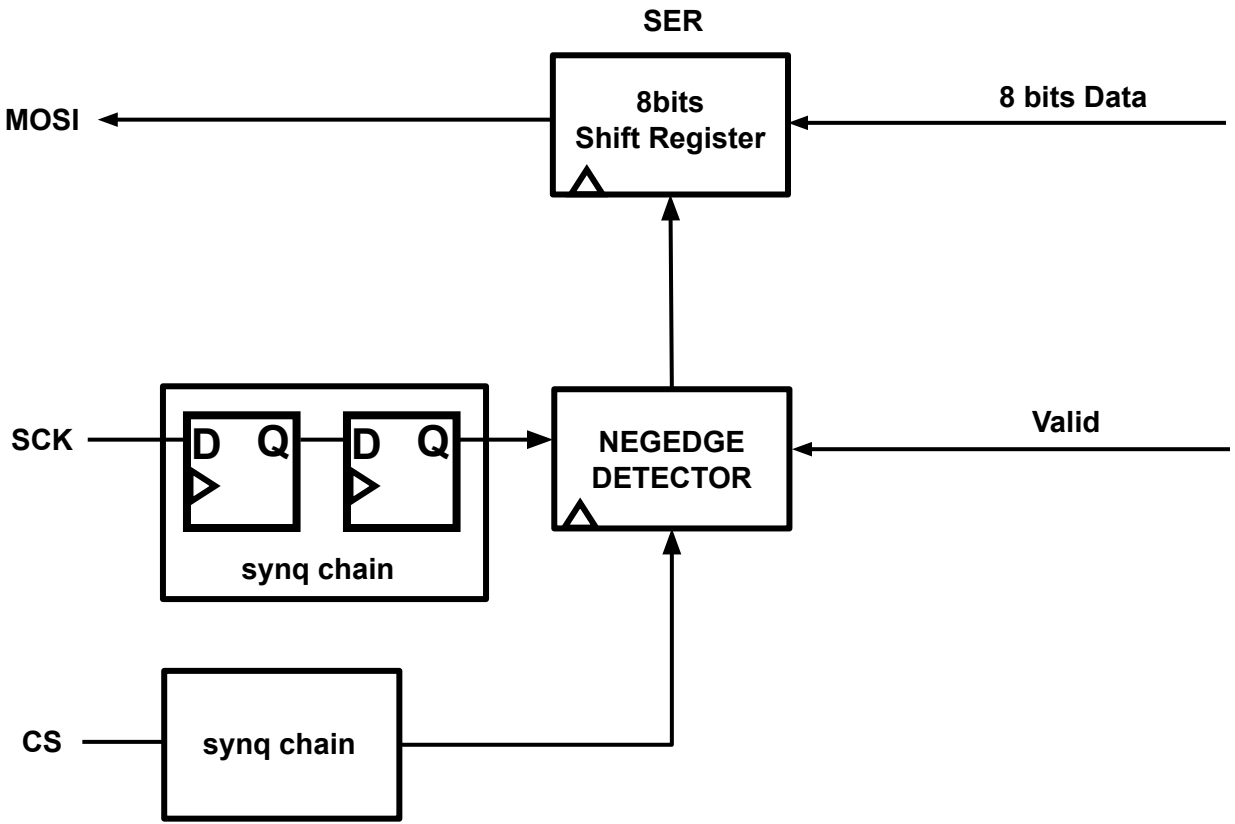
Write Transaction Wave Form

Example of a write transaction over address 0 :



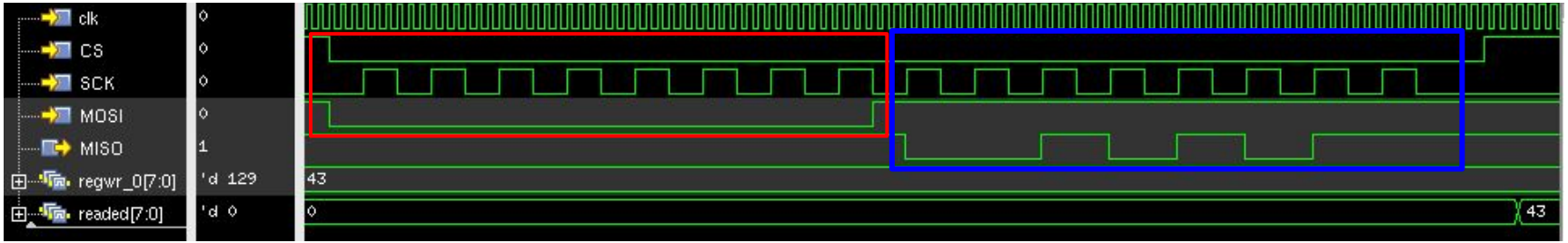
Frequency limitation for write transactions its ***Fsck < (Fclk / 2)***
In Amazilia Fsck< 156 MHz

Serial Interface Controller TX

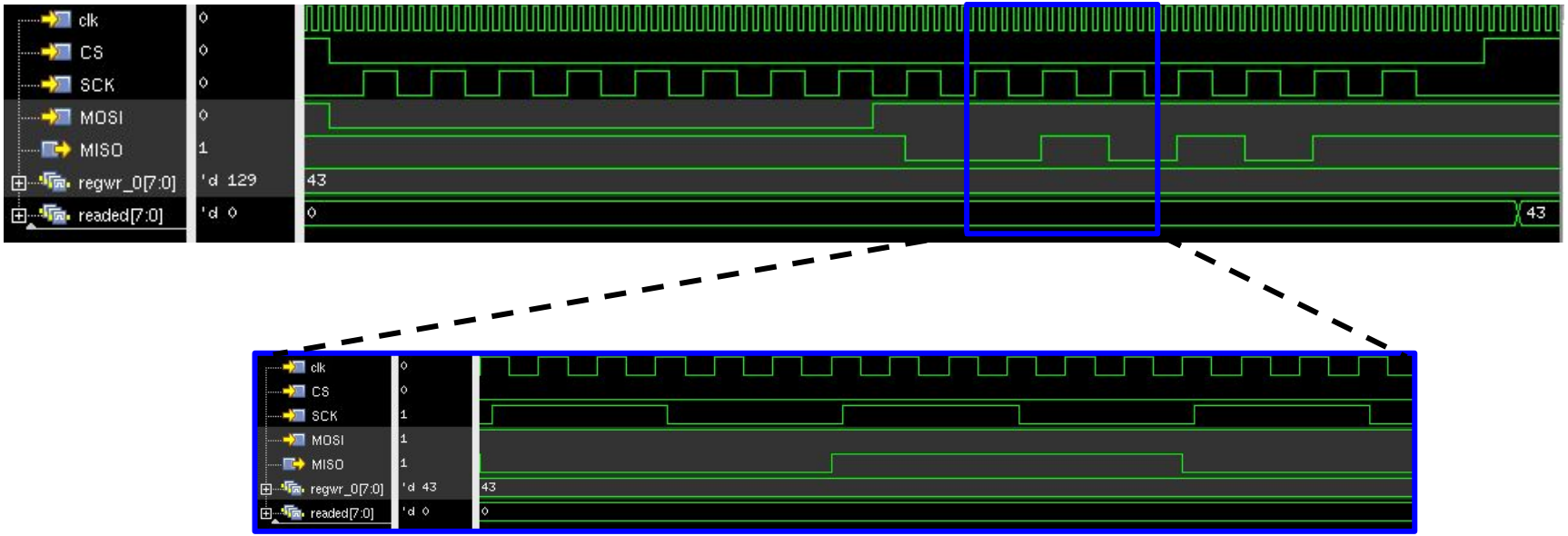


Single Read Transaction Wave Form

Example of a read transaction over address 0 :

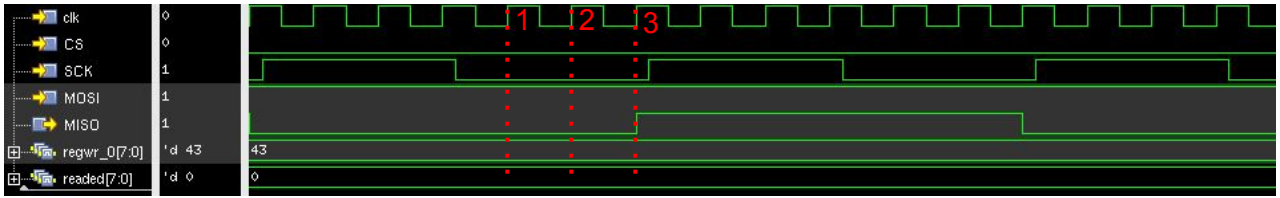


Frequency Limitation for Read Transactions

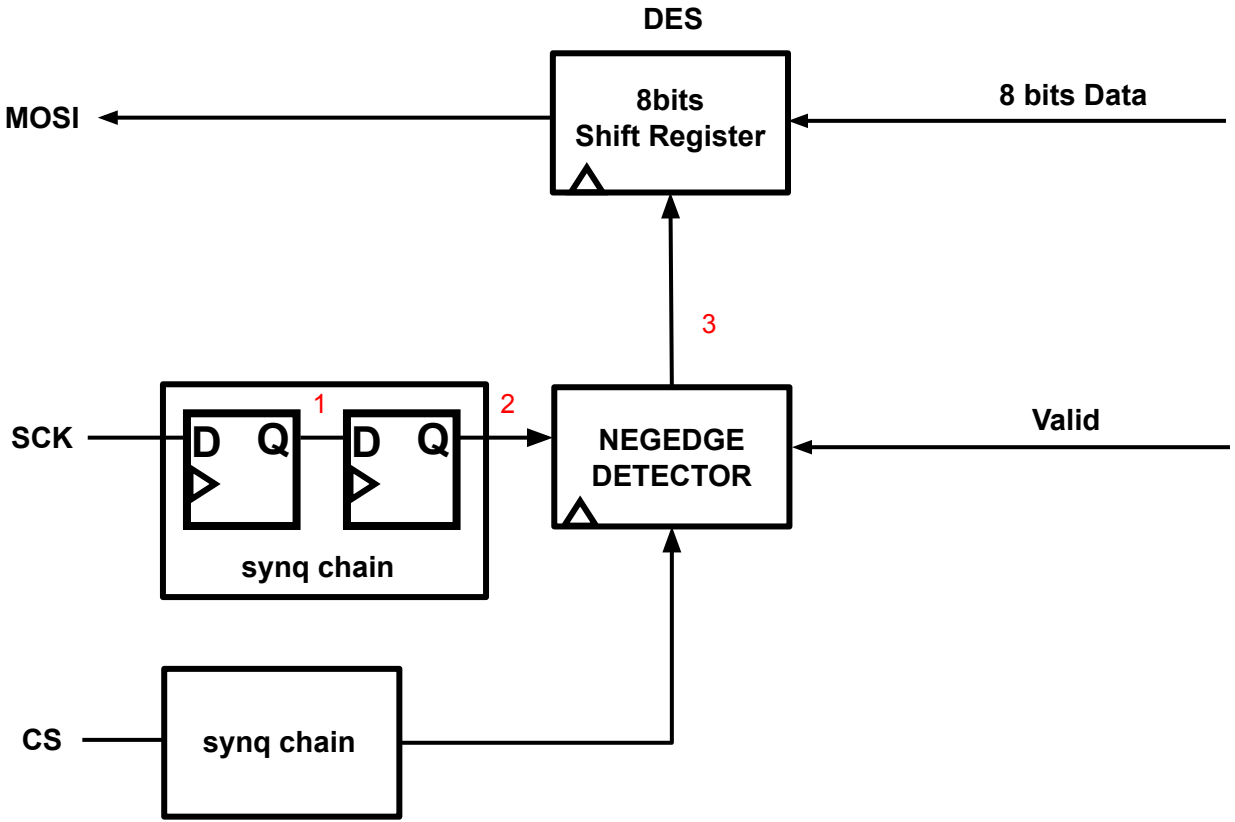


Frequency Limitation for Read Transactions

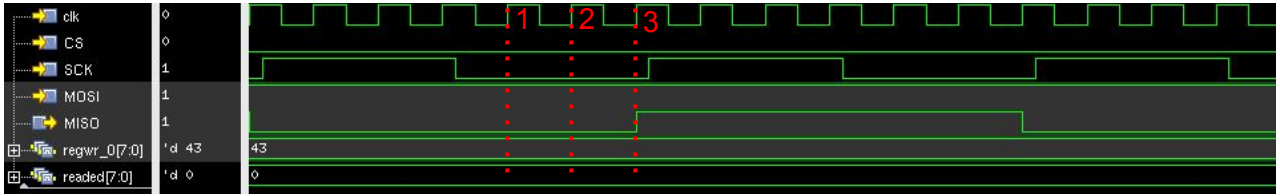
Number latency between sck negedge and MISO :



Serial Interface Controller TX

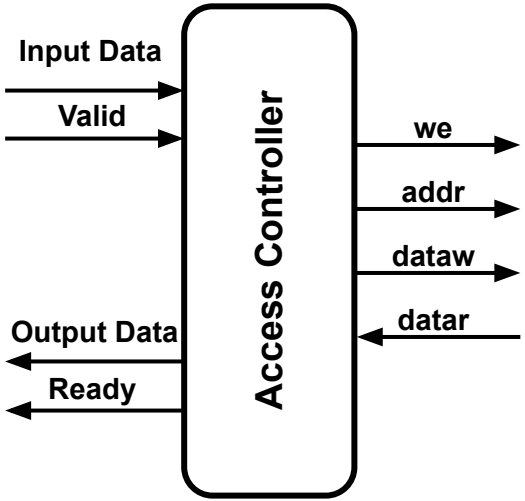


Frequency Limitation for Read Transactions



Frequency limitation for read transactions its ***Fsck < (Fclk / 6)***
In Amazilia Fsck< 52 MHz

Access Controller



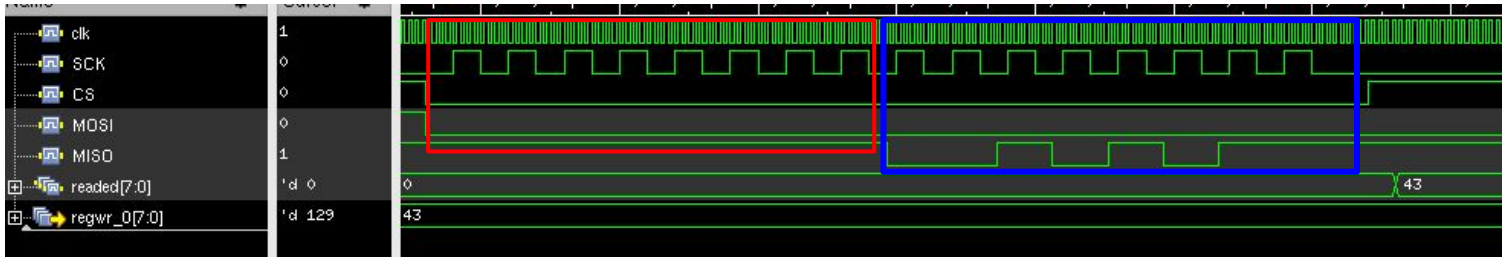
Single Read Transactions
Single Write Transactions
Burst Write Transactions

Write Transaction Wave Form

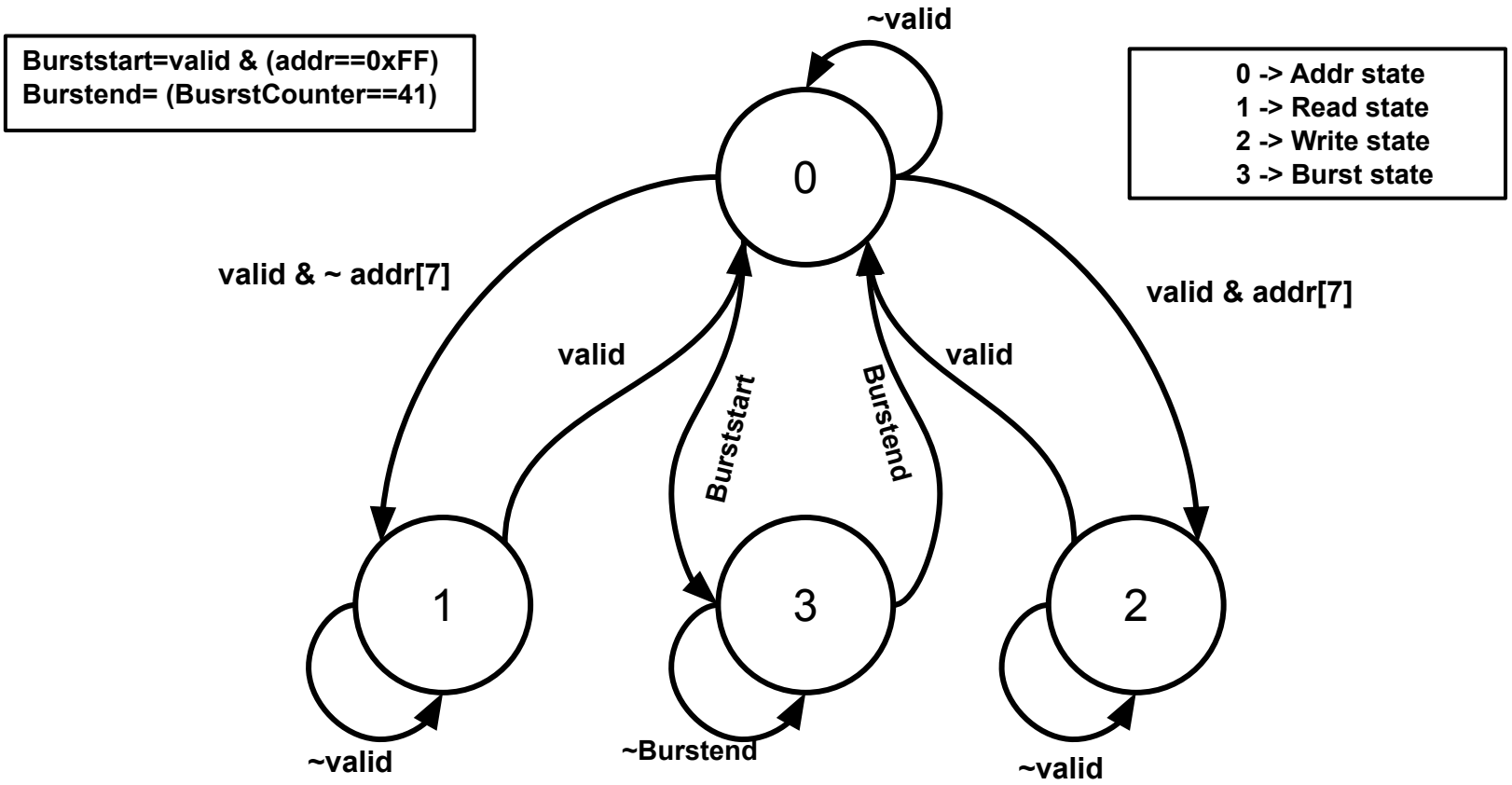
Example of a write transaction over address 0 :

Single Read Transaction Wave Form

Example of a read transaction over address 0 :

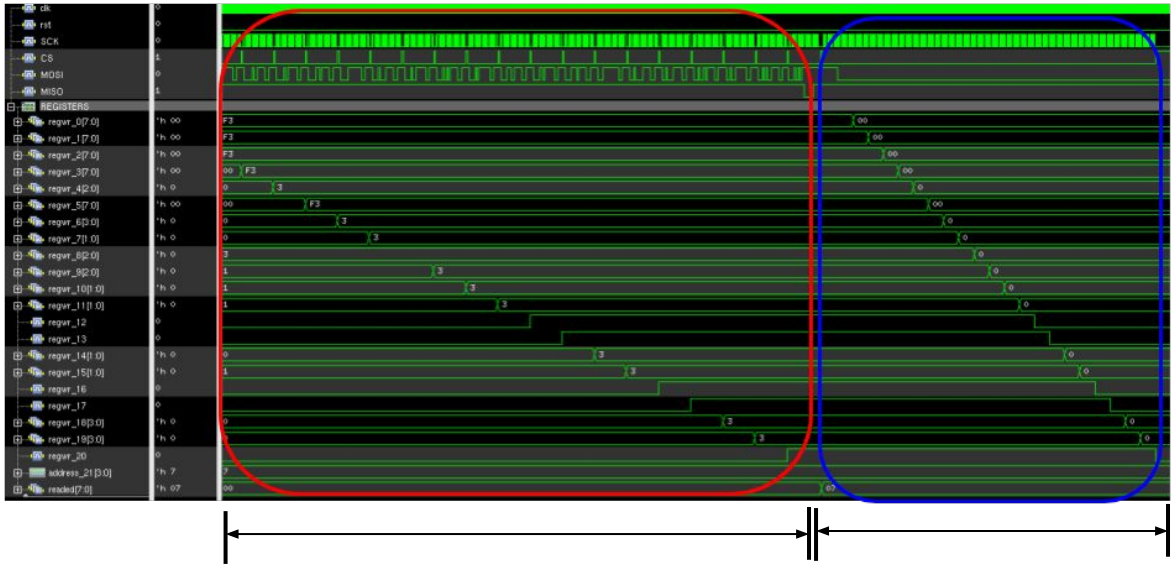


Access Controller



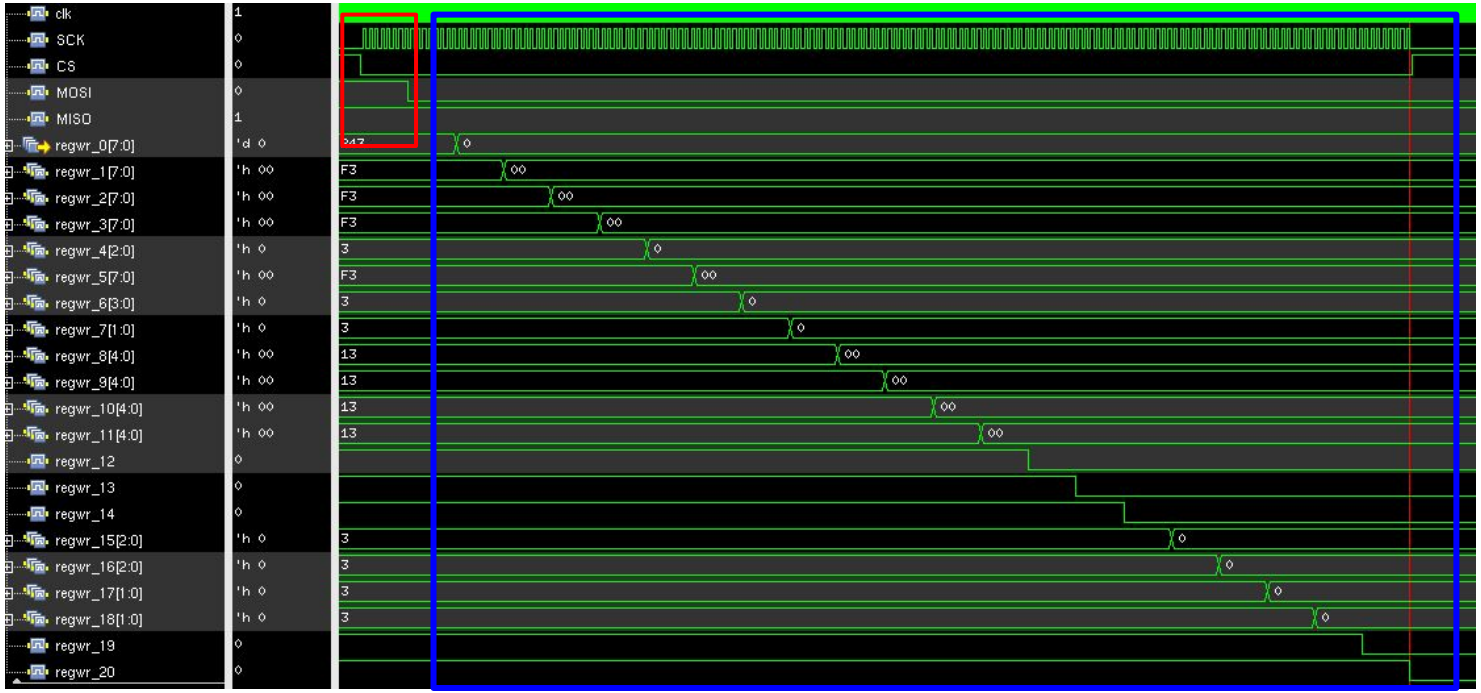
Burst Write Transaction

Burst transaction compared with multiple write transactions:

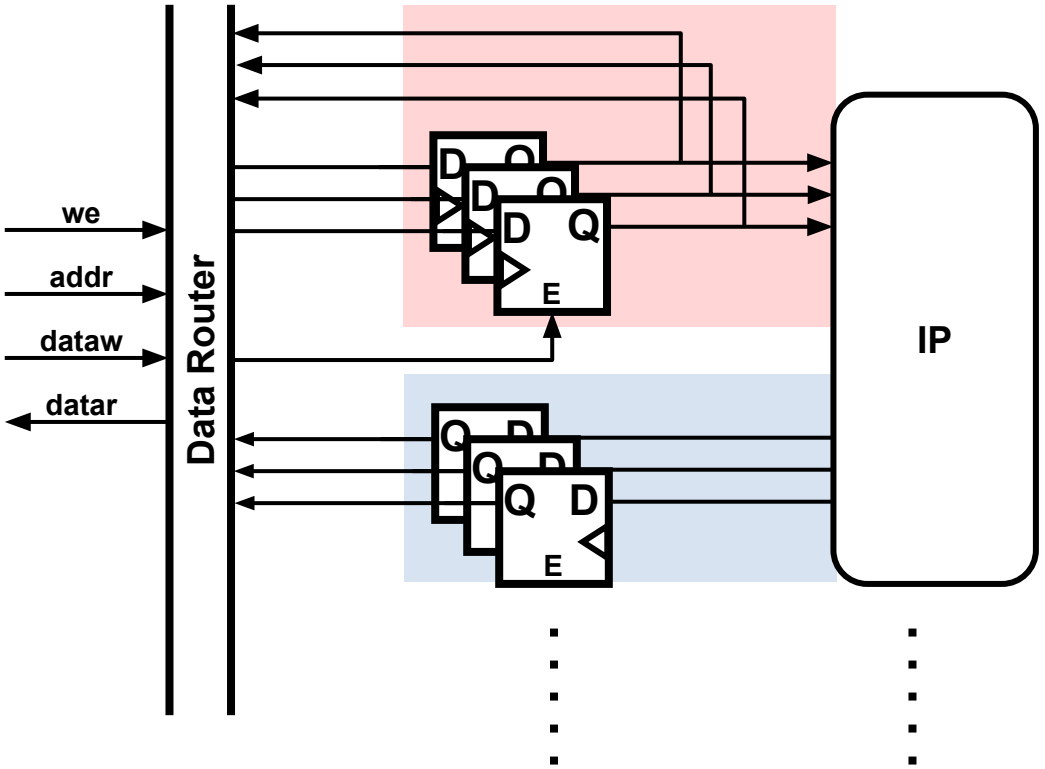


Burst Write Transaction

Burst transaction stages:

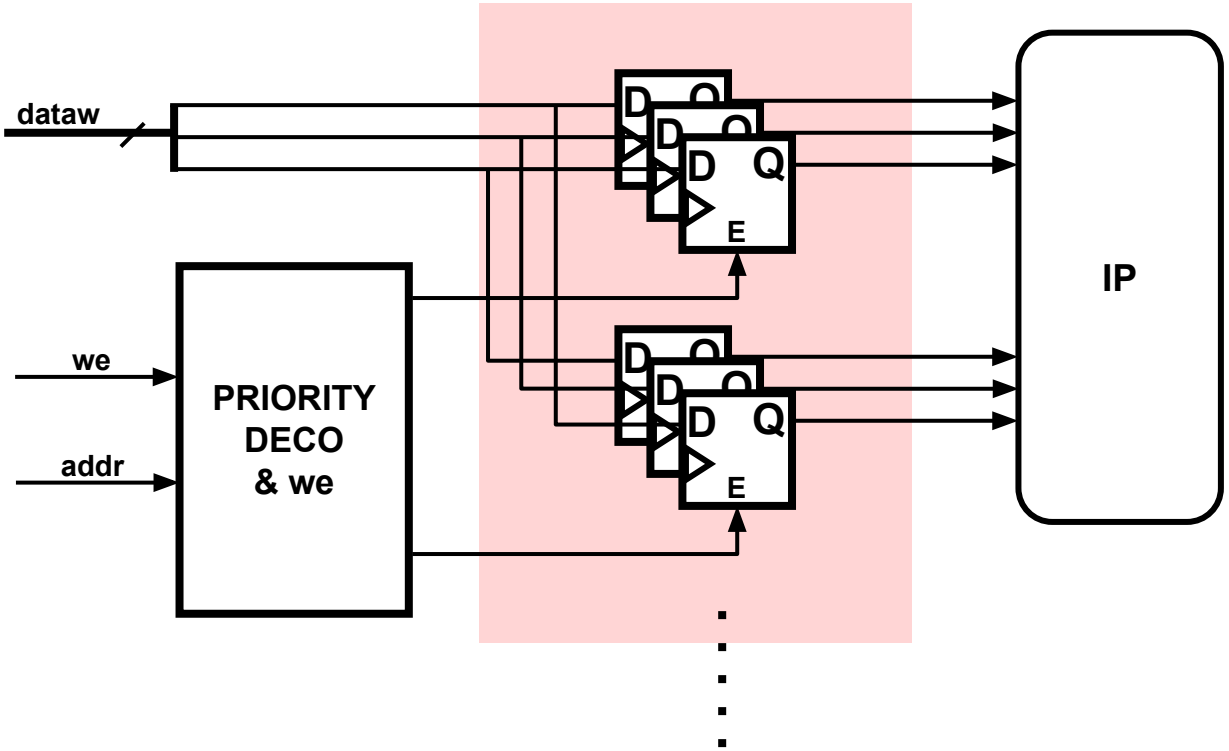


Registers Bank and Data Router

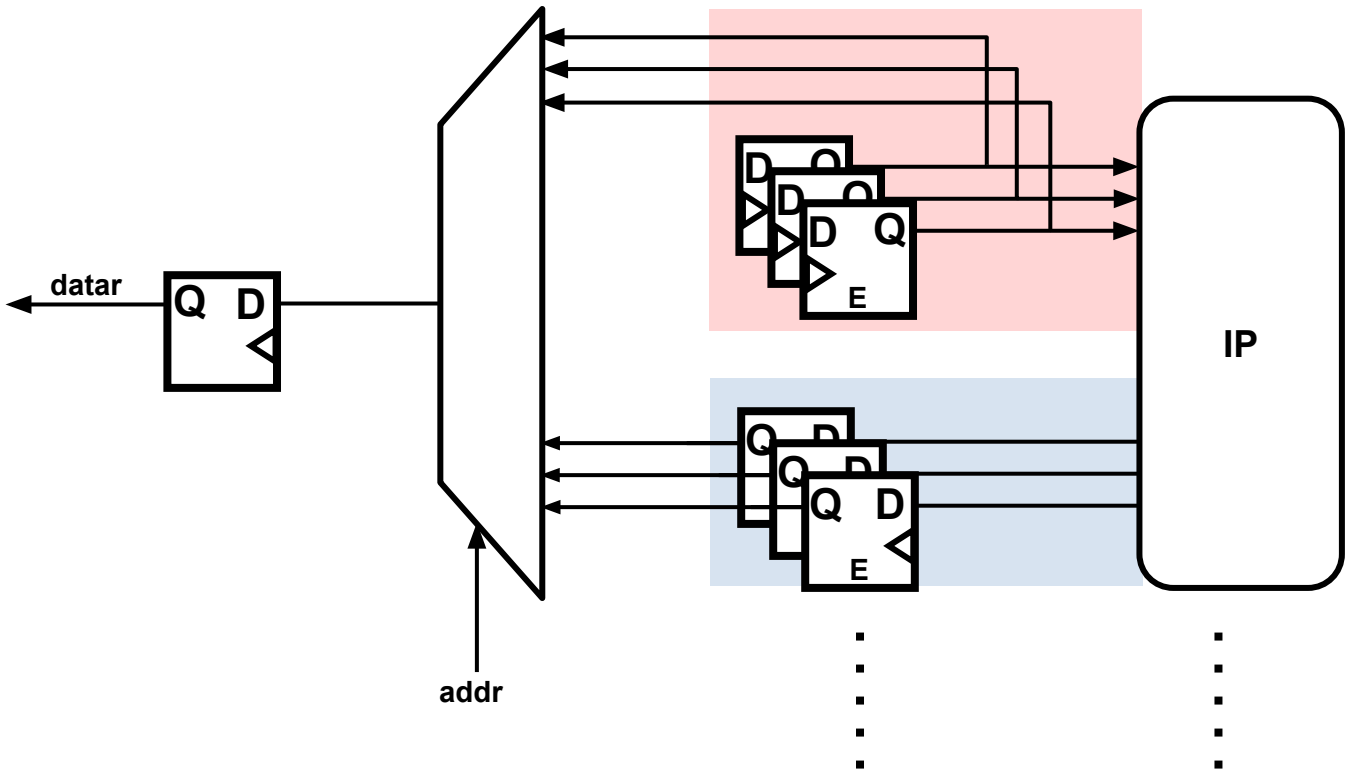


W/R Reg Read Only Reg

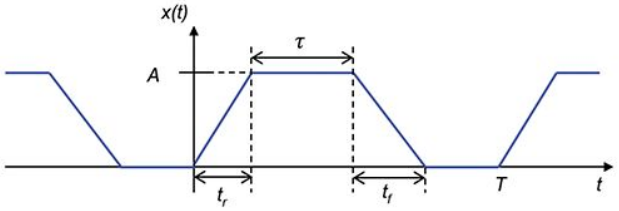
Write Functionality



Read Functionality



Synthesis Constraints



Period	**3.2 ns**
Rise and fall times	**200 ps**
Maximum hold and setup uncertainty	**70 ps**
Maximum delay from input or output	**80 ps**
Output load	**500 fF**

Elaboration Warnings

```
Info    : Elaborating Design. [ELAB-1]
        : Elaborating top-level block 'drac' from file '../verilog/drac.v'.
Warning : Using default parameter value for module elaboration. [CDFG-818]
        : Elaborating block 'drac' with default parameters value.
Info    : Elaborating Subdesign. [ELAB-2]
Info    : Elaborating Subdesign. [ELAB-2]
        : Elaborating block 'access_controler_nreqwr41_nreqr6' from file '../verilog/access_controler.v'.
Warning : Using default parameter value for module elaboration. [CDFG-818]
        : Elaborating block 'access_controler' with default parameters value.
  Checking the design.

          Check Design Report
          -------------------

  Unresolved References & Empty Modules
  -------------------------------------
No unresolved references in design 'drac'

No empty modules in design 'drac'

  Done_Checking the design.
```

Synthesis Report

QoS Summary for drac

Metric	generic	mapnoinc	incremental	mapped
Slack (ps):	1172.4	190.5	5.5	5.5
R2R (ps):	1172.4	190.5	5.5	5.5
I2R (ps):	2772.9	2532.1	2534.4	2534.4
R2O (ps):	2401.1	1150.3	1150.9	1150.9
I2O (ps):	no_value	no_value	no_value	no_value
CG (ps):	no_value	no_value	no_value	no_value
TNS (ps):	0	0	0	0
R2R (ps):	0	0	0	0
I2R (ps):	0	0	0	0
R2O (ps):	0	0	0	0
I2O (ps):	no_value	no_value	no_value	no_value
CG (ps):	no_value	no_value	no_value	no_value
Failing Paths:	0	0	0	0
Area:	27304	21757	21039	21039
Instances:	756	911	846	846
Utilization (%):	0.00	0.00	0.00	0.00
Tot. Net Length (um):	no_value	no_value	no_value	no_value
Avg. Net Length (um):	no_value	no_value	no_value	no_value
Total Overflow H:	0	0	0	0
Total Overflow V:	0	0	0	0
Route Overflow H (%):	no_value	no_value	no_value	no_value
Route Overflow V (%):	no_value	no_value	no_value	no_value
CPU Runtime (m:s):	00:12	00:22	00:03	00:00
Real Runtime (m:s):	00:28	01:07	00:02	00:01
CPU Elapsed (m:s):	00:15	00:37	00:40	00:40
Real Elapsed (m:s):	00:28	01:35	01:37	01:38
Memory (MB):	159.64	194.53	194.53	194.53

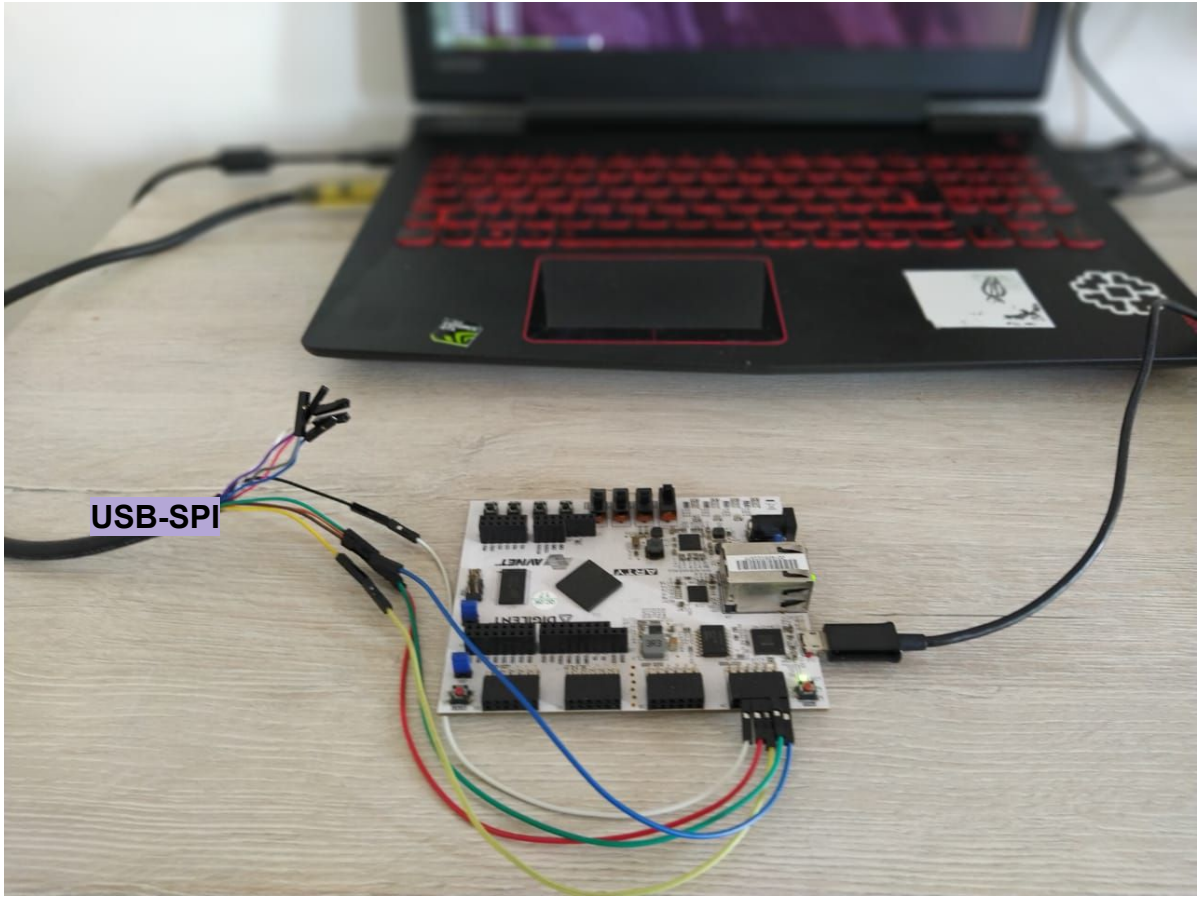
RAC WC Synthesis Area Report 180nm

Registers Bank (181 registers)	**16960 (µm)^2**
Total RAC	**21039 (µm)^2 eq 145 µm x 145 µm**
Overhead	**19.3 %**

WC Synthesis Report 180nm

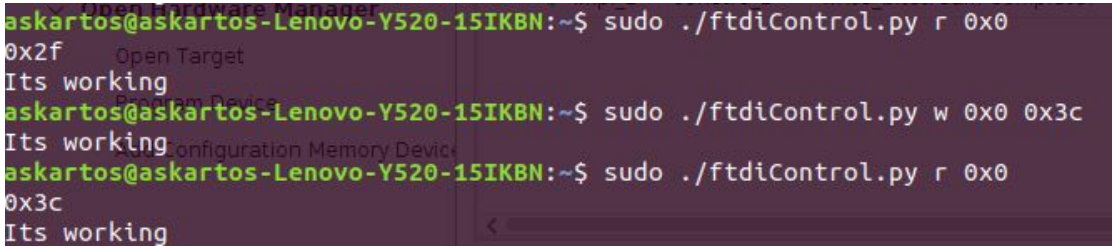
Registers Bank (181 registers)	**16960 (µm)^2**
Total RAC	**21039 (µm)^2 eq 145 µm x 145 µm**
Chip Percentage (1.6mm x 1.6mm)	**0.82 %**

FPGA Prototype



Command Line Use

Single Read and Single Write Transactions been used:



Command Line Use

Burst transaction been used :

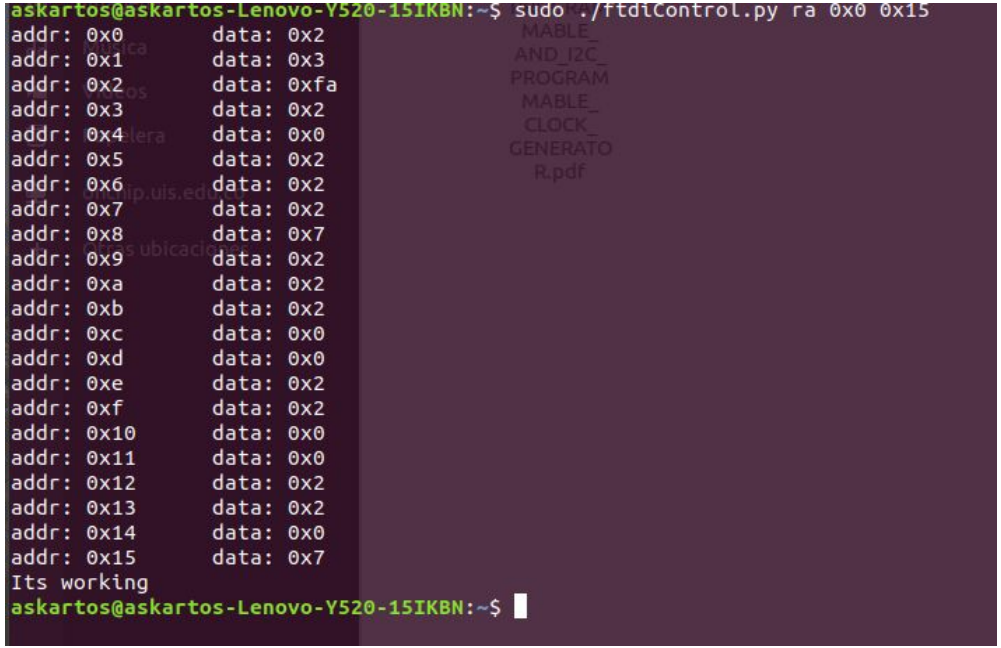
```
askartos@askartos-Lenovo-Y520-15IKBN:~$ sudo ./ftdiControl.py b test.json
21
Its working
askartos@askartos-Lenovo-Y520-15IKBN:~$
```

Abrir | test.json ~/amazilia_stk/jsons | Guardar

```
1 [2,3,250,2,0,2,2,2,7,
2 2,2,2,0,0,2,2,0,7,2,2,
3 2,2,2,2,2,2,2,2,2,1,100]
```

Command Line Use

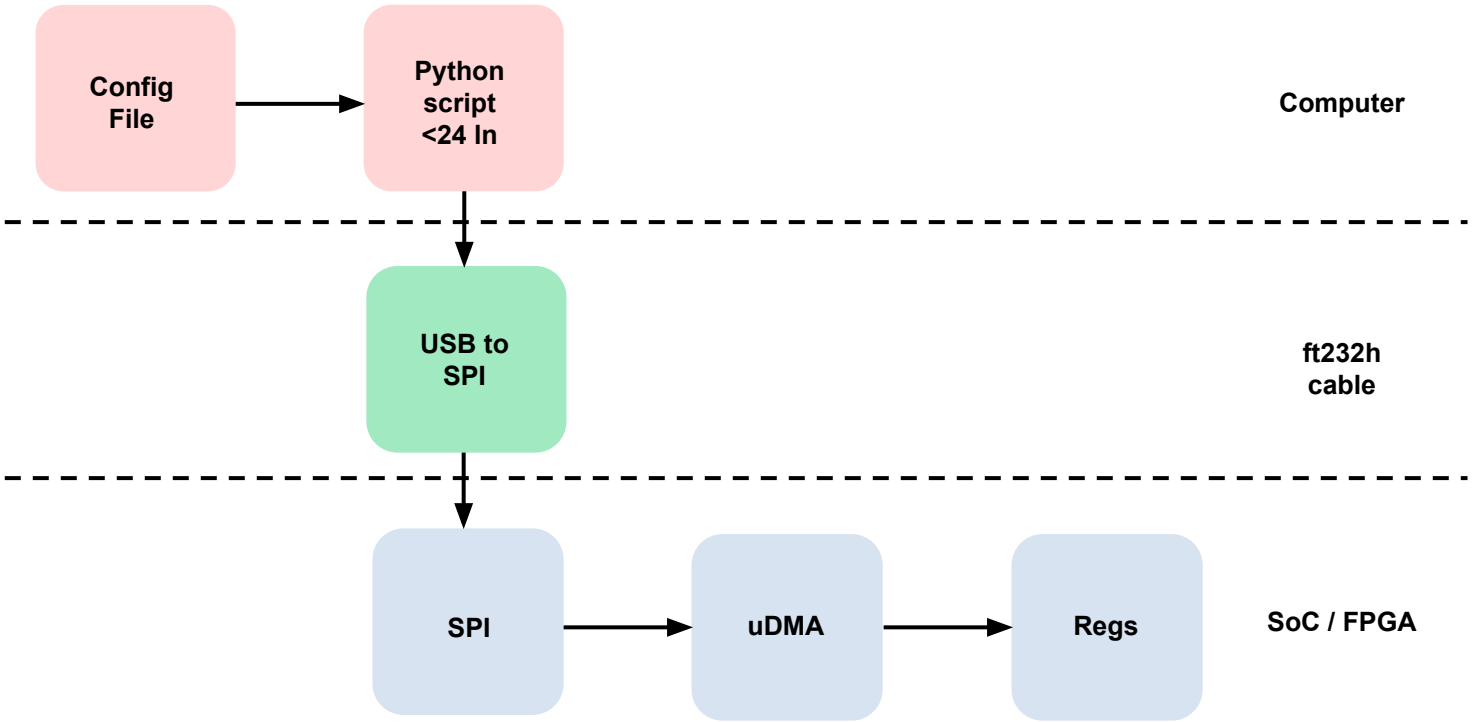
Multiple read software implemented transaction :



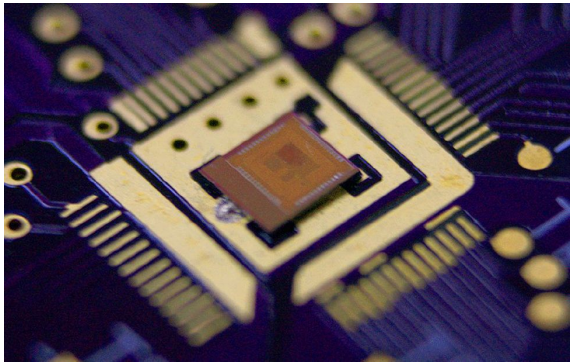
Scripting Capabilities

```
#!/usr/bin/python3
import amazilia



print(amazilia.read(0)) #READS ADDRESS 0

amazilia.write(0,243)   #WRITES ADDRESS 0

print(amazilia.read(0)) #READS ADDRESS 0


print("old data")
amazilia.multiread(0,31)  #READS COMPLETE MEMORY MAP

data=[20,3,11,2,10,2,2,2,11,2,2,2,2,2,2,2,2,2,2,2,2,2,2,2,2,2,2,1,100]

amazilia.burst(data)      #WRITE COMPLETE MEMORY MAP

print("new data")
amazilia.multiread(0,31)  #READS COMPLETE MEMORY MAP
```

Amazilia Config Flow



Thanks! Questions?



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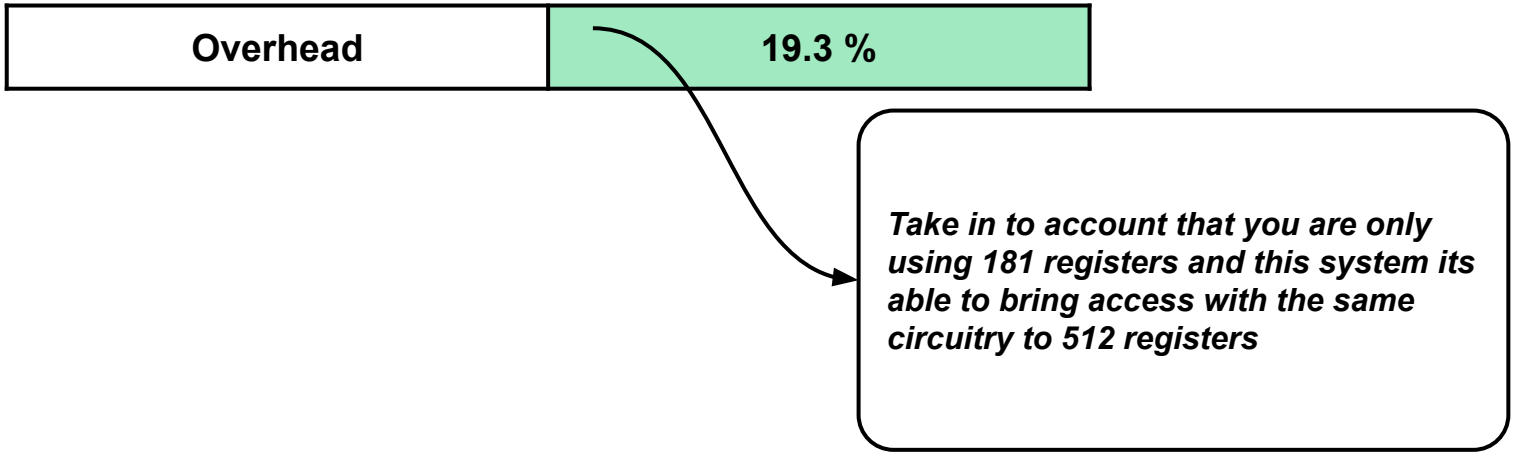
WC Synthesis Report



RAC Synthesis Results Expected WC

Frequency Target	**312,5 MHz**
Number of Flops	**164**

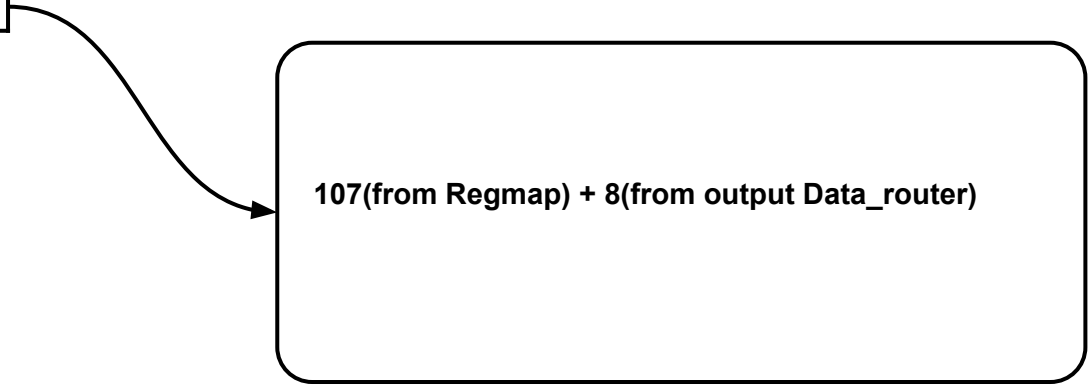
16(from Shift registers) + 107(from Regmap) + 8(from Data_router) + 9 (synq) + 13(from Access Controller) + 5 (burst counter) + 6 (FSMs)

RAC Incremental Synthesis Results WC

Frequency Target	333 MHz
Number of Flops	180 (why ?)
Area	108.5 µm x 108.5 µm

Registers Bank Synthesis Results Expected

Frequency Target	**312,5 MHz**
Number of Flops	**115**



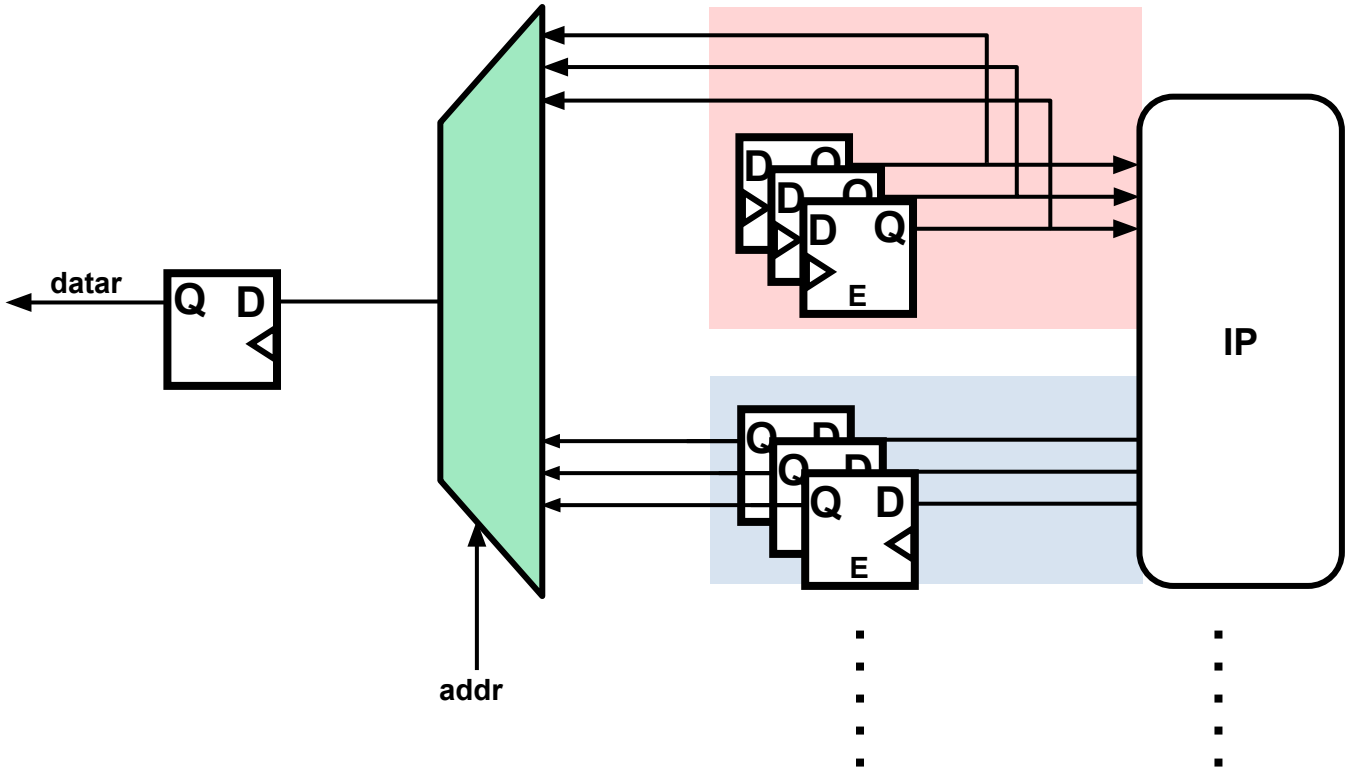
Registers Bank Generic Synthesis Obtained WC

Frequency Target	333 MHz
Number of Flops	115
Area	-

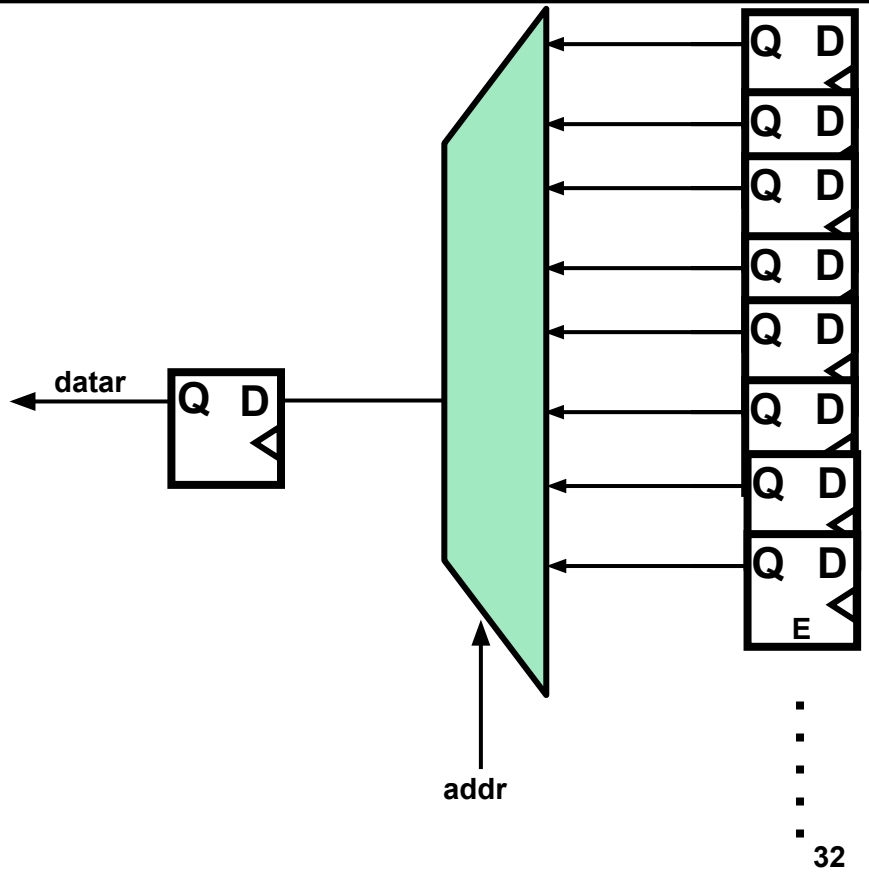
Incremental Synthesis Results Obtained WC

Frequency Target	333 MHz
Number of Flops	144 (guilty)
Area	103.8 µm x 103.8 µm

Re-time Increases number of flops

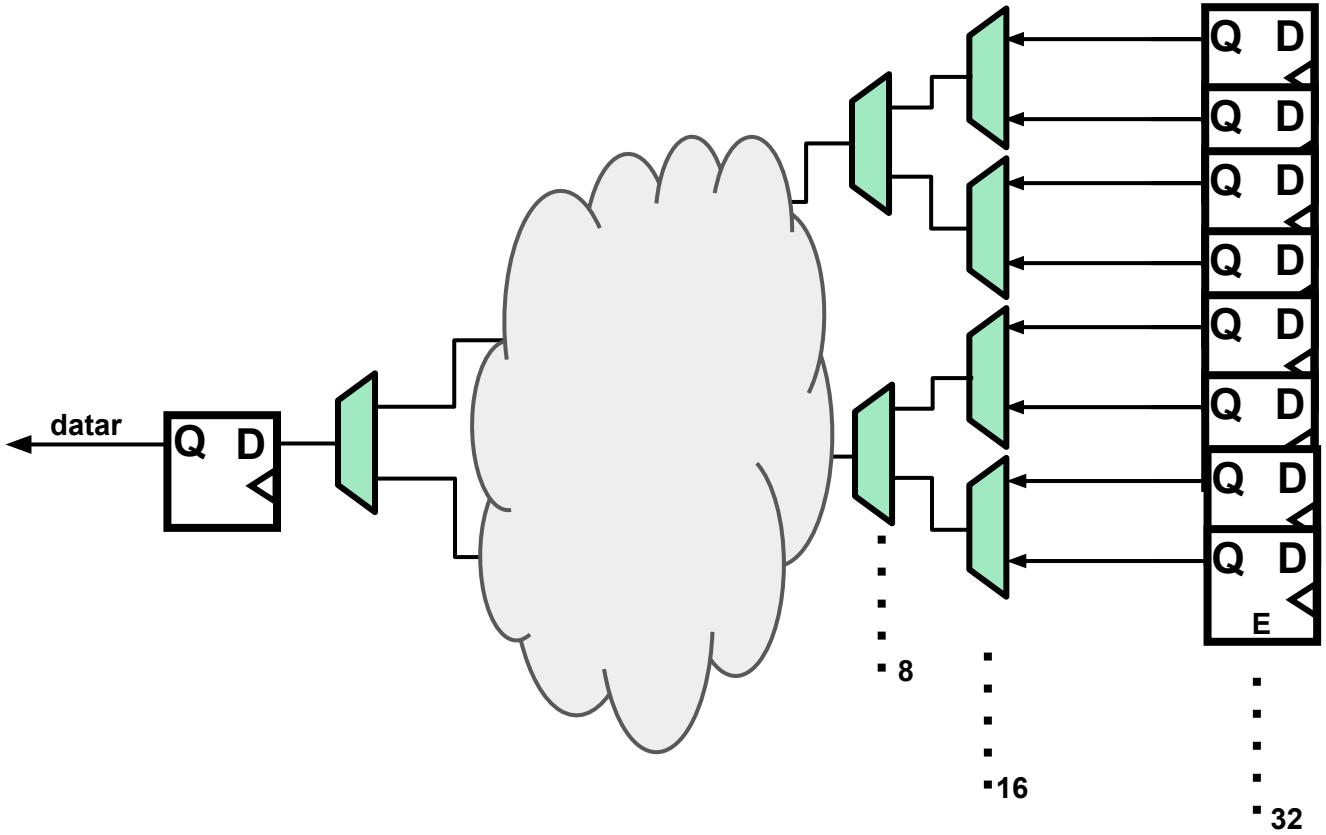


Re-time Increases number of flops



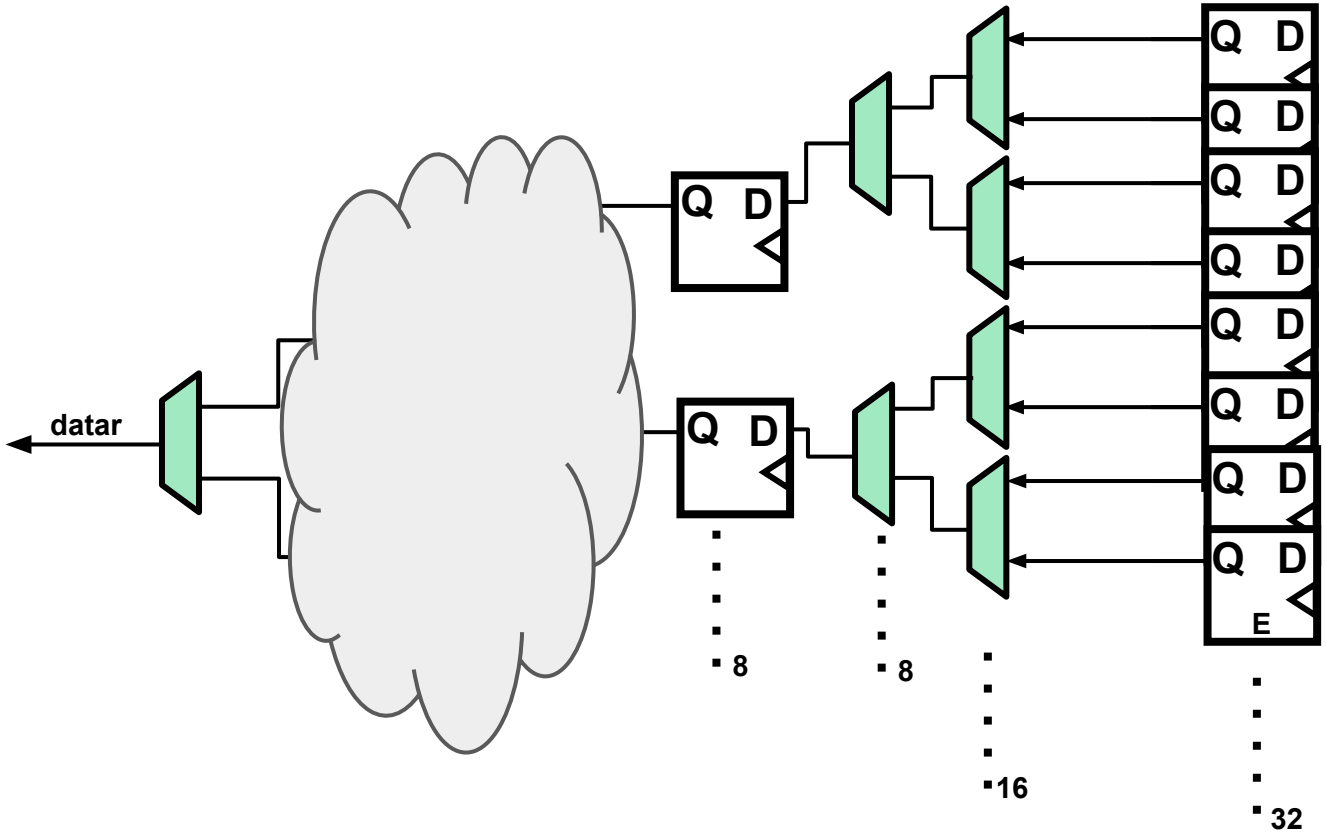
W/R Reg Read Only Reg

Re-time Increases number of flops



W/R Reg Read Only Reg

Re-time Increases number of flops



W/R Reg Read Only Reg