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Road vehicles — Controller area network (CAN) —

Part 2: High-speed medium access unit

Véhicules routiers — Gestionnaire de réseau de communication (CAN) —

Partie 2: Unité d'accès au support à haute vitesse

Reference number
ISO 11898-2:2016(E)

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Foreword

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The procedures used to develop this document and those intended for its further maintenance are described in the ISO/IEC Directives, Part 1. In particular the different approval criteria needed for the different types of ISO documents should be noted. This document was drafted in accordance with the editorial rules of the ISO/IEC Directives, Part 2 (see www.iso.org/directives).

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The committee responsible for this document is ISO/TC 22, *Road vehicles*, Subcommittee SC 31, *Data communication*.

This second edition cancels and replaces the first edition (ISO 11898-2:2003), which has been technically revised, with the following changes:

— max output current on CANH/CANL has been defined (Table 4);

— optional TXD timeout has been defined (Table 7);

— receiver input resistance range has been changed (Table 10);

— Bit timing parameters for CAN FD for up to 2 Mbps have been defined (Table 13);

— Bit timing parameters for CAN FD for up to 5 Mbps have been defined (Table 14);

— content of ISO 11898-5 and ISO 11898-6 has been integrated to ensure there is one single ISO Standard for all HS-PMA implementations;

— selective wake-up (formerly ISO 11898-6) CAN FD tolerance has been defined;

— wake-filter timings (formerly in ISO 11898-5) have been changed (Table 20)

— requirements and assumptions about the PMD sublayer have been shifted to Annex A, to clearly focus on the HS-PMA implementation.

A list of all parts in the ISO 11898 series can be found on the ISO website.

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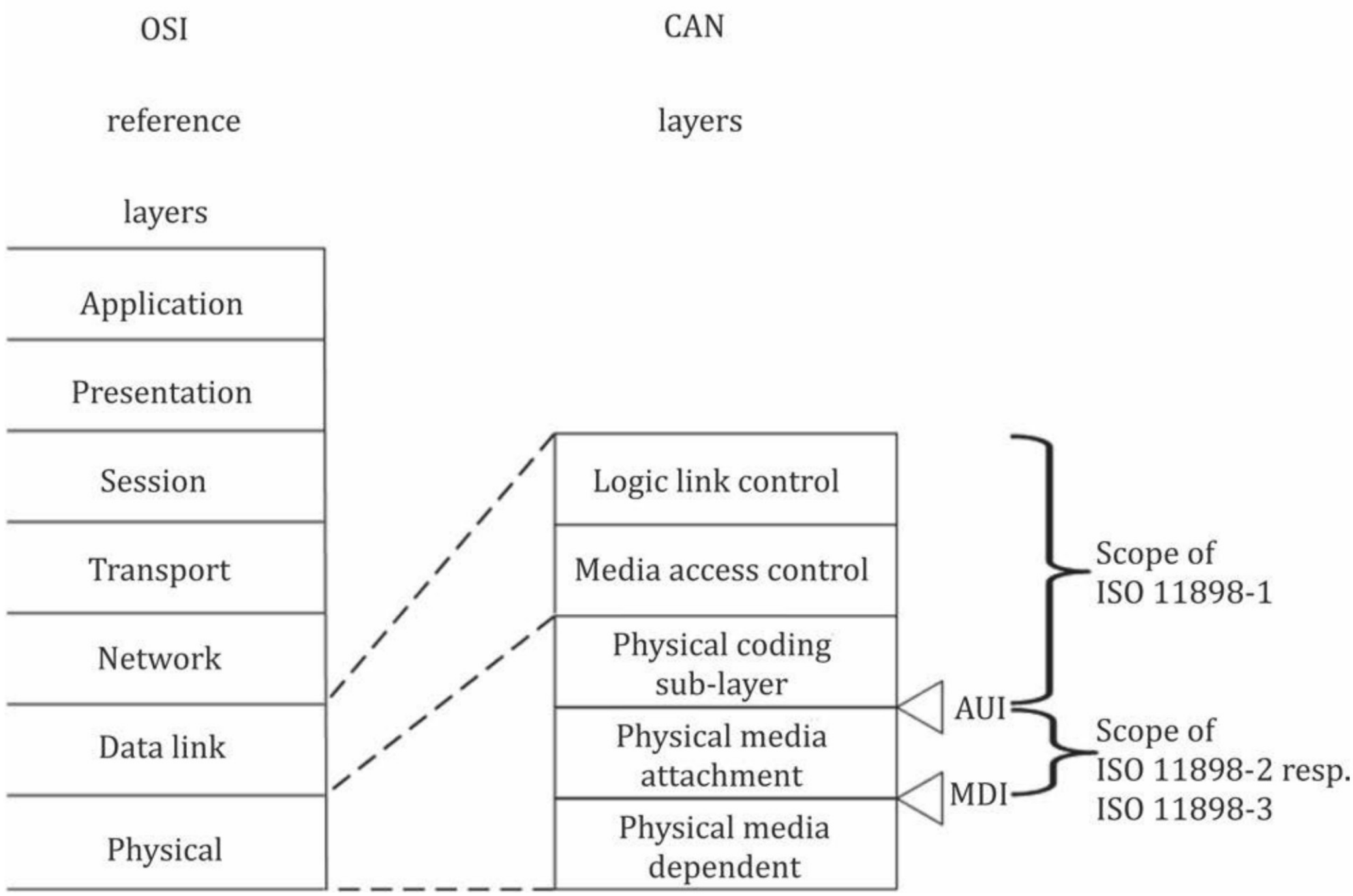
Introduction

ISO 11898 was first published as one document in 1993. It covered the CAN data link layer as well as the high-speed physical layer. In the reviewed and restructured ISO 11898 series, ISO 11898-1 and ISO 11898-4 defined the CAN protocol and time-triggered CAN (TTCAN) while ISO 11898-2 defines the high-speed physical layer, and ISO 11898-3 defined the low-speed fault tolerant physical layer.

Figure 1 shows the relation of the Open System Interconnection (OSI) layers and its sublayers to ISO 11898-1, this document as well as ISO 11898-3.



Key

AUI attachment unit interface

MDI media dependant interface

OSI open system interconnection

Figure 1 — Overview of ISO 11898 specification series

The International Organization for Standardization (ISO) draws attention to the fact that it is claimed that compliance with this document may involve the use of a patent concerning the selective wake-up function given in 5.9.4.

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Road vehicles — Controller area network (CAN) —

Part 2:
High-speed medium access unit

1 Scope

This document specifies the high-speed physical media attachment (HS-PMA) of the controller area network (CAN), a serial communication protocol that supports distributed real-time control and multiplexing for use within road vehicles. This includes HS-PMAs without and with low-power mode capability as well as with selective wake-up functionality. The physical media dependant sublayer is not in the scope of this document.

2 Normative references

The following documents are referred to in the text in such a way that some or all of their content constitutes requirements of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

ISO 11898-1:2015, *Road vehicles — Controller area network (CAN) — Part 1: Data link layer and physical signalling*

ISO 16845-2, *Road vehicles — Controller area network (CAN) conformance test plan — Part 2: High-speed medium access unit with selective wake-up functionality*

3 Terms and definitions

For the purposes of this document, the terms and definitions given in ISO 11898-1 and the following apply.

ISO and IEC maintain terminological databases for use in standardization at the following addresses:

— IEC Electropedia: available at http://www.electropedia.org/

— ISO Online browsing platform: available at http://www.iso.org/obp

NOTE See Figure A.1 for a visualization of the definitions.

3.1
attachment unit interface
AUI
interface between the PCS that is specified in ISO 11898-1 and the PMA that is specified in this document

3.2
ground
GND
electrical signal ground

3.3
legacy implementation
HS-PMA implementation that has been released prior to the publication of this document

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3.4
low-power mode
mode in which the transceiver is not capable of transmitting or receiving messages, except for the purposes of determining if a WUP or WUF is being received

3.5
medium attachment unit
MAU
unit that comprises the physical media attachment and the media dependent interface

3.6
media dependent interface
MDI
interface that ensures proper signal transfer between the media and the physical media attachment

3.7
normal-power mode
mode in which the transceiver is fully capable of transmitting and receiving messages

3.8
physical coding sublayer
PCS
sublayer that performs bit encoding/decoding and synchronization

3.9
physical media attachment
PMA
sublayer that converts physical signals into logical signals and vice versa

3.10
transceiver
implementation that comprises one or more physical media attachments

4 Symbols and abbreviated terms

For the purposes of this document, the symbols and abbreviated terms given in ISO 11898-1 and the following apply. Some of these abbreviations are also defined in ISO 11898-1. If the definition of the term in this document is different from the definition in ISO 11898-1, this definition applies.

AUI	attachment unit interface
DLC	data length code
EMC	electromagnetic compatibility
ESD	electro static discharge
GND	ground
HS-PMA	high-speed PMA
MAU	medium attachment unit
MDI	media dependent interface
PCS	physical coding sublayer
PMA	physical media attachment

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PMD physical media dependent

WUF wake-up frame

WUP wake-up pattern

5 Functional description of the HS-PMA

5.1 General

The HS-PMA comprises one transmitter and one receiving entity. It shall be able to bias the connected physical media, an electric two-wire cable, relative to a common ground. The transmitter entity shall drive a differential voltage between the CAN_H and CAN_L signals to signal a logical 0 (dominant) or shall not drive a differential voltage to signal a logical 1 (recessive) to be received by other nodes connected to the very same media. These two signals are the interface to the physical media dependent sublayer.

The HS-PMA shall provide an AUI to the physical coding sublayer as specified in ISO 11898-1. It comprises the TXD and RXD signals as well as the GND signal. The TXD signal receives from the physical coding sublayer the bit-stream to be transmitted on the MDI. The RXD signal transmits to the physical coding sublayer the bit-stream received from the MDI.

Implementations that comprise one or more HS-PMAs shall at least support the normal-power mode of operation. Optionally, a low-power mode may be implemented.

Some of the items specified in the following depend on the operation mode of the (part of the) implementation, in which the HS-PMA is included.

Table 1 shows the possible combinations of HS-PMA operating modes and expected behaviour.

Table 1 — HS-PMA operating modes and expected behaviour

Operating mode	Bus biasing behaviour	Transmitter behaviour
Normal	Bus biasing active	Dominant or recessive[a]
Low-power	Bus biasing active or inactive	Recessive

[a] Depends on input conditions as described in this document.

All parameters given in this subclause shall be fulfilled throughout the operating temperature range and supply voltage range (if not explicitly specified for unpowered) as specified individually for every HS-PMA implementation.

5.2 HS-PMA test circuit

The outputs of the HS-PMA implementation to the CAN signals are called CAN_H and CAN_L, TXD is the transmit data input and RXD is the receive data output. Figure 2 shows the external circuit that defines the measurement conditions for all required voltage and current parameters. R_L represents the effective resistive load (bus load) for an HS-PMA implementation, when used in a network, and C_1 represents an optional split-termination capacitor. The values of R_L and C_1 vary for different parameters that the HS-PMA implementation needs to meet and are given as condition in Tables 2 to 20.

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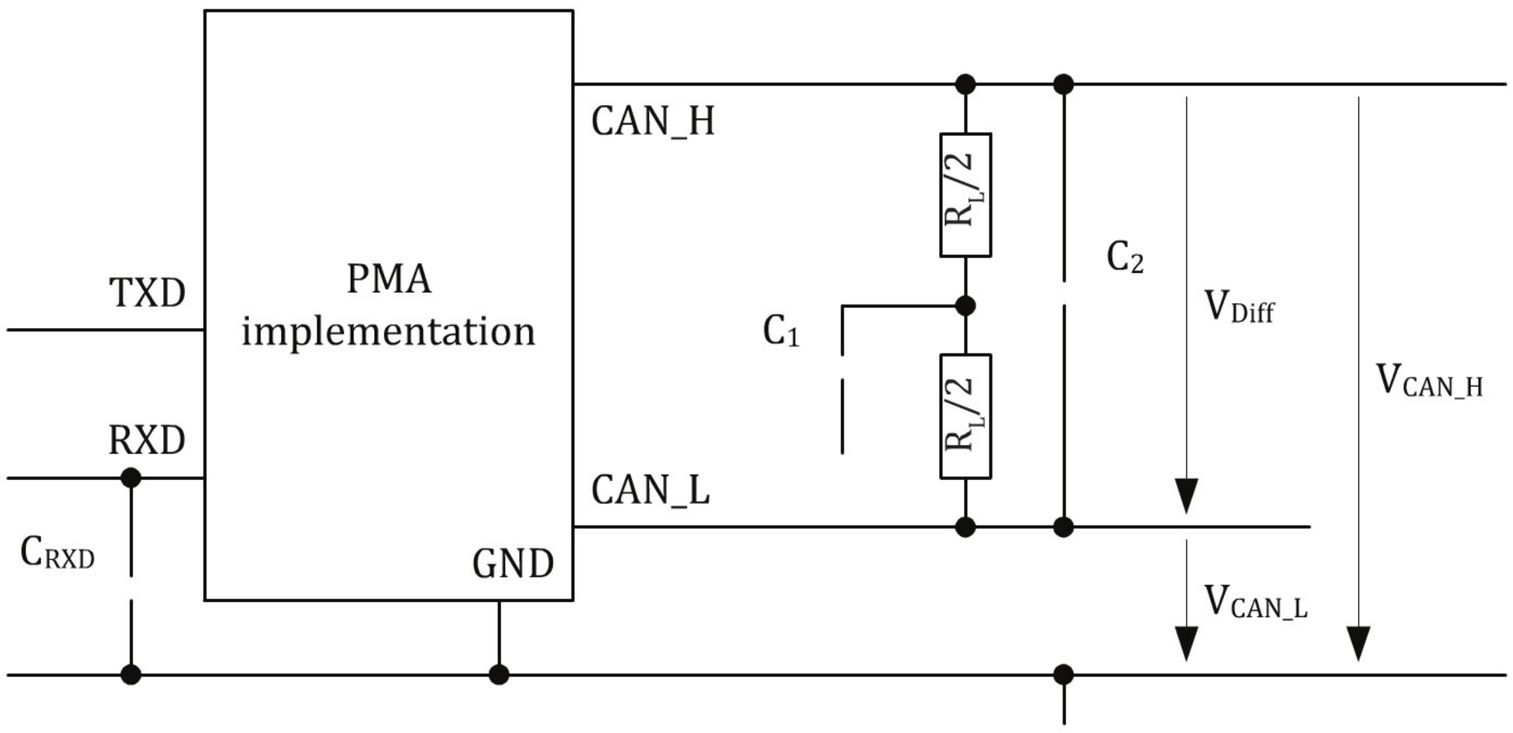

Key

V_{Diff} differential voltage between CAN_H and CAN_L wires

V_{CAN_H} single ended voltage on CAN_H wire

V_{CAN_L} single ended voltage on CAN_L wire

C_{RXD} capacitive load on RXD

Figure 2 — HS-PMA test circuit

5.3 Transmitter characteristics

This subclause specifies the transmitter characteristics of a single HS-PMA implementation under the conditions as depicted in Figure 2; so no other HS-PMA implementations are connected to the media. The behaviour of an HS-PMA implementation connected to other HS-PMAs is outside the scope of this subclause. Refer to A.2 for consideration when multiple HS-PMAs are connected to the same media. The voltages and currents that are required on the CAN_L and CAN_H signals are specified in Tables 2 to 6. Table 2 specifies the output characteristics during dominant state.

Figure 3 illustrates the voltage range for the dominant state.

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Table 2 — HS-PMA dominant output characteristics

Parameter	Notation	Value			Condition
		Min V	Nom V	Max V	
Single ended voltage on CAN_H	V_{CAN_H}	+2,75	+3,5	+4,5	R_L = 50 Ω ...65 Ω
Single ended voltage on CAN_L	V_{CAN_L}	+0,5	+1,5	+2,25	R_L = 50 Ω ...65 Ω
Differential voltage on normal bus load	V_{Diff}	+1,5	+2,0	+3,0	R_L = 50 Ω ...65 Ω
Differential voltage on effective resistance during arbitration	V_{Diff}	+1,5	Not defined	+5,0	R_L = 2 240 Ω[a]
Optional: Differential voltage on extended bus load range	V_{Diff}	+1,4	+2,0	+3,3	R_L = 45 Ω ...70 Ω

[a] 2 240 Ω is emulating a situation with up to 32 nodes sending dominant simultaneously. In such case, the effective load resistance for a single node decreases (a node does drive only a part of the nominal bus load). Assuming a MAX R_L of 70 Ω, this scenario covers a 32 nodes network. (2 240 Ω/70 Ω per node = 32 nodes.)

All requirements in this table apply concurrently. Therefore, not all combinations of V_{CAN_H} and V_{CAN_L} are compliant with the defined differential voltage (see Figure 3).

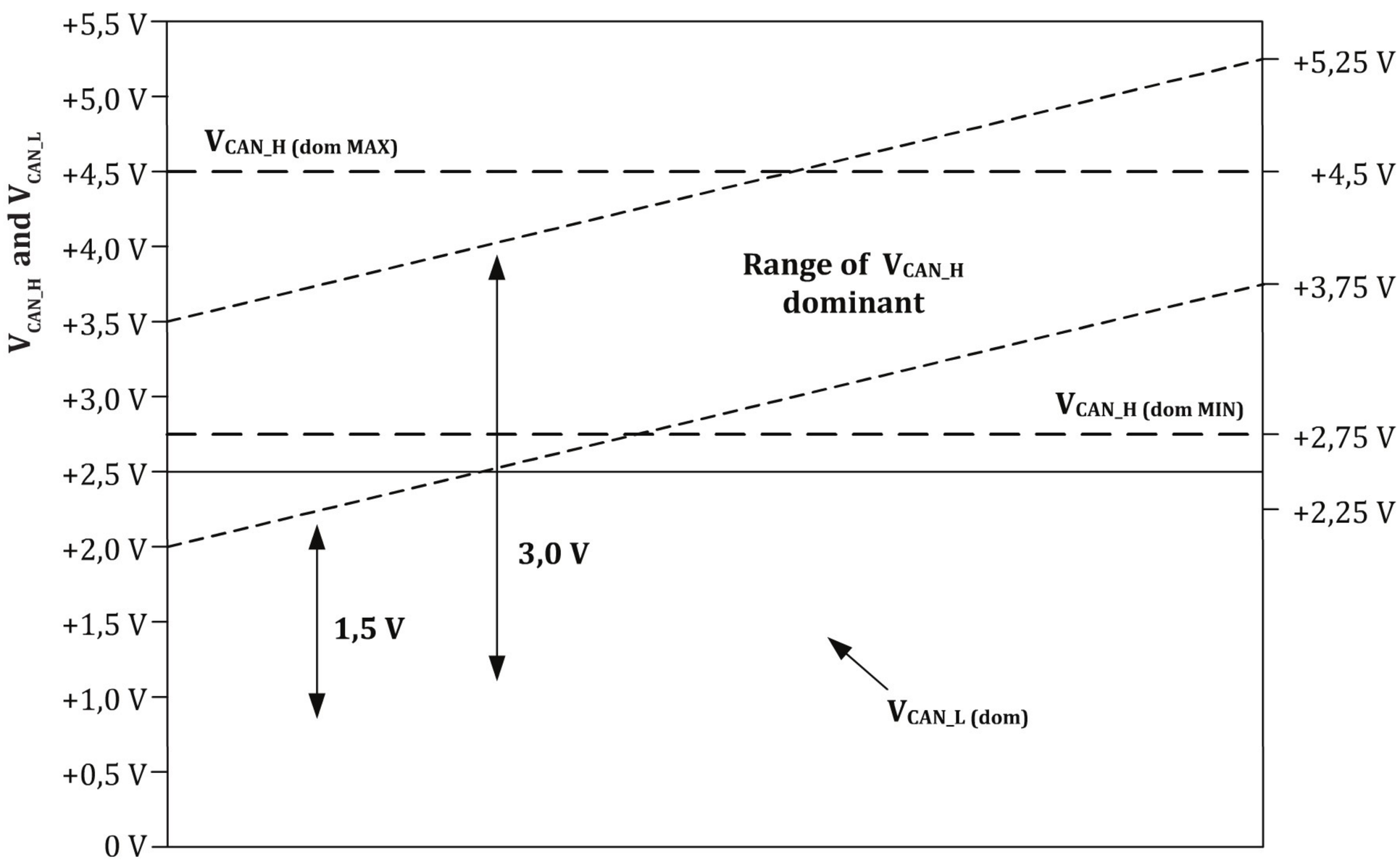
Measurement setup according to Figure 2 (only one HS-PMA present):

R_L, see "Condition" column above

C_1 = 0 pF (not present)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)



Key

V_{Diff} differential voltage between CAN_H and CAN_L wires

V_{CAN_H} single ended voltage on CAN_H wire

V_{CAN_L} single ended voltage on CAN_L wire

Figure 3 — Voltage range of V_{CAN_H} during dominant state of CAN node, when V_{CAN_L} varies from minimum to maximum voltage level (50 Ω ... 65 Ω bus load condition)

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In order to achieve a level of RF emission that is acceptably low, the transmitter shall meet the driver signal symmetry as required in Table 3.

Table 3 — HS-PMA driver symmetry

Parameter	Notation	Value		
		Min	Nom	Max
Driver symmetry[a]	v_{sym}	+0,9	+1,0	+1,1

[a] $v_{sym} = (V_{CAN_H} + V_{CAN_L})/V_{CC}$, with V_{CC} being the supply voltage of the transmitter.

v_{sym} shall be observed during dominant and recessive state and also during the transition from dominant to recessive and vice versa, while TXD is stimulated by a square wave signal with a frequency that corresponds to the highest bit rate for which the HS-PMA implementation is intended, however, at most 1 MHz (2 Mbit/s) (HS-PMA in normal mode).

Measurement setup according to Figure 2:

R_L = 60 Ω (tolerance ≤ ±1 %)

C_1 = 4,7 nF (tolerance ≤ ±5 %)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)

The maximum output current of the transmitter shall be limited according to Table 4.

Table 4 — Maximum HS-PMA driver output current

Parameter	Notation	Value		Condition
		Min mA	Max mA	
Absolute current on CAN_H	I_{CAN_H}	not defined	115	$-3\ V \le V_{CAN_H} \le +18\ V$
Absolute current on CAN_L	I_{CAN_L}	not defined	115	$-3\ V \le V_{CAN_L} \le +18\ V$

Measurement setup according to Figure 2 with either V_{CAN_H} or V_{CAN_L} enforced to voltage levels as mentioned in the conditions by connection to an external voltage source, while the HS-PMA is driving the output dominant. The absolute maximum value does not care about the direction in which the current flows.

$R_L > 10^{10}$ Ω (not present)

C_1 = 0 pF (not present)

C_2 = 0 pF (not present)

C_{RXD} = 0 pF (not present)

NOTE It is expected that the implementation does not stop driving its output dominant when the differential voltage between CAN_H and CAN_L is outside the limits given in the Condition column. The minimum output current is implicitly defined in Table 2 and thus can be expected to be above 30 mA.

Table 5 specifies the recessive output characteristics when bus biasing is active.

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Table 5 — HS-PMA recessive output characteristics, bus biasing active

Parameter	Notation	Value		
		Min V	Nom V	Max V
Single ended output voltage on CAN_H	V_{CAN_H}	+2,0	+2,5	+3,0
Single ended output voltage on CAN_L	V_{CAN_L}	+2,0	+2,5	+3,0
Differential output voltage	V_{Diff}	−0,5	0	+0,05
All requirements in this table apply concurrently. Therefore, not all combinations of V_{CAN_H} and V_{CAN_L} are compliant with the defined differential output voltage. Measurement setup according to Figure 2: $R_L > 10^{10}$ Ω (not present) C_1 = 0 pF (not present) C_2 = 0 pF (not present) C_{RXD} = 0 pF (not present)				

Table 6 specifies the recessive output characteristics when bus biasing is inactive.

Table 6 — HS-PMA recessive output characteristics, bus biasing inactive

Parameter	Notation	Value		
		Min V	Nom V	Max V
Single ended output voltage on CAN_H	V_{CAN_H}	−0,1	0	+0,1
Single ended output voltage on CAN_L	V_{CAN_L}	−0,1	0	+0,1
Differential output voltage	V_{Diff}	−0,2	0	+0,2
See 5.10 to determine when bias shall be inactive. Measurement setup according to Figure 2: $R_L > 10^{10}$ Ω (not present) C_1 = 0 pF (not present) C_2 = 0 pF (not present) C_{RXD} = 0 pF (not present)				

The implementation of an HS-PMA may limit the duration of dominant transmission in order not to prevent other CAN nodes from communication when the TXD input is permanently asserted. The HS-PMA implementation should implement a timeout within the limits specified in Table 7.

Table 7 — Optional HS-PMA transmit dominant timeout

Parameter	Notation	Value	
		Min ms	Max ms
Transmit dominant timeout[a]	t_{dom}	0,8	10,0
[a] A minimum value of 0,3 ms is accepted for legacy implementations.			

NOTE There is a relation between the t_{dom} minimum value and the minimum bit rate. A t_{dom} minimum value of 0,8 ms accommodates 17 consecutive dominant bits at bit rates greater than or equal to 21,6 kbit/s and 36 consecutive dominant bits at bit rates greater than or equal to 45,8 kbit/s. The value 17 reflects PMA implementation attempts to send a dominant bit and every time sees a recessive level at the receive data input. The value 36 reflects six consecutive error frames when there is a bit error in the last bit of the first five attempts.

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5.4 Receiver characteristics

The receiver uses the transmitter output signals CAN_H and CAN_L as differential input. Figure 2 shows the definition of the voltages at the connections of the HS-PMA's implementation.

When the HS-PMA implementation is in its low-power mode and bus biasing is active, then the recessive and dominant state differential input voltage ranges according to Table 8 apply.

Table 8 — HS-PMA static receiver input characteristics, bus biasing active

Parameter	Notation	Value		Condition
		Min V	Max V	
Recessive state differential input voltage range	V_{Diff}	−3,0	+0,5	$-12{,}0\ V \le V_{CAN_L} \le +12{,}0\ V$ $-12{,}0\ V \le V_{CAN_H} \le +12{,}0\ V$
Dominant state differential input voltage range	V_{Diff}	+0,9	+8,0	$-12{,}0\ V \le V_{CAN_L} \le +12{,}0\ V$ $12{,}0\ V \le V_{CAN_H} \le +12{,}0\ V$
Measurement setup according Figure 2: $R_L > 10^{10}\ \Omega$ (not present) $C_1 = 0$ pF (not present) $C_2 = 0$ pF (not present) $C_{RXD} = 0$ pF (not present) NOTE A negative differential voltage may temporarily occur when the HS-PMA is connected to a media in which common mode chokes and/or unterminated stubs are present. The maximum positive differential voltage may temporarily occur when the HS-PMA is connected to a media while more than one HS-PMA is sending dominant and concurrently a ground shift between the sending HS-PMAs is present.				

When the HS-PMA implementation is in its low-power mode and bus biasing is inactive, then the recessive and dominant state differential input voltage ranges according to Table 9 apply.

Table 9 — HS-PMA static receiver input characteristics, bus biasing inactive

Parameter	Notation	Value		Condition
		Min V	Max V	
Recessive state differential input voltage range	V_{Diff}	−3,0	+0,4	$-12{,}0\ V \le V_{CAN_L} \le +12{,}0\ V$ $-12{,}0\ V \le V_{CAN_H} \le +12{,}0\ V$
Dominant state differential input voltage range	V_{Diff}	+1,15	+8,0	$-12{,}0\ V \le V_{CAN_L} \le +12{,}0\ V$ $-12{,}0\ V \le V_{CAN_H} \le +12{,}0\ V$
Measurement setup according Figure 2: $R_L > 10^{10}\ \Omega$ (not present) $C_1 = 0$ pF (not present) $C_2 = 0$ pF (not present) $C_{RXD} = 0$ pF (not present) NOTE A negative differential voltage may temporarily occur when the HS-PMA is connected to a media in which common mode chokes and/or unterminated stubs are present. The maximum positive differential voltage may temporarily occur when the HS-PMA is connected to a media while more than one HS-PMA is sending dominant and concurrently a ground shift between the sending HS-PMAs is present.				

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5.5 Receiver input resistance

The implementation of an HS-PMA shall have an input resistance according to Table 10. Furthermore, the internal resistance shall meet the requirement given in Table 11. Figure 4 shows an equivalent circuit diagram.

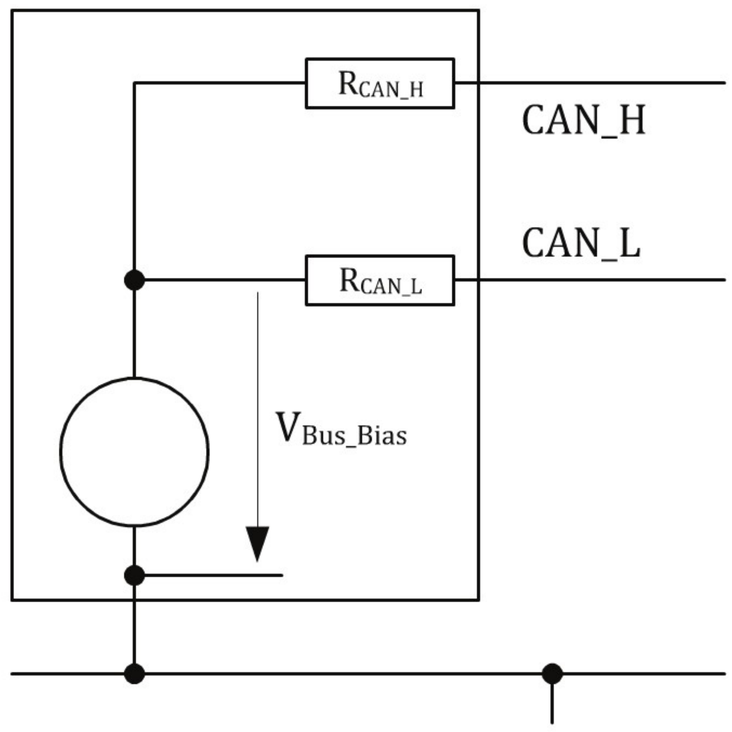

Figure 4 — Illustration of HS-PMA internal differential input resistance

Table 10 — HS-PMA receiver input resistance

Parameter	Notation	Value		Condition
		Min kΩ	Max kΩ	
Differential internal resistance	R_{Diff}	12	100	$-2\ V \le V_{CAN_L}$, $V_{CAN_H} \le +7\ V$
Single ended internal resistance	R_{CAN_H}, R_{CAN_L}	6	50	
$R_{Diff} = R_{CAN_H} + R_{CAN_L}$				

Table 11 — HS-PMA receiver input resistance matching

Parameter	Notation	Value		Condition
		Min	Max	
Matching[a] of internal resistance	m_R	−0,03	+0,03	V_{CAN_L}, V_{CAN_H}: +5 V
[a] The matching shall be calculated as $m_R = 2 \times (R_{CAN_H} - R_{CAN_L})/(R_{CAN_H} + R_{CAN_L})$.				

5.6 Transmitter and receiver timing behaviour

The timing is defined under consideration of the test circuit that is shown in Figure 2. The parameters are given in Tables 12, 13 and 14 and shall be measured at the RXD output and TXD input of the HS-PMA implementation as well as on the differential voltage between CAN_H and CAN_L.

Figure 5 shows how to measure the timing in the signal traces.

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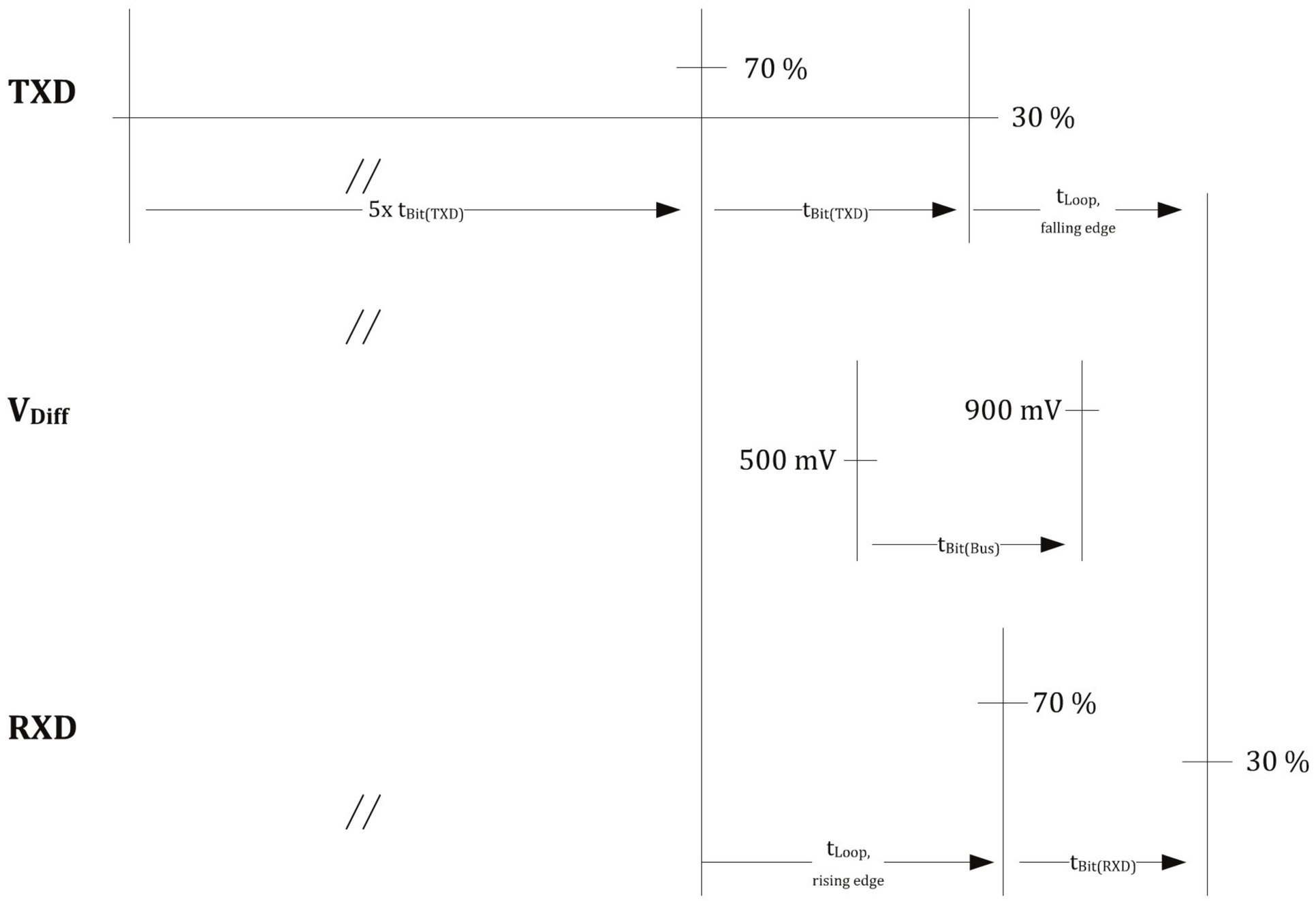

Key

$t_{Bit(TXD)}$ = 1 000 ns if the implementation of the HS-PMA supports bit rates of up to 1 Mbit/s
$t_{Bit(TXD)}$ = 500 ns if the implementation of the HS-PMA supports bit rates of up to 2 Mbit/s
$t_{Bit(TXD)}$ = 200 ns if the implementation of the HS-PMA supports bit rates of up to 5 Mbit/s

Figure 5 — HS-PMA implementation timing diagram

Table 12 — HS-PMA implementation loop delay requirement

Parameter	Notation	Value	
		Min ns	Max ns
Loop delay[a]	t_{Loop}	not defined	255

[a] Time span from signal edge on TXD input to the next signal edge with the same polarity on RXD output, the maximum of delay of both signal edges is to be considered.

Measurement setup according to Figure 2:

R_L = 60 Ω (tolerance ≤ ±1 %)

C_1 = 0 pF (not present)

C_2 = 100 pF (tolerance ≤ ±1 %)

C_{RXD} = 15 pF (tolerance ≤ ±1 %)

Measurement according to Figure 5:

The input signal on TXD shall have rise and fall times (10 %/90 %) of less than 10 ns.

NOTE Limits for $t_{Bit(Bus)}$ and $t_{Bit(RXD)}$ are not defined for intended use with bit rates up to 1 Mbit/s.

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Table 13 — Optional HS-PMA implementation data signal timing requirements for use with bit rates above 1 Mbit/s and up to 2 Mbit/s

Parameter	Notation	Value	
		Min ns	Max ns
Transmitted recessive bit width at 2 Mbit/s	$t_{Bit(Bus)}$	435	530
Received recessive bit width at 2 Mbit/s	$t_{Bit(RXD)}$	400	550
Receiver timing symmetry at 2 Mbit/s	Δt_{Rec}[a]	−65	+40

[a] $\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$

All requirements in this table apply concurrently. Therefore, not all combinations of $t_{Bit(Bus)}$ and Δt_{Rec} are compliant with $t_{Bit(RXD)}$.

Measurement setup according to Figure 2:

R_L = 60 Ω (tolerance ≤ ±1 %)

C_1 = 0 pF (not present)

C_2 = 100 pF (tolerance ≤ ±1 %)

C_{RXD} = 15 pF (tolerance ≤ ±1 %)

Measurement according to Figure 5:

The input signal on TXD shall have rise and fall times (10 %/90 %) of less than 10 ns.

NOTE Limits for $t_{Bit(Bus)}$ and $t_{Bit(RXD)}$ are not defined for intended use with bit rates up to 1 Mbit/s.

Table 14 — Optional HS-PMA implementation data signal timing requirements for use with bit rates above 2 Mbit/s and up to 5 Mbit/s

Parameter	Notation	Value	
		Min ns	Max ns
Transmitted recessive bit width at 5 Mbit/s, intended	$t_{Bit(Bus)}$	155	210
Received recessive bit width at 5 Mbit/s	$t_{Bit(RXD)}$	120	220
Receiver timing symmetry at 5 Mbit/s	Δt_{Rec}[a]	−45	+15

[a] $\Delta t_{Rec} = t_{Bit(RXD)} - t_{Bit(Bus)}$

All requirements in this table apply concurrently. Therefore, not all combinations of $t_{Bit(Bus)}$ and Δt_{Rec} are compliant with $t_{Bit(RXD)}$.

Measurement setup according to Figure 2:

R_L = 60 Ω (tolerance ≤ ±1 %)

C_1 = 0 pF (not present)

C_2 = 100 pF (tolerance ≤ ±1 %)

C_{RXD} = 15 pF (tolerance ≤ ±1 %)

Measurement according to Figure 5:

The input signal on TXD shall have rise and fall times (10 %/90 %) of less than 10 ns.

NOTE Limits for $t_{Bit(Bus)}$ and $t_{Bit(RXD)}$ are not defined for intended use with bit rates up to 1 Mbit/s.

5.7 Maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}

Table 15 reflects upper and lower limit static voltages, which may be connected to CAN_H and CAN_L without causing damage, while V_{Diff} stays within in its own maximum rating range.

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Table 15 — HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}

Parameter	Notation	Value	
		Min V	Max V
Maximum rating V_{Diff}[a]	V_{Diff}	−5,0	+10,0
General maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H}, V_{CAN_L}	−27,0	+40,0
Optional: Extended maximum rating V_{CAN_H} and V_{CAN_L}	V_{CAN_H}, V_{CAN_L}	−58,0	+58,0

[a] This is required regardless whether general or extended maximum rating for V_{CAN_H} and V_{CAN_L} is fulfilled.

Applies to HS-PMA implementation powered and unpowered conditions. Applies to transmit data input de-asserted and transmit data becomes asserted while CAN_H or/and CAN_L connected to a fixed voltage.

The maximum rating for V_{Diff} excludes that all combinations of V_{CAN_H} and V_{CAN_L} are compliant to this document. $V_{Diff} = V_{CAN_H} - V_{CAN_L}$, see Figure 2.

5.8 Maximum leakage currents of CAN_H and CAN_L

An unpowered HS-PMA implementation shall not disturb the communication of other HS-PMAs that are connected to the same media. The required maximum leakage currents are given in Table 16.

Table 16 — HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered

Parameter	Notation	Value	
		Min µA	Max µA
Leakage current on CAN_H, CAN_L	I_{CAN_H}, I_{CAN_L}	−10	+10
V_{CAN_H} = 5 V, V_{CAN_L} = 5 V, all supply inputs are connected to GND. Positive currents are flowing into the implementation.			

5.9 Wake-up from low-power mode

5.9.1 Overview

When an implementation comprising one or more HS-PMAs implements a low-power mode, the HS-PMA shall be able to signal a wake-up event to its implementation. Table 17 lists the required wake-up mechanism for defined types of HS-PMA implementations.

Table 17 — HS-PMA wake-up implementations

Type of HS-PMA implementation	Required wake-up mechanism
CAN wake-up, implementations without low-power mode	No wake-up
CAN wake-up, implementations with low-power mode but without selective wake-up	Either basic wake-up or wake-up pattern (WUP) wake-up
CAN wake-up, implementations with selective wake-up	Selective wake-up frame (WUF) and wake-up pattern (WUP) wake-up

When more than one wake-up mechanism is implemented in an HS-PMA, the wake-up mechanism to be used shall be configurable.

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5.9.2 Basic wake-up

Upon receiving once a dominant state for duration of at least t_{Filter}, a wake-up event shall happen.

5.9.3 Wake-up pattern wake-up

Upon receiving two consecutive dominant states each for duration of at least t_{Filter}, separated by a recessive state with a duration of at least t_{Filter}, a wake-up event shall happen. This method follows the description of activating the bus biasing as described in 5.10.3.

5.9.4 Selective wake-up

5.9.4.1 General

Upon detection of a wake-up frame (WUF), a wake-up event shall happen. Decoding of CAN frames in either CBFF or CEFF and acceptance as a WUF is done by the HS-PMA. If enabled, decoding of CAN frames shall be possible in normal- and low-power modes. The acceptance procedure is described in detail in the following subclauses.

After the bias reaction time, t_{Bias}, has elapsed, the implementation may ignore up to four (or up to eight when bit rate higher than 500 kbit/s) frames in CBFF and CEFF and shall not ignore any following frame in CBFF and CEFF.

In case of erroneous communication, the HS-PMA shall signal a wake-up upon or after an overflow of the internal error counter.

5.9.4.2 Behaviour during transitions between normal- to low-power modes

If selective wake-up is enabled prior to the mode change and the HS-PMA is not anymore ignoring frames, decoding of CAN data and remote frames shall also be supported during mode transitions, which have frame detection IP enabled. If the received frame is a valid WUF, the transceiver shall indicate a wake-up. If enabled, decoding of CAN data shall be possible in normal- and low-power mode.

5.9.4.3 Bit decoding

A received Classical CAN frame shall be decoded correctly when the timing of the differential voltage between CAN_H and CAN_L complies with one of the two following types of signals:

— the bit stream consists of multiple instances of the signal shape A (to handle ringing);

— the bit stream can be assembled out of multiple instances of the signal shape B1 and one instance of signal shape B2 (to handle sender clock tolerance and loss of arbitration).

These two types of signals are specified in Figure 6.

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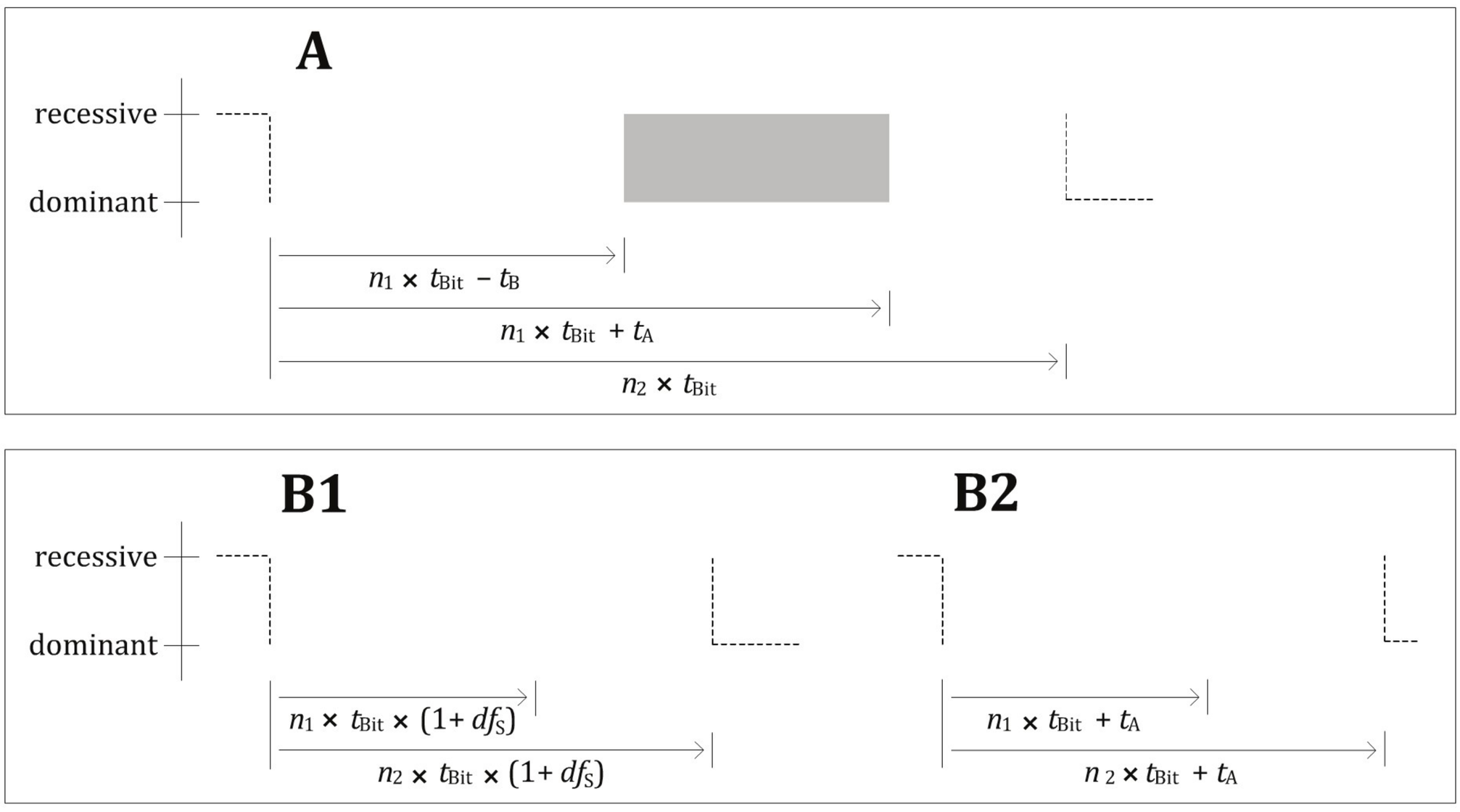

Key

n_1 number of consecutive dominant bits {1, 2, 3, 4, 5}

n_2 number of bits between two falling edges {2, 3, ..., 10}; $n_2 > n_1$

t_A $0 \le t_A \le 55$ % of t_{Bit} (product specific higher maximum values for t_A are allowed)

t_B $0 \le t_B \le 5$ % of t_{Bit} (product specific higher maximum values for t_B are allowed)

t_{Bit} nominal bit time

df_S transceivers according to this document shall tolerate sender clock frequency deviations up to at least 0,5 %

NOTE Often used values for t_{Bit} are 2 µs, 4 µs and 8 µs.

Figure 6 — Signal shape A and B of V_{Diff} for bit reception

Edges in the time span from "$n_1 \times t_{Bit} - t_B$" to "$n_1 \times t_{Bit} + t_A$" of signal shape A shall be ignored and shall not cause decoding errors.

5.9.4.4 Wake-up frame evaluation

If all of the following conditions are met, a valid Classical CAN frame shall be accepted as a valid WUF.

a) The received frame is a Classical CAN data frame when DLC matching [see c)] is not disabled. The frame may also be a remote frame when DLC matching is disabled.

b) The ID (as defined in ISO 11898-1:2015, 8.4.2.2) of the received Classical CAN frame is exactly matching a configured ID (in the HS-PMA implementation) in the relevant bit positions. The relevant bit positions are given by an ID-mask (in the HS-PMA implementation). See the mechanism illustrated in 5.9.4.7.

c) The DLC (as defined in ISO 11898-1:2015, 8.4.2.4) of the received Classical CAN data frame is exactly matching a configured DLC. See the mechanism illustrated in 5.9.4.8. Optionally, this DLC matching condition may be disabled by configuration in the HS-PMA implementation.

d) When the DLC is greater than 0 and DLC matching is enabled, the data field (as defined in ISO 11898-1:2015, 8.4.2.5) of the received frame has at least one bit set in a bit position which corresponds to a set bit in the configured data mask. See the mechanism illustrated in 5.9.4.9.

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e) A correct cyclic redundancy check (CRC) has been received, including a recessive CRC delimiter, and no error (according to ISO 11898-1:2015, 10.11) is detected prior to the acknowledgement (ACK) Slot. Figure 7 depicts the bits, which are considered as "don't care".

NOTE There is no requirement for the SRR bit to be received as dominant in CEFF to recognize the frame as a valid WUF.

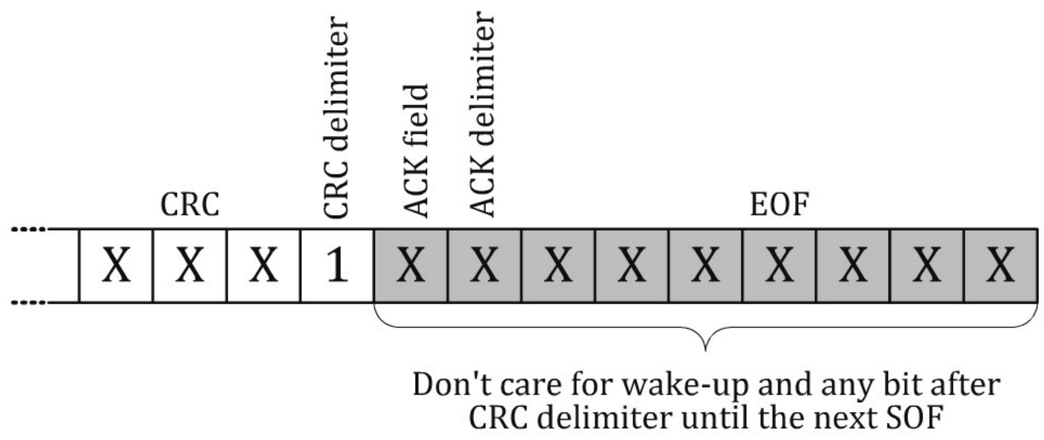

Figure 7 — Don't care bits for frame decoding

5.9.4.5 Frame error counter mechanism

Upon activating the selective wake-up function (e.g. by a connected host controller) and also on expiration of $t_{Silence}$, the counter for erroneous CAN frames shall be set to zero. The initial value of the counter is zero. This counter shall be incremented by one when a bit stuffing, CRC or CRC delimiter form error (according to ISO 11898-1) is detected. If a Classical CAN frame has been received, which is valid according to the definition in 5.9.4.4, and the counter is not zero, then the counter shall be decremented by one. Dominant bits between the CRC delimiter and the end of the intermission field shall not increase the frame error counter.

On each increment or decrement of this counter, the decoder unit in the HS-PMA shall wait for n_{Bits_idle} recessive bits before considering a dominant bit as a start of frame. Figure 8 depicts the position of the mandatory start of frame (SOF) detection when a Classical CAN frame was received and in case of an error scenario.

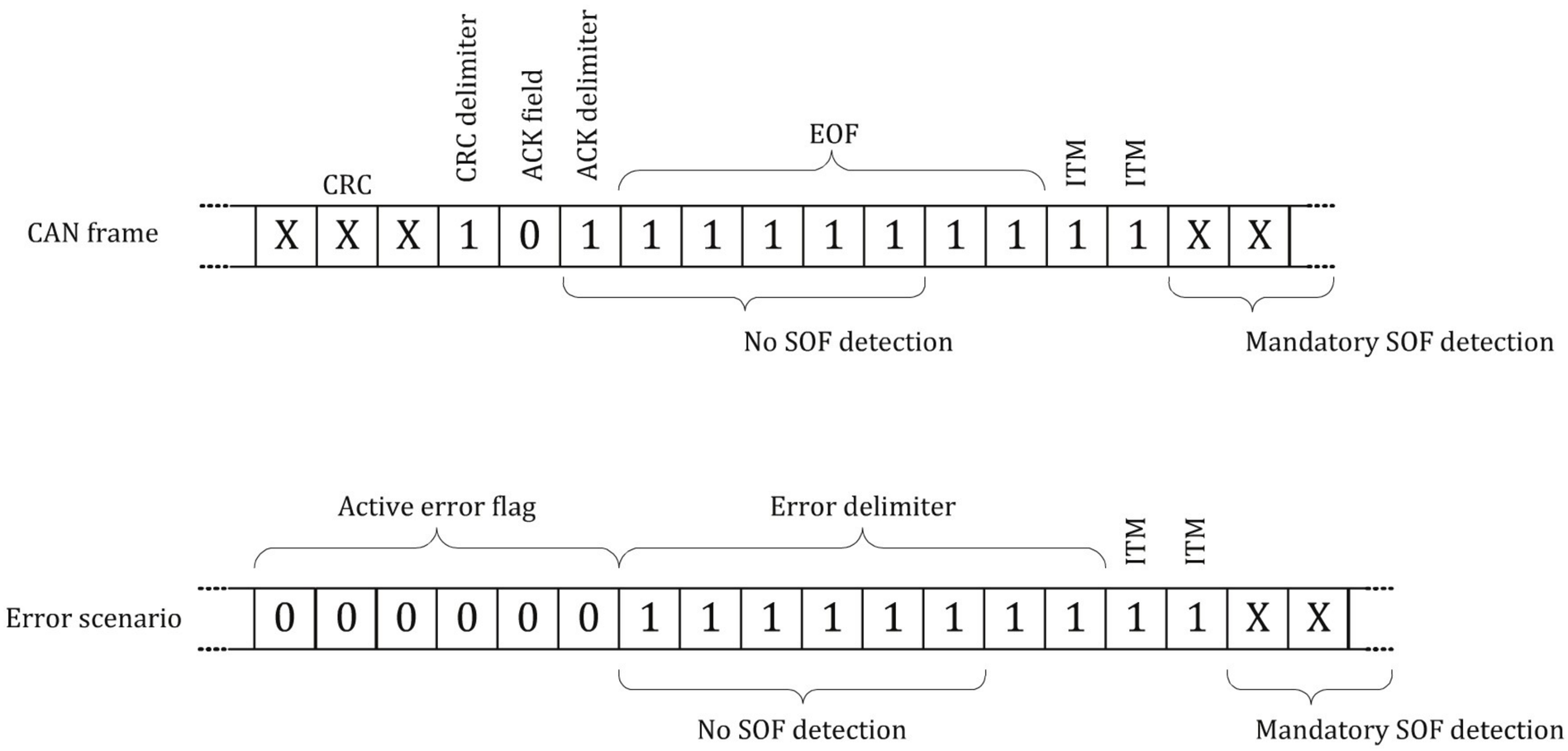

Figure 8 — Mandatory SOF detection after Classical CAN frames and error scenarios

A wake-up shall happen immediately or upon the next received WUP when the counter has reached a threshold value. The default threshold value is 32, other values might be configurable.

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Up to four (or up to eight when bit rate >500 kbit/s) consecutive Classical CAN data and remote frames that start after the bias reaction time, t_{Bias}, has elapsed might be either ignored (no error counter increase of failure) or judged as erroneous (error counter increase even in case of no error).

Receiving a frame in CEFF with non-nominal reserved bits (SRR, r0) shall not lead to an increase of the error counter.

5.9.4.6 Tolerance to CAN FD frames (optional)

After receiving a recessive FDF bit followed by a dominant res bit, the decoder unit in the HS-PMA shall wait for n_{Bits_idle} recessive bits before considering a further dominant bit as a start of frame. Figure 8 depicts the position of the mandatory SOF detection when a CAN FD data frame was received and in case of an error scenario. Table 18 specifies the valid range for n_{Bits_idle}.

The behaviour, when the FDF bit is received recessively and the following bit position is also received recessively, is outside the scope of this document.

One of the following bitfilter options shall be implemented to support different combinations of arbitration and data phase bit rates.

— Bitfilter option 1: A data phase bit rate less or equal to four times the arbitration bit rate or 2 Mbit/s, whichever is lower, shall be supported.

— Bitfilter option 2: A data bit rate less or equal to ten times the arbitration bit rate or 5 Mbit/s, whichever is lower, shall be supported.

Dominant signals less than or equal to the minimum of pBitfilter of the arbitration bit time in duration shall not be considered to be a valid bit and shall not restart the recessive bit counter. Dominant signals longer than or equal to maximum of pBitfilter of the arbitration bit time in duration shall restart the recessive bit counter. Table 19 specifies pBitfilter depending on the chosen bitfilter option as percentage of the arbitration bit time.

Table 18 — Number of recessive bit before next SOF

Parameter	Notation	Value	
		Min	Max
Number of recessive bits before a new SOF shall be accepted	n_{Bits_idle}	6	10

Table 19 — Bitfilter in CAN FD data phase

Parameter	Notation	Value	
		Min	Max
CAN FD data phase bitfilter (option 1)	$pBitfilter_{option1}$	5 %	17,5 %
CAN FD data phase bitfilter (option 2)	$pBitfilter_{option2}$	2,5 %	8,75 %

5.9.4.7 Wake-up frame ID evaluation

A CAN-ID mask mechanism shall be supported to exclude ID-bits from comparison. 11-bit and 29-bit CAN-IDs and ID-masks shall be supported. The user selects whether a WUF has to appear in CBFF or CEFF. The IDE bit is not part of the ID-mask. It has to be evaluated in any case.

All masked ID-bits except “don’t care” shall match exactly the configured ID-bits. If the masked ID-bits are configured as “don’t care”, then both “1” and “0” shall be accepted.

The masking mechanism is implementation dependent.

Figure 9 shows an example for valid WUF IDs corresponding to the ID-mask register.

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Configured ID	1	0	0	0	1	0	1	0	0	1	0
Mask register	c	c	c	c	c	c	c	c	c	d	d
Valid WUF IDs	1	0	0	0	1	0	1	0	0	0	0
	1	0	0	0	1	0	1	0	0	0	1
	1	0	0	0	1	0	1	0	0	1	0
	1	0	0	0	1	0	1	0	0	1	1
Non-valid WUF IDs	1	0	0	0	1	0	1	0	1	x	x
	1	0	0	0	1	0	1	1	0	x	x
	1	0	0	0	1	0	1	1	1	x	x
	1	0	0	0	1	0	0	0	0	x	x
	⋮										⋮

Key

d don't care

c care

Figure 9 — Example for ID masking mechanism

5.9.4.8 Wake-up frame DLC evaluation

If the DLC matching condition is enabled, then a Classical CAN frame can only be a valid WUF when the DLC of the received frame matches exactly the configured DLC.

If the DLC matching condition is disabled, then the DLC and data field are not evaluated and a Classical CAN frame is already a valid WUF when the identifier matches (see 5.9.4.7) and the CRC is correct.

5.9.4.9 Wake-up frame data field evaluation

If the DLC matching condition is enabled, then a Classical CAN frame can only be a valid WUF if at least one logic 1 bit within the data field of the received WUF matches to a logic 1 bit of the data field within the configured WUF.

If the DLC matching condition is disabled, then the DLC and data field are not evaluated and a Classical CAN frame is already a valid WUF when the identifier matches (see 5.9.4.7) and the CRC is correct.

Figure 10 shows an example with a non-matching and a matching ID field.

	Byte 7								Byte 6								------	Byte 0							
Configured data field	1	1	0	1	0	0	0	0	1	1	0	1	0	0	0	0	------	1	1	0	1	0	0	0	0
WUF data fields, matching	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	------	0	0	0	0	0	0	0	0
WUF data fields, None matching	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	------	0	0	0	0	0	1	1	1

Figure 10 — Example of the data field within a received Classical CAN data frame

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With this mechanism, it is possible to wake-up up to 64 independent groups of ECUs with only one wake-up frame.

5.10 Bus biasing

5.10.1 Overview

The HS-PMA implementation shall bias CAN_H and CAN_L according to Tables 5 and 6.

When the HS-PMA implementation features a low-power mode and selective wake-up, automatic voltage biasing is required. For all other implementation, either normal biasing or automatic voltage biasing shall be implemented.

5.10.2 Normal biasing

Normal biasing means bus biasing is active in normal mode and inactive in low-power mode.

5.10.3 Automatic voltage biasing

Automatic voltage biasing means bus biasing is active in normal mode and is controlled by the differential voltage between CAN_H and CAN_L in low-power mode. The following state machine illustrates the mechanism.

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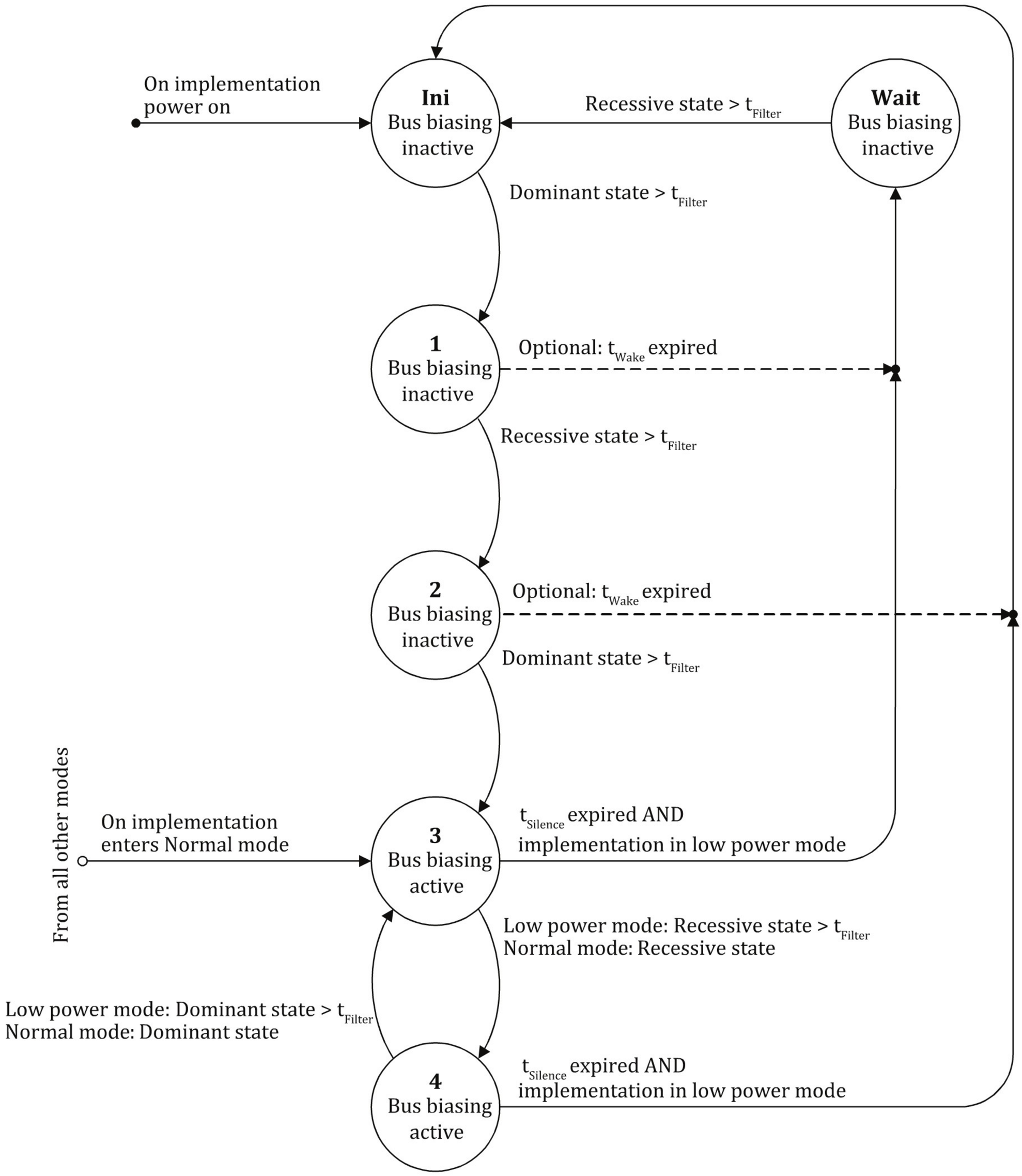

Figure 11 — Bus biasing control for automatic voltage biasing

The state machine in Figure 11 defines the bus biasing behaviour for all operation modes. When entering state 1, the optional timer, t_{Wake}, shall be reset and restarted; when entering state 3 or 4, the timer, $t_{Silence}$, shall be reset and restarted.

Table 20 specifies the bus biasing control timings and Figure 12 the bias reaction time.

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Table 20 — HS-PMA bus biasing control timings

Parameter	Notation	Value		Condition
		Min µs	Max µs	
CAN activity filter time, long[a]	t_{Filter}	0,5	5,0	Bus voltages according to Table A.2
CAN activity filter time, short[b]	t_{Filter}	0,15	1,8	Bus voltages according to Table A.2
Wake-up timeout[c]	t_{Wake}	800,0	10 000,0	Optional timeout parameter
Timeout for bus inactivity	$t_{Silence}$	$0,6 \times 10^6$	$1,2 \times 10^6$	Timer is reset and restarted, when bus changes from dominant to recessive or vice versa.
Bus bias reaction time	t_{Bias}	Not defined	250,0	Measured from the start of a dominant-recessive-dominant sequence (each phase 6 µs) until $v_{sym} \geq 0,1$. See Figure 12 v_{sym} as defined in Table 3.

[a] The implementation does not need to meet this timing, in case the "CAN activity filter time, short" is met. It should be noted that the maximum filter time has an impact to the suitable wake-up messages, especially at high bit rates. For example, a 500 kbit/s system, a message shall carry at least three similar bit levels in a row in order to safely pass the wake-up filter. Shorter filter time implementations might increase the risk for unwanted bus wake-ups due to noise. The specified range is a compromise between robustness against unwanted wake-ups and freedom in message selection.

[b] The implementation does not need to meet this timing, in case the "CAN activity filter time, long" is met.

[c] For legacy implementations, a minimum value of 350 µs is acceptable.

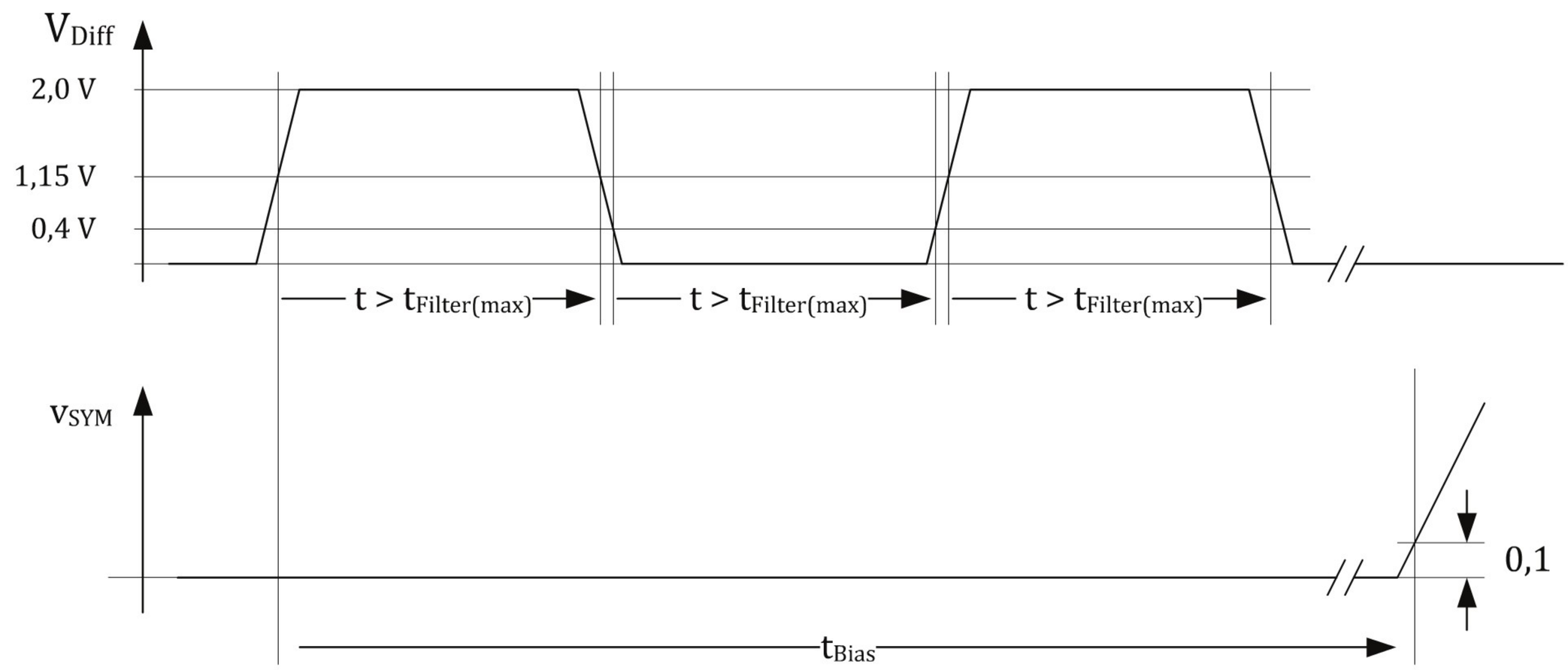

Figure 12 — Test signal definition for bias reaction time measurement

6 Conformance

The conformance test case definition and measurement setups to derive the parameters are outside the scope of this document. A conformance test plan is given in ISO 16845-2.

For an implementation to be compliant with this document, the HS-PMA implementation shall comply with all mandatory specifications and values given in this document. If optional specifications and values are implemented, they shall comply too. More information is given in A.4.

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Annex A
(informative)

ECU and network design

A.1 Implementation options

This clause specifies the physical media attachment sublayer. It can be implemented in a stand-alone CAN transceiver chip or in a system basis chip comprising additional functionality, e.g voltage regulators, wake-up logic and watchdog. These implementations can also provide additional functions, which are outside the scope of this document.

Figure A.1 shows an optional digital processing unit, which hides CAN FD data frames to the CAN data link layer implementation. Another optional feature is a galvanic isolation. Note that these optional functions cause some timing delays.

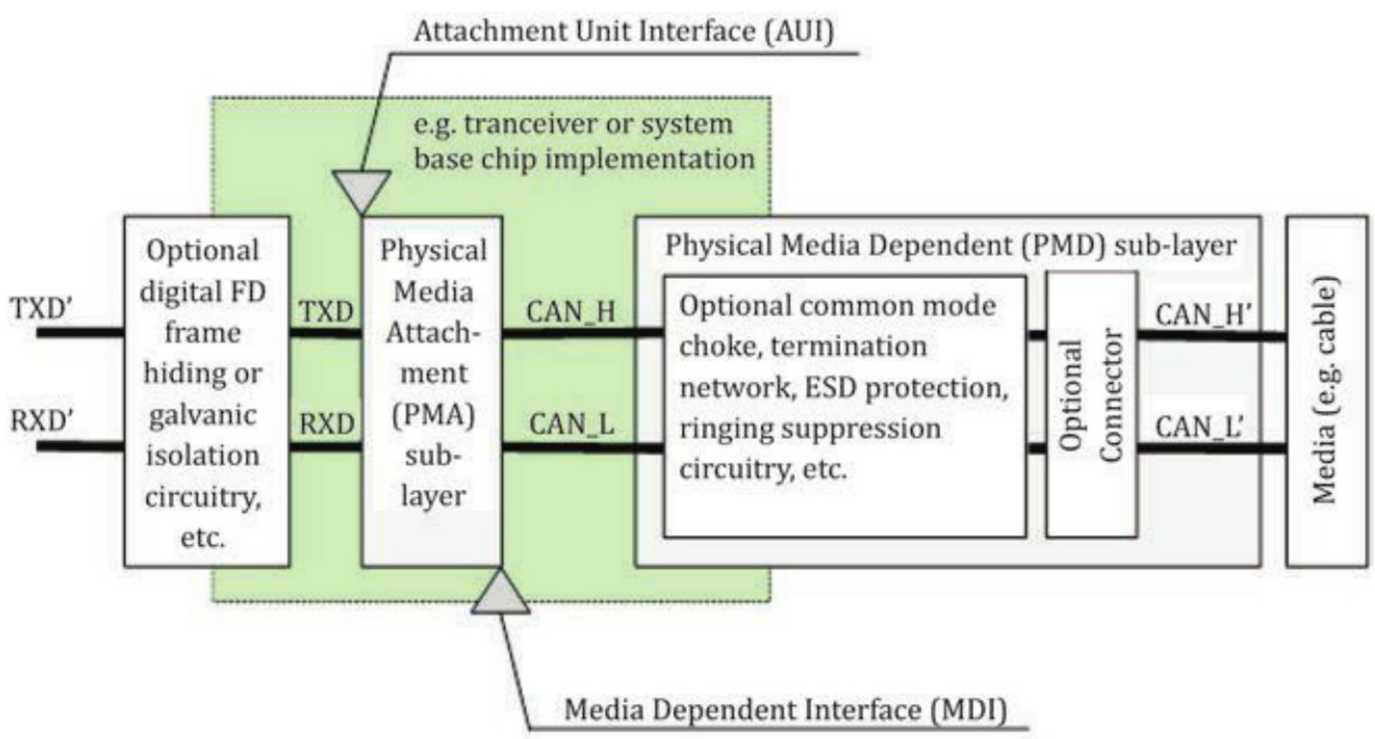

Figure A.1 — Optional functions in this document, compliant transceiver and their relation to the OSI sublayers

Figure A.1 shows also some optional functionality belonging to the physical media dependent sublayer. This includes, for example, a ringing suppression circuitry. These optional functionalities can improve the signal integrity of the analogue signals on the bus wires (CAN_L' and CAN_H').

NOTE These functions can have impacts on the EMC performance.

When implementing a ringing suppression circuitry, the differential internal resistance is typically 120 Ω in a bit-width interval [$t_{Bit(Bus)}$] after the dominant-to-recessive edge.

A.2 Expectations on a CAN network

This clause outlines which input voltages on V_{CAN_L} and V_{CAN_H} are recommended for proper operation of HS-PMA implementations connected to a media.

Table A.1 shows the CAN interface voltage parameters for the reception of recessive state.

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Table A.1 — Input voltage parameters for reception of recessive state

Parameter	Notation	Value			Condition
		Min V	Nom V	Max V	
Operating input voltage	V_{CAN_H}	−12,0	+2,5	+12,0	Measured with respect to the individual ground of each CAN node
	V_{CAN_L}	−12,0	+2,5	+12,0	
Differential input voltage	V_{Diff}	−3,0	0	+0,012	Measured at each CAN node connected to the media
The differential input voltage is determined by a combination of the recessive state output voltages of the individual CAN nodes present. Therefore, V_{Diff} is approximately zero.					

Figure A.3 shows the voltages V_{CAN_H} and V_{CAN_L} in their interdependency during recessive state.

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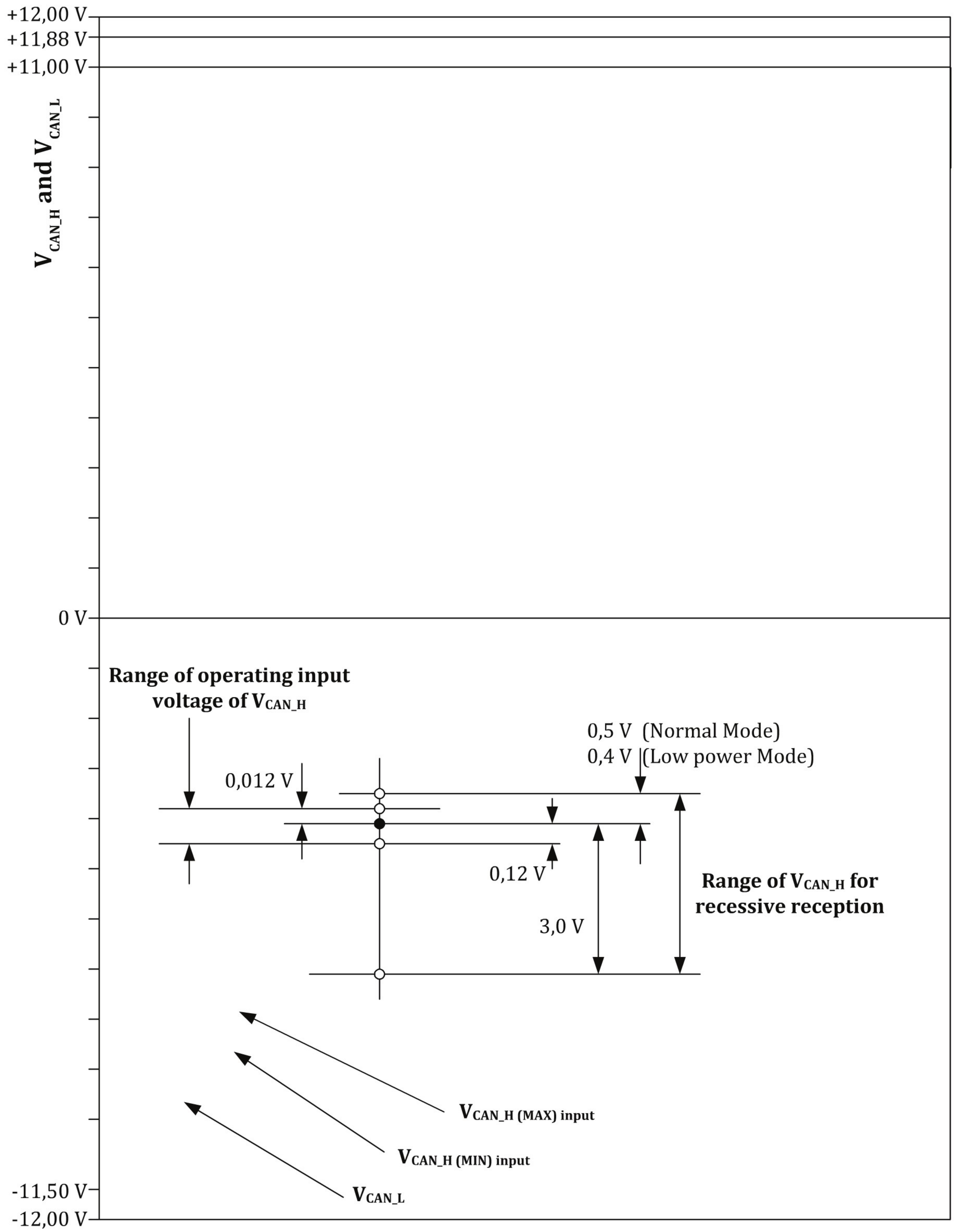

Figure A.2 — Valid voltage range of V_{CAN_H} for recessive state, when V_{CAN_L} varies from minimum to maximum common mode range

Table A.2 shows the CAN interface voltage parameters for reception of dominant state.

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Table A.2 — Input voltage parameters for reception of dominant state

Parameter	Notation	Value			Condition
		Min V	Nom V	Max V	
Common mode voltage	V_{CAN_H}	−10,8	+3,5	+12,0	Measured with respect to the individual ground of each CAN node
	V_{CAN_L}	−12,0	+1,5	+10,8	
Differential voltage[a]	V_{Diff}	+1,2	+2,0	+3,0	Measured at each CAN node connected to the media

[a] Normal bus load range, no arbitration.

The minimum value of V_{CAN_H} is determined by the minimum value of V_{CAN_L} plus the minimum value of V_{Diff}. The maximum value of V_{CAN_L} is determined by the maximum value of V_{CAN_H} minus the minimum value of V_{Diff}.

The bus load increases as CAN nodes are added to the media by R_{Diff}. Consequently, V_{Diff} decreases. The minimum value of V_{Diff} determines the number of CAN nodes allowed to be connected to the media. Also, the cable material, length and cross-section between the HS-PMA implementations, as well as connectors, impact the V_{Diff} that can be measured at the receiving HS-PMA's input.

Figure A.4 shows the voltages V_{CAN_H} and V_{CAN_L} in their interdependency during dominant state according to Table A.2.

Table A.3 — Input voltage parameters for reception of dominant state during arbitration

Parameter	Notation	Value		Condition
		Min V	Max V	
Common mode voltage	V_{CAN_H}	−10,8	+12,0	Measured with respect to the individual ground of each CAN node
	V_{CAN_L}	−12,0	+10,8	—
Differential voltage	V_{Diff}	+1,2	+8,0	Measured at each CA node connected to the media

The minimum value of V_{CAN_H} is determined by the minimum value of V_{CAN_L} plus the minimum value of V_{Diff}. The maximum value of V_{CAN_L} is determined by the maximum value of V_{CAN_H} minus the minimum value of V_{Diff}.

The maximum value of V_{Diff} is specified by the upper limit during arbitration plus a ground shift of up to 3 V.

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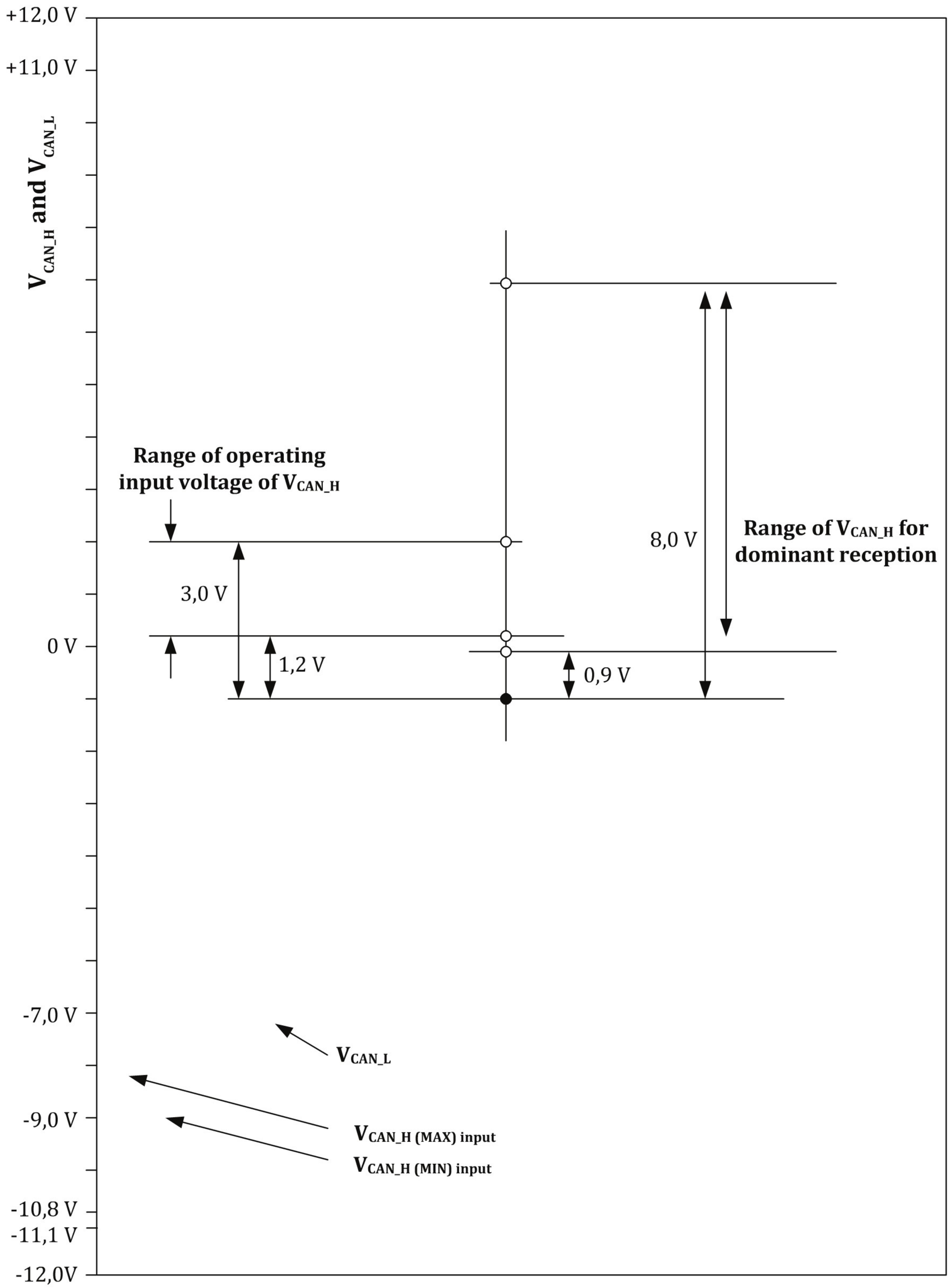

Figure A.3 — Valid voltage range of V_{CAN_H} for monitoring dominant state, when V_{CAN_L} varies from minimum to maximum common mode range during normal mode, arbitration free scenario

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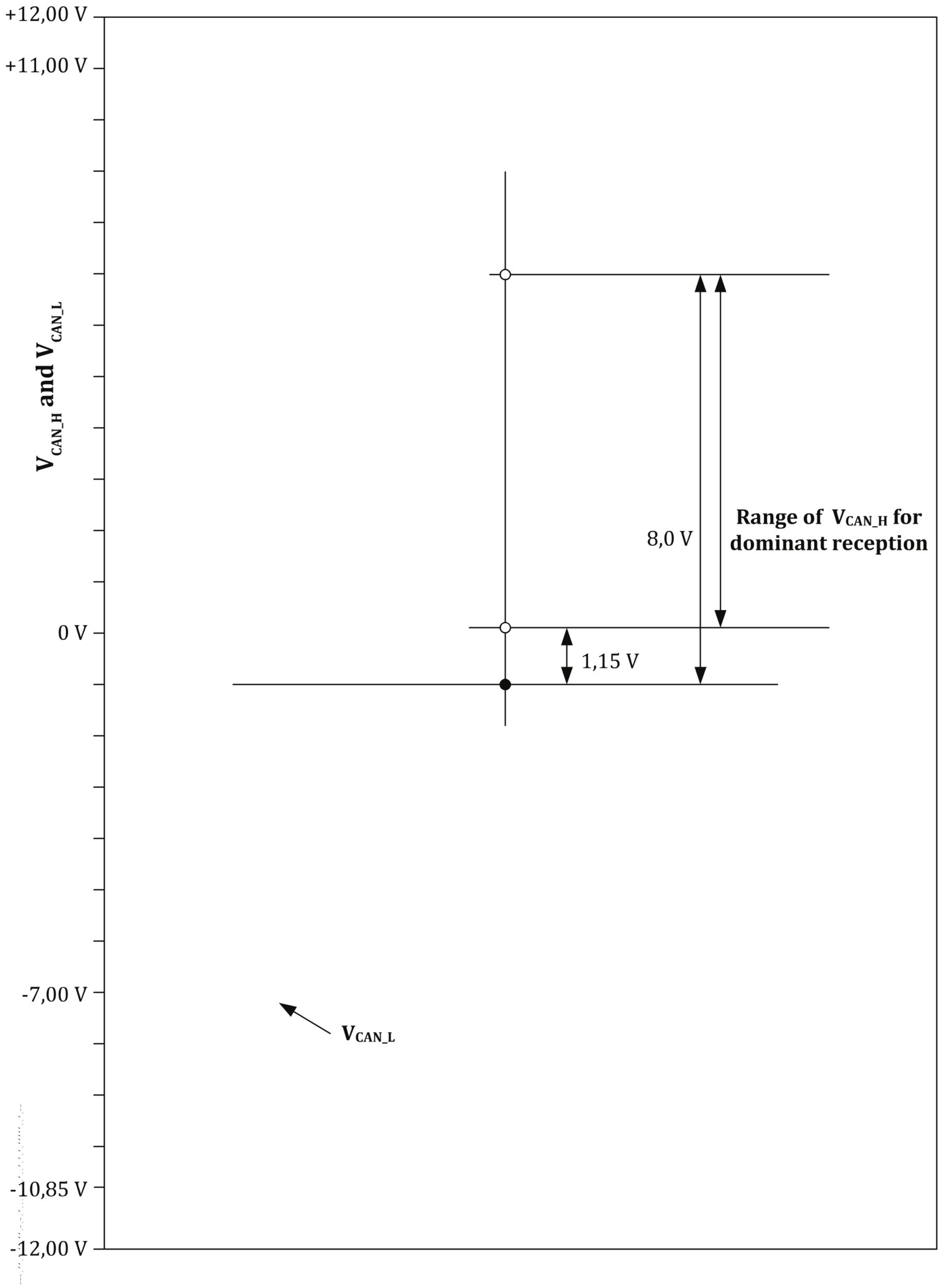

Figure A.4 — Valid voltage range of V_{CAN_H} for monitoring dominant state while the HS-PMA is not connected to the media, when V_{CAN_L} varies from minimum to maximum common mode range during low-power mode

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A.3 Expectations on a datasheet of an HS-PMA implementation

The datasheet needs to state the maximum supported bit rate according to the bit time requirements given in Tables 13 and 14.

The datasheet needs to state the supported arbitration bit rates for partial networking in case selective wake-up functionality is implemented.

In case the implemented selective wake-up functionality is tolerant to frames in FBFF and FEFF, the maximum supported ratio of data bit rate and arbitration bit rate needs to be stated, as well as the absolute maximum data bit rate.

The datasheet needs to state which of the functionalities classified as optional in this document are implemented in the particular HS-PMA implementation (e.g. extended bus load range, transmit dominant timeout, CAN activity filter time, etc.)

A.4 Overview of optional features and implementation choices

This document offers the following options for an HS-PMA. Table A.4 lists functional options that are specified in this document.

Table A.4 — Optional features and functions

No.	Option	Reference
1	Support of extended bus load range	5.3, Table 2
2	Transmit dominant timeout function	5.3, Table 7
3	Support of bit rates above 1 Mbit/s and up to 2 Mbit/s	5.6, Table 13
4	Support of bit rates above 2 Mbit/s and up to 5 Mbit/s	5.6, Table 14
5	Support of extended maximum ratings for CAN_H and CAN_L	5.7, Table 15
6	Support of wake-up	5.9, Table 17

In case the HS-PMA implementation implements low-power mode(s), then a wake-up mechanism according to Table 18 needs to be implemented. Each Wake-up mechanism has options and alternatives, which are summarized in Tables A.5, A.6, A.7 and A.8.

Table A.5 — Alternative timings within the wake-up features

No.	Alternative 1	Alternative 2	Alternative 3	Reference
1	CAN activity filter time, long	CAN activity filter time, short	CAN activity filter time, long and CAN activity filter time, short	5.9, Table 17
2	Wake-up timeout, short[a]	Wake-up timeout, long	No wake-up timeout	5.9, Table 17

[a] Only applicable for legacy devices.

Table A.6 — Options of the selective wake-up functions

No.	Option	Reference
1	Support of disabling DLC matching	5.9.4.4.

Table A.7 — Alternative for handling of CAN FD frames by the selective wake-up function

No.	Alternative 1	Alternative 2	Alternative 3	Reference
1	No tolerance (not recommended for new designs)	Tolerance to CAN FD frames with bit rate ratio of up to 1:4 or maximum 2 Mbit/s in data phase	Tolerance to CAN FD frames with bit rate ratio of up to 1:10 or maximum 5 Mbit/s in data phase	5.9.4.6

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Table A.8 — Alternatives for TXD dominant timeout function

No.	Alternative 1	Alternative 2	Alternative 3	Reference
1	No timeout	Timeout, short[a]	Timeout, long	5.3

[a] Only applicable for legacy devices.

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Annex B
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PN physical layer modes

Table B.1 provides a summary of features of PN physical layer implementations.

Table B.1 — PN physical layer features

PN-capable FD-tolerant transceiver mode	End of frame detection for CAN FD messages (glitch filtering), from FDF = recessive to EOF, when selective wake-up is enabled	Bus wake-up detection	Frame error counting	Frame error counter value	$t_{Silence}$ functionality
Normal	Required when frame error counting active/Not required when frame error counting inactive	WUF detection required	Optional	Counting up/ down active or no change	Active or inactive
Transition normal to low-power	Required when frame error counting active/Not required when frame error counting inactive	WUF detection required	Optional	Counting up/ down active or no change	Active or inactive
Low-power and $t_{Silence}$ not expired and bus biasing active	Required	WUF detection required	Required	Counting up/ down active	Active
Low-power and $t_{Silence}$ expired	Inactive	WUP detection required	Inactive	Set value to zero	Inactive
Low-power and $t_{Silence}$ not expired and bus biasing inactive (from WUP to bus bias active)	Inactive	WUP detection required	Inactive	No change	Active
Transition low-power to normal	Required when frame error counting active/Not required when frame error counting inactive	WUF detection optional	Optional	Counting up/ down active or no change	Active or inactive

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[2] ISO 11898-3, *Road vehicles — Controller area network (CAN) — Part 3: Low-speed, fault-tolerant, medium-dependent interface*

[3] ISO 11898-4, *Road vehicles — Controller area network (CAN) — Part 4: Time-triggered communication*

[4] ISO 11898-5, *Road vehicles — Controller area network (CAN) — Part 5: High-speed medium access unit with low-power mode*

[5] ISO 11898-6, *Road vehicles — Controller area network (CAN) — Part 6: High-speed medium access unit with selective wake-up functionality*

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