8-bit Calculator

By Team Exemplary

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For the module Hardware Engineering.

Picture source: https://auto.economictimes.indiatimes.com/news/auto-components/top-10-semiconductor-buyers-increased-chip-spending-by-25-in-2021/89335809?redirect=1

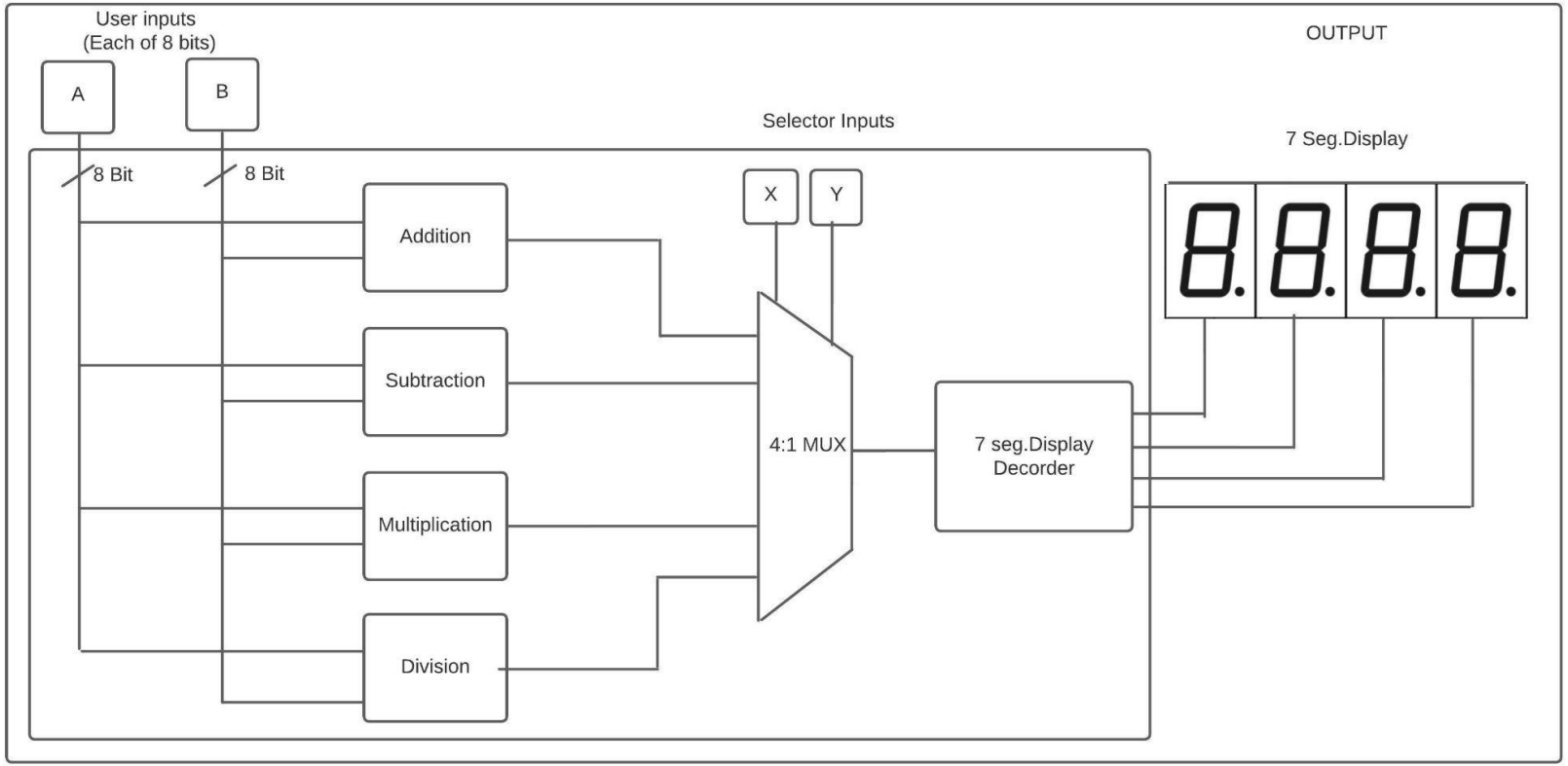
Agenda

1) Introduction.
2) Concept description.
3) Technologies.
4) Implementation.
5) Results.
6) PCB Design + PCB Layout.
7) BOM list.
8) Summary.

1. Introduction

2. Concept Description

Block Diagram



3. Technologies

VHDL:

- The VHSIC Hardware Description Language (VHDL) is a hardware description language (HDL) that can model the behavior and structure of digital systems at multiple levels of abstraction.

- For our project is helps mainly for developing a code, checking syntax, compiling and the main advantage is that it provides the facility to simulate the code, with a very user friendly user interface.

AutoCAD Eagle:

- EAGLE is electronic design automation (EDA) software that lets printed circuit board (PCB) designers easily connect schematic diagrams, component placement, PCB routing, and comprehensive library content.

- For this project it was a requirement to design a PCB which includes integration of FPGA module ,switches for inputs, and 7 Segment displays.

- We designed a two-layer PCB using AutoDesk Eagle.

FPGA:

- FPGA (Field Programmable Gate Array) is a hardware circuit (IC's) that a user can program to carry out one or more logical operations.

- For this calculator project, the FPGA used is EP4CE22E22C8N from Intel. The library used is from Ultralibrarian.com.

- FPGA specifications used:
  - FPGA CycloneR IV E Family.
  - 22320 Cells 60 nm technology.
  - 1.2 V.
  - 144-Pin EQFP EP.

Xilinx ISE (Integrated Synthesis Environment):

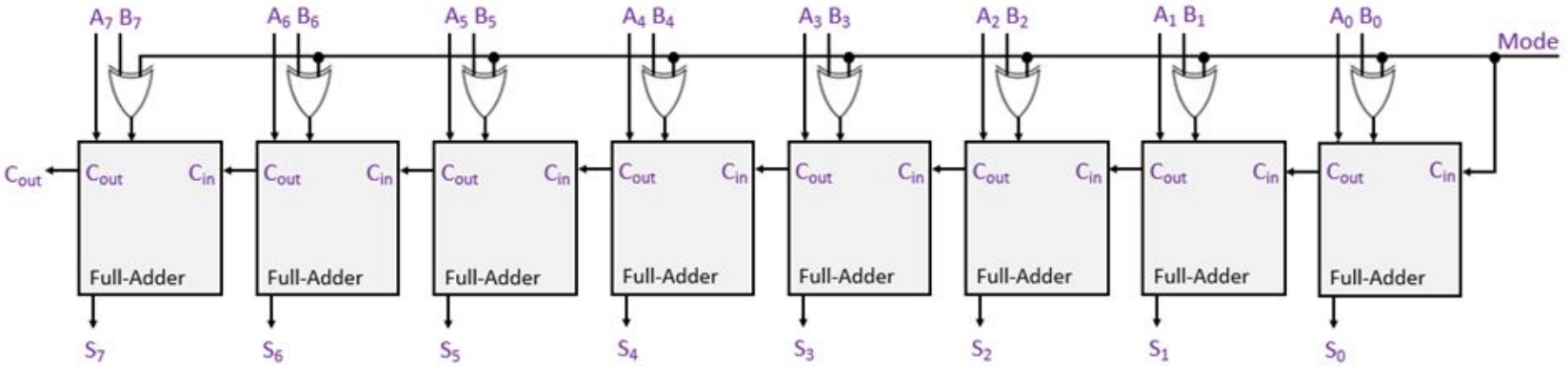
- The Xilinx ISE is primarily used for circuit synthesis and design.
- The User constraint file (.ucf) is used for mapping the ports of the VHDL code with the physical pins of the FPGA.

4. Implementation

Components:

A. 8-bit Adder.
B. 8-bit Subtractor.
C. 8-bit Multiplier.
D. (Upto 16-bit) Divider.
E. 4:1 MUX.
F. BCD and 7-segment display.

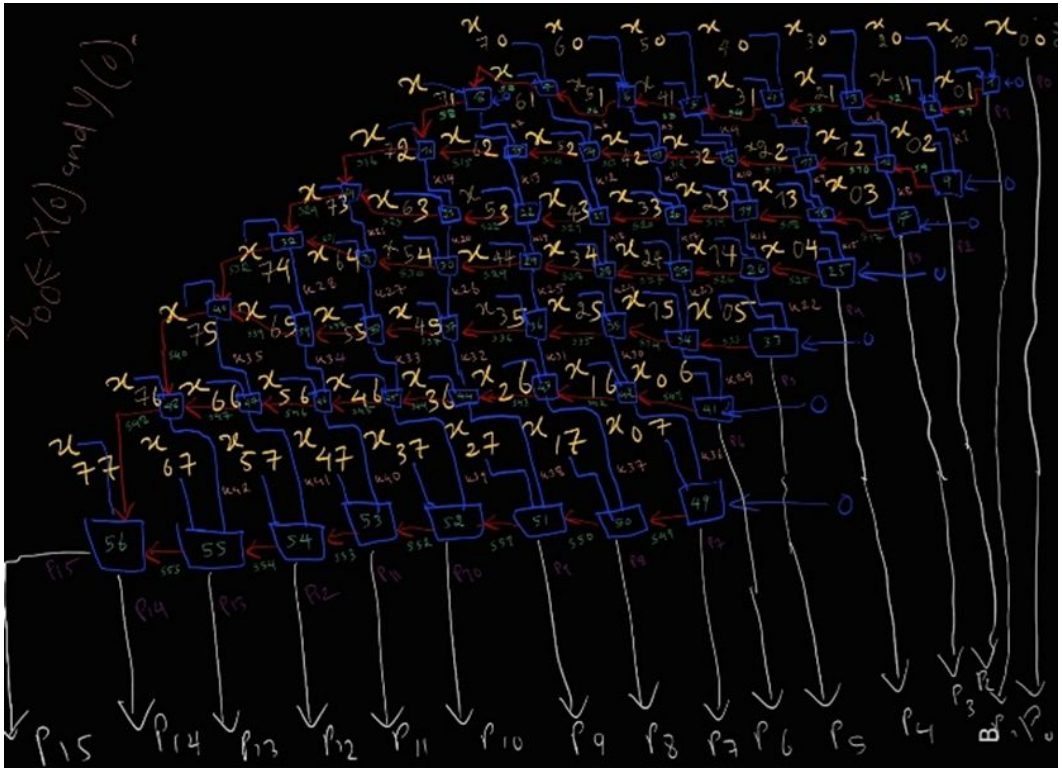
A. Adder/Subtractor



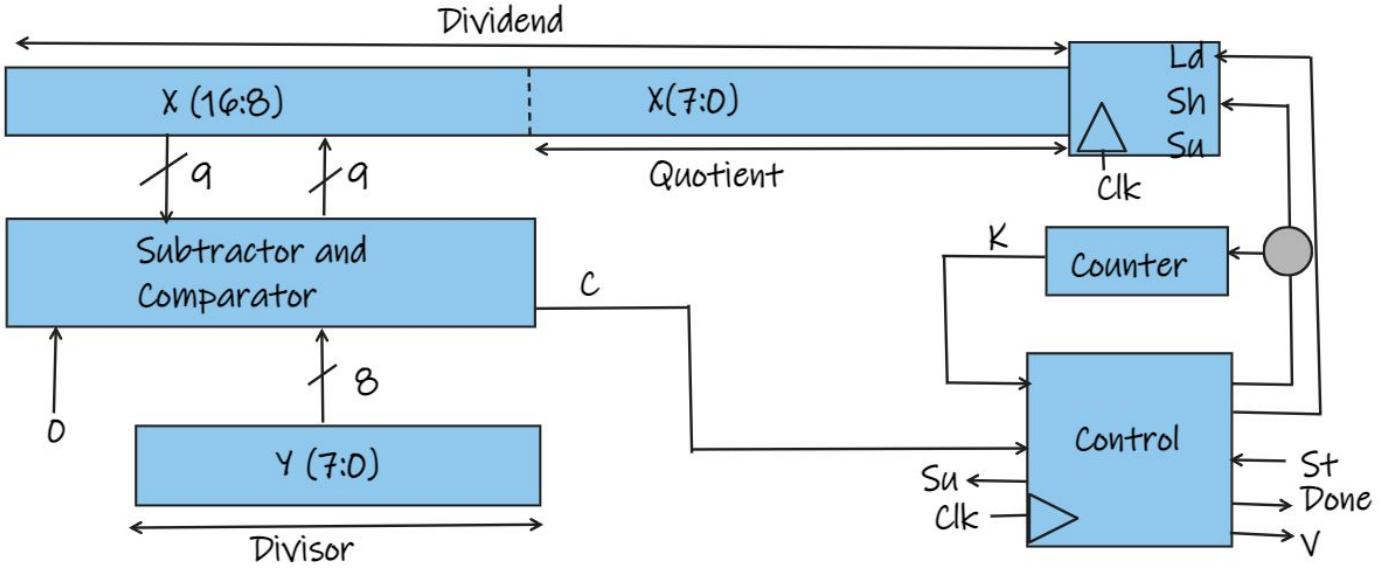
[2]

C. Multiplier

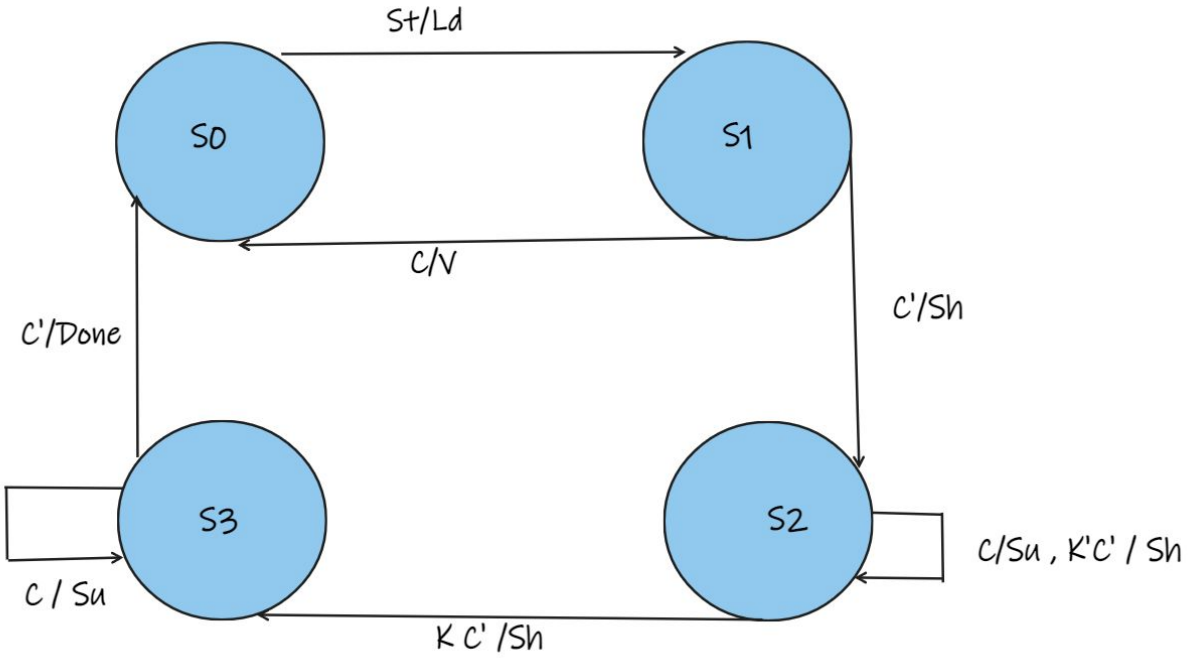
56 Full Adders



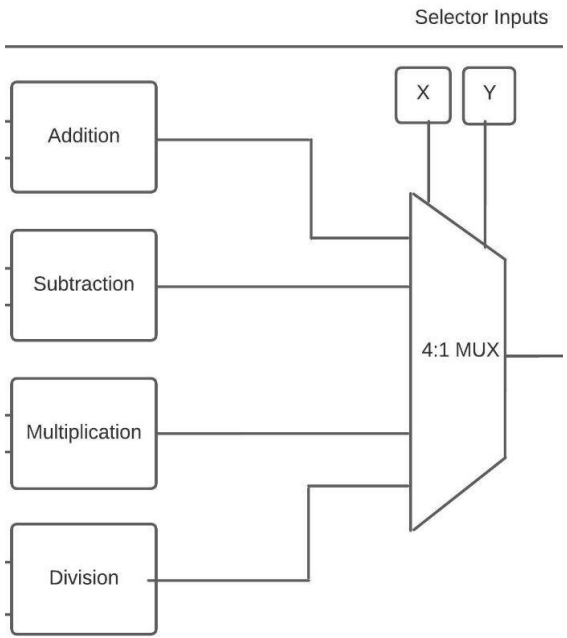
D. Divider (Block Diagram)



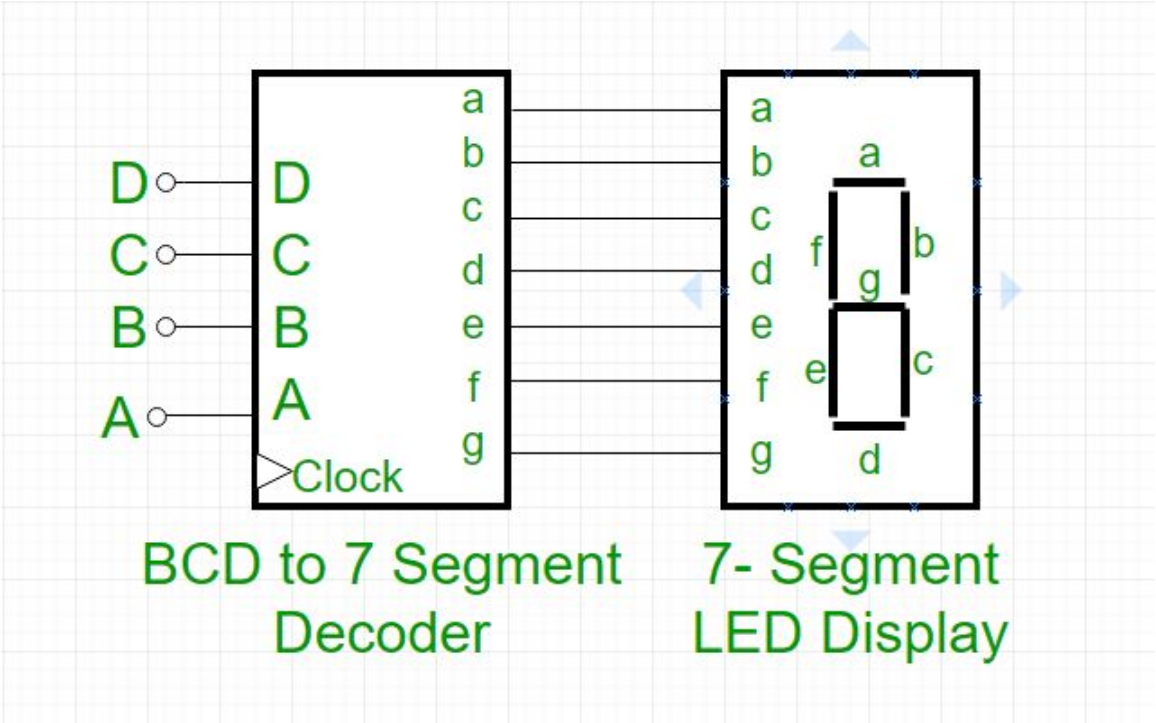
D. Divider (Finite-State Machine)



E. Multiplexer

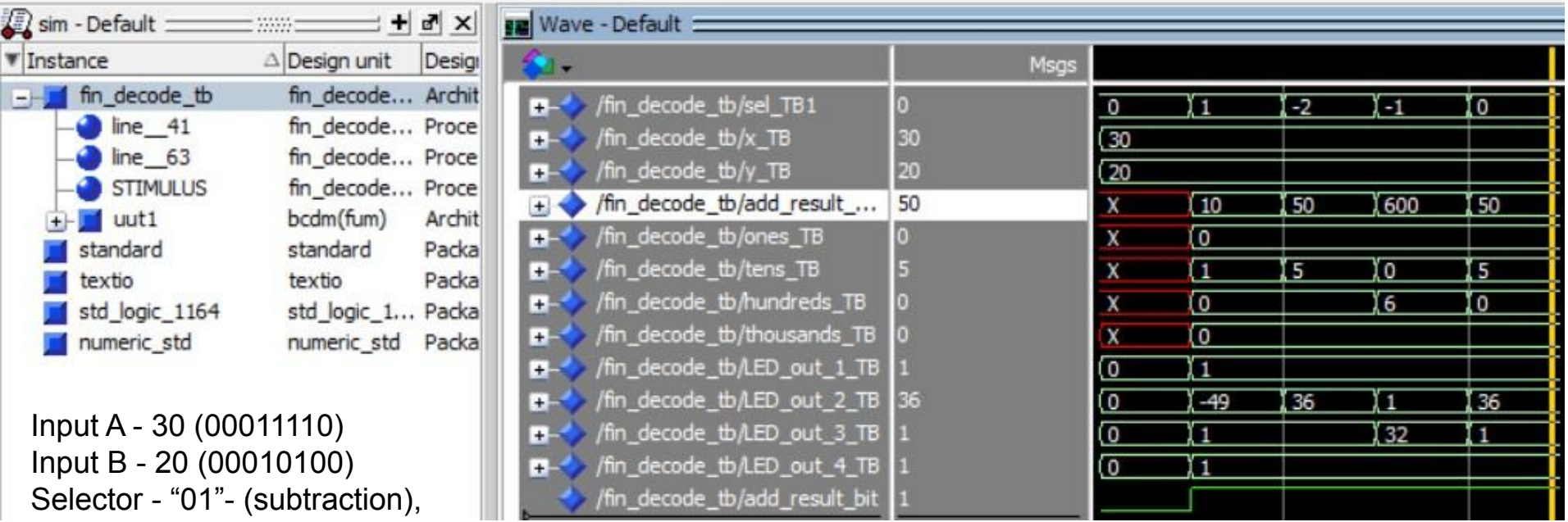


F. BCD and 7-segment display



Picture source: https://www.sxcco.com/?category_id=2970710

ModelSim Simulation



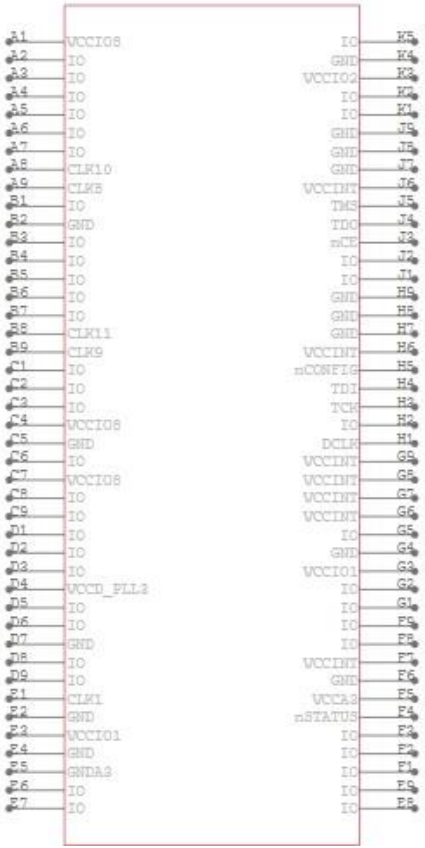
Input A - 30 (00011110)
Input B - 20 (00010100)
Selector - “01”- (subtraction),
“10” - (addition),
”11”- (multiplication),
”00” - (Division)

Assert/ report for verification

Severity→ NOTE/FAILURE

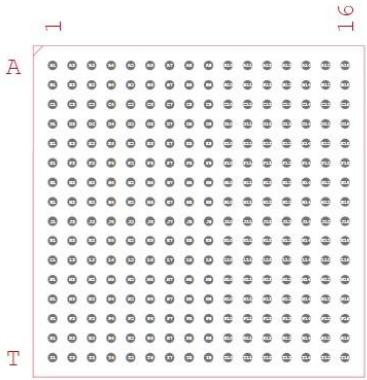
```
VSIM 10> run
# ** Note: passed test for calculation
#    Time: 200 ns  Iteration: 0  Instance: /fin_decode_tb
# ** Note: passed test for calculation
#    Time: 250 ns  Iteration: 0  Instance: /fin_decode_tb

VSIM 11>
```

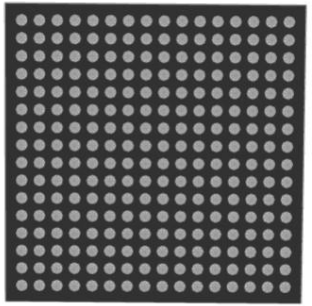
FPGA



Library downloaded from Ultralibrarian.com

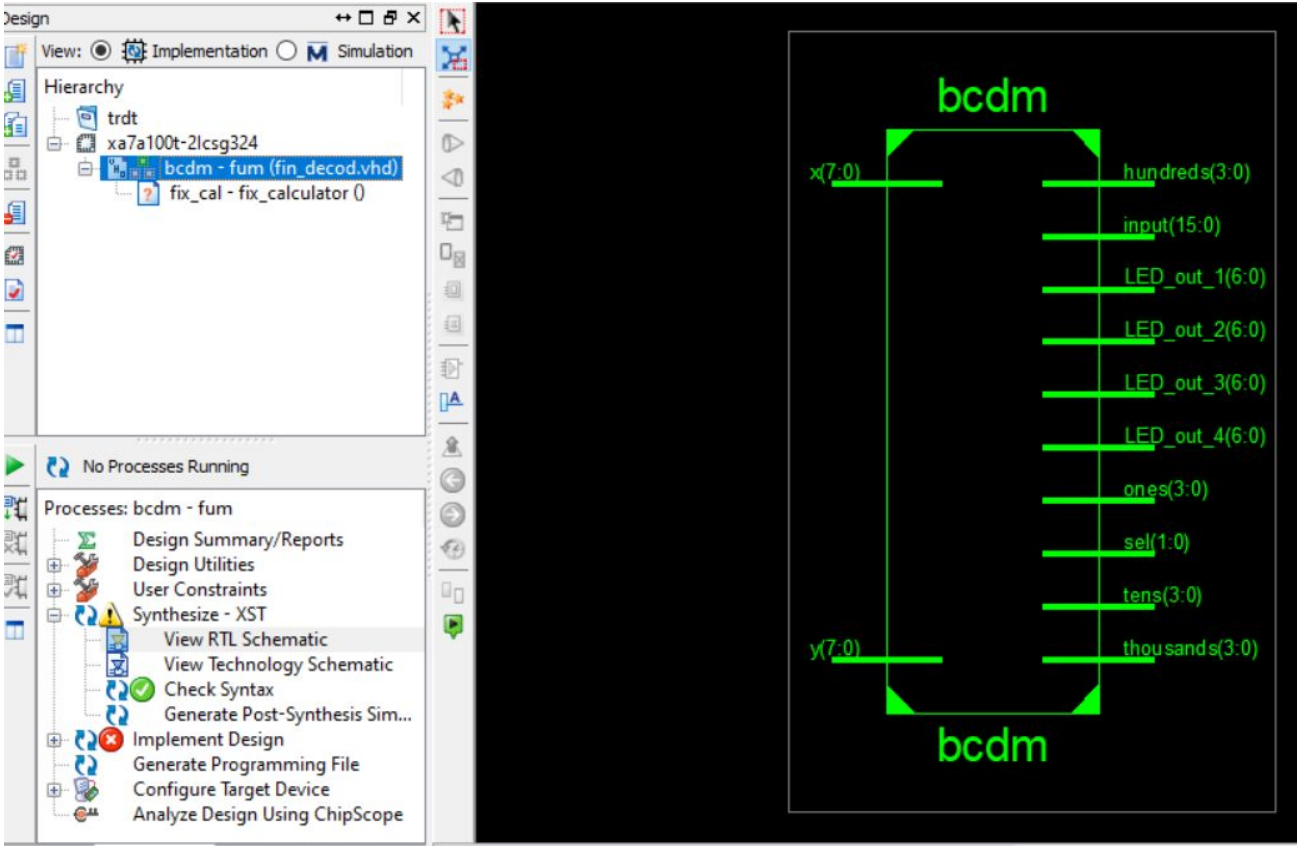
- EP4CE22E22C8N from Intel.



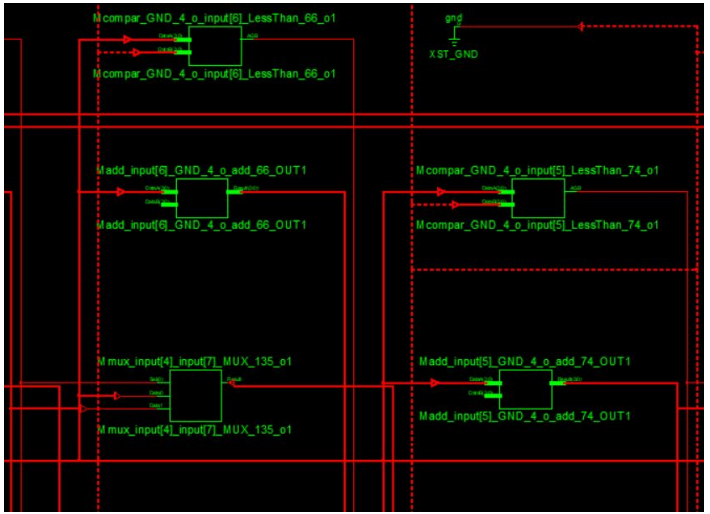


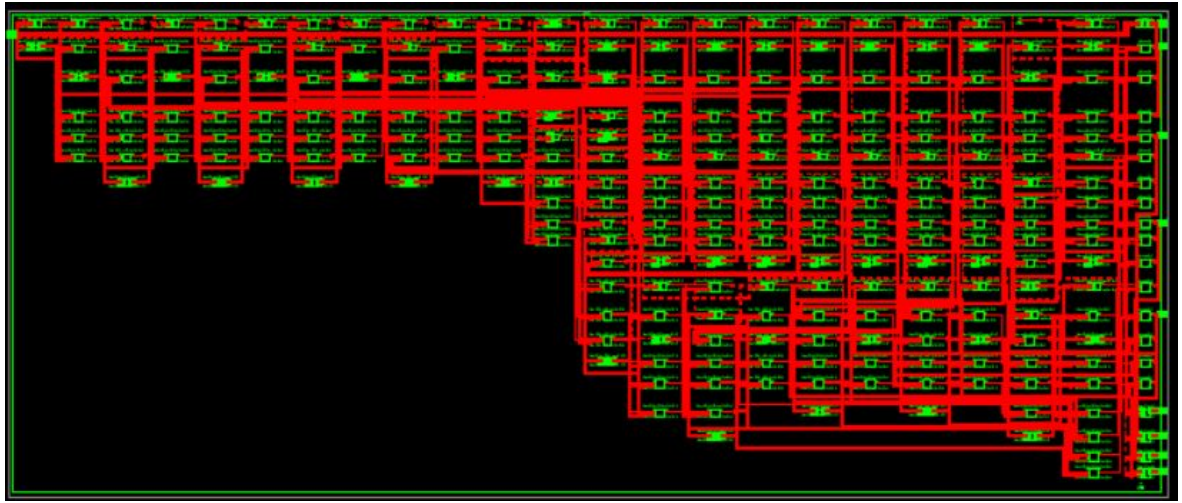
- FPGA CycloneR IV E Family
- 22320 Cells 60 nm Technology
- 1.2V
- **144-Pin** EQFP EP

RTL Schematic

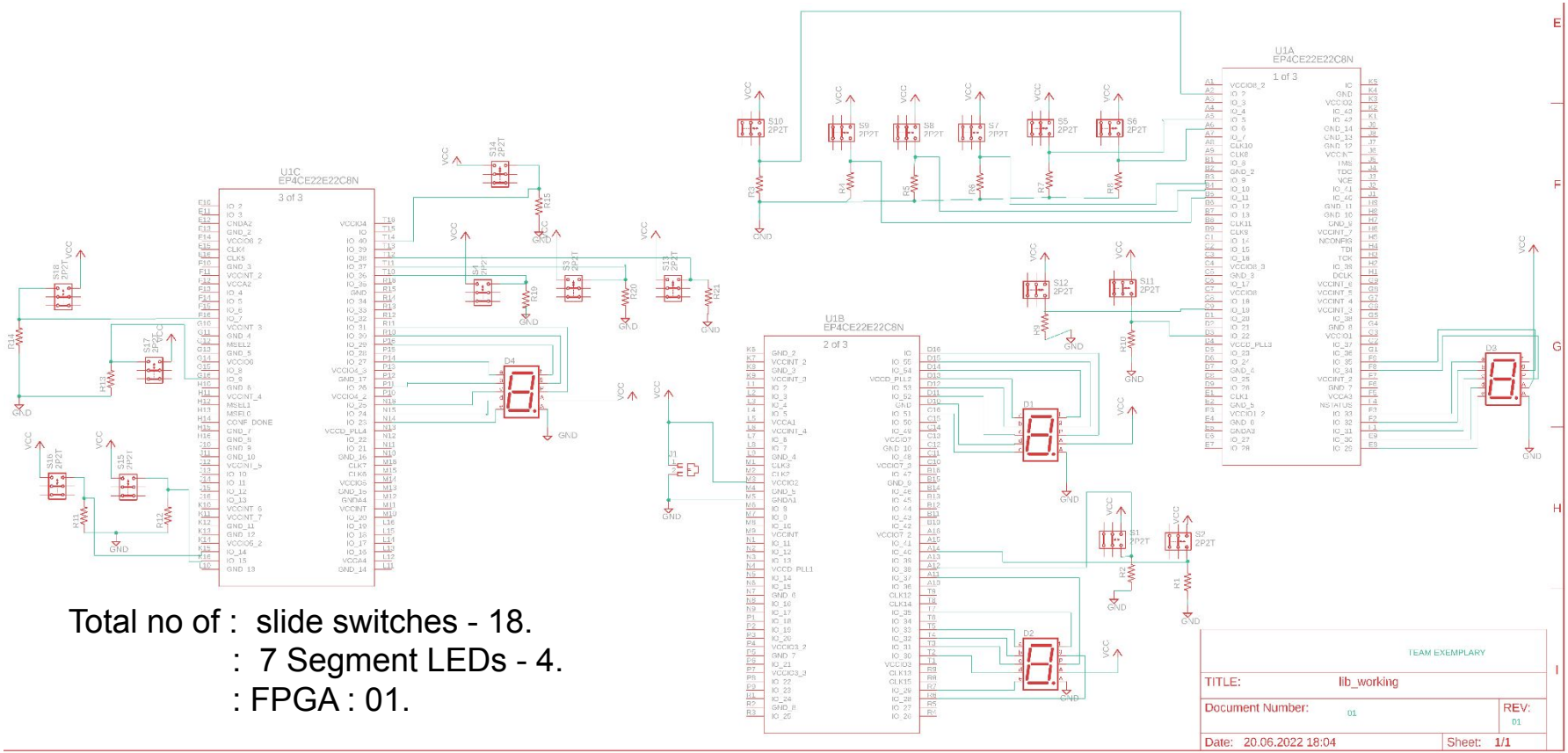


Technology schematic





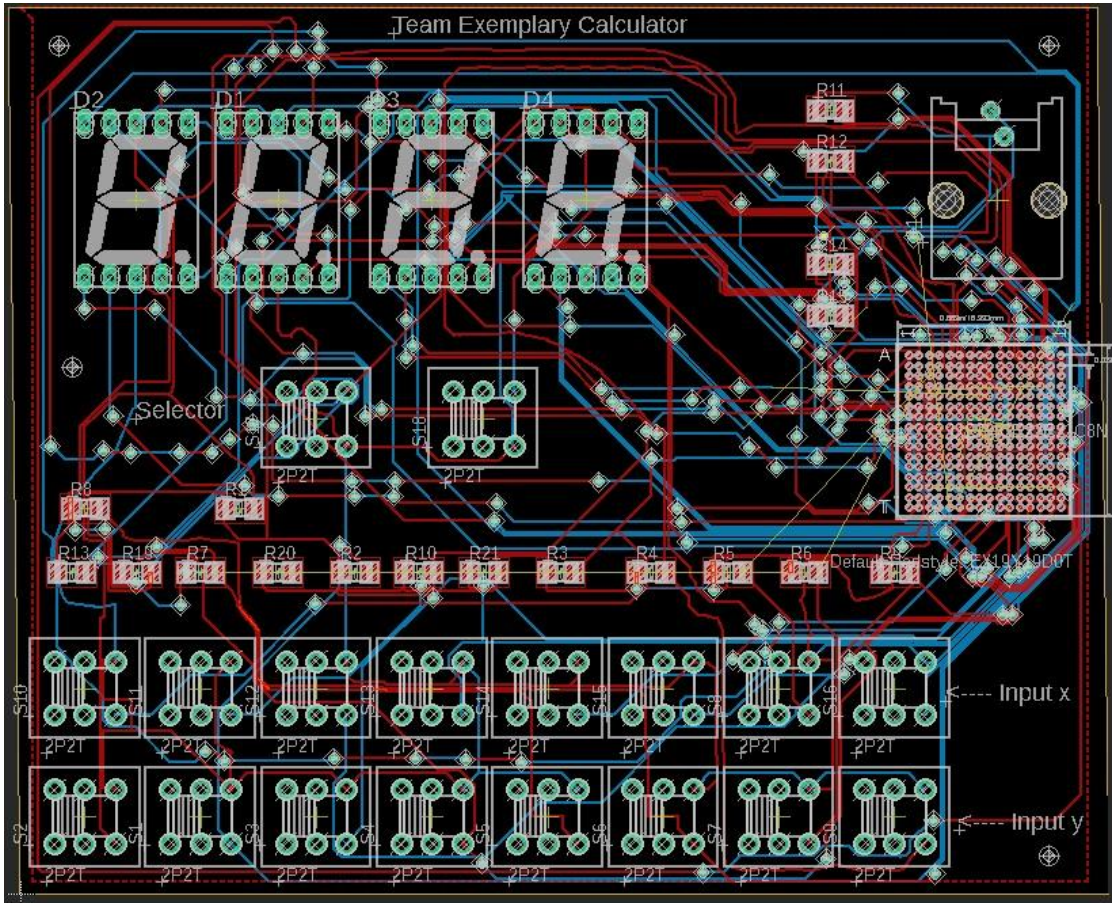
PCB Schematic diagram



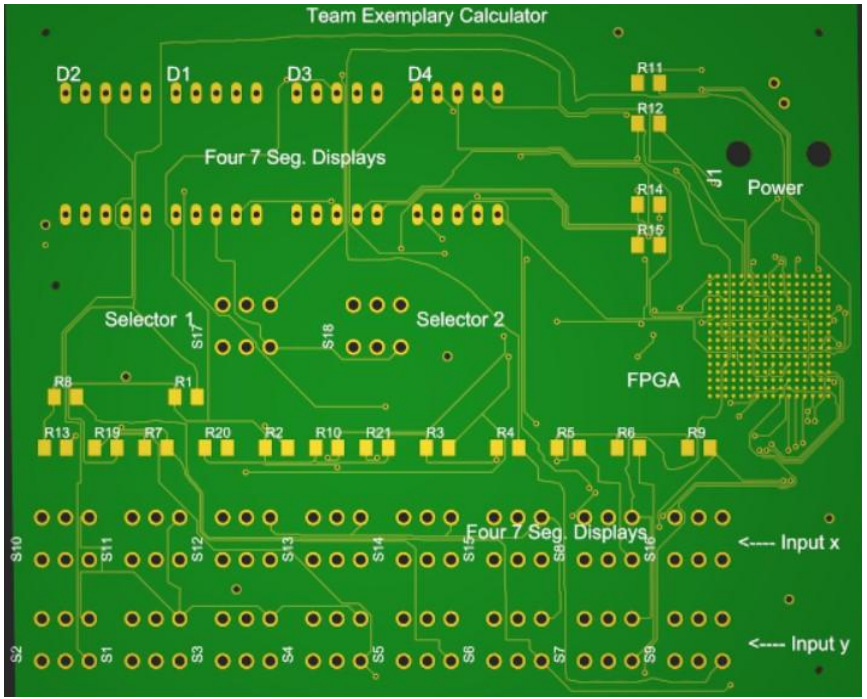
Total no of : slide switches - 18.
: 7 Segment LEDs - 4.
: FPGA : 01.

PCB layout

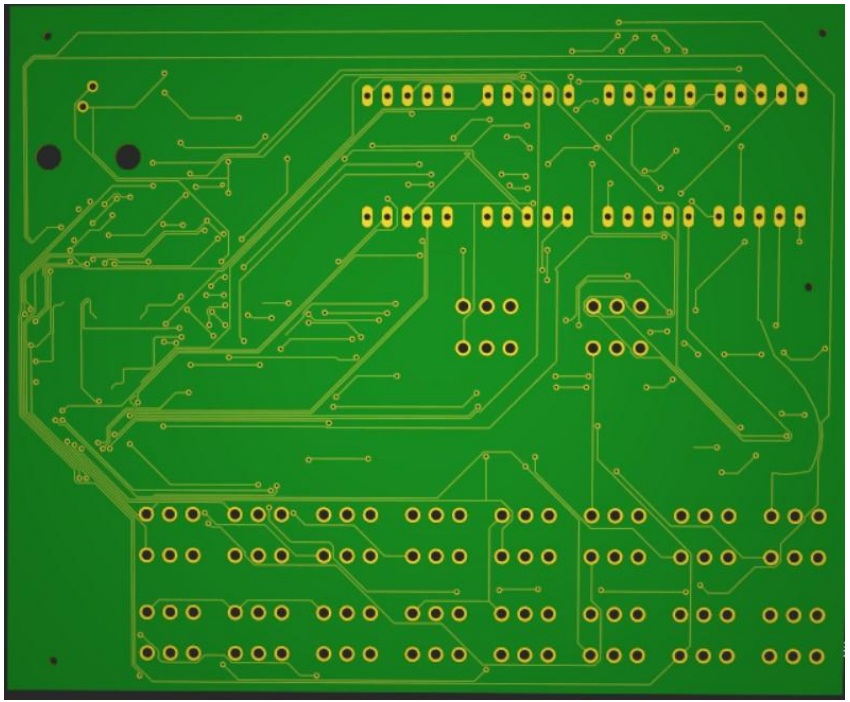
- Layout - Size :
  4610 x 3453 mil
- Auto routing +
  manual routing



PCB - (Printed Circuit Board)
No. of layers -2

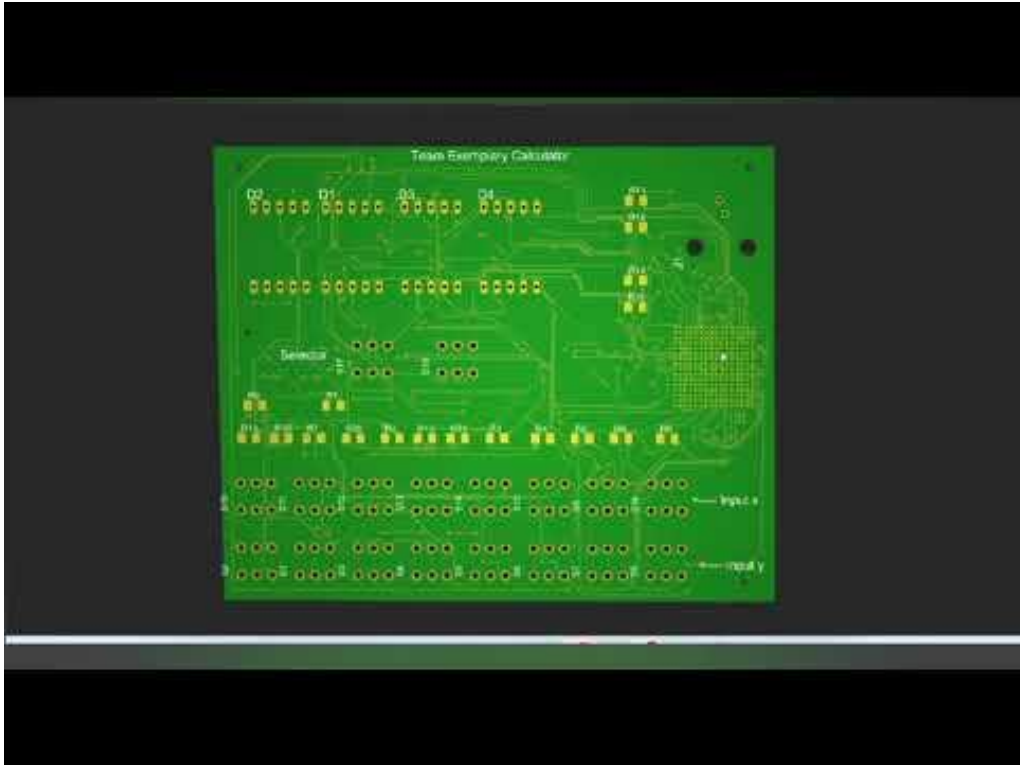


Front View (Top layer)



Rear View (bottom layer)

- Track width 6 mil.


Team Exempary Calculator

7. BOM List and estimated price of PCB

Qty Value	Device	Package	Parts	Description	Unit price	price sum
1	215876-7	215876-7	J1	AMP connector	~ 2$	2
4	7SEG-CA	7SEG-13	D1, D2, D3, D4	7-segment DISPLAY	$0.84	$3.36
18	R-US_M1206	M1206	R1- R21	RESISTOR, American symbol	$0.11	$1.98
18	2P2T	2P2T	S1-S18	SLIDE SWITCH 2P2T Part No. SS-22F05-G(A)4	$1.48	$26.64
1	EP4CE22E22C8N	EP4CE22E22C8N	FBGA256	_THIN_WIRE-BOND-A:1.55_	$71.04	$71.04
Total cost						$105.02

Total Component Cost only = ~ $105.02

Further requirements

- Inclusion of Power supply for the PCB.
- Implementation of JTAG programmer.
- Use of Oscillator/Clock module.

Testing/refining

- Should meet the EMC Regulations
- EMI requirements/tests.
- Output/Input ports accessibility. (e.g ;power jack)
- Refine the distance between traces.

8. Summary

- How to implement combinational and sequential logics in VHDL.
- How to simulate VHDL codes using ModelSim.
- How to synthesize using Xilinx ISE.
- How to choose the right library and components for PCB.
- How to design PCB boards using AutoDesk Eagle.

Resources

1. https://www.facebook.com/cyhardwareengineer/
2. https://www.101computing.net/binary-subtraction-using-logic-gates/8-bit-subtractor-block-diagram-using-full-adders/