Requirements:

The following requirements must be considered in this project:

1. You are required to design a 4-bit ripple carry adder shown in Figure 2. The building block of the design is a 1-bit Full Adder circuit constructed as a 24- transistor mirror shown in Figure 3. USE TSMC13RF from Cadence.

2. You are required to calculate the size of each transistor in the full adder circuit to minimize the input to output delay. Given that the critical path in the ripple carry adder is well defined (carry propagation path), the design effort needs to be spent on reducing the carry propagation delay of the full adder (Ci to Co delay).

3. The optimization goal for the ripple carry adders is to obtain the least delay and layout area simultaneously. The carry propagation path of the full adder is composed of the pull down network of MN1, MN2, and MN3, and the pull up network of MP1, MP2, and MP3 (Figure 3). The full adder is required to operate at a target frequency of 450 MHz for this project. This means that the carry propagation time is to be at 2.5 ns at maximum. The optimization should be performed with proper loading of the full adder carry output (Co). For proper loading, two identical Full Adders (FA) need to be cascaded where the second FA acts as the load of the first FA.

Find the carry propagation delay and the sizes of transistors.

Bonus: decrease the carry propagation delay to 1.5 ns at maximum

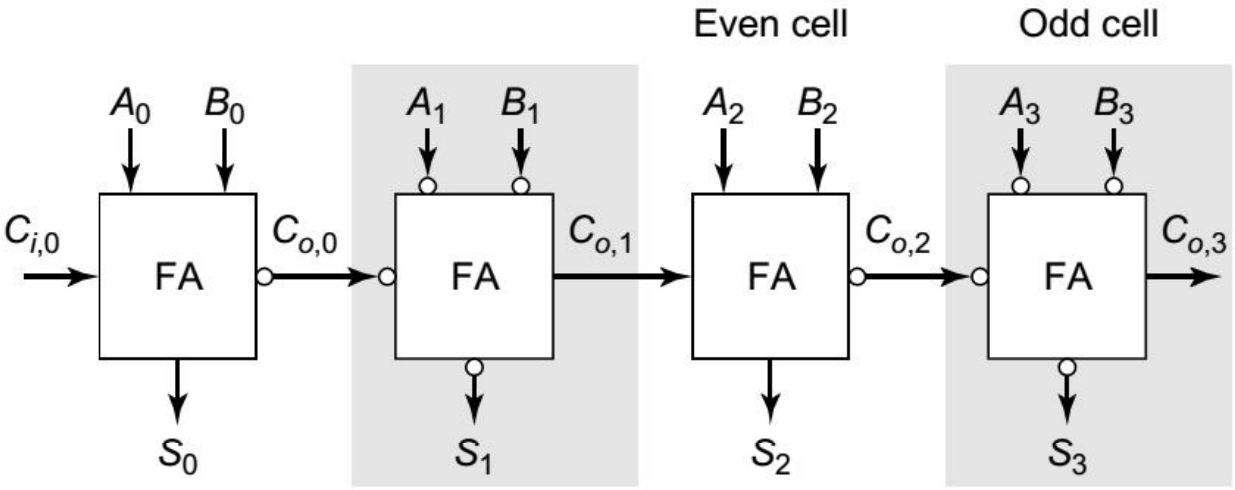

Figure 2: 4-bit ripple carry adder

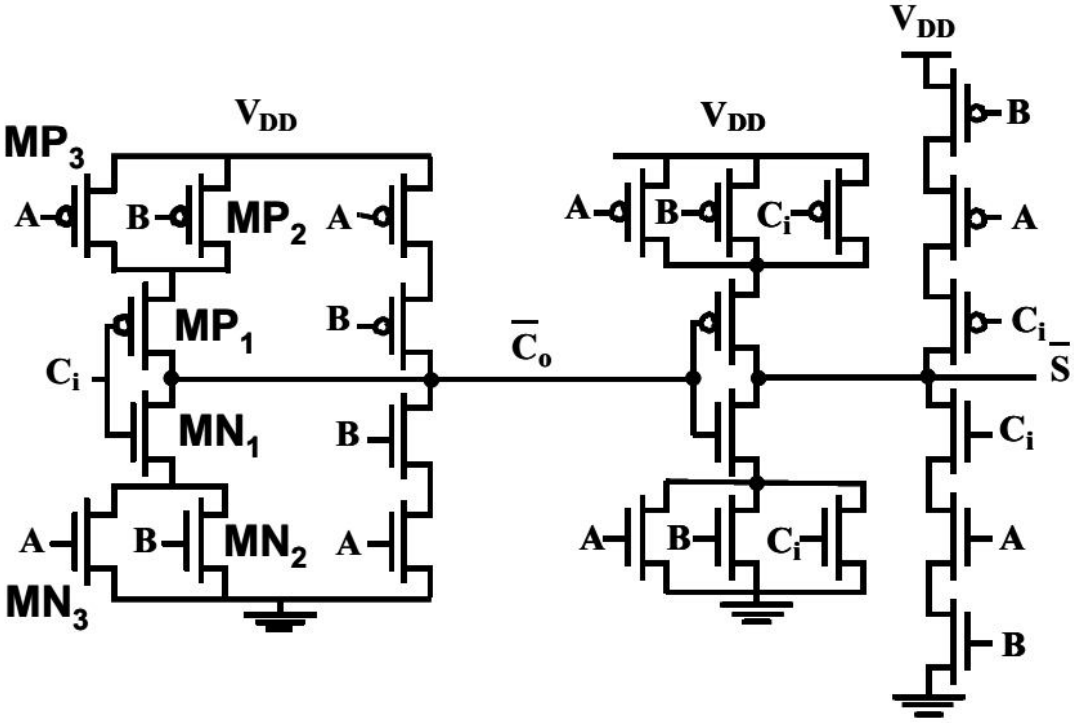

Figure 3: 1-bit Mirror full adder schematic