Faculty of engineering
Alexandria University
Department of Electrical engineering
Commination and Electronic
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VLSI

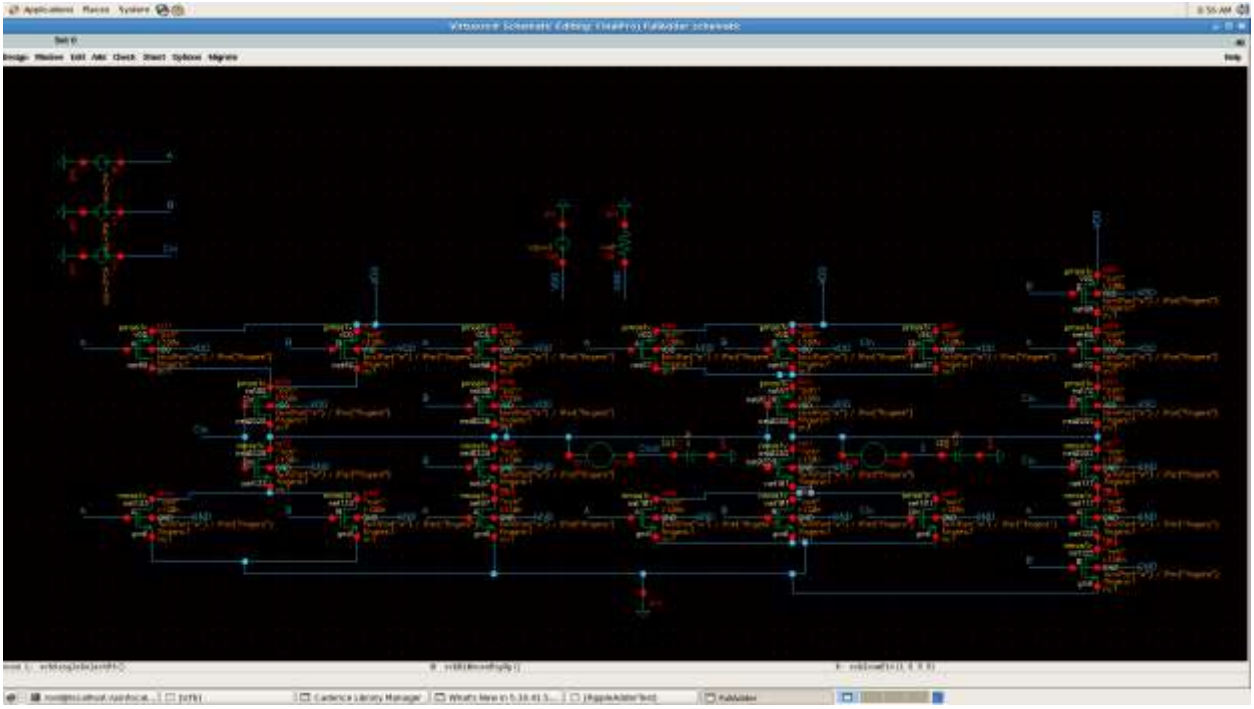
FINAL PROJECT

4-BIT RIPPLE CARRY ADDER

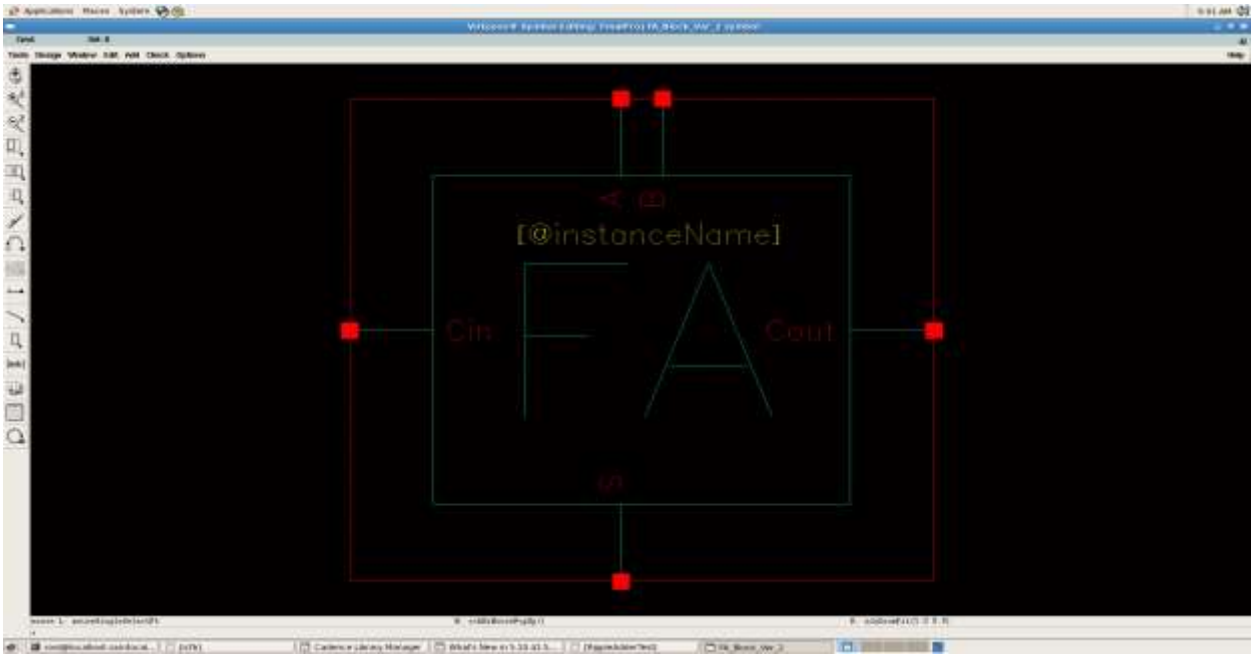
Name	ID
Asmaa Gamal Abdel-Halem	**15010473**
Mohamed Ezzat Faiq	**18011553**
Khaled Ali Diab	**18010598**
Hasan Mostafa Hasan	**18010573**
Tasneem Samy Hasan	**6(لائحة قديمة)**

A) 1- Bit Full Adder constructed as a 24- transistor mirror

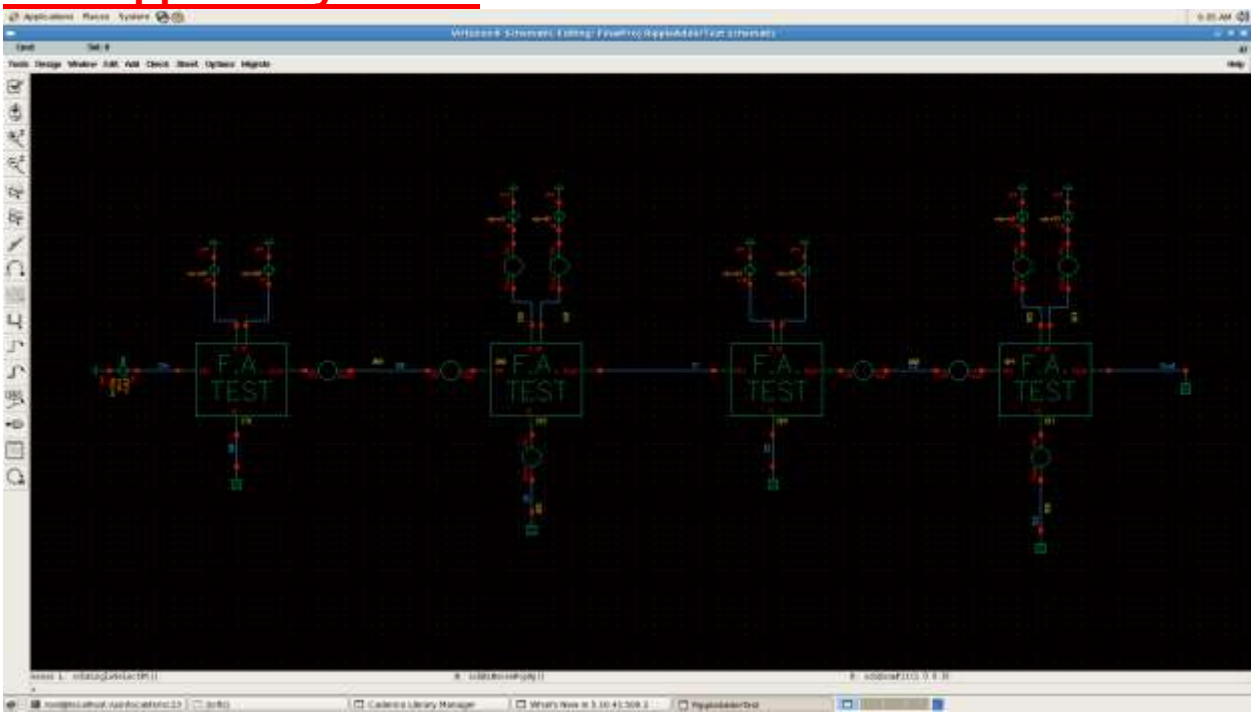
- **Schematic:**



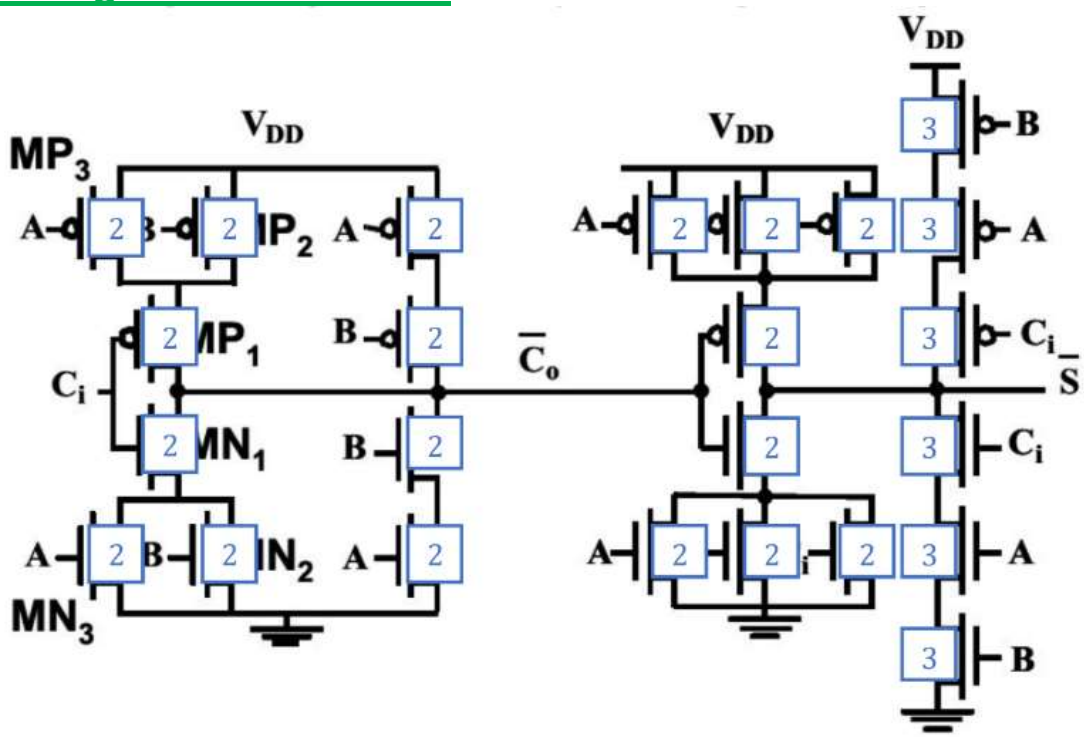
- **Symbol:**



4-bit ripple carry adder:



B) Sizing each transistor:

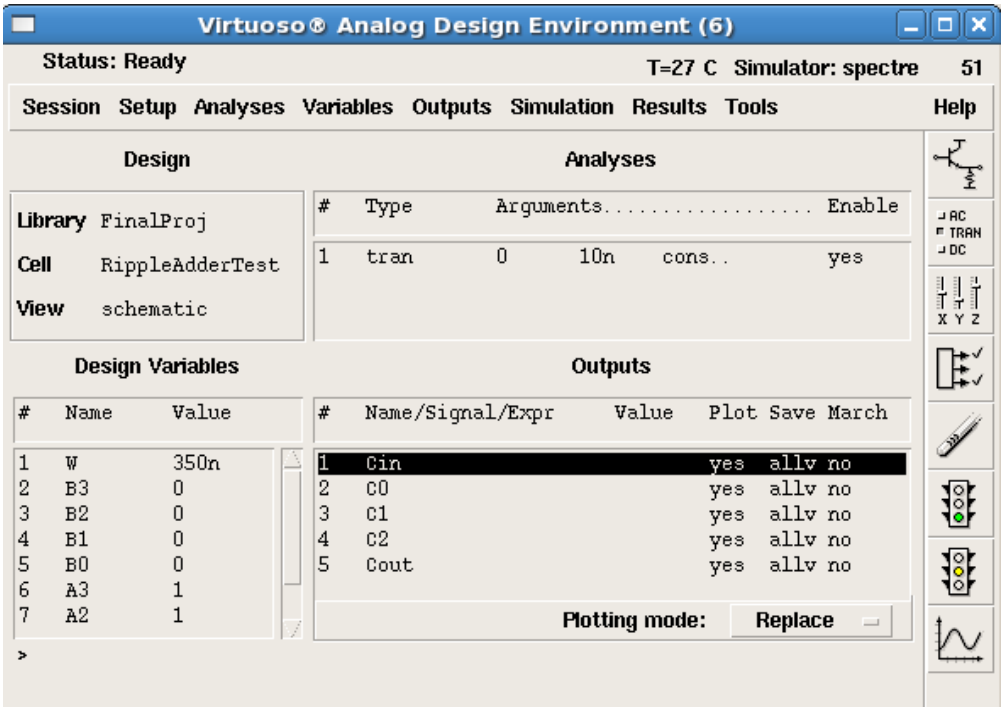


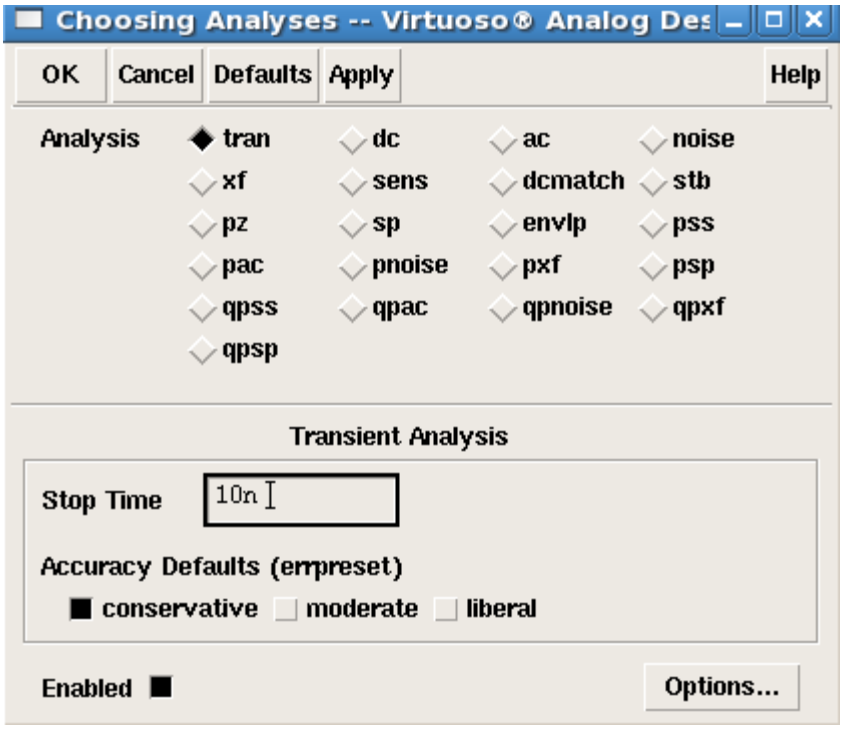
However, we keep in mind that the size of P-MOS must be double that of N-MOS. Therefore when testing, we applied a × 2 to every PMOS, such that we need only to set one variable up (Which we refer to as W).

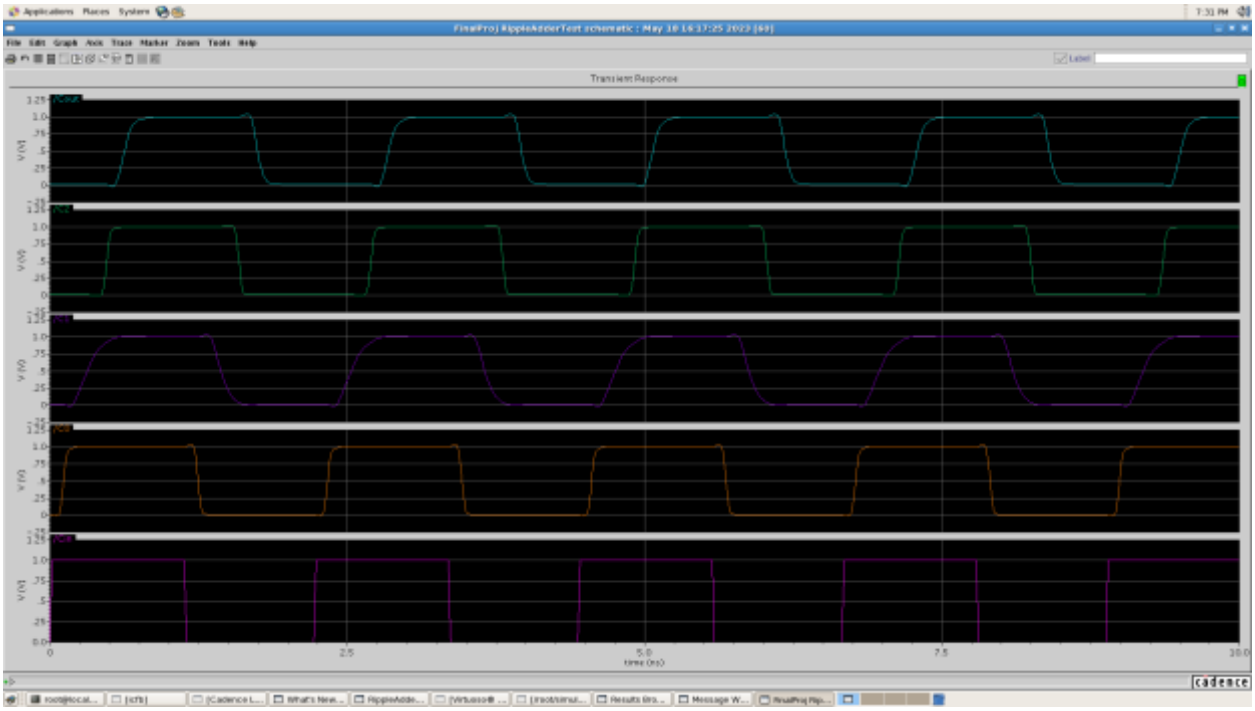
C) Full adder operation and optimization:

For propagation delay <1.5 nsec we first choosing the W_P=1200nm and W_P=600nm resulting delay to be in 0.8ns but this high sizing. So to make the best trade off between sizing and delaying as set in assignment we choose W_P=700nm and W_P=3500nm resulting delay =1.2ns This has the advantage of having a better practical applicability, having minimal area and delay.

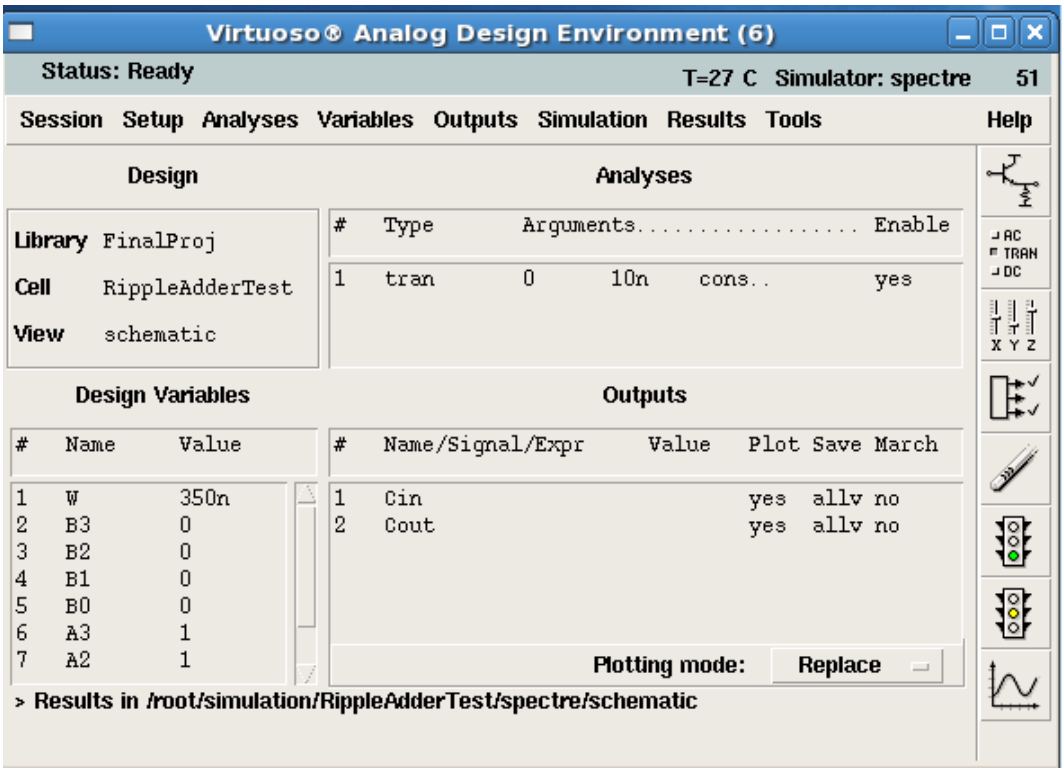
Also for the operation of full adder choosing that B0-B3 pulses set to be zeros and A0-A3 set to be ones.
SO the result will be :
A = 0000, B = 1111, Cin = Pulse with amplitude = 1
This should result in:
S = 0000, $Cout$ = Pulse with amplitude = 1
$Cout$ should have the same period as Cin and only equating to 1 when Cin also happens to be equal to 1. As such, we know have a good method to quantify the resulting delay upon changing the widths.

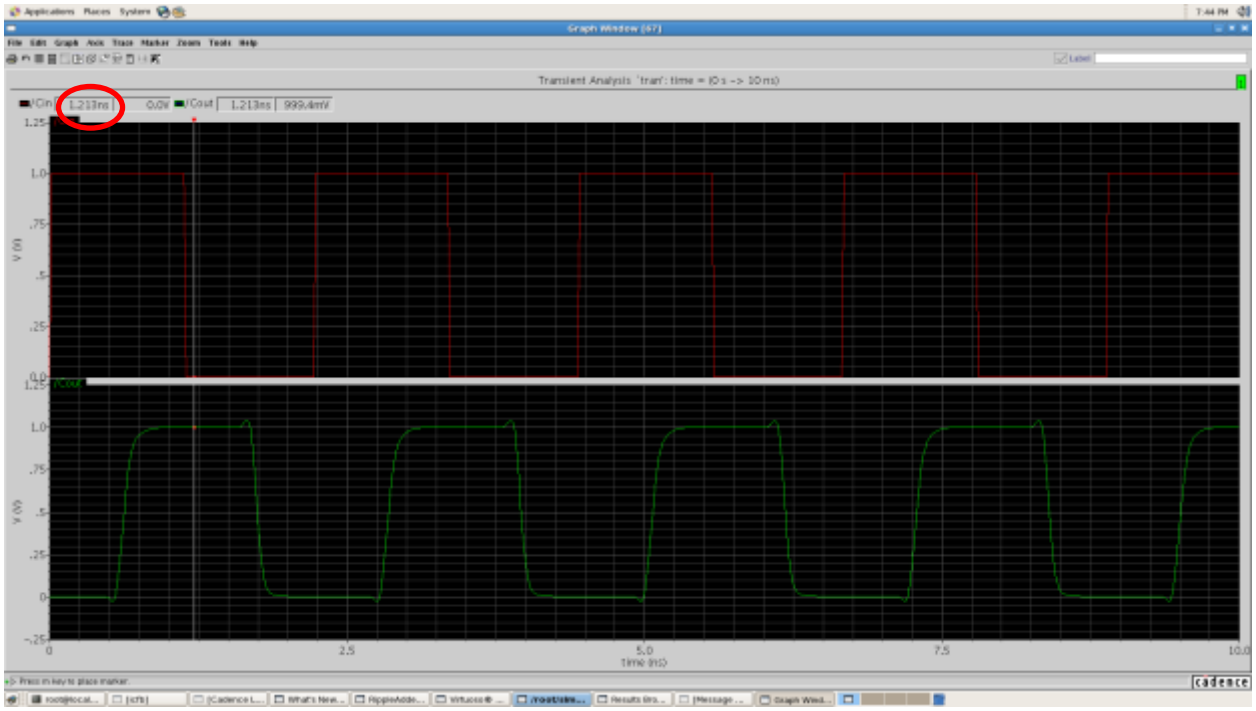



Choosing Analyses -- Virtuoso® Analog Des
OK
Cancel
Defaults
Apply
Help
Analysis
tran
dc
ac
noise
xf
sens
dcmatch
stb
pz
sp
envlp
pss
pac
pnoise
pxf
psp
qpss
qpac
qpnoise
qpxf
qpsp
Transient Analysis
Stop Time
10n
Accuracy Defaults (errpreset)
conservative
moderate
liberal
Enabled
Options...


Transient Response
cadence

Calculating Delay:





Delay =1.213 ns