

Faculty of engineering
Alexandria University
Department of Electrical engineering
Commination and Electronic
4th year 2022/2023



VLSI

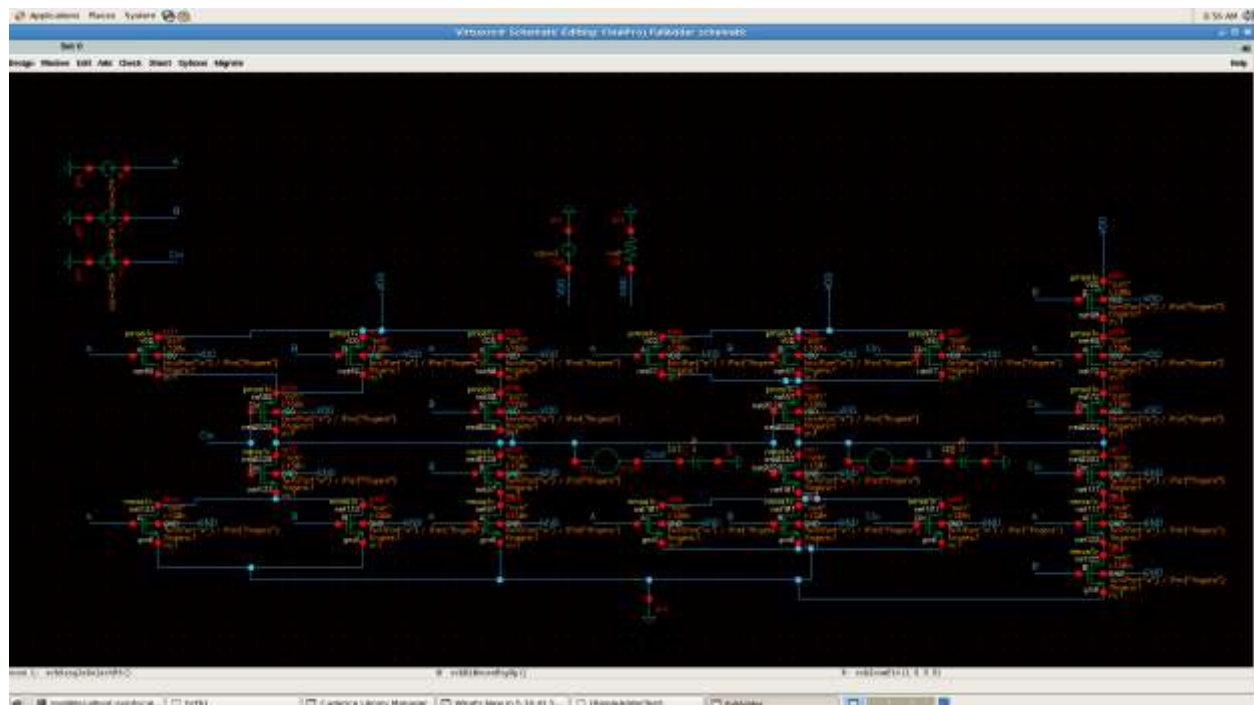
FINAL PROJECT

4-BIT RIPPLE CARRY ADDER

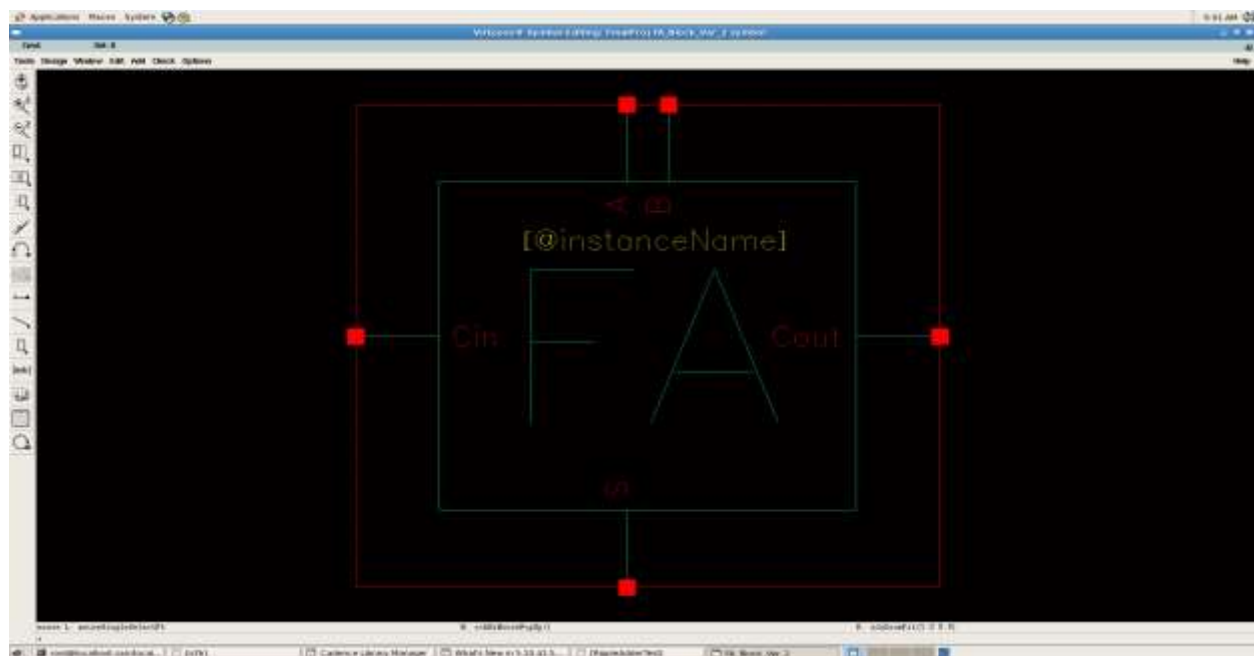
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A) 1- Bit Full Adder constructed as a 24- transistor mirror

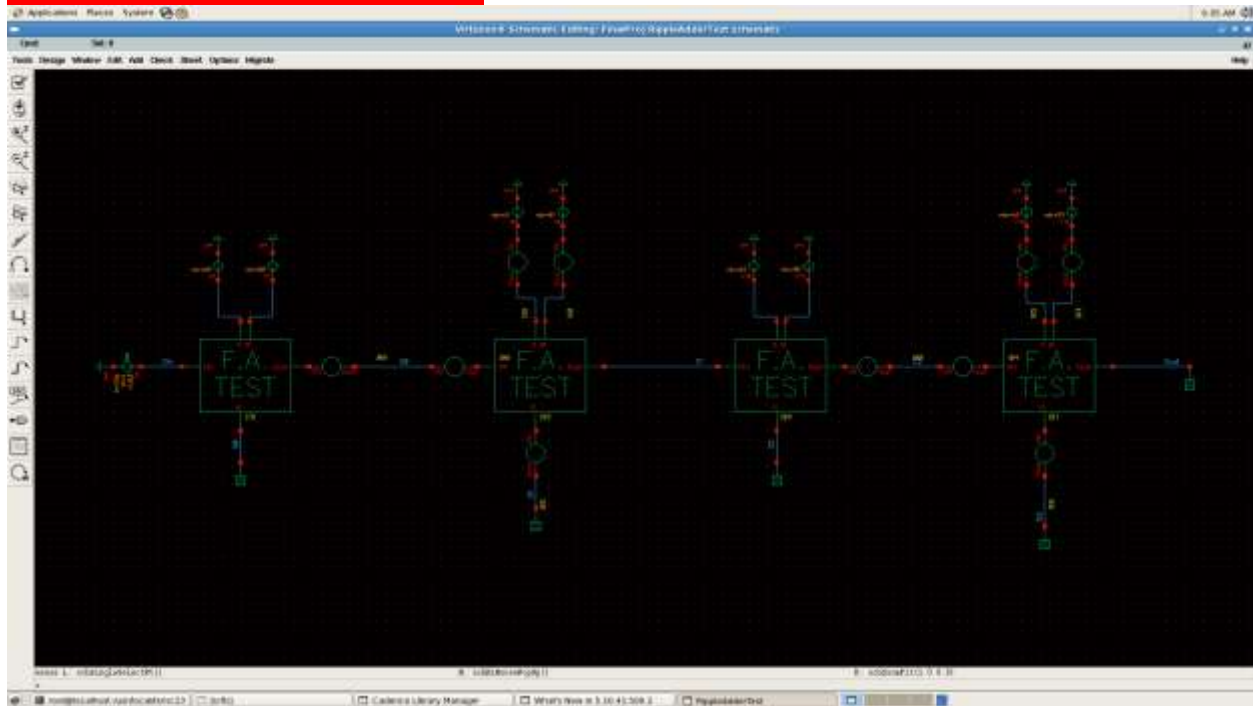
- Schematic:



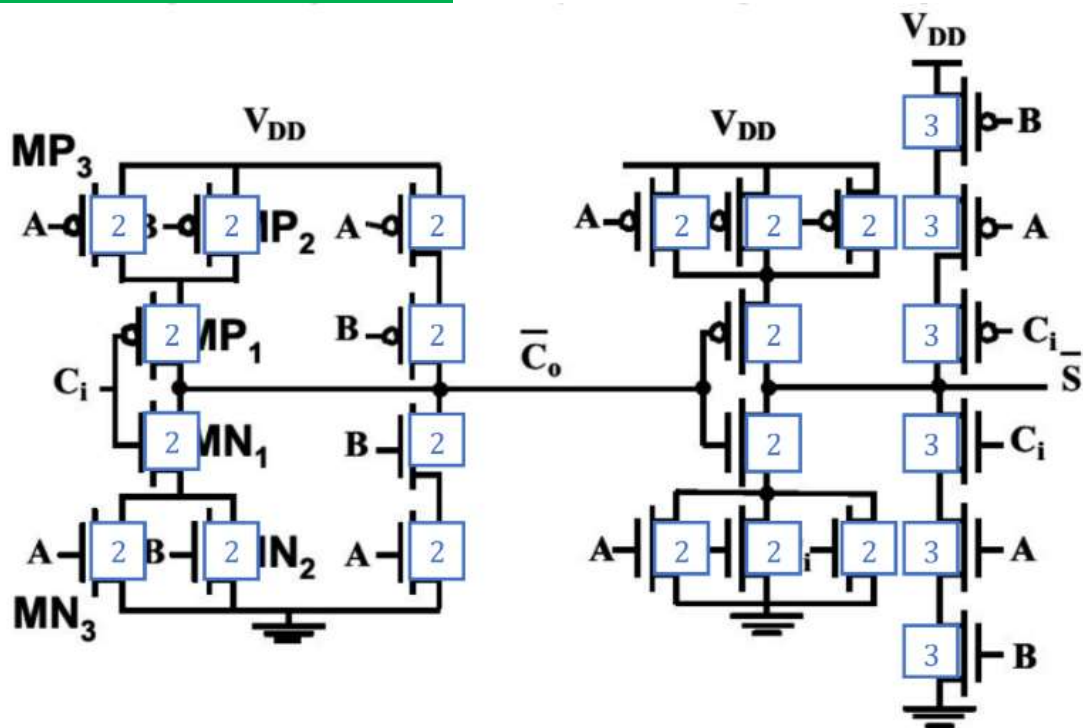
- Symbol:



4-bit ripple carry adder:



B) Sizing each transistor:



However, we keep in mind that the size of P-MOS must be double that of N-MOS. Therefore when testing, we applied a $\times 2$ to every PMOS, such that we need only to set one variable up (Which we refer to as W).



C) Full adder operation and optimization:

For propagation delay < 1.5 nsec we first choosing the $W_P=1200\text{nm}$ and $W_P=600\text{nm}$ resulting delay to be in 0.8ns but this high sizing. So to make the best **trade off** between sizing and delaying as set in assignment we choose **$W_P=700\text{nm}$ and $W_P=3500\text{nm}$ resulting delay $=1.2\text{ns}$** This has the advantage of having a better practical applicability, having minimal area and delay.

Also for the operation of full adder choosing that B0-B3 pulses set to be zeros and A0-A3 set to be ones.

SO the result will be :

$A = 0000$, $B = 1111$, $C_{in} = \text{Pulse with amplitude} = 1$

This should result in:

$S = 0000$, $C_{out} = \text{Pulse with amplitude} = 1$

C_{out} should have the same period as C_{in} and only equating to 1 when C_{in} also happens to be equal to 1. As such, we know have a good method to quantify the resulting delay upon changing the widths.

The screenshot shows the Virtuoso Analog Design Environment (6) interface. The top status bar indicates "Status: Ready", "T=27 C", "Simulator: spectre", and "51". The main menu bar includes "Session", "Setup", "Analyses", "Variables", "Outputs", "Simulation", "Results", "Tools", and "Help".

The "Design" tab is active, showing the "Library" as "FinalProj", the "Cell" as "RippleAdderTest", and the "View" as "schematic".

The "Analyses" tab is also active, showing a table of simulation analyses:

#	Type	Arguments.....	Enable
1	tran	0 10n cons..	yes

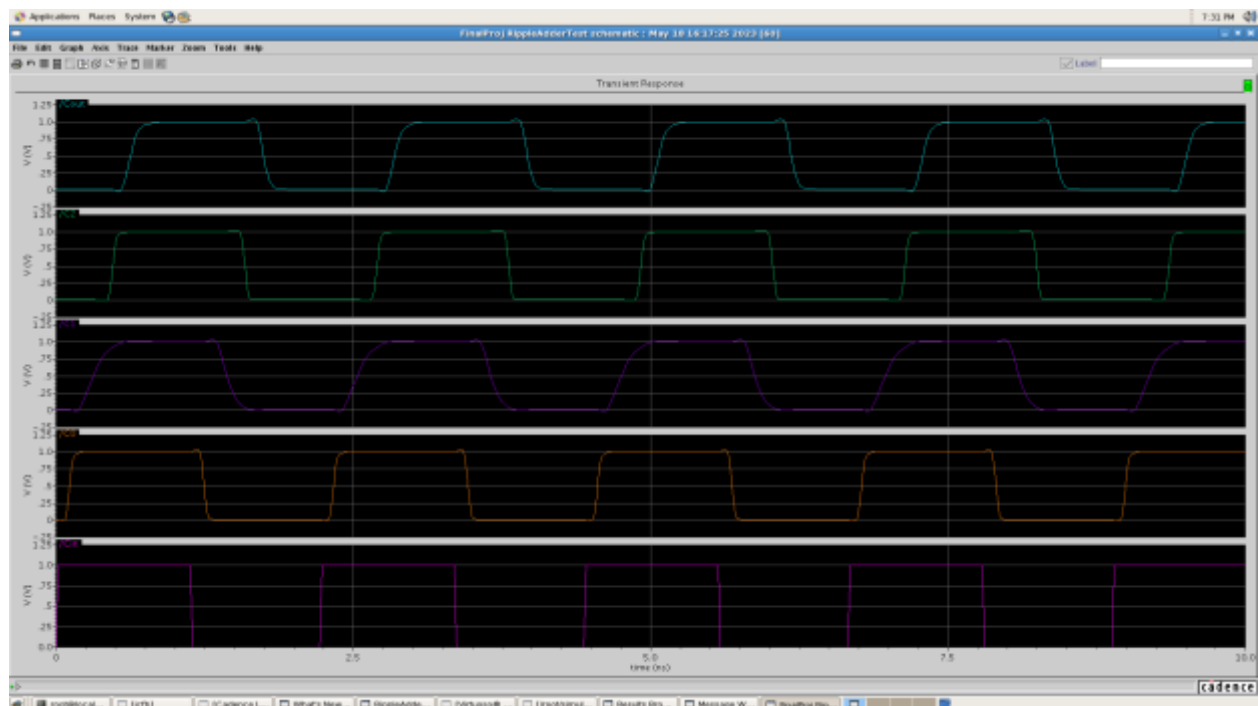
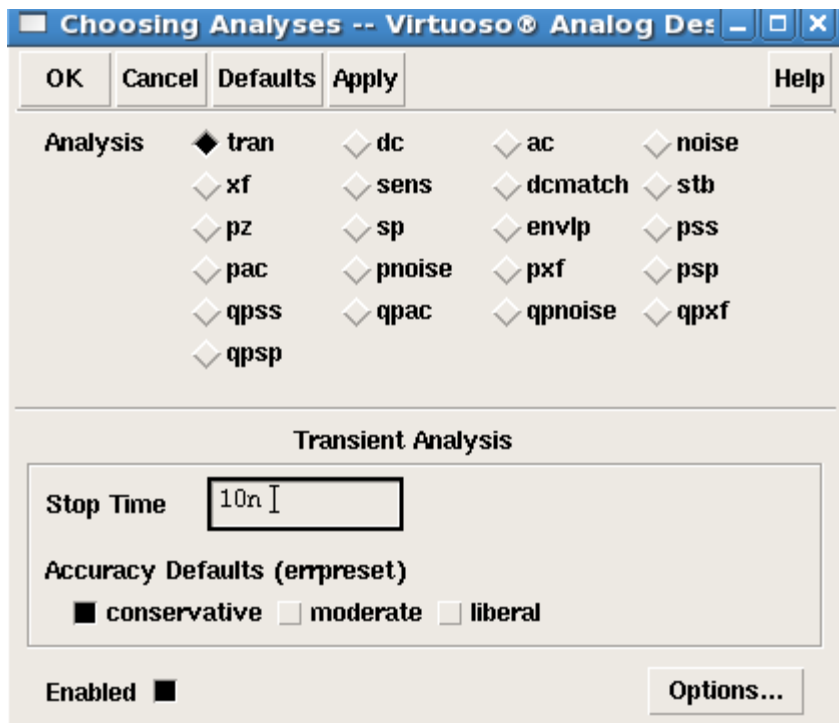
The "Outputs" tab is active, showing a table of simulation outputs:

#	Name/Signal/Expr	Value	Plot	Save	March
1	Cin	yes	allv	no	
2	C0	yes	allv	no	
3	C1	yes	allv	no	
4	C2	yes	allv	no	
5	Cout	yes	allv	no	

The "Design Variables" tab is also active, showing a table of design variables:

#	Name	Value
1	W	350n
2	B3	0
3	B2	0
4	B1	0
5	B0	0
6	A3	1
7	A2	1

The "Plotting mode" is set to "Replace".



Calculating Delay:

Virtuoso® Analog Design Environment (6)

Status: Ready T=27 C Simulator: spectre 51

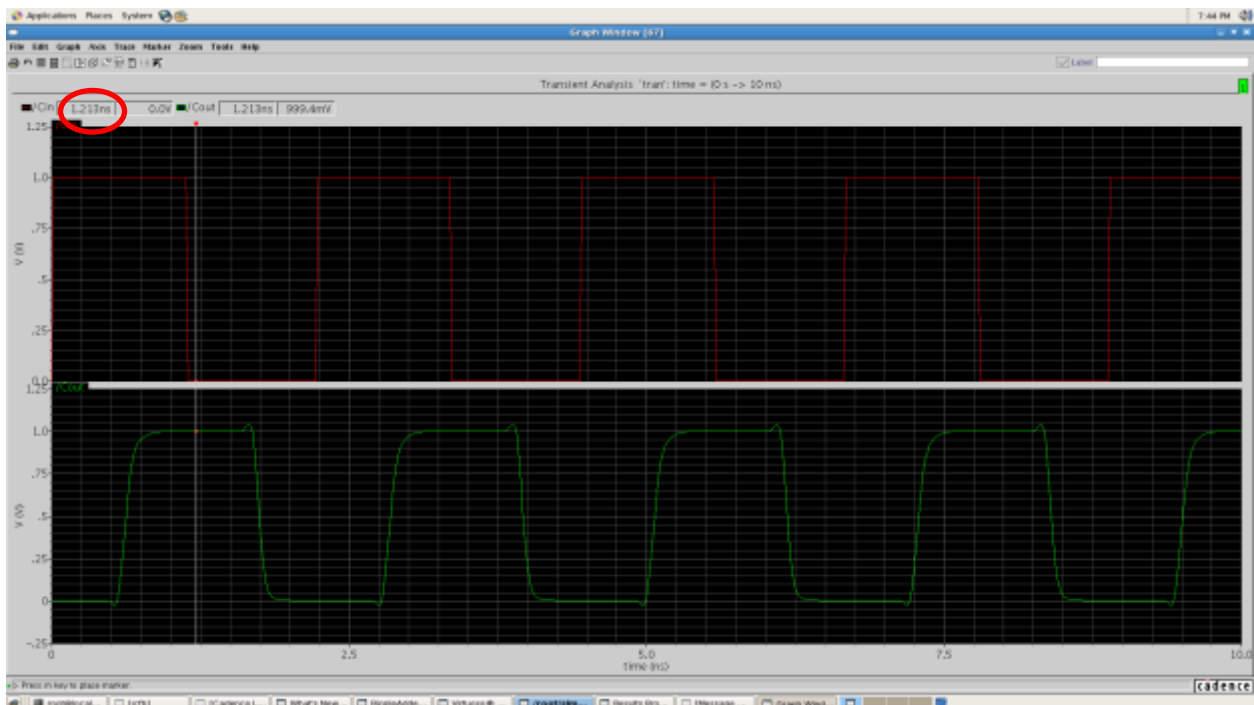
Session Setup Analyses Variables Outputs Simulation Results Tools Help

Design			Analyses			
Library	Cell	View	#	Type	Arguments.....	Enable
FinalProj	RippleAdderTest	schematic	1	tran	0 10n cons..	yes

Design Variables			Outputs			
#	Name	Value	#	Name/Signal/Expr	Value	Plot Save March
1	W	350n	1	Cin		yes allv no
2	B3	0	2	Cout		yes allv no
3	B2	0				
4	B1	0				
5	B0	0				
6	A3	1				
7	A2	1				

Plotting mode: Replace

> Results in /root/simulation/RippleAdderTest/spectre/schematic



Delay = 1.213 ns