International Institute of Information Technology Bangalore

SRAM Write Assist Circuit Using Cell Supply Voltage Self-Collapse With Bitline Charge Sharing for Near-Threshold Operation

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CONTENTS

OBJECTIVE

Design a Write-Assist circuit using Cell VDD (CV_{DD}) self-collapse with Bitline (BL) charge sharing in the near threshold voltage (V_{TH}) region by utilising –

1. CV_{DD} self-collapse
2. Feedback operation by detecting a write failure

INTRODUCTION TO SRAM

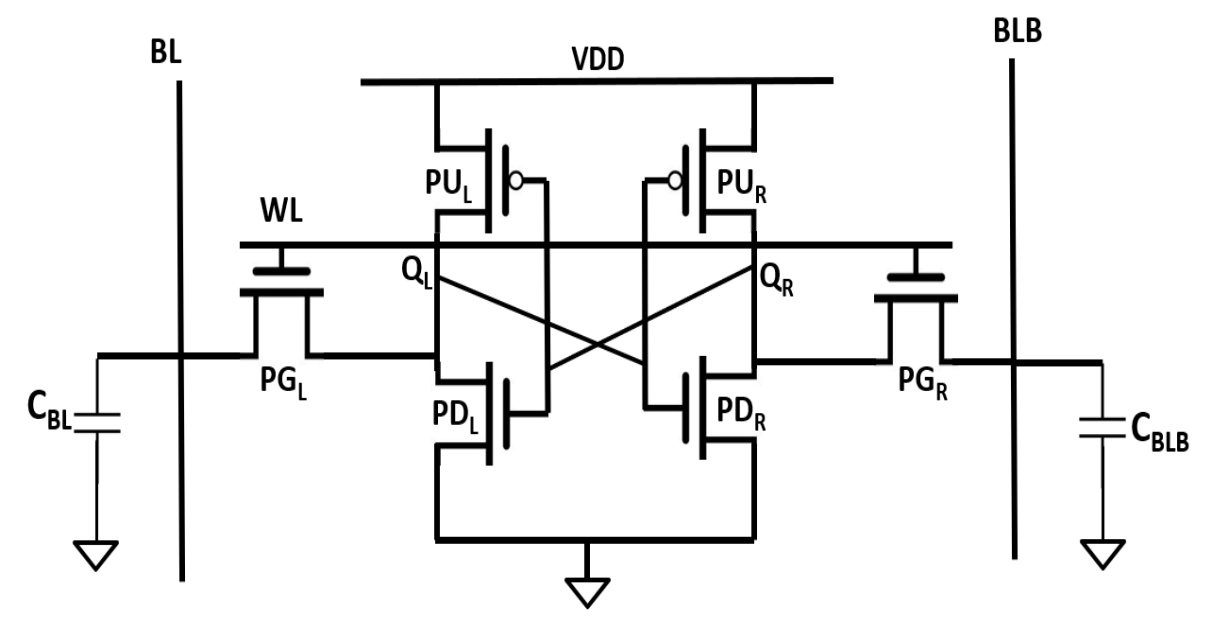
Static random-access memory (static RAM or SRAM) is a type of **random-access memory (RAM)** that uses **latching circuitry (flip-flop)** to store each bit. SRAM will **hold its data permanently in the presence of power**, but data is lost as soon as power is removed.

SRAM is a popular choice for microcontrollers when **fast and efficient operations with low power** consumption are needed. In computer systems, it is commonly used as the **primary working memory,** including the internal registers and cache of a CPU.

6T SRAM CELL – READ OPERATION

1. Pre charge BL and BLB to HIGH.
2. Turn on WL
3. BL or BLB pulled down to 0 based on Q_L and Q_R. So, for eg – if Q_L=0, Q_R=1, BL discharges via PG_L , PD_L, GND; and; BLB stays HIGH but Q_L bumps up slightly.

NOTE – In order to prevent Q from changing its value, **strength of PD_L > PG_L**, that is, ON resistance of PD_L < PG_L.

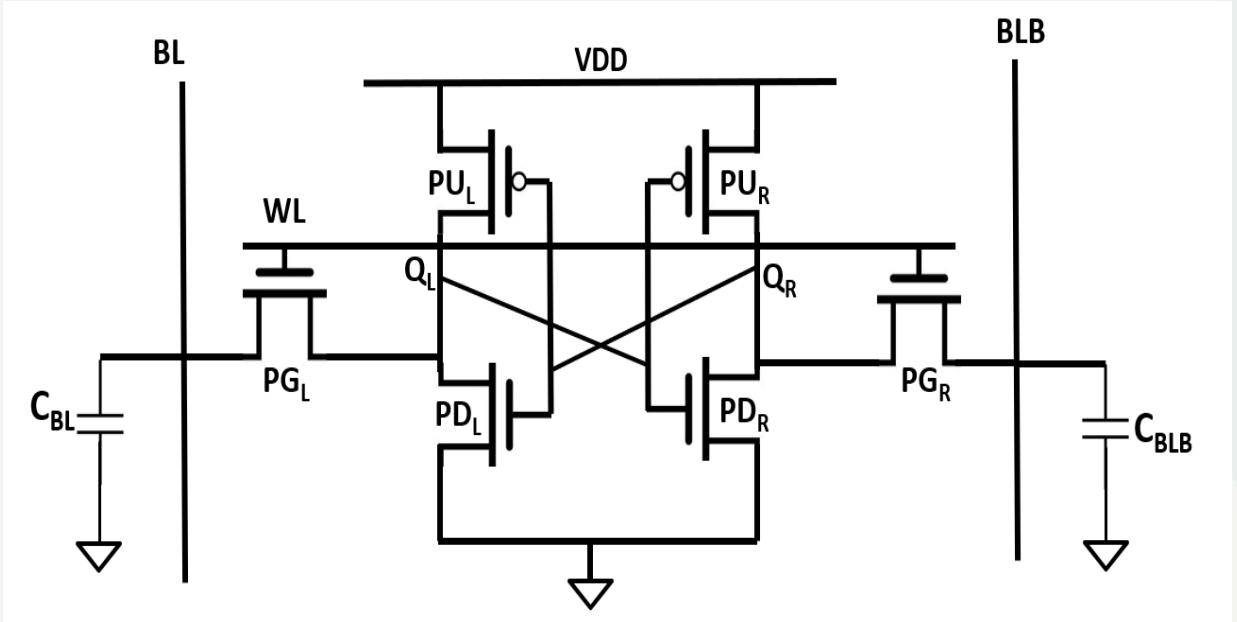


6T SRAM CELL – WRITE OPERATION

1. Drive BL and BLB to necessary values.
2. Turn on WL.
3. BL or BLB will drive Q_L and Q_R with new values. So, for eg – if Q_L=0, Q_R=1, BL =1 and BLB =0, This would force Q_R to low and Q_R to high.

NOTE – **Strength of PGL > PUL**, that is, ON resistance of $PG_L < PU_L$.

Hence strength of $PD_L > PG_L > PU_L$.



MOTIVATION

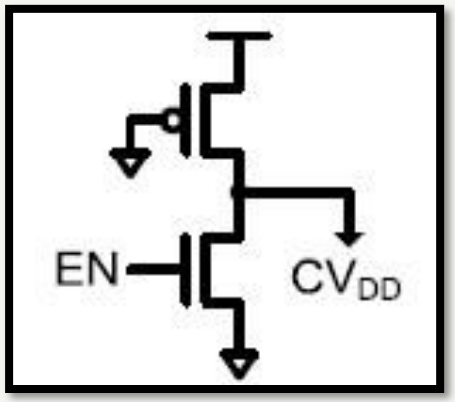
To achieve energy efficiency in System-on-Chip designs imperative for applications like wearables and bio-implant devices, lowering the supply voltage NEAR to the threshold voltage (V_{th}) is the most effective approach. However, this is limited by the minimum operating voltage (V_{MIN}) of the SRAM, which depends on the balance between its read-stability and write-ability as well as area constraints.

Some previous works utilising the CV_{DD} collapse, Negative bitline (NBL) concept and Gate modulated self-collapse (GSC) have been implemented but they do no offer significant improvements in energy efficiency.

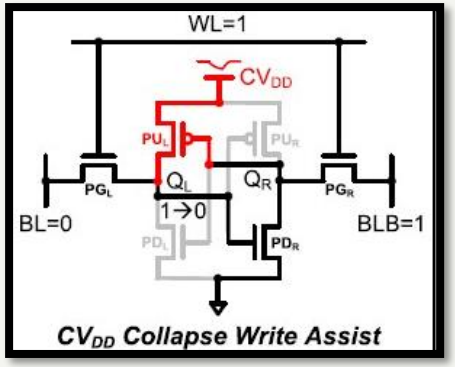
This paper's work aims to provide a design that would not only improve V_{MIN} but also use minimal write energy while doing so.

PREVIOUS WORKS 1 – SB-TVC

Write Assist Circuit - **Strong-bias Transient CVDD Collapse**

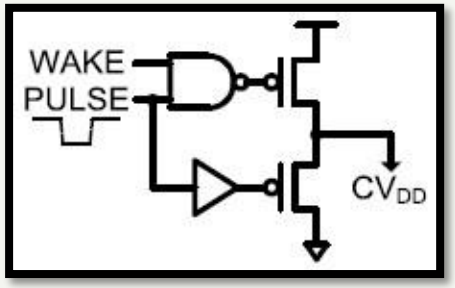


1. CV_{DD} lowered by voltage divider of nMOS and pMOS transistors.
2. **DISADV - Consumes significant write energy.** This is because of the large static current that would flow through the write assist circuit due to the pMOS being always ON and nMOS being ON due to Enable.

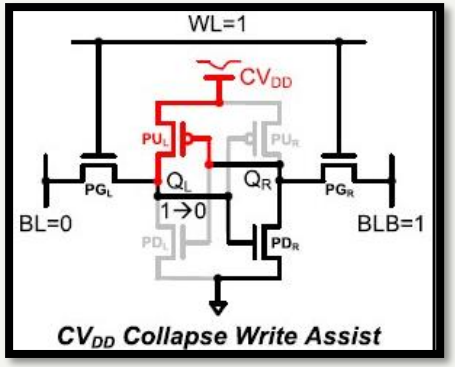


PREVIOUS WORKS 2 – PP-TVC

Write Assist Circuit - **Pulsed-pMOS Transient CV_{DD} Collapse**

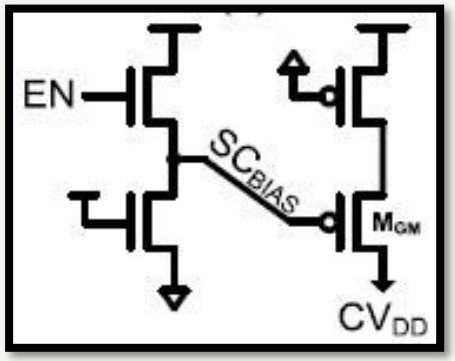


1. pMOS pull-down transistor lowers the CV_{DD} instantaneously by using the PULSE signal.
2. **DISADV - Write energy of PP-TVC is large because CV_{DD} in all selected columns should be lowered to the voltage level that ensures the write-ability of the worst SRAM cell. Generation of accurate pulse signal also consumes energy.**

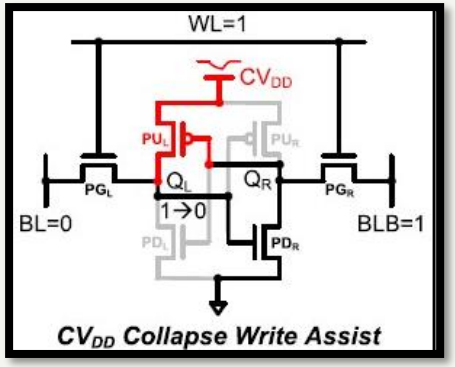


PREVIOUS WORKS 3 – GSC

Write Assist Circuit - **Gate-modulated Self-collapse**

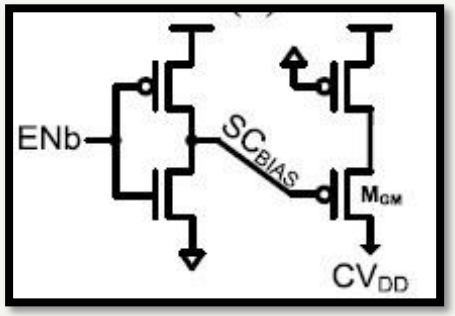


1. CVDD is lowered by the write contention current that would come in PUL and PGL in the write assist circuit.
2. CVDD collapse ∝ 1/Write ability, hence for a cell with high write ability, energy used to collapse CVDD (write energy) is reduced.
3. But CV_{DD} collapse speed is low as the contention current would flow through the min. sized PU_L Transistor.
4. CV_{DD} collapse level would also depend on strength of M_{GM} transistor controlled by the SC_{BIAS} signal. **DISADV – as SC_{BIAS} increases, M_{GM} weakens, CV_{DD} collapse level would decrease, but write energy to generate large SC_{BIAS} would increase due to static current in the 2 nMOS transistors.**

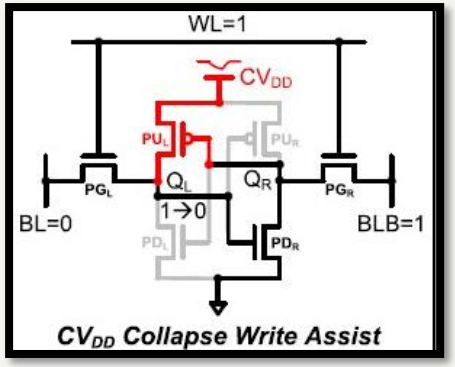


PREVIOUS WORKS 4 – SC

Write Assist Circuit - **Self-collapse**



1. M_{GM} is completely turned off and SC_{BIAS} is driven to V_{DD}.
2. No static current.
3. CV_{DD} collapse level not determined by strength of M_{GM} transistor.

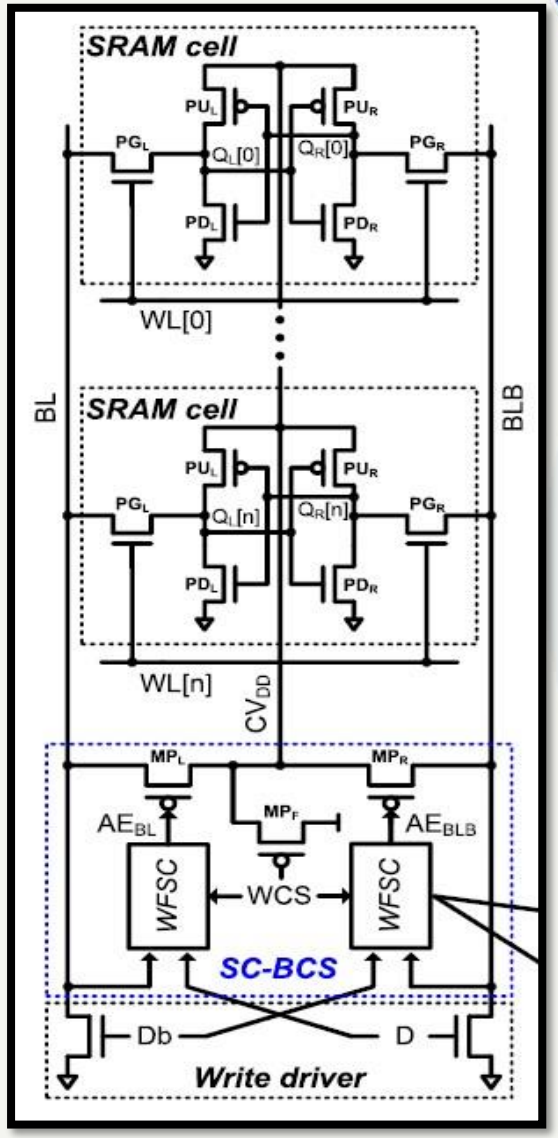


PROPOSED WORK – SC-BCS

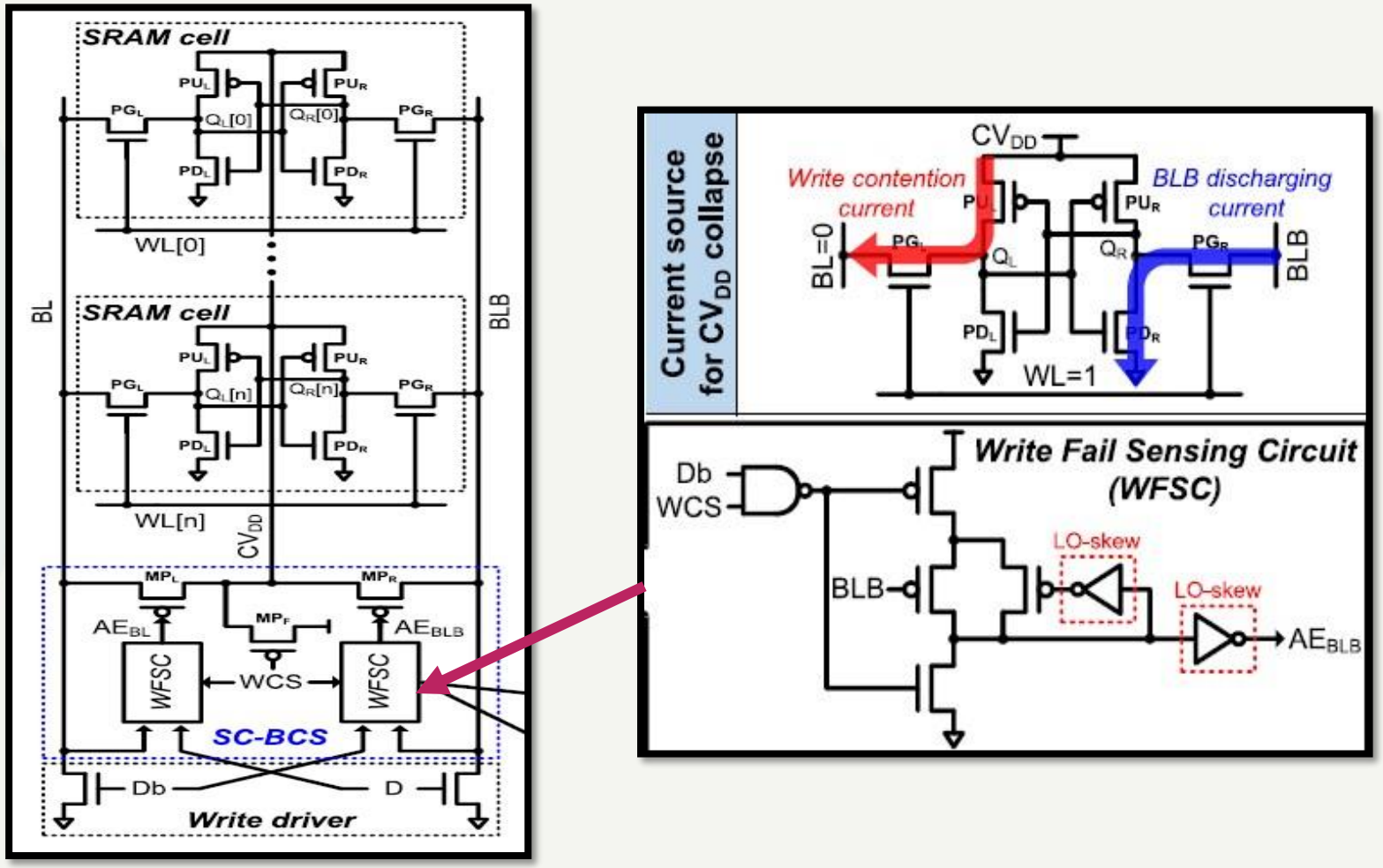
Cell Supply Voltage Self-collapse With Bitline Charge Sharing

The proposed SC-BCS consists of a transistor to disconnect CV_{DD} from V_{DD} (MP_F), transistors for the charge sharing between CV_{DD} and BL or BLB (MP_L and MP_R, respectively), and a write fail sensing circuit (WFSC) to detect the write failure.

There are two phases of Operation. In the write-0 (or write-1) operation, the write driver drives BL (or BLB) to GND and WL is enabled.



PROPOSED WORK – COMPLETE CIRCUIT

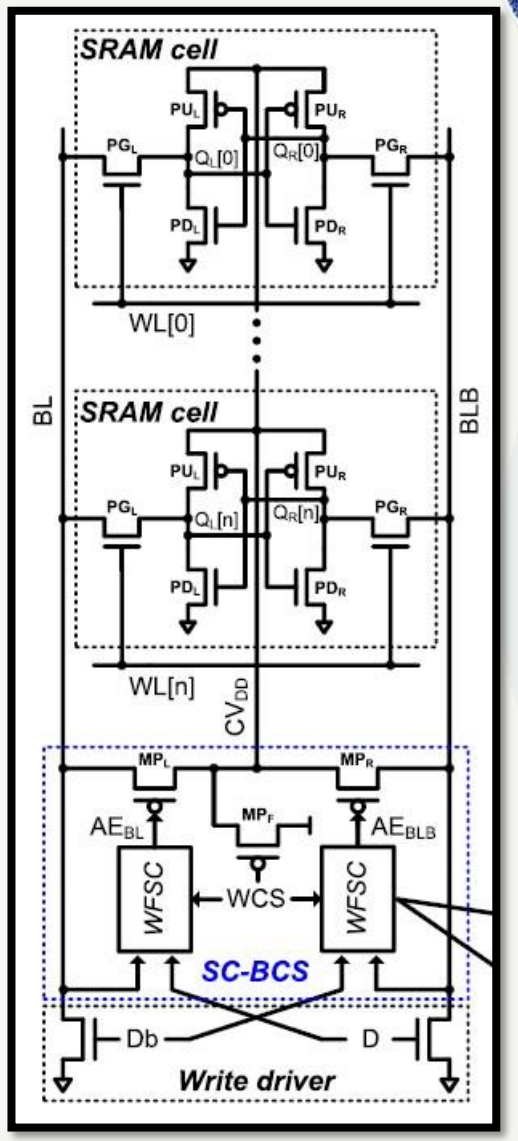


PROPOSED WORK – SC-BCS (Phase 1)

Cell Supply Voltage Self-collapse With Bitline Charge Sharing

Phase I (P1):

1. During P1, CV_{DD} is lowered by the write contention current of the selected cell and thus the write-ability is gradually improved.
2. Most SRAM cells are successfully written in P1.
3. In the case of the high-σ cell (SRAM cell with a low write-ability), the write operation fails.

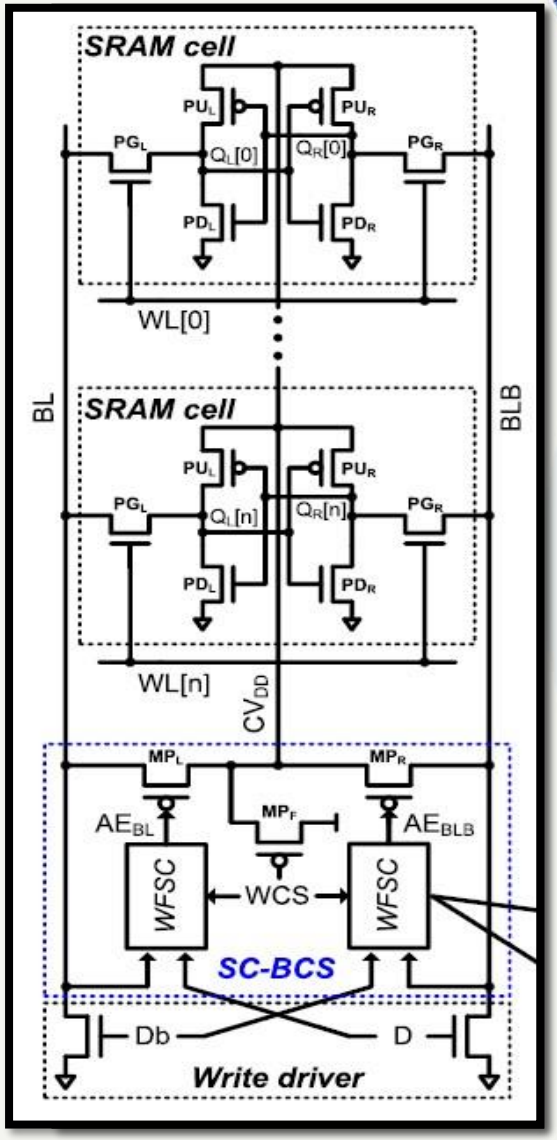


PROPOSED WORK – SC-BCS (Phase 2)

Cell Supply Voltage Self-collapse With Bitline Charge Sharing

Phase II (P2):

1. As the storage nodes are not flipped, a pre-charged BLB (or BL) decreases by the discharging current flowing through the PG_R (or PG_L) and PDR (or PD_L) transistors in the high-σ cell during P1.
2. P2 starts when WFSC detects the write failure through the discharged BLB (or BL).
3. WFSC turns on MP_R (or MP_L), which performs charge sharing between CV_{DD} and BLB (or BL).
4. CVDD is lowered more by the discharged BLB (or BL) and the write-ability is improved.



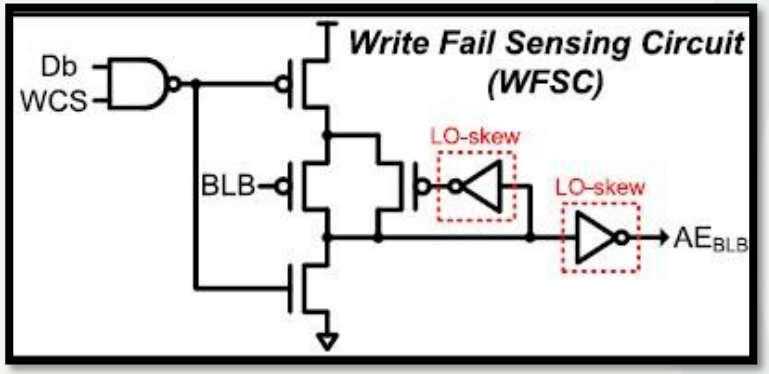
PROPOSED WORK – WFSC

Write Fail Sensing circuit

A key component to perform the feedback process in SC-BCS.

In the write-0 operation, the data(bar) signal D(Db) is GND (V_{DD}) and the write column select signal (WCS) is enabled to V_{DD}.

1. In the write-1 operational path, Pre discharged node floats and evaluation mode starts.
2. In the case of the high-σ cell, as BLB is discharged, the pMOS transistor is gradually turned on, and the voltage of the pre-discharged node starts to increase.
3. The LOW-skew inverters are applied to speed up the sensing of the pre-discharged node.



PROPOSED WORK – Advantages

1. Improves the write-ability with a smaller delay overhead than GSC and SC in the near-Vth region. This is because CV_{DD} can be lowered much faster by the two-phase operation of the proposed SC-BCS, which is achieved by utilizing not only the write contention current on the write-0 path but also the discharging current on the write-1 path.

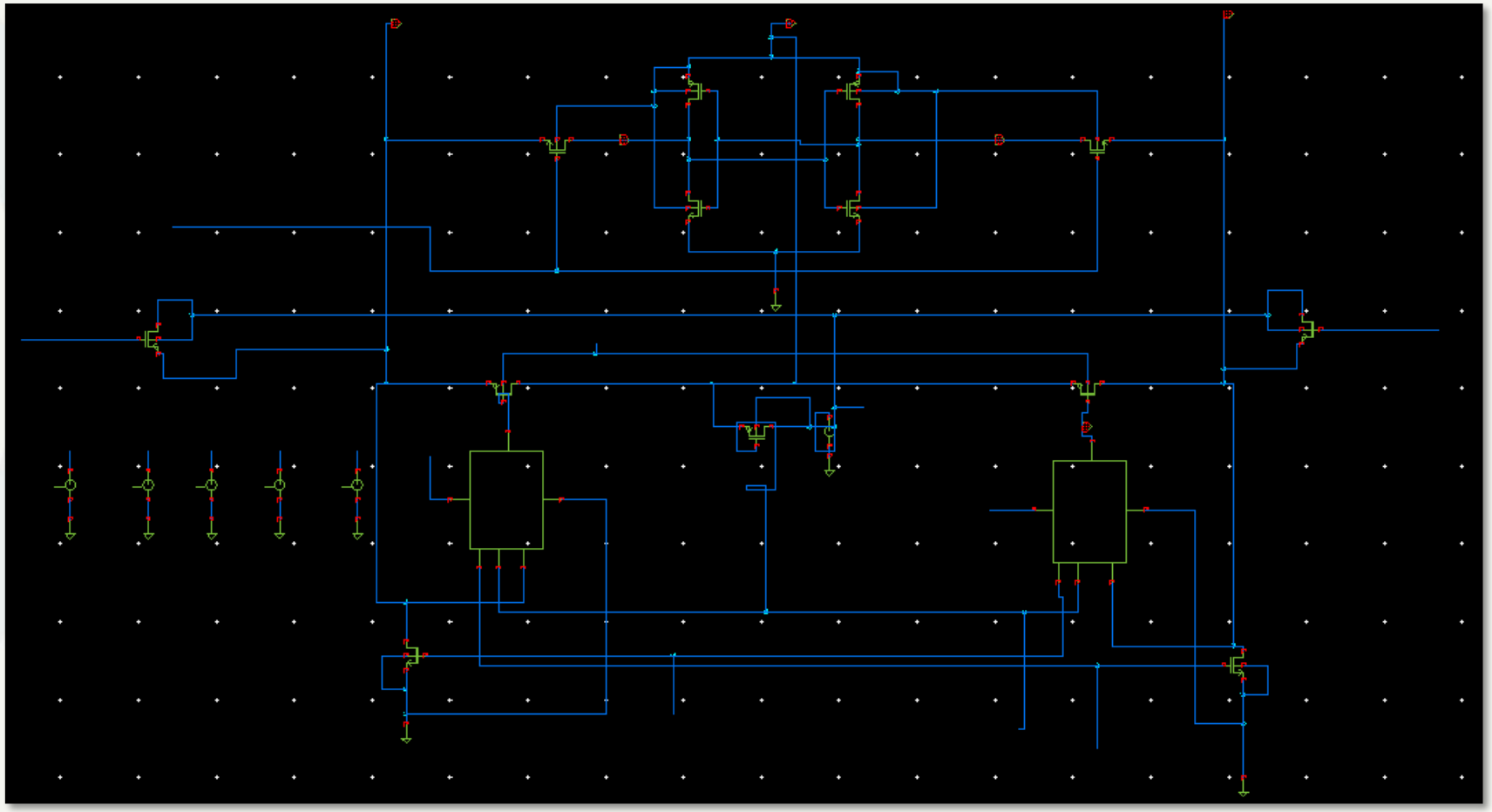
2. While GSC and SC use both nMOS and pMOS transistors for the write driver and write MUX, the proposed SC-BCS uses only the nMOS transistor. This is because GSC and SC should prevent BL or BLB on the write-1 path from being discharged through the SRAM cell during the self-collapse, whereas the proposed SC-BCS detects the write fail and lowers CV_{DD} by utilizing the discharged BL or BLB on the write-1 path.

3. The proposed SC-BCS can reduce the energy consumed on the write-1 path. The write driver in GSC and SC drives BL or BLB on the write-1 path to V_{DD} and thus the static current flows through the SRAM cell until the stored data is flipped. However, because the proposed SC-BCS has a faster CV_{DD} collapse time than GSC and SC, the stored data is flipped much faster and the energy on the write-1 path is reduced.

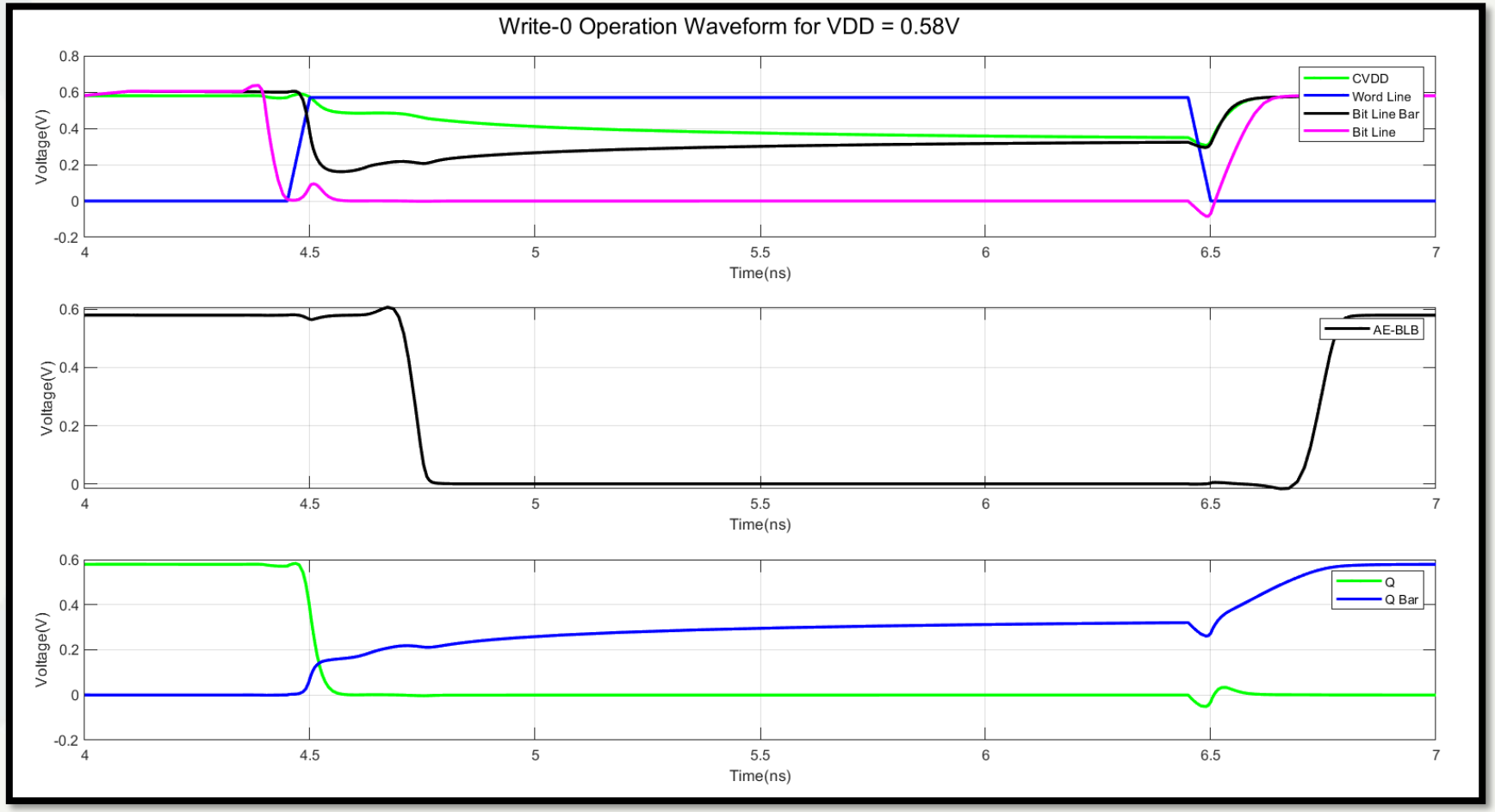
SIMULATION RESULTS AND COMPARISIONS

Cadence Virtuoso circuit Schematics, Graphs and Comparison Tables

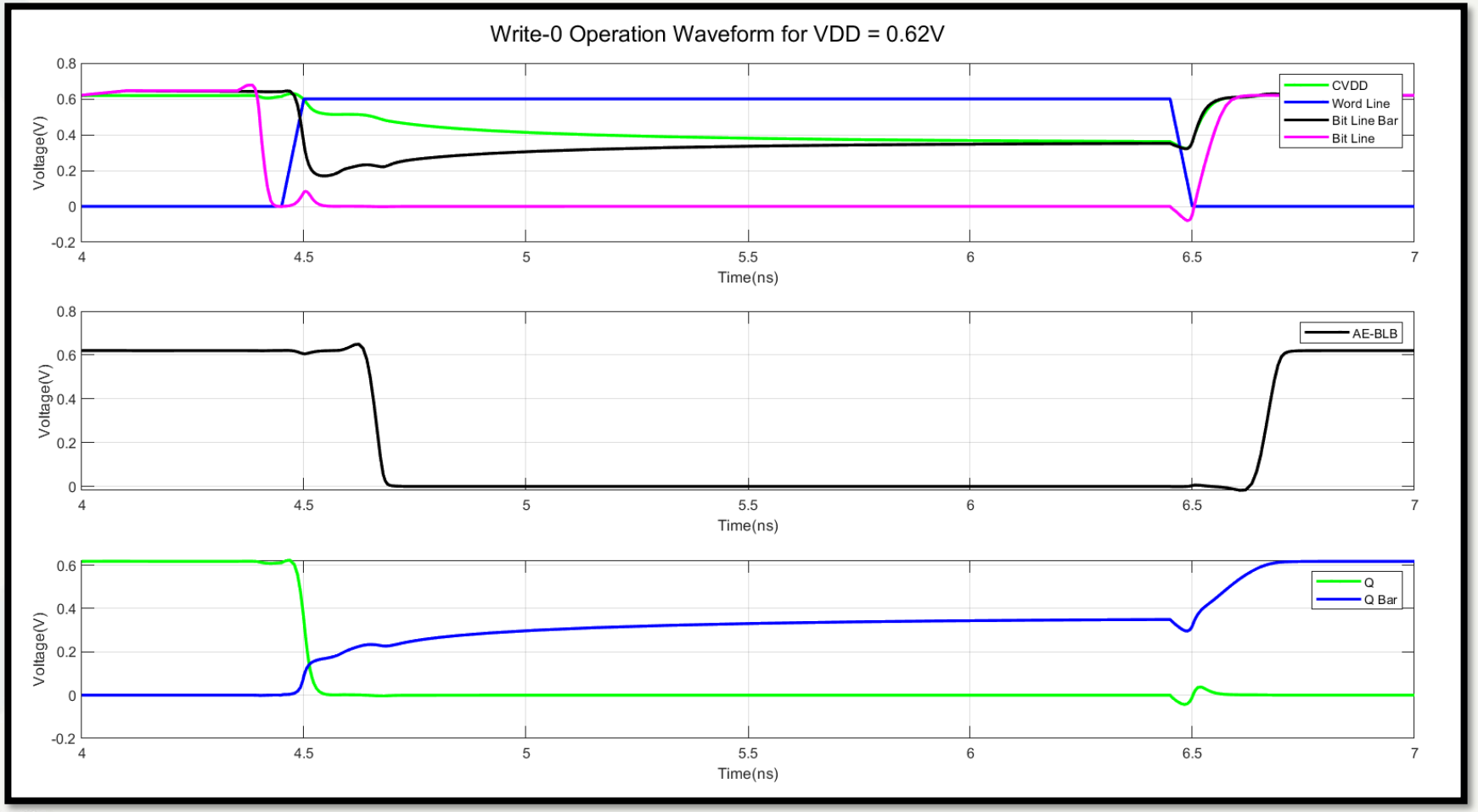
Schematic of SC-BCS SRAM cell



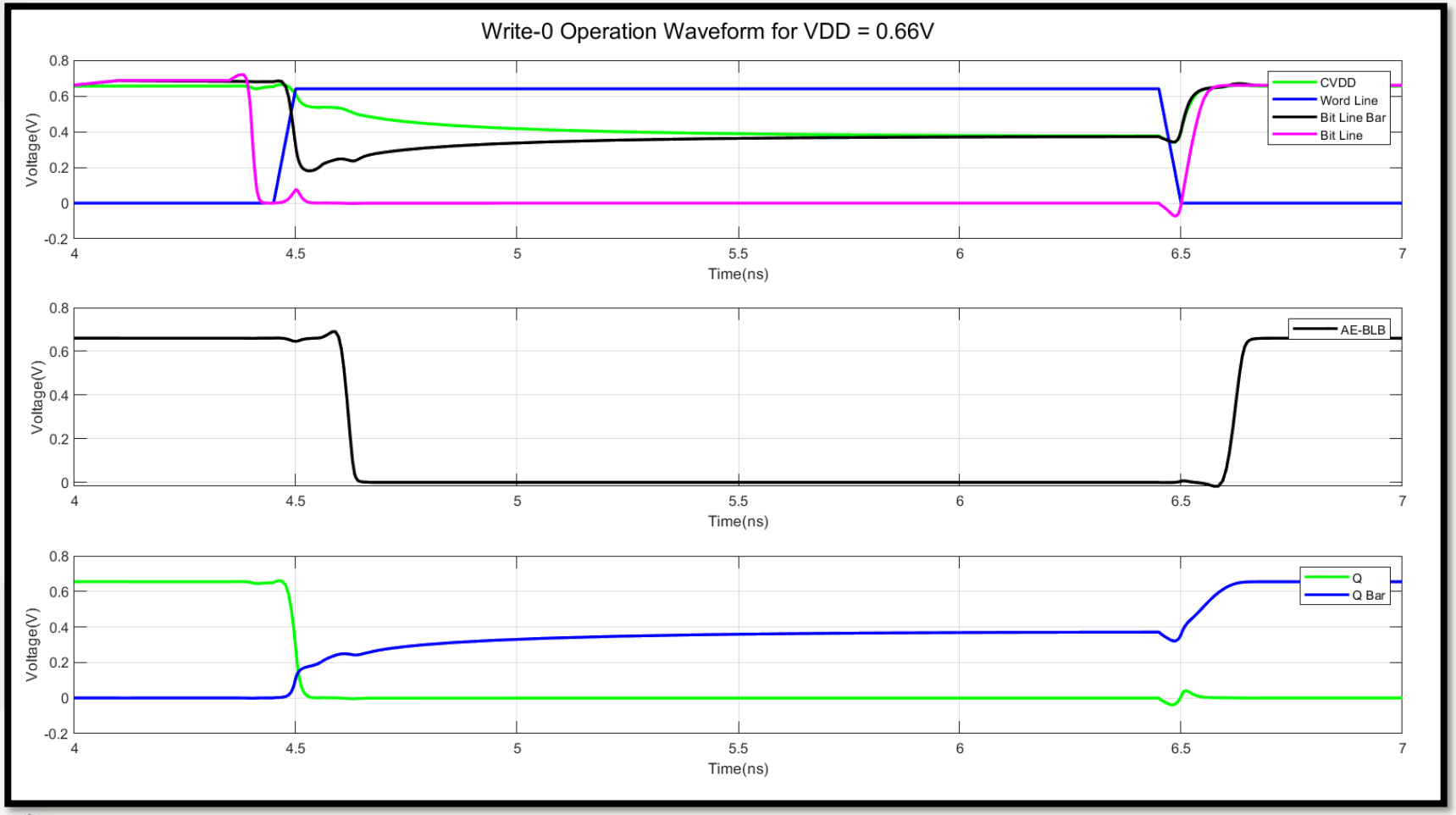
Write-0 Operation Waveform for HIGH-σ SC-BCS cell



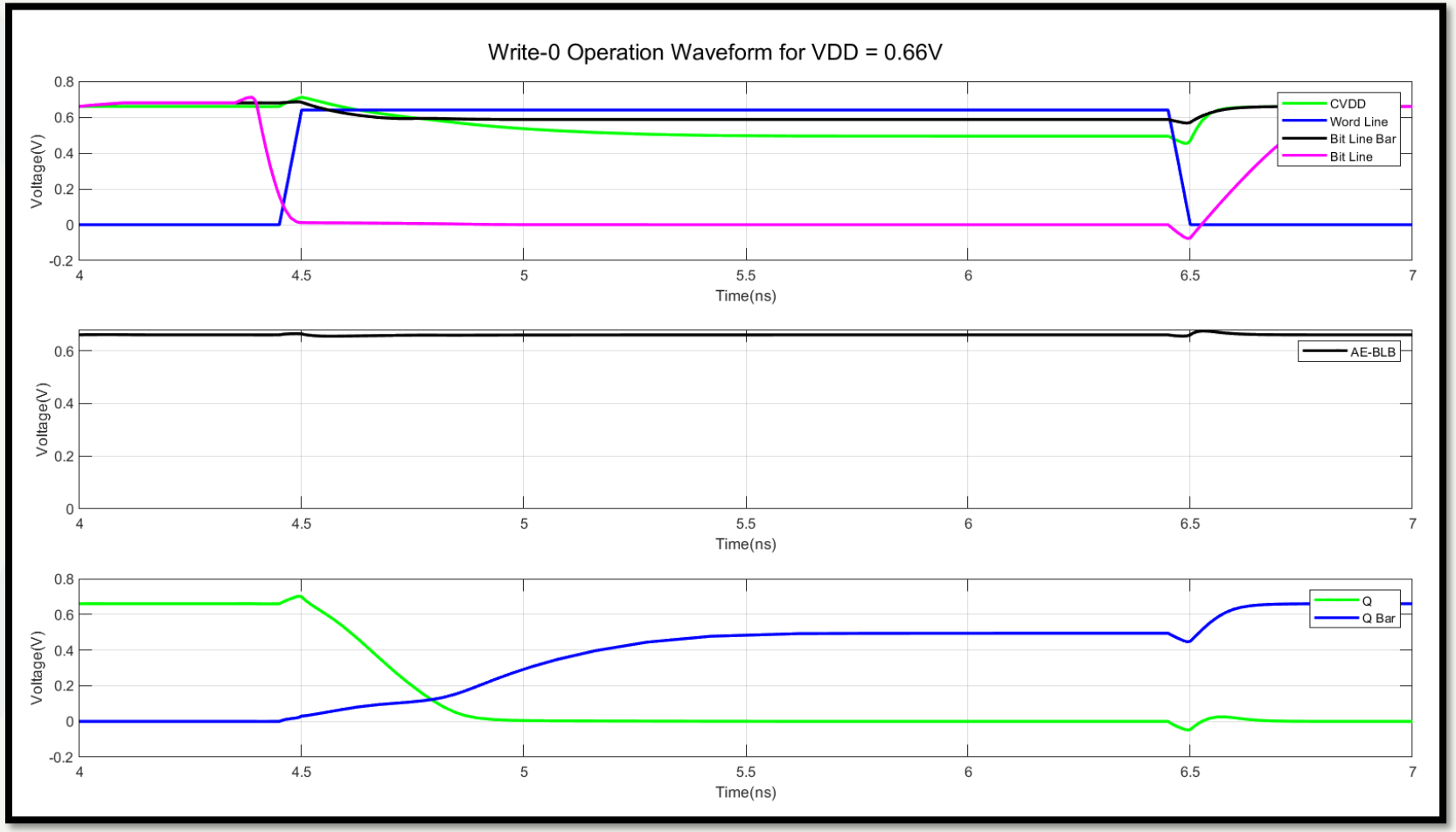
Write-0 Operation Waveform for HIGH-σ SC-BCS cell



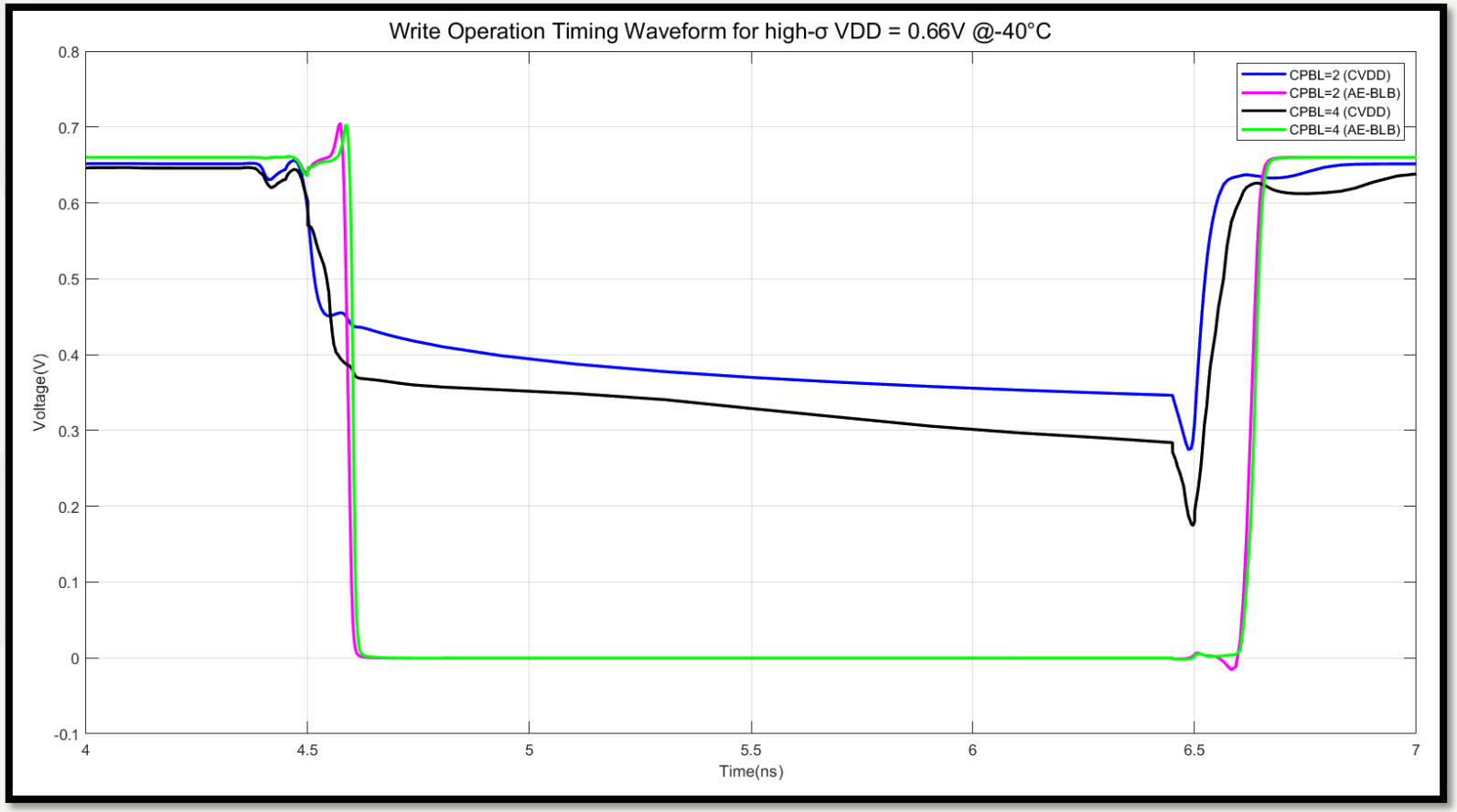
Write-0 Operation Waveform for HIGH-σ SC-BCS cell



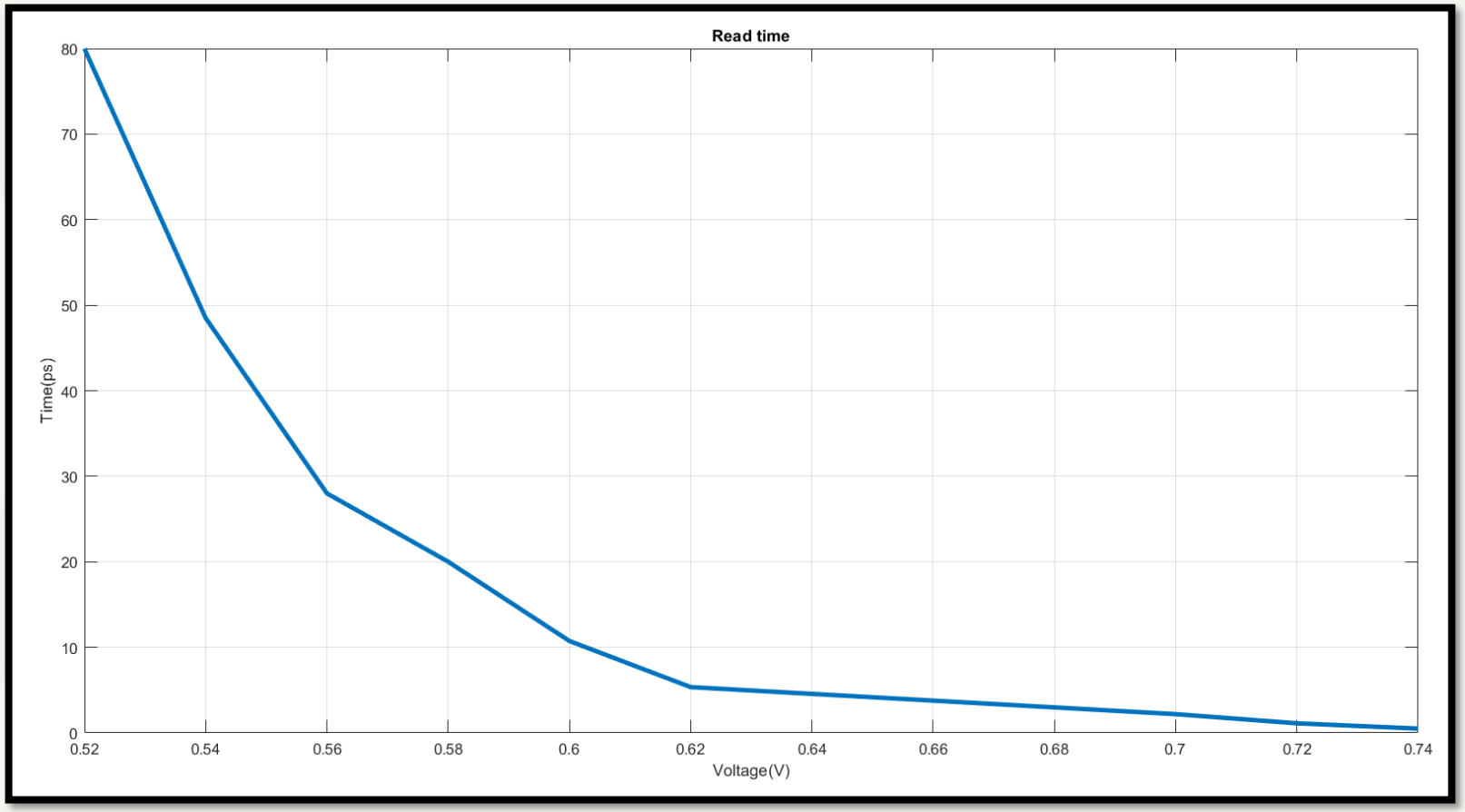
Write-0 Operation Waveform for MEDIUM-σ SC-BCS cell



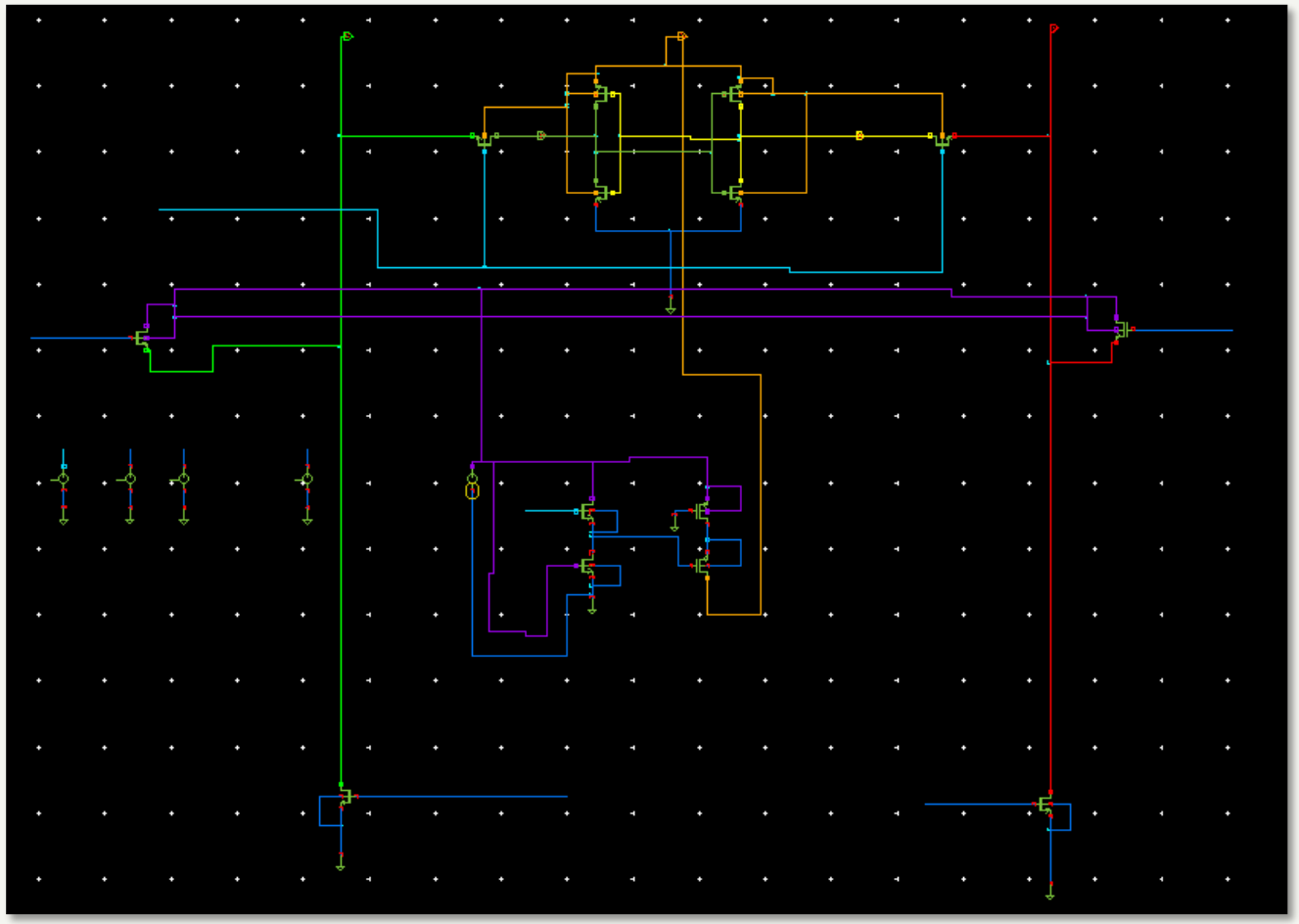
Write operation timing waveform in High-σ SC-BCS cell according to Cell Per Bitline (CPBL)



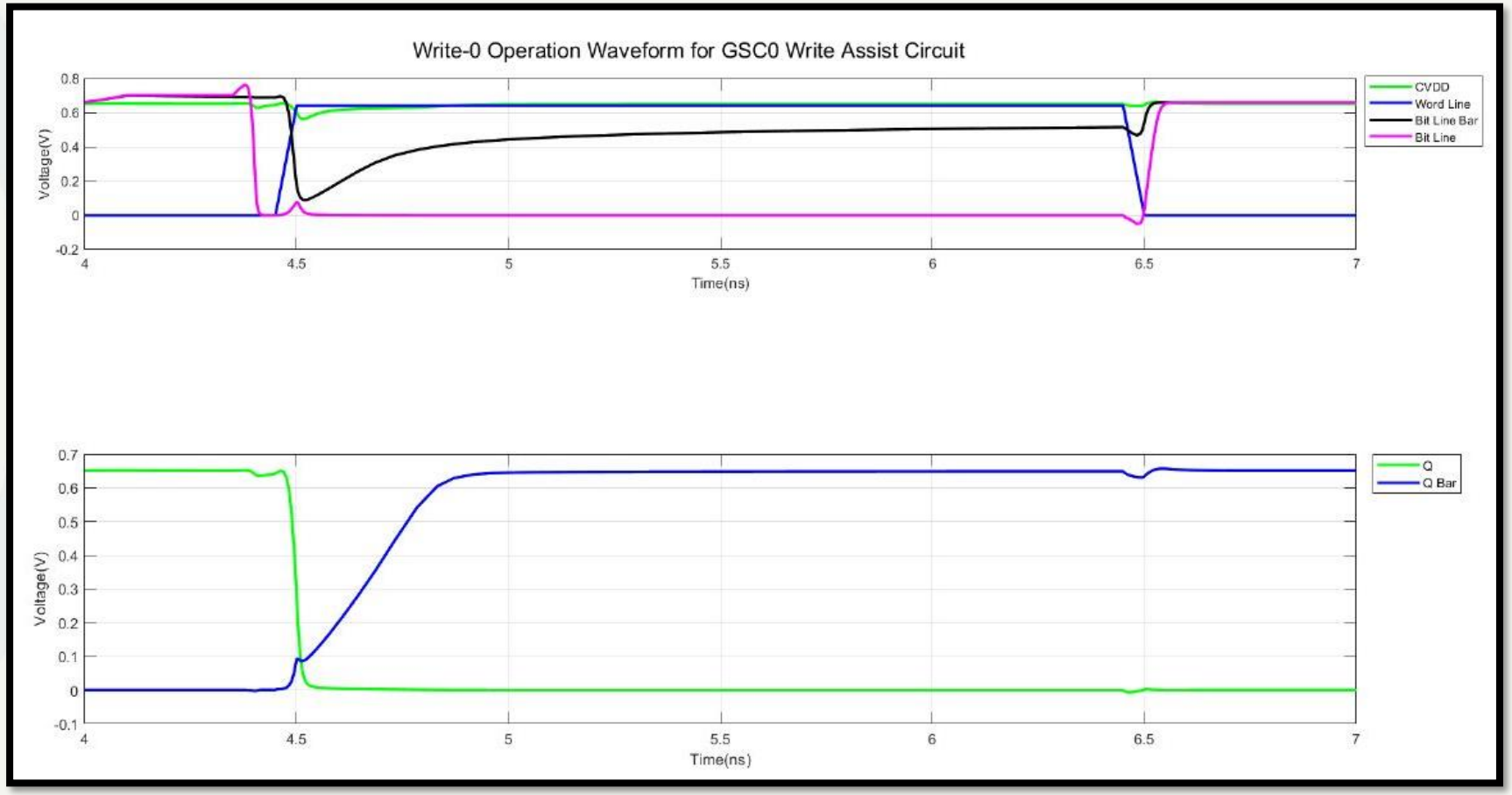
Read Time in High-σ SC-BCS cell



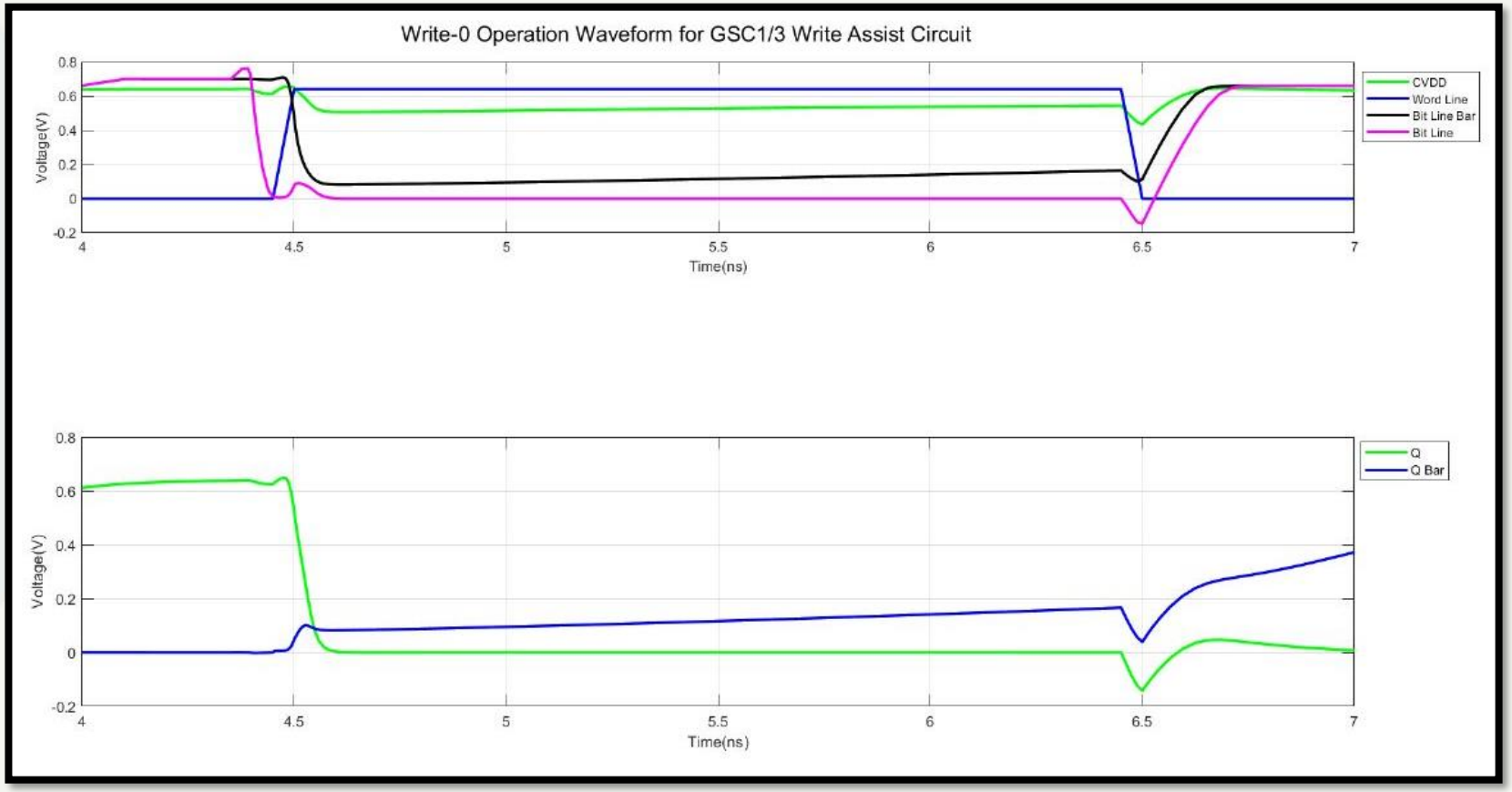
Schematic of GSC SRAM cell



Write-0 Operation Waveform for GSC0 cell



Write-0 Operation Waveform for GSC1/3 cell



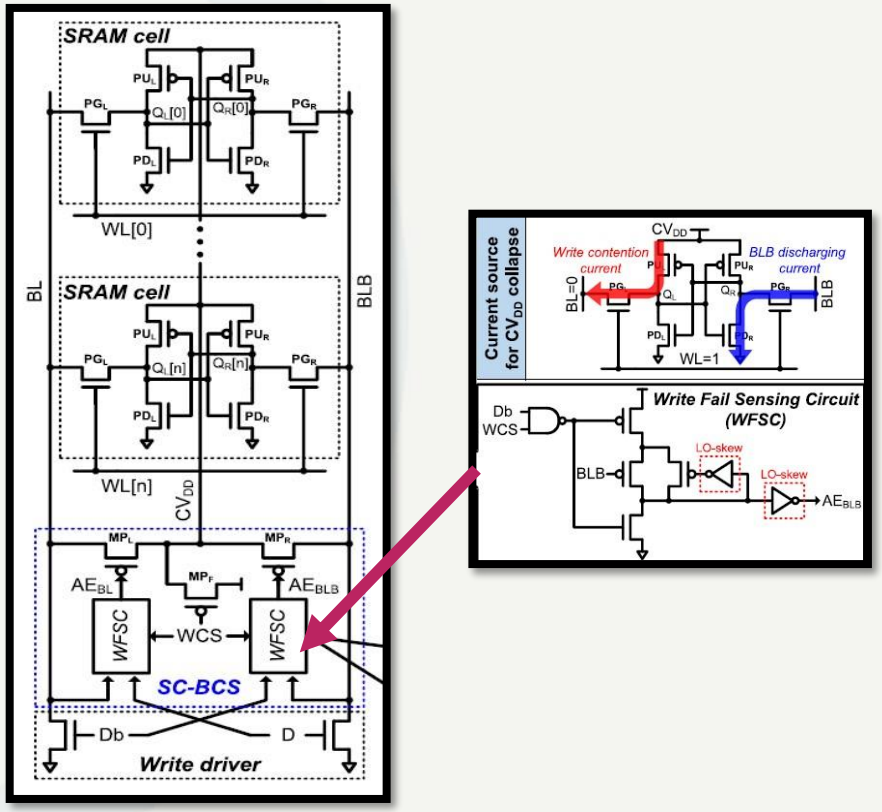
Comparison Table for HIGH-σ SC-BCS cell

	T_{WL}	Write Energy	Q_L Delay
V_{DD} = 0.58 V	2.03 ns	3.347 pJ	34.11 ps
V_{DD} = 0.62 V	1.52 ns	3.252 pJ	26.6 ps
V_{DD} = 0.66 V	1.34 ns	3.55 pJ	22.89 ps

Table for Write Energy Comparison

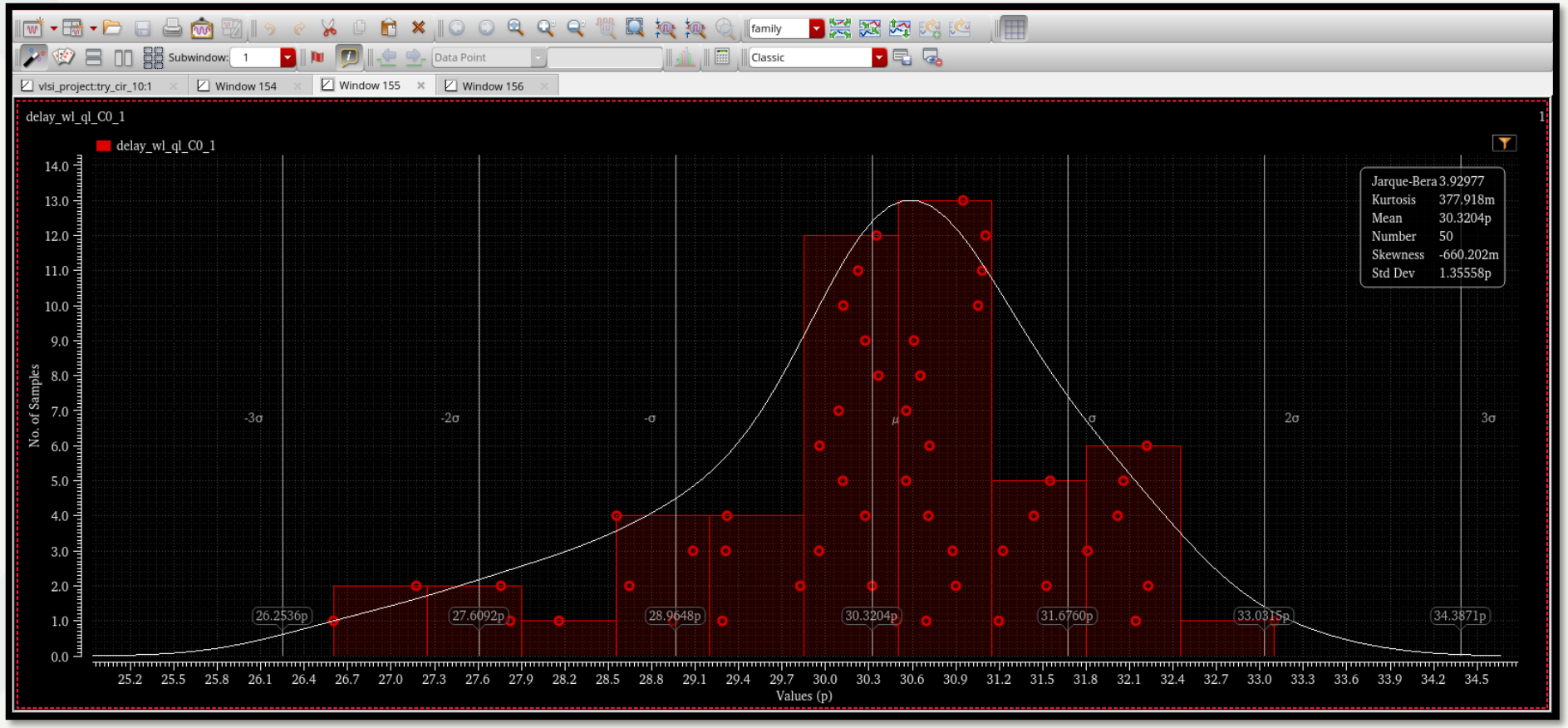
%Age Difference In Write Energy Between SC-BCS And GSC0	%Age Difference In Write Energy Between SC-BCS And GSC1/3
SC-BCS is 42.27% lower	SC-BCS is 88.4% lower

Sizing of Transistors in SC-BCS circuit using Parametric Analysis

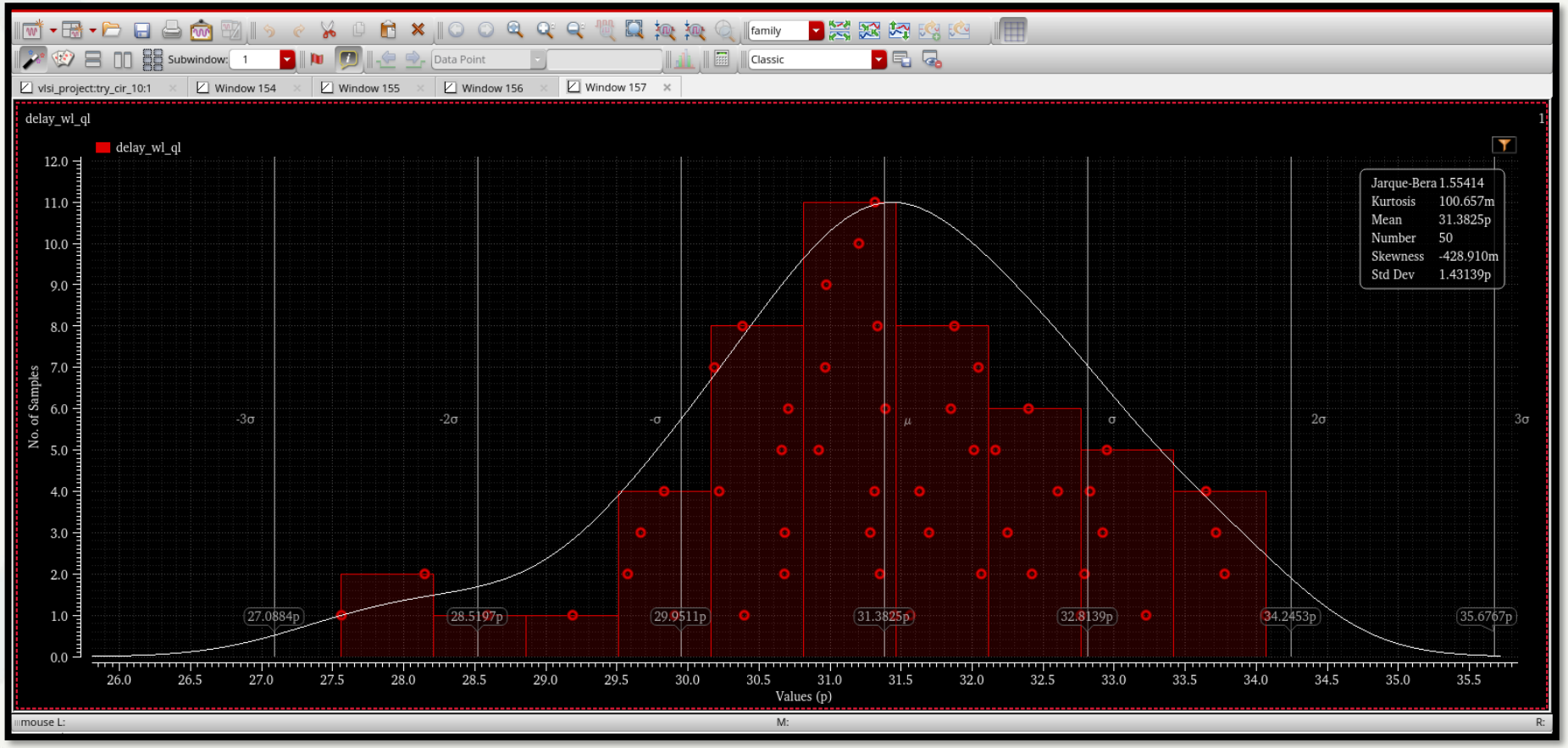


PG_L , PG_R	180 nm
PU_L , PU_R	160 nm
PD_L , PD_R	360 nm
MP_L , MP_R	240 nm
MP_F	240 nm
Db, D Transistors in Write Driver	720 nm
WFSC Nand gate	3:2 using 45 nm Tech node
WFSC LO-SKEW Not gate	1:1.5 using 45 nm Tech node
WFSC $Pmos_{1,2,3}$	360 nm
WFSC Nmos	120 nm

Monte Carlo Simulation for delay at temp(120°C), Vt variations of transistors



Monte Carlo Simulation for delay at nominal temp, Vt variations of transistors



CONCLUSION

1. In our simulations, we achieved better T_{WL} as compared to the proposed design in the paper by 2.48 ns or 64.92%.
2. The overall write energy is 42.27% lower than GSC0 and 88.4% lower than GSC1/3. Hence, the proposed circuit is more energy efficient.

FUTURE WORK

To study and calculate the write ability yield for high and low σ for the write assist circuits.

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