University of Virginia
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ECE 4332: Introduction to VLSI Design
Design Project Assignment

Spring 2024

Issued: 1/23/24
Form Group: 2/1/24
Design Review 1 Due: 2/29/24
Project Proposal Due: 3/14/24
Design Review 2 Due: 4/4/24
Final Report and Presentation Due: 4/23/24

You work on a design team (3 people) for a startup company that specializes in digital IC design. Your team has learned of the opportunity to win a large contract from Portable Instruments Company (PICo) to develop an embedded SRAM design in the FreePDK 45nm technology. You know that PICo is requesting bids for two different types of designs, and your team gets to **select one** of these options to develop. To win the contract, you must design and implement a standalone proof of concept IC to demo your SRAM. You will be competing with teams from other companies to win the contract. Prof. Calhoun is the liaison to your group from PICo.

Design Application 1 – Low power SRAM (Mem1)
The first application for the PICo memory is a microsensor node. PICo requires that this application have as long a lifetime as possible, so the driving constraint centers on energy consumption. The SRAM capacity is 1Mb. The key metric for evaluating your design is:
(1) (Active Energy per Access)^2*Delay*Area*IdlePower.

Design Application 2 – High speed cache (Mem2)
PICo's second request is for a high speed memory that can be used as a local cache in a new mobile communications node. This cache will be powered on only during periods of maximum data transfer, when it will be used for storing data during encryption and compression. For this reason, the key metric focuses more attention on delay:
(1) (Active Energy per Access)*Delay^2*Area*IdlePower.
The total capacity of this cache is 64kb.
Each team will select one design application to pursue

Specification for both designs
For the metrics, the *Energy per Access* is measured with a throughput of one access per cycle and an average of 5 reads for each write operation. The *delay* is worst case access delay. The *area* is a rectangular bounding box around your layout encompassing all physical layers. The *IdlePower* is the total power consumed with the clock stopped.

Word size:	32 bits
Address:	N bits

Inputs:	**ADDR<N-1:0>, Din<31:0>, Read, Write, CLK**
Outputs:	**Dout<31:0>**
Accesses/Cycle:	1 read *or* 1 write access per clock cycle
Access Time:	Mem1: ≤3 cycles ; Mem2: 1 cycle

Note that for Mem1, despite the up-to-3 cycle access time, the memory must support starting a new access every cycle (i.e. the memory supports a throughput of 1 access per cycle). You may choose to pipeline this design if you wish.

You may assume that your design will interface with pads that connect to the outside world (you do not have to design the pads). All **inputs** are valid 0.5 FO4 (inverter fan out of 4 delay) before the rising edge of the clock and hold for 1 FO4 after the rising edge of the clock. You may assume that the input drivers that supply the inputs to your design (including the clock) can drive a maximum of 512λ of gate. The **outputs** of your block must be valid 0.5 FO4 before the rising edge of the clock and must hold for 1 FO4 after the rising edge of the clock to interface properly with the pads.

The two control signals *read* and *write* specify the type of operation that the memory should perform. You may assume that they are mutually exclusive (cannot both be 1 at the same time). If both are low, the memory should execute NOP.

Clocking
Your design must be functional for clock cycle times ranging from infinity (e.g. stopped clock) to the maximum clock period that you specify (*delay*). Because of the stopped clock requirement, all dynamic nodes in your design must have keepers if the nodes could be floating when the clock is stopped. You are responsible for distributing the clock within your own design.

PVT
Memory designs must be robust across process, voltage, and temperature corners. You should demonstrate your design in simulation at V=[1.2V, 1.1V, and 1.0V] and at T=[50C, 27C, and 0C]. There will also be a set of process corners for demonstration that will be built into the model files. Your design must operate properly across these corners.

Special Features
Special features are not required, but they will give your design an advantage in the final comparison with other teams. Examples include: Single-bit correcting ECC, low voltage operation, multiple ports, current sense amps, leakage reduction mode, enhanced margins, redundancy, etc. Consult with Prof. Calhoun about these and other ideas.

Major Requirements and Deliverables
The major deliverable of this project is a functional SRAM that meets the specifications. Your team must first select one of these design applications and then develop the memory IC design. The design should include a top level symbol view, full schematics, and complete layout. You will use the 45nm FreePDK for your design. PICo will evaluate

your design based on functionality across corners, the specified metric, and special features. Use IEEE Explore to get references for your work: http://ieeexplore.ieee.org/

Graded Elements: Your project grade is based on the following five components. All of these components are delivered by the group.

1) Project proposal (1/group) –Turn in a 3-4 page proposal clearly describing the problem that you will address, the approach you plan to take, what you need to design, the novelty (e.g. research component), and the expected outcomes. You must cite relevant references. More details about the proposal will become available later in a separate document from PICo. *NB – Your group must meet with Prof. Calhoun to have your ideas approved prior to submitting the proposal.*

2) Create and update your group's page on the wiki to describe your project and your results (ongoing assignment). Go here to create your group page: http://venividiwiki.ee.virginia.edu/mediawiki/index.php/ClassECE43326332Spring24

3) Design reviews (Design Review 1&2 and Final Design) – Each design review is intended to give you a chance to update the PICo review board of your progress and to get feedback and suggestions. You will turn in copies of simulations and/or schematics to show your progress. You will also turn in a 1 page typed description of your group's progress and of the remaining tasks. The final design review will accompany the Final Report and Final Presentation. You will receive separate assignments related to each design review to give more details. NB – the first design review is before the proposal.

4) Final Report – Turn in a 4 page conference-style paper describing your project. A template will be available to show the format.

5) Final Presentation – Your group will present your results to the class in a conference-style presentation using slides.

Requirement	Goals addressed
Form Teams	3
Design Review 1	1, 2, 3, 4, 5, 6
Proposal due	1, 2, 3, 4, 5, 6 See proposal document
Design Review 2	1, 2, 3, 4, 5, 6
Final project due	1, 2, 3, 4, 5, 6 Paper, presentation, and design review

This is a large design project, so you are encouraged to begin early and work steadily on it throughout the semester. The Professor and TAs are available in office hours for discussion about your project.