Combinational Circuits:

1. Logic Gates:
   - AND Gate
   - OR Gate
   - NOT Gate
   - XOR Gate
   - NAND Gate
   - NOR Gate
   - XNOR Gate

2. Multiplexers (MUX):
   - 2-to-1 MUX
   - 4-to-1 MUX
   - 8-to-1 MUX
   - n-to-1 MUX

3. Demultiplexers (DEMUX):
   - 1-to-2 DEMUX
   - 1-to-4 DEMUX
   - 1-to-8 DEMUX
   - 1-to-n DEMUX

4. Encoders:
   - Binary-to-Decimal Encoder
   - Priority Encoder

5. Decoders:
   - Binary Decoder
   - BCD (Binary Coded Decimal) Decoder

6. Arithmetic Circuits:
   - Half Adder
   - Full Adder
   - Half Subtractor
   - Full Subtractor
   - Multiplexer-based Adder
   - Carry Lookahead Adder
   - Ripple Carry Adder
   - Carry Save Adder
   - Comparator

Sequential Circuits:

1. Latches:
   - SR Latch
   - D Latch
   - JK Latch

2. Flip-Flops:
   - D Flip-Flop
   - T Flip-Flop
   - JK Flip-Flop
   - SR Flip-Flop

3. Counters:
   - Asynchronous Counter
   - Synchronous Counter
   - Up Counter
   - Down Counter
   - Mod-N Counter

4. Shift Registers:
   - Serial In Serial Out (SISO)
   - Serial In Parallel Out (SIPO)
   - Parallel In Serial Out (PISO)
   - Parallel In Parallel Out (PIPO)

5. Memory Units:
   - Random Access Memory (RAM)
   - Read-Only Memory (ROM)
   - Shift Register Memory
   - Register

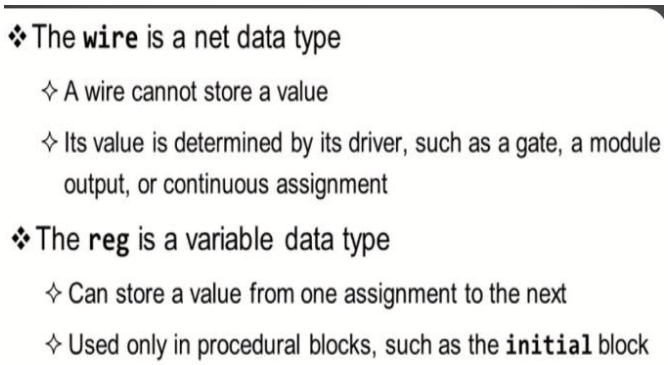
6. State Machines:
   - Mealy Machine
   - Moore Machine

Verilog

Ref: https://youtu.be/ZgGDLuHmpOE?feature=shared

- Install icarus verilog sw
- describe ur hw ckt/ mp/ ff/ mem using verilog (hdl- hardware description language)

more useful than a schematic esp for larger ckts.



- Hello world pgm in verilog

  Steps: create a file with .vl extension, run the cmd to generate output file. Run the output file using vvp cmd.

```
D:\iverilog\asranisanjana_VLcodes>iverilog -o HelloWorld-Output HelloWorld.vl

D:\iverilog\asranisanjana_VLcodes>vvp HelloWorld-Output
Hello, World
HelloWorld.vl:6: $finish called at 0 (1s)

D:\iverilog\asranisanjana_VLcodes>
```

- Now the same task using a testbench,

So create 2 files, one hello_world.vl and one hello_world_tb

Compile the modules using cmds:

- ✓ iverilog -o hello_world-Output hello_world.vl (no need to run this cmd explicitly actually)
- ✓ iverilog -o hello_world_tb-Output hello_world.vl hello_world_tb.vl

3 is the most significant bit (MSB) and 0 is the least significant bit (LSB). So [3:0] represents a 4-bit vector, where a[3] is the MSB and a[0] is the LSB.

In modulename_tb file,
Modulename my_name(parameters)
think of this like calling a function with some specificied parameters
it is also similar to how we create an object in oopl, with name of module here being in place of classname, my_gate is basically my objname and the parameters passed inside parantheses are the initialization parameters.