ASSAF AFRIAT

Digital Design Engineer | RTL | FPGA | SystemVerilog

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SUMMARY

Digital Design Engineer focused on RTL architecture, multi-clock domain systems, and FPGA-based SoC design. Hands-on experience designing, debugging, and integrating SystemVerilog RTL with emphasis on timing behavior, CDC robustness, and interface correctness. Background in control systems engineering contributes strong state-machine design skills, deterministic system thinking, and disciplined debugging of corner cases.

TECHNICAL SKILLS

RTL Design	SystemVerilog, Verilog, FSM Design, Pipelining, Parameterized Modules, Packed Structs
Clock Domains	2-FF/3-FF Synchronizers, Async FIFOs, Gray-Code Pointers, Glitch Guards, Multi-Clock Architectures
Protocols	UART, Handshake Flow Control, DMA, SRAM Interfaces, Register Files
Tools	Xilinx Vivado (Synthesis, Place & Route, BRAM), Cadence Virtuoso, QuestaSim, Python

EDUCATION

Chip Design & Verification Certificate 2026
Google & Reichman Tech School

B.Sc. Electrical & Computer Engineering 2016 - 2021
Ben-Gurion University | VLSI Specialization

RTL DESIGN PROJECTS

UART Image Processing SoC 2026

- Architected full UART communication stack (PHY, MAC, Classifier, Composer) operating at 5.5 Mbaud with 32x oversampling on 176 MHz clock domain
- Implemented robust clock domain crossing between 176 MHz UART and 100 MHz system domains using 2-FF/3-FF synchronizers with registered glitch guards
- Designed async FIFOs with gray-code pointers for TX burst readout; built 7-message protocol with byte-level validation
- Built burst DMA engine with RX/TX sequencers for streaming 65,536 pixels to triple-channel SRAM (R/G/B) frame buffer at full wire speed
- Debugged multi-layer CDC issues including combinational glitch propagation, handshake pulse width, and SRAM pipeline latency hazards

> **Results:** 5.5 Mbaud | 527 KB/s sustained throughput | Pixel-perfect 256x256 image round-trip | 15+ RTL modules

Technologies: SystemVerilog, Xilinx Vivado, SRAM, Async FIFO, CDC, Python

CPM Packet Modifier IP (Verification & Design Analysis) 2026

- Analyzed and verified a 2-stage pipelined packet processing IP with mode-dependent latency across four transformation modes
- Developed RTL-level understanding of pipeline control, backpressure handling, and configuration sequencing
- Built UVM verification environment to validate architectural assumptions and identify three critical RTL bugs

Technologies: SystemVerilog, UVM, QuestaSim, SVA

EXPERIENCE

Control Engineer / Project Manager 2022 - Present

Contel

- Designed state machines for industrial automation using OOP principles; developed modular, reusable code structures for scalable PLC applications
- Led project delivery ensuring timely completion of complex systems; created SCADA interfaces with focus on reliability and user experience

Military: Engineer Corps, IDF (2009-2012)

Languages: Hebrew (Native) | English (Native Level)