ASSAF AFRIAT

Verification Engineer | UVM | SystemVerilog | RTL & Functional Coverage

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SUMMARY

Verification Engineer with hands-on experience building complete UVM-based verification environments. Strong background in SystemVerilog, constrained-random verification, functional coverage, and RAL integration. Experienced in identifying RTL bugs, writing self-checking scoreboards, and driving coverage closure. Background in control systems engineering brings a structured debugging mindset, strong edge-case awareness, and a quality-driven approach to verification.

TECHNICAL SKILLS

Verification	UVM 1.1d, Constrained Random Verification, Coverage-Driven Verification, Self-Checking Scoreboards, Reference Models
UVM Features	RAL (Register Abstraction Layer), Virtual Sequences, Factory Overrides, Callbacks, Functional Coverage
Assertions	SVA (Concurrent Assertions, Cover Properties, Bounded Liveness, Stability Checks)
Tools	QuestaSim (Simulation & Coverage Analysis), Xilinx Vivado, Python, Git

EDUCATION

Chip Design & Verification Certificate 2026
Google & Reichman Tech School

B.Sc. Electrical & Computer Engineering 2016 - 2021
Ben-Gurion University | VLSI Specialization

VERIFICATION PROJECTS

CPM Packet Modifier – UVM Verification Environment 2026

- Built complete UVM testbench with self-checking scoreboard and transaction-level reference model, achieving full functional correctness across 500+ transactions per test run
- Implemented Register Abstraction Layer (RAL) including adapter, predictor, and automated reset sequence verification
- Developed SVA assertions for protocol compliance, including input/output stability and bounded liveness properties
- Designed functional coverage model with mode × opcode cross coverage (64 bins) and an 8-phase virtual sequence driving end-to-end test execution
- Applied UVM factory overrides and callbacks for extensible test infrastructure; developed Python-based test runner with real-time coverage reporting

> **Bugs Found (3 Critical):** COUNT_OUT increment timing | Output stability under backpressure | Configuration race condition

> **Results:** 100% functional coverage | 88.6% code coverage | 4 SVA assertions with zero violations

Technologies: SystemVerilog, UVM, QuestaSim, SVA, RAL, Python

UART SoC – Verification Support 2026

- Developed SystemVerilog testbenches for module-level verification of a multi-clock domain UART communication system
- Built Python-based automation for serial communication testing, focusing on clock-domain behavior, data integrity, and end-to-end verification of UART data paths

Technologies: SystemVerilog, Python, Xilinx Vivado

EXPERIENCE

Control Engineer / Project Manager 2022 - Present

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- Developed state-machine-based control logic with emphasis on corner cases, timing behavior, and failure scenarios
- Defined and executed test procedures to ensure reliable system operation; led projects with a strong focus on quality and correctness

Military: Engineer Corps, IDF (2009–2012)

Languages: Hebrew (Native) | English (Native)