ASSAF AFRIAT

Digital Design & Verification Engineer

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PROFESSIONAL SUMMARY

Digital Design and Verification Engineer with hands-on experience in RTL design, UVM verification, and FPGA implementation. Recently completed Google's Chip Design & Verification program with expertise in SystemVerilog, UVM methodology, and clock domain crossing. Background in control systems engineering brings strong debugging skills, systematic problem-solving, and experience delivering complex projects on schedule.

TECHNICAL SKILLS

HDL & Verification	SystemVerilog, Verilog, UVM, SVA, Constrained Random Verification, Functional Coverage, RAL
Design Expertise	RTL Design, FSM, Clock Domain Crossing, Async FIFOs, Pipelining, UART Protocol, DMA
Tools	QuestaSim, Xilinx Vivado, Cadence Virtuoso, Python, Git
Programming	Python, C, Assembly

EDUCATION & TRAINING

Chip Design & Verification Certificate 2026
Google & Reichman Tech School
Intensive program covering RTL design, UVM verification, and FPGA implementation.

B.Sc. Electrical and Computer Engineering 2016 - 2021
Ben-Gurion University of the Negev
Specialization: Telecommunication and VLSI

CAPSTONE PROJECTS

UART Image Processing SoC - RTL Design 2026

Multi-clock domain UART system for real-time 256x256 image transfer between PC and FPGA.

- Architected full UART stack (PHY, MAC, Classifier) at 5.5 Mbaud with 32x oversampling on 176 MHz clock
- Implemented CDC between 176/100 MHz domains using 2-FF/3-FF synchronizers and async FIFOs
- Designed burst DMA engine for streaming RGB images to triple-channel SRAM at full wire speed
- Achieved pixel-perfect image round-trip with zero data loss on Xilinx FPGA

SystemVerilog, Xilinx Vivado, SRAM, CDC, Python

CPM IP Verification Environment - UVM 2026

Complete UVM verification for configurable packet modifier IP with 4 transformation modes.

- Developed self-checking scoreboard with reference model achieving 100% match rate
- Implemented RAL with adapter, predictor, and automated reset sequence verification
- Created SVA assertions for protocol compliance; identified 3 critical RTL bugs
- Achieved 100% functional coverage using covergroups with mode × opcode cross

SystemVerilog, UVM, QuestaSim, SVA, RAL, Python

EMPLOYMENT EXPERIENCE

Control Engineer / Project Manager 2022 - Present
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- Led system design and project delivery for industrial automation solutions
- Developed PLC applications using OOP principles, state machines, and modular code structures
- Drove process improvements, optimizing workflows and reducing costs

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Military: Engineer Corps, IDF (2009-2012)

Languages: Hebrew (Native), English (Native Level)