ASSAF AFRIAT

Verification Engineer | UVM / SystemVerilog | Constrained-Random & Coverage-Driven Verification

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SUMMARY

Verification Engineer specializing in UVM-based constrained-random environments with strong emphasis on coverage closure, assertion-based verification, and RTL debug. Architected modular UVM infrastructures including RAL, reusable agents, and layered sequence architectures. Proven ability to identify critical RTL bugs through structured root cause analysis and protocol-level debug. Background in PLC-based state machine design reinforces deterministic logic thinking and systematic validation methodology.

TECHNICAL SKILLS

Verification	UVM 1.1d, Constrained Random, Coverage-Driven Verification, Self-Checking Scoreboards, Reference Models
UVM Features	RAL (Register Abstraction Layer), Virtual Sequences, Factory Overrides, Callbacks, Functional Coverage
Assertions	SVA (Concurrent Assertions, Cover Properties, Bounded Liveness, Stability Checks)
RTL & Debug	RTL Reading, Waveform Analysis, Protocol-Level Debug, Multi-Clock / CDC Awareness
Tools	QuestaSim (Simulation, Coverage Analysis), Xilinx Vivado, Python, Git
Methodology	Coverage planning, constrained-random stimulus design, assertion-based verification, root cause analysis

EDUCATION

Chip Design & Verification Certificate 2026
Google & Reichman Tech School

B.Sc. Electrical & Computer Engineering 2016 - 2021
Ben-Gurion University | VLSI Specialization

VERIFICATION PROJECTS

CPM Packet Modifier - UVM Verification Environment 2026

Architected and owned complete UVM environment for 4-mode packet processing IP — ready for tape-out verification flow.

- Architected modular UVM testbench with reusable agents, RAL integration, and layered sequence architecture; self-checking scoreboard and transaction-level reference model; 100% match rate across 500+ transactions per run
- Implemented SVA assertions (input/output stability, bounded liveness); functional coverage with mode × opcode cross (64 bins)
- Designed 8-phase virtual sequence; factory overrides and callbacks for extensible infrastructure; Python GUI test runner
- Verification plan with sign-off criteria and traceable bug tracking; coverage-driven test design achieved functional closure

> **Critical RTL Bugs — Structured Debug Methodology:**
> **1. COUNT_OUT timing:** Root cause: register update misaligned with valid cycle. Reproduced via constrained sequence. Impact: incorrect packet count.
> **2. Output stability under backpressure:** Root cause: valid deasserted before consumer ready. Protocol analysis + stress test. Impact: undefined data sampling.
> **3. Configuration race:** Root cause: reg writes visible before pipeline flush. Directed + random config sequences. Impact: wrong mode on in-flight packets.

> **Results:** 100% functional coverage | 88.6% code coverage | 4 SVA assertions, 0 violations

Technologies: SystemVerilog, UVM, QuestaSim, SVA, RAL, Python

UART SoC - Verification Support 2026

- Verified multi-clock UART SoC data integrity under asynchronous clock domains; identified and resolved CDC synchronization issues via waveform-driven debug
- Created SystemVerilog testbenches and Python automation for serial communication testing

Technologies: SystemVerilog, Python, Xilinx Vivado

EXPERIENCE

System Validation & PLC Control Engineer / Project Manager 2022 - Present

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- Designed PLC-based control logic and finite state machines for industrial automation systems
- Developed HMI interfaces for real-time monitoring, fault handling, and system interaction
- Performed system-level validation including timing analysis, edge-case testing, and failure scenario simulation
- Conducted structured root cause analysis for field failures, improving system reliability and stability
- Defined validation plans and sign-off criteria; delivered multiple automation projects through controlled verification methodology

Military: Engineer Corps, IDF (2009-2012)

Languages: Hebrew (Native) | English (Native Level)