ASSAF AFRIAT

Digital Design Engineer | RTL & Verification | SystemVerilog

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SUMMARY

Digital Design Engineer with hands-on experience in SystemVerilog RTL design, multi-clock domain architectures, and FPGA-based SoC implementation. Strong background in verification using UVM and SVA, enabling robust, verification-aware design and early detection of architectural corner cases. Prior experience in control systems engineering contributes a disciplined, timing-conscious, and failure-oriented debugging mindset.

TECHNICAL SKILLS

RTL Design	SystemVerilog, Verilog, FSM Design, Clock Domain Crossing, Async FIFOs, Pipelining, UART, DMA Engines
Verification	UVM, SVA, Constrained Random Verification, Functional Coverage, RAL
Tools	Xilinx Vivado, QuestaSim, Cadence Virtuoso, Python, Git

EDUCATION

Chip Design & Verification Certificate 2026
Google & Reichman Tech School

B.Sc. Electrical & Computer Engineering 2016 – 2021
Ben-Gurion University | VLSI Specialization

PROJECTS

UART Image Processing SoC – RTL Design 2026

- Designed complete UART-based image processing SoC including PHY, MAC, DMA engine, and SRAM-backed frame buffer
- Implemented robust CDC between 176 MHz UART and 100 MHz system domains using synchronizers and async FIFOs with gray-code pointers
- Developed burst DMA engine enabling reliable streaming of 256×256 RGB images with pixel-perfect end-to-end integrity
- Debugged timing and CDC issues including glitch propagation, handshake alignment, and SRAM pipeline latency

Technologies: SystemVerilog, Xilinx Vivado, SRAM, CDC, Python

CPM Packet Modifier – Design-Aware Verification 2026

- Analyzed RTL microarchitecture including pipelined data path, control logic, and mode-dependent latency behavior
- Built UVM-based verification environment to validate architectural assumptions and uncover three critical RTL bugs related to timing and backpressure
- Developed SVA assertions for protocol compliance and output stability, achieving full functional coverage

Technologies: SystemVerilog, UVM, SVA, QuestaSim

EXPERIENCE

Control Engineer / Project Manager 2022 – Present

Contel

- Designed deterministic state-machine-based control logic for real-time systems with strict timing and reliability requirements
- Led end-to-end project delivery, emphasizing structured debugging, failure-mode analysis, and system robustness

Military: Engineer Corps, IDF (2009–2012)

Languages: Hebrew (Native) | English (Native)