ASSAF AFRIAT

RTL Design Engineer | ASIC / FPGA | SystemVerilog

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SUMMARY

RTL Design Engineer specializing in SystemVerilog-based digital design, multi-clock domain architectures, and FPGA/ASIC-ready RTL. Hands-on experience designing communication pipelines, DMA engines, FIFOs, and control-oriented state machines with strong emphasis on timing behavior, determinism, and CDC correctness. Proven ability to take designs from architectural definition through implementation, debug, and system-level integration.

TECHNICAL SKILLS

RTL Design	SystemVerilog RTL, Verilog, FSM Design, Pipelining, Parameterized Modules, Reset Strategy, Timing-Aware & Synthesis-Friendly Coding
Clock Domains	2-FF / 3-FF Synchronizers, Async FIFOs, Gray-Code Pointers, Pulse Stretching, Glitch Mitigation, Multi-Clock Architectures
Interfaces	UART, DMA Engines, SRAM Interfaces, Register Files, Handshake Flow Control
Tools	Xilinx Vivado (Synthesis, P&R, BRAM), QuestaSim, Python, Git

EDUCATION

Chip Design & Verification Certificate 2026
Google & Reichman Tech School

B.Sc. Electrical & Computer Engineering 2016 – 2021
Ben-Gurion University | VLSI Specialization

RTL DESIGN PROJECTS

UART Image Processing SoC 2026

- Architected and implemented a complete UART-based image processing SoC, including PHY, MAC, DMA engine, and SRAM-backed frame buffer
- Designed multi-clock domain architecture between 176 MHz UART domain and 100 MHz system domain using synchronizers and async FIFOs
- Implemented burst-based DMA sequencers enabling sustained high-throughput data movement across clock domains
- Resolved timing and CDC hazards including pulse-width issues, combinational glitch propagation, and pipeline latency alignment

> **Results:** 5.5 Mbaud | 527 KB/s sustained throughput | Pixel-perfect 256×256 image round-trip | 15+ RTL modules

Technologies: SystemVerilog, Xilinx Vivado, Async FIFO, CDC, SRAM, Python

CPM Packet Modifier IP – Microarchitecture Analysis 2026

- Analyzed RTL microarchitecture including pipeline staging, control flow, and latency behavior across multiple operational modes
- Identified architectural corner cases related to backpressure, configuration sequencing, and output stability

Technologies: SystemVerilog, RTL Analysis, SVA

EXPERIENCE

Control Engineer / Project Manager 2022 – Present

Contel

- Designed deterministic state-machine-based control logic for real-time industrial systems with strict timing requirements
- Led end-to-end delivery of complex systems, emphasizing reliability, failure-mode analysis, and structured debugging

Military: Engineer Corps, IDF (2009–2012)

Languages: Hebrew (Native) | English (Native)