CPM Verification Sign-Off Document

Project: Configurable Packet Modifier (CPM) Verification

Version: 1.1

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Date: 2026-02-15

Status: SIGNED OFF

1. Executive Summary

The CPM (Configurable Packet Modifier) UVM verification environment has been completed and all closure criteria have been met. The design (RTL v1.1) has been verified to function correctly across all 4 operation modes, with comprehensive functional coverage achieved. All previously reported DUT bugs have been fixed and verified.

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2. Closure Criteria Checklist

2.1 Mandatory Requirements

#	Criterion	Status	Evidence
1	All tests pass (no runtime hangs)	**PASS**	All tests complete successfully
2	Scoreboard reports 0 mismatches	**PASS**	485 matched, 0 mismatched
3	All assertions pass (no failures)	**PASS**	4/4 assertions (100%) - 0 violations
4	Functional coverage targets achieved	**PASS**	See coverage section
5	RAL reset sequence passes cleanly	**PASS**	CpmRalResetTest PASS
6	End-of-test invariants checked	**PASS**	Counter invariant verified via RAL
7	UVM_ERROR count = 0	**PASS**	0 errors in simulation
8	Callback mechanism demonstrated	**PASS**	CpmPacketStatsCb tracks 505 packets

2.2 UVM Mechanisms Demonstrated

Mechanism	Requirement	Status	Implementation
RAL	Mandatory	**Implemented**	CpmRegModel, CpmRegAdapter, uvm_reg_predictor
Virtual Sequence	Mandatory	**Implemented**	CpmTopVirtualSeq with full 8-step flow
Factory Override	Mandatory	**Implemented**	CpmBaseTrafficSeq → CpmCoverageTrafficSeq
Callbacks	Mandatory	**Implemented**	CpmPacketStatsCb with real statistics tracking
Functional Coverage	Mandatory	**Implemented**	CpmPacketCoverage, CpmRegCoverage
SVA Assertions	Mandatory	**Implemented**	4 assertions + 4 cover properties in CpmStreamIf.sv

3. Test Results

3.1 Test Execution Summary

Test	Execution Time	Result	Errors	Warnings
CpmSmokeTest	~1 sec	**PASS**	0	0
CpmMainTest	~2 sec	**PASS**	0	1 (expected)
CpmRalResetTest	~1 sec	**PASS**	0	0

3.2 Scoreboard Results (CpmMainTest - RTL v1.1)

Metric	Value
Packets Input	505
Packets Matched	485
Packets Dropped (intentional)	20
Packets Mismatched	**0**
Match Rate	**100%**

3.3 Callback Statistics (NEW in v1.1)

Metric	Value
Total Packets Tracked	505
Opcodes Exercised	16/16 (100%)
Payload Range	0x0000 - 0xFFFF

4. Coverage Results

4.1 Functional Coverage (Mandatory Targets)

Coverpoint	Target	Achieved	Status
MODE	100%	**100.00%**	**MET**
OPCODE	90%	**100.00%**	**MET**
MODE × OPCODE	80%	**100.00%**	**MET**
Drop bin	Hit once	**50%**	**MET**
Stall bin	Hit once	**50%**	**MET**

4.2 Covergroup Summary

Covergroup	Coverage	Status
cg_packet	100.00%	**MET**
cg_register	75.00%	**MET**

4.3 Code Coverage (DUT)

Metric	Coverage
Statements	100.00%
Branches	95.55%
Expressions	100.00%
Conditions	88.88%
Toggles	58.62%
Total DUT	**88.61%**

4.4 Assertion Coverage

Metric	Result
Total Assertions	4
Passed	4
Failed	0
Cover Properties	4
Pass Rate	**100%**

5. Feature Verification

5.1 Operation Modes

Mode	Transformation	Latency	Verified
PASS (0)	payload unchanged	0 cycles	**Yes**
XOR (1)	payload ^ mask	1 cycle	**Yes**
ADD (2)	payload + constant	2 cycles	**Yes**
ROT (3)	rotate left by 4	1 cycle	**Yes**

5.2 Registers

Register	Address	Reset Value	Verified
CTRL	0x00	0x00000000	**Yes**
MODE	0x04	0x00000000	**Yes**
PARAMS	0x08	0x00000000	**Yes**
DROP_CFG	0x0C	0x00000000	**Yes**
STATUS	0x10	0x00000000	**Yes**
COUNT_IN	0x14	0x00000000	**Yes**
COUNT_OUT	0x18	0x00000000	**Yes**
DROPPED_COUNT	0x1C	0x00000000	**Yes**

5.3 Protocol Properties

Property	Status
Input stability under stall	**Verified (0 violations)**
Output stability under stall	**Verified (0 violations - RTL v1.1 fixed)**
Bounded liveness	**Verified (0 violations - drop awareness)**
Counter invariant	**Verified (RTL v1.1 fixed)**

6. Bug Summary

6.1 DUT Bugs (RTL v1.1)

Bug ID	Description	Severity	Status
DUT-001	COUNT_OUT over-count	High	**FIXED**
DUT-002	Output stability violation	High	**FIXED**
DUT-003	ROT_AMT not configurable	Medium	**Resolved (spec clarified)**

6.2 Testbench Bugs

Bug ID	Description	Severity	Status
TB-001	VIF config_db collision	Critical	**Closed**
TB-002	Reset wait race	High	**Closed**
TB-003	Zero-time loop	High	**Closed**
TB-004	Ref model config stale	Medium	**Closed**
TB-005	FIFO ordering assumption	Medium	**Closed**
TB-006	RAL model not built	Critical	**Closed**

Total Open Bugs: 0

7. Spec Compliance (v1.1)

7.1 Resolved Items

Item	Status	Notes
ROT_AMT value	**Resolved**	Spec v1.1 confirms fixed at 4 bits
Counter invariant timing	**Resolved**	STATUS.BUSY defines when invariant holds
SOFT_RST scope	**Resolved**	"clears counters and internal state"

7.2 Resolved Spec Ambiguities (v1.0 → v1.1)

Item	Original Concern	Resolution
Ordering contradiction	Different latencies vs "no reordering"	**Resolved - RTL maintains FIFO ordering regardless of mode latency**
Counter overflow	Undefined 32-bit wrap behavior	**Resolved - RTL uses standard wrap-around (implementation-defined per spec)**
ENABLE deassertion	In-flight packet handling	**Resolved - RTL flushes pipeline when ENABLE deasserted (implementation-defined)**
in_ready when disabled	Value when ENABLE=0	**Resolved - RTL correctly deasserts in_ready when ENABLE=0**

All spec ambiguities from v1.0 have been resolved.

8. Deliverables Checklist

Deliverable	Status
UVM Testbench Source Code	**Complete**
SVA Assertions	**Complete**
RAL Code	**Complete**
Verification Plan	**Complete**
Coverage Report	**Complete**
Test Results	**Complete**
Bug Tracker	**Complete**
Documentation	**Complete**
Callback Implementation	**Complete**

9. Sign-Off

9.1 Verification Engineer

Name	Role	Date	Signature
Assaf Afriat	Verification Engineer	2026-02-07	**Approved**

9.2 Approval

This document confirms that the CPM verification environment meets all mandatory closure criteria as defined in the CPM Final Project Verification Requirements and Deliverables document.

Verification Status: COMPLETE

RTL Version: v1.1 (all bugs fixed)

Spec Version: v1.1

Document End

Last Updated: 2026-02-15