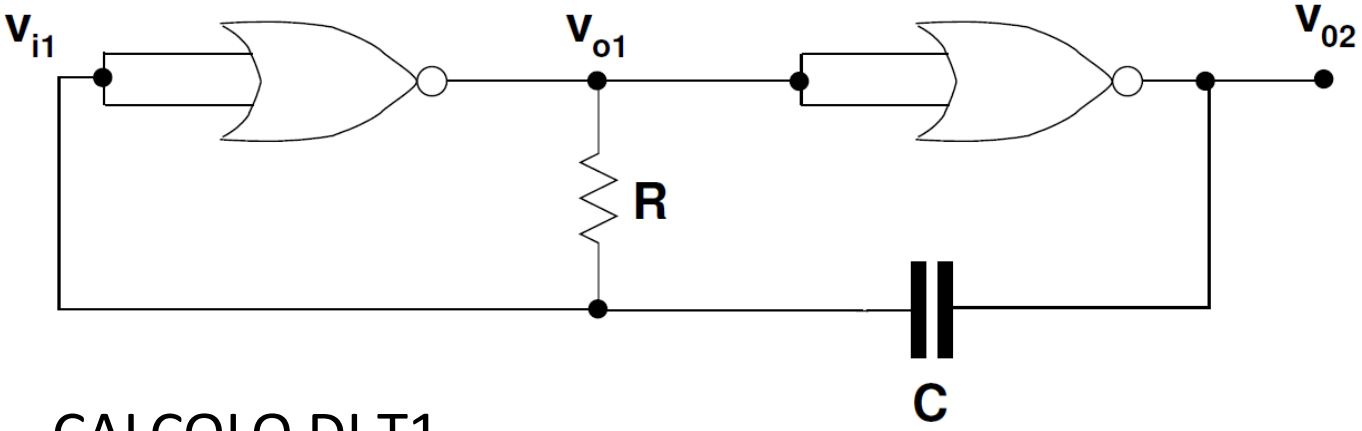
Elettronica Digitale
A.A. 2020-2021

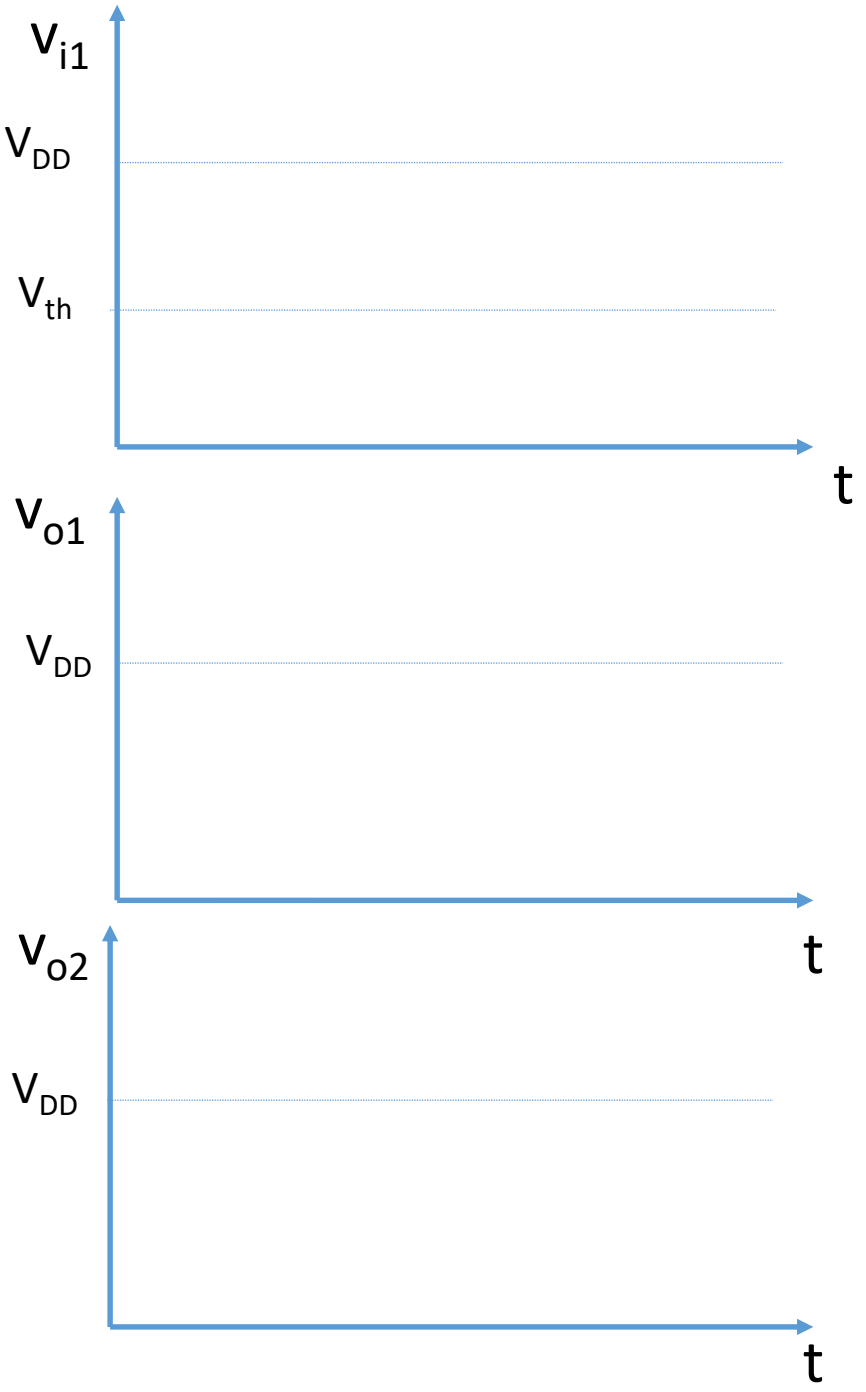
Lezione 20/05/2021

Multivibratore astabile a porte logiche CMOS

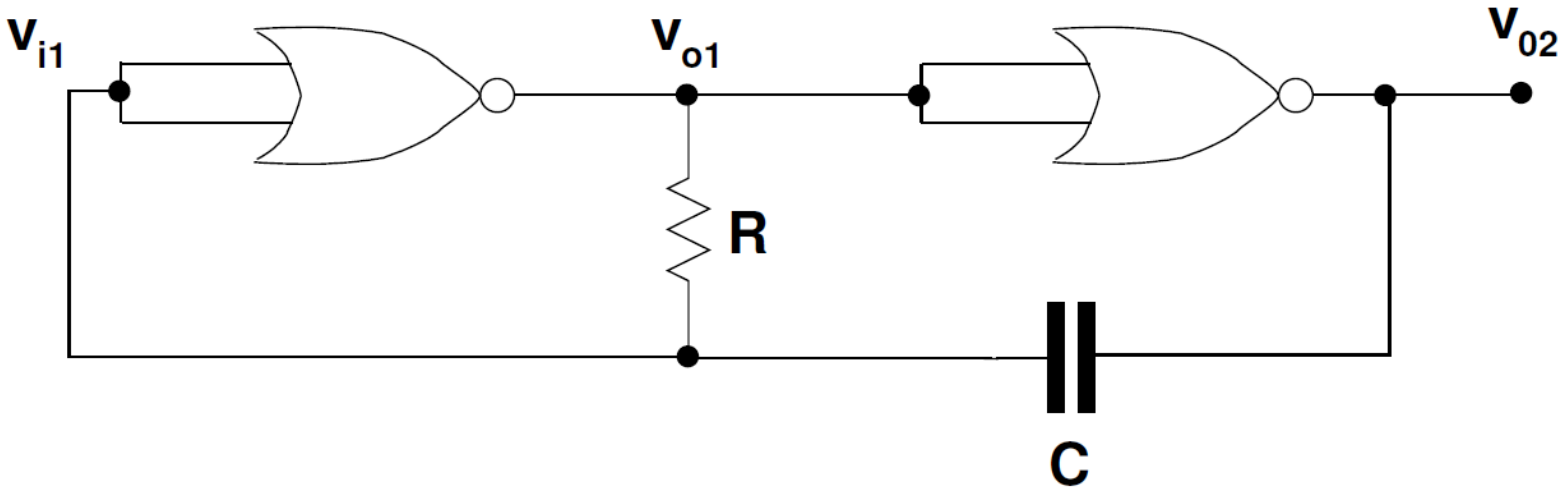


CALCOLO DI T1

$$T = \tau \ln\left(\frac{V_i - V_f}{V_{com} - V_f}\right)$$



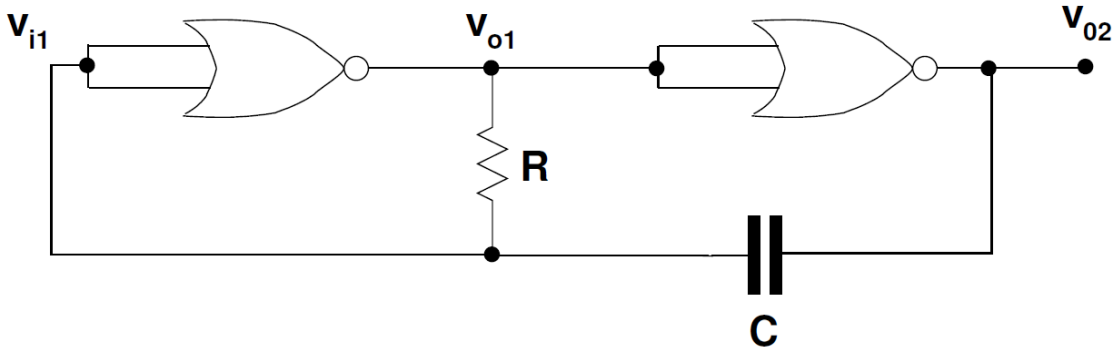
Multivibratore astabile a porte logiche CMOS

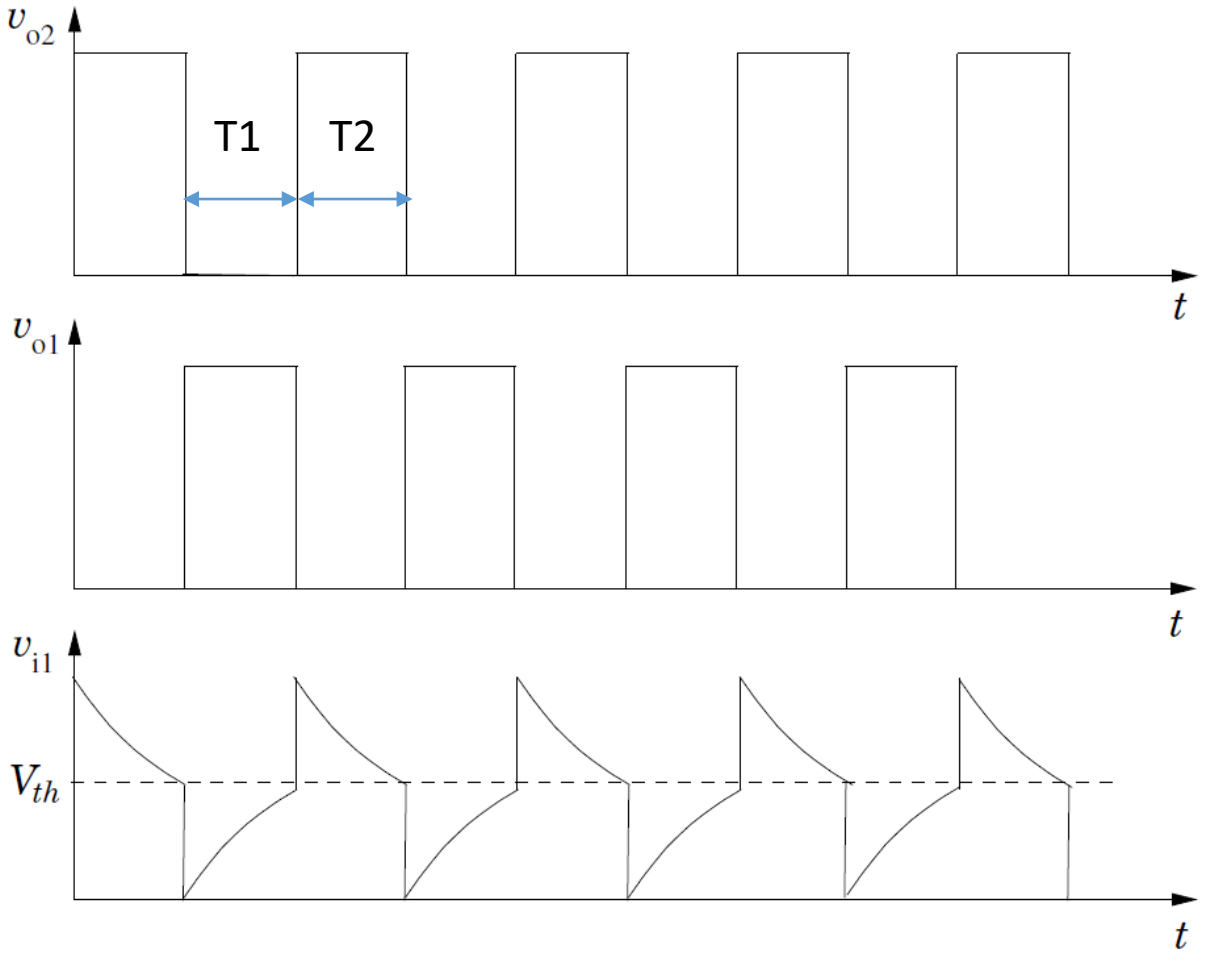


CALCOLO DI T2

$$T = \tau \ln\left(\frac{V_i - V_f}{V_{com} - V_f}\right)$$

Multivibratore astabile a porte logiche CMOS



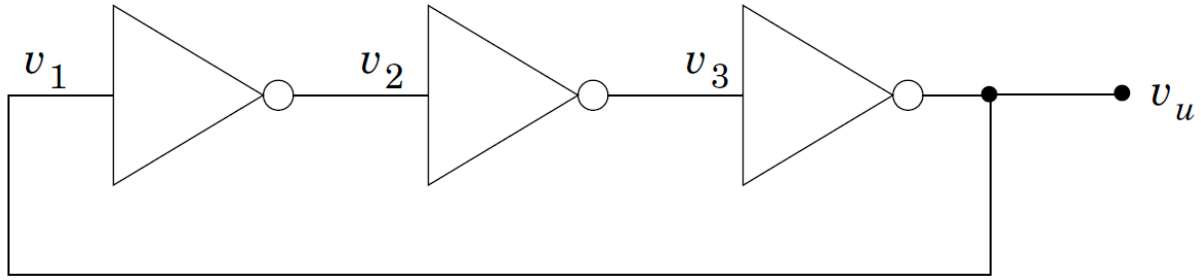


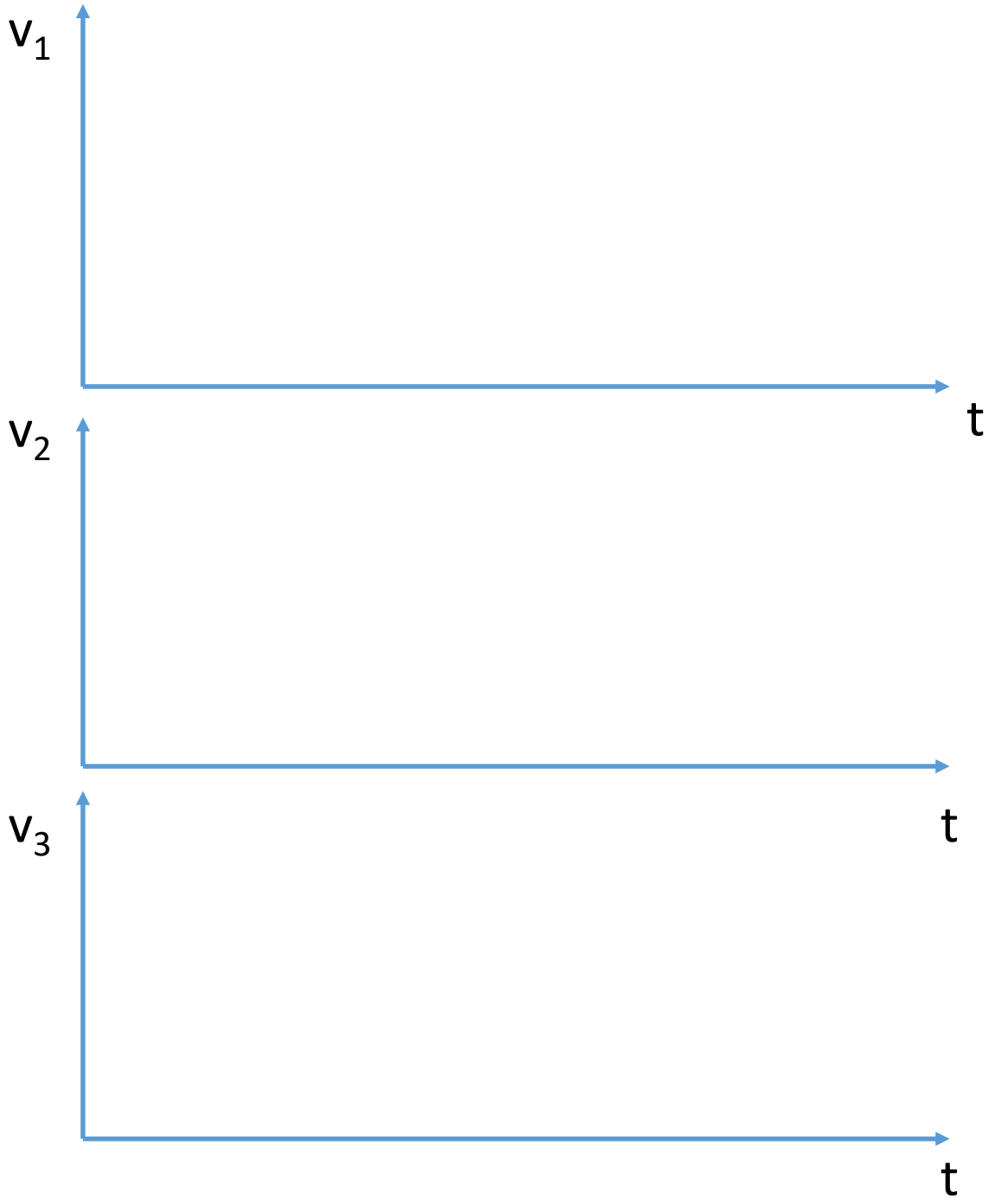
$$T_1 = RC \ln\left(\frac{V_{DD}}{V_{DD} - V_{th}}\right)$$

$$T_2 = RC \ln\left(\frac{V_{DD}}{V_{th}}\right)$$

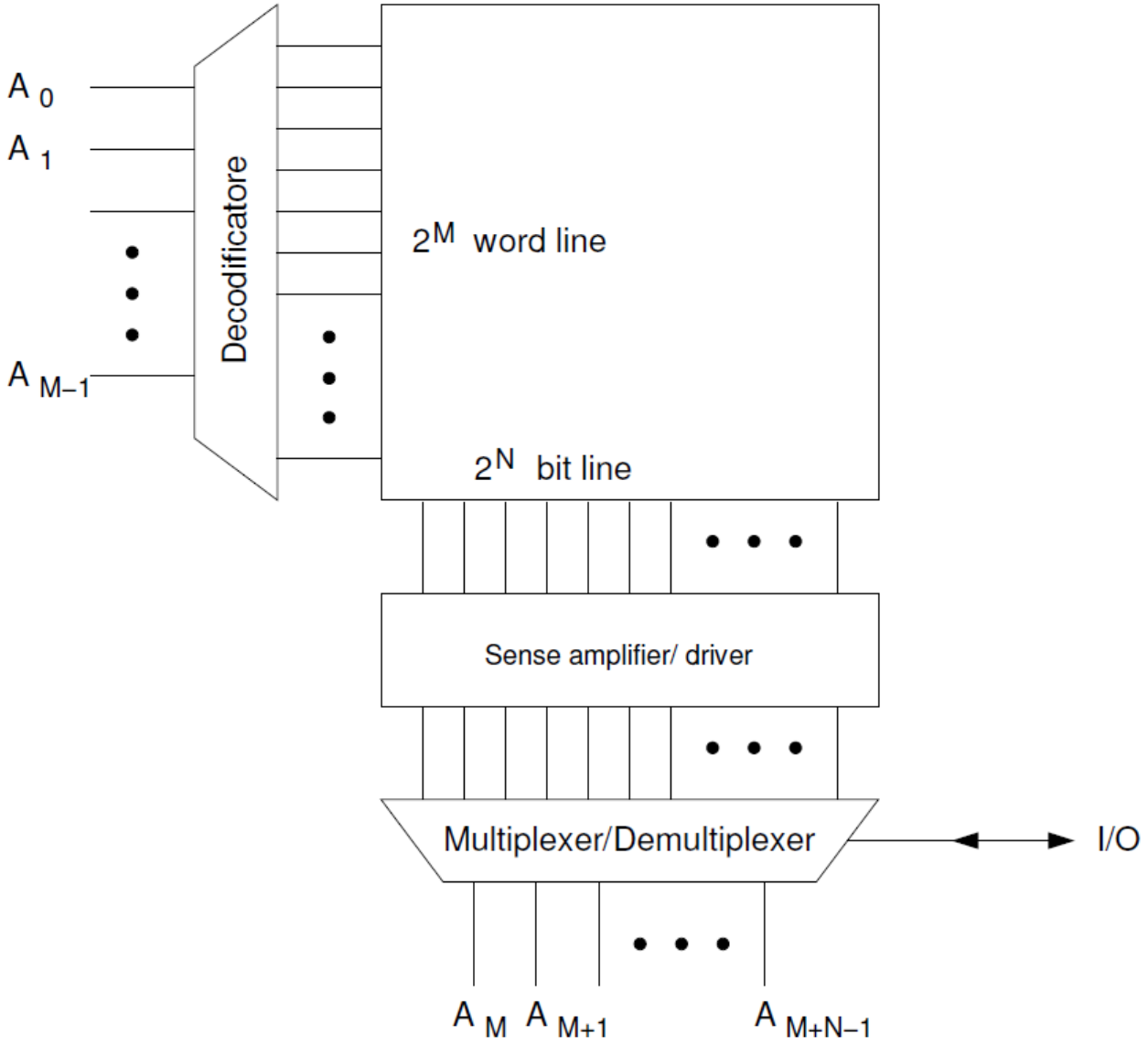
$$T_1 = RC\left[\ln\left(\frac{V_{DD}}{V_{DD} - V_{th}}\frac{V_{DD}}{V_{th}}\right)\right] = \left(\text{se } V_{th} = \frac{V_{DD}}{2}\right) = RC\ln(4)$$

Oscillatore ad anello

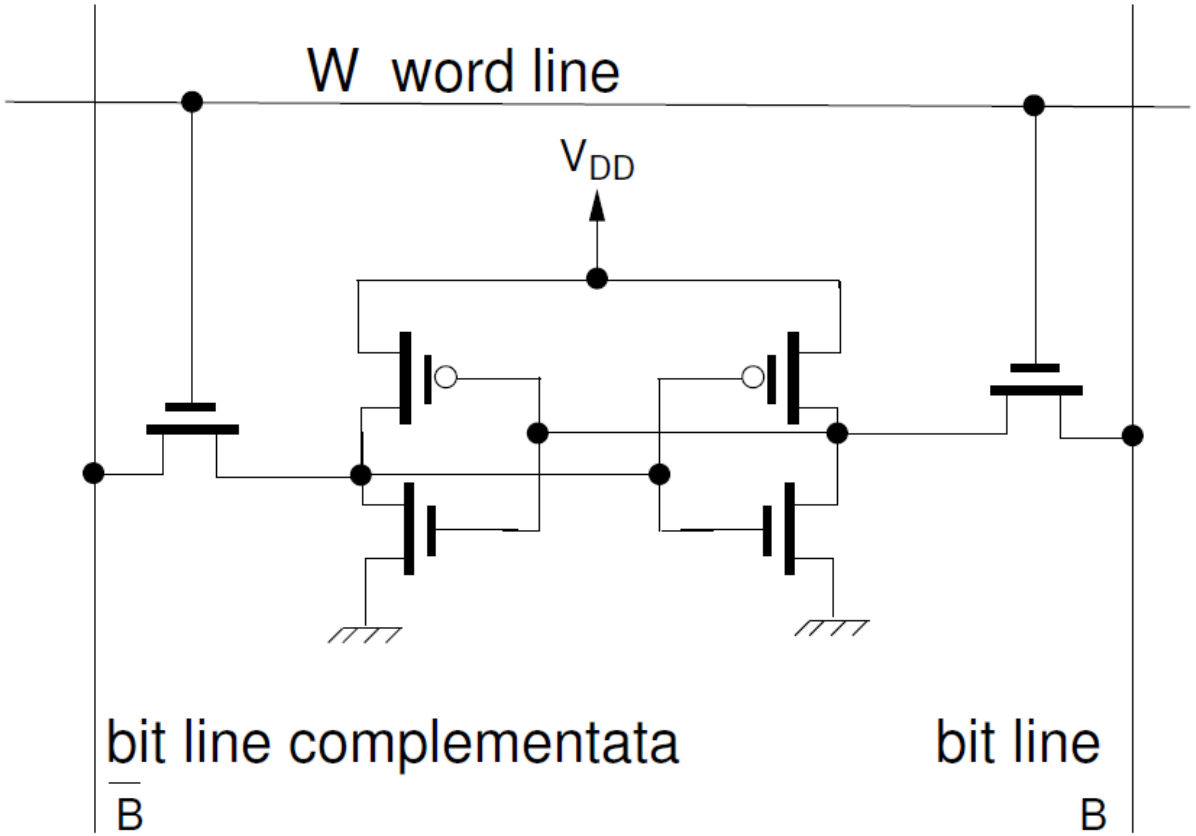




Architettura delle memorie

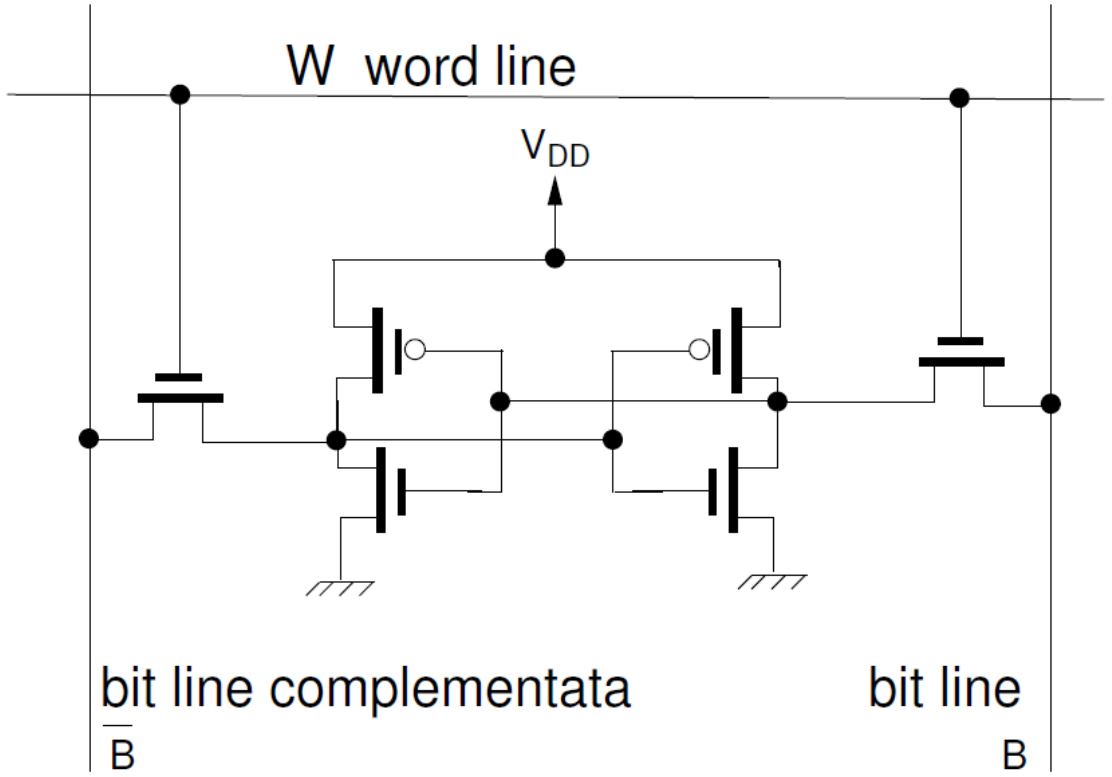


RAM statiche (SRAM)



SCRITTURA

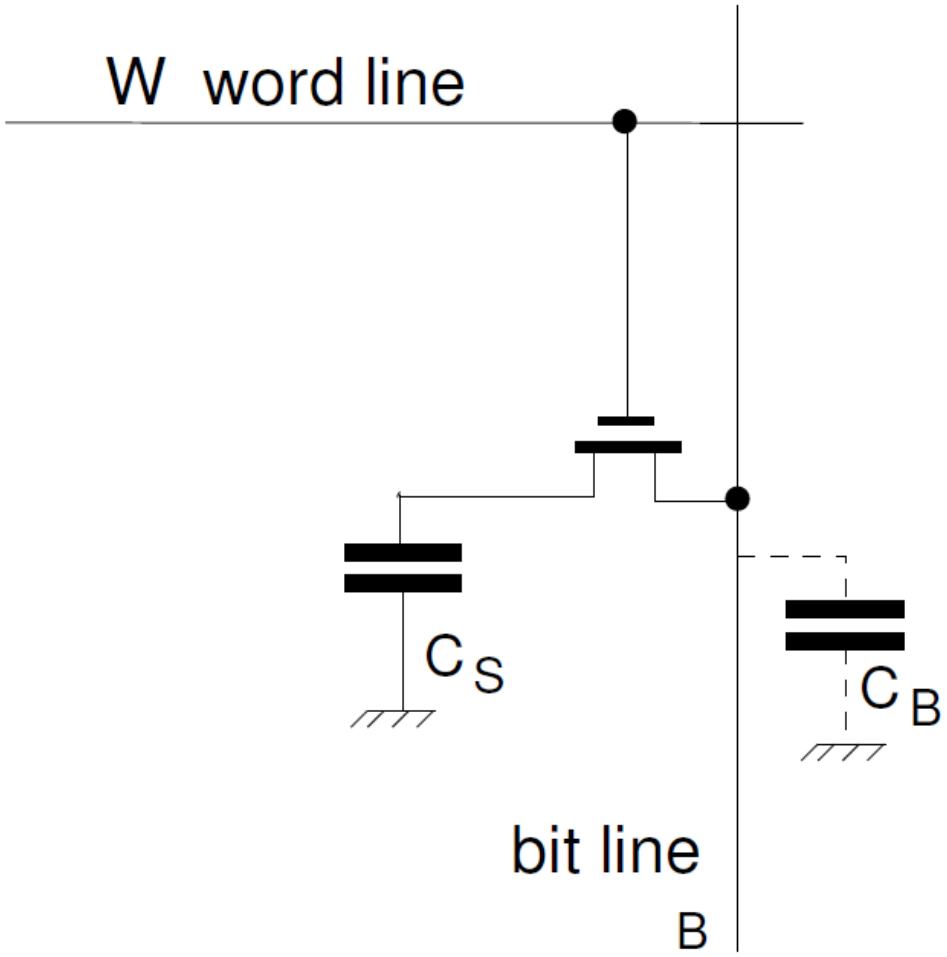
RAM statiche (SRAM)



LETTURA

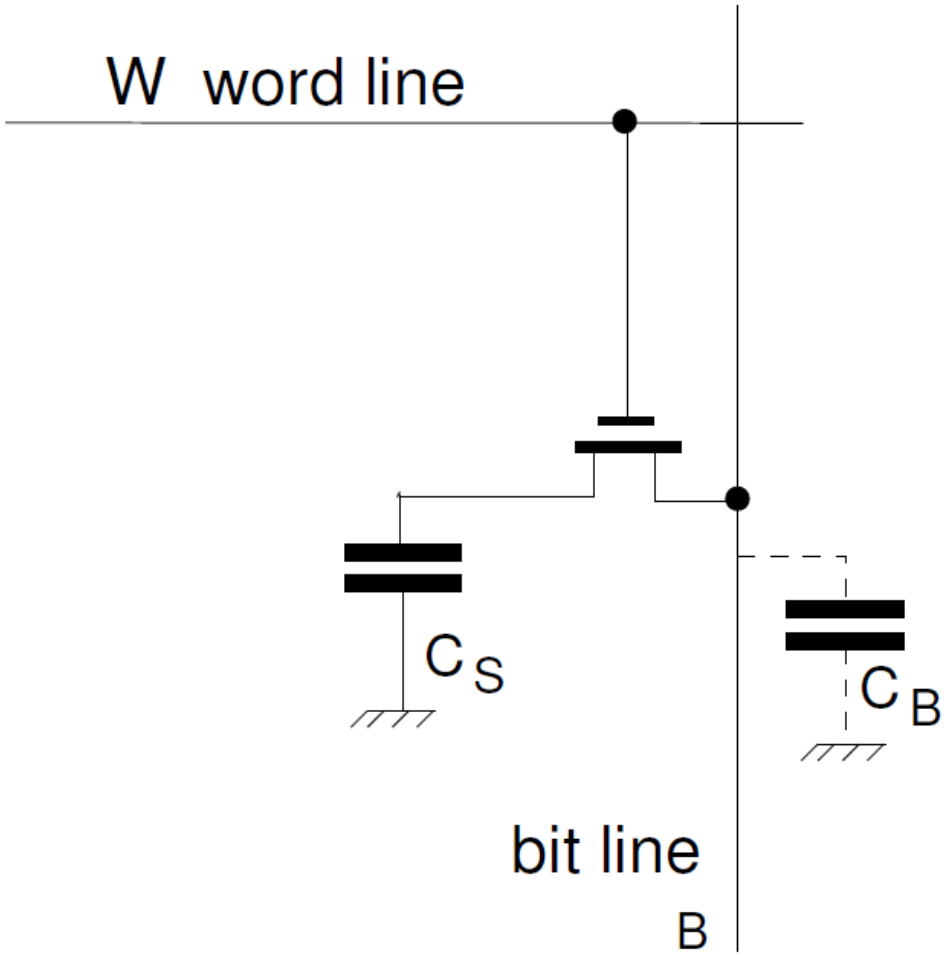
RAM dinamiche (DRAM)

SCRITTURA

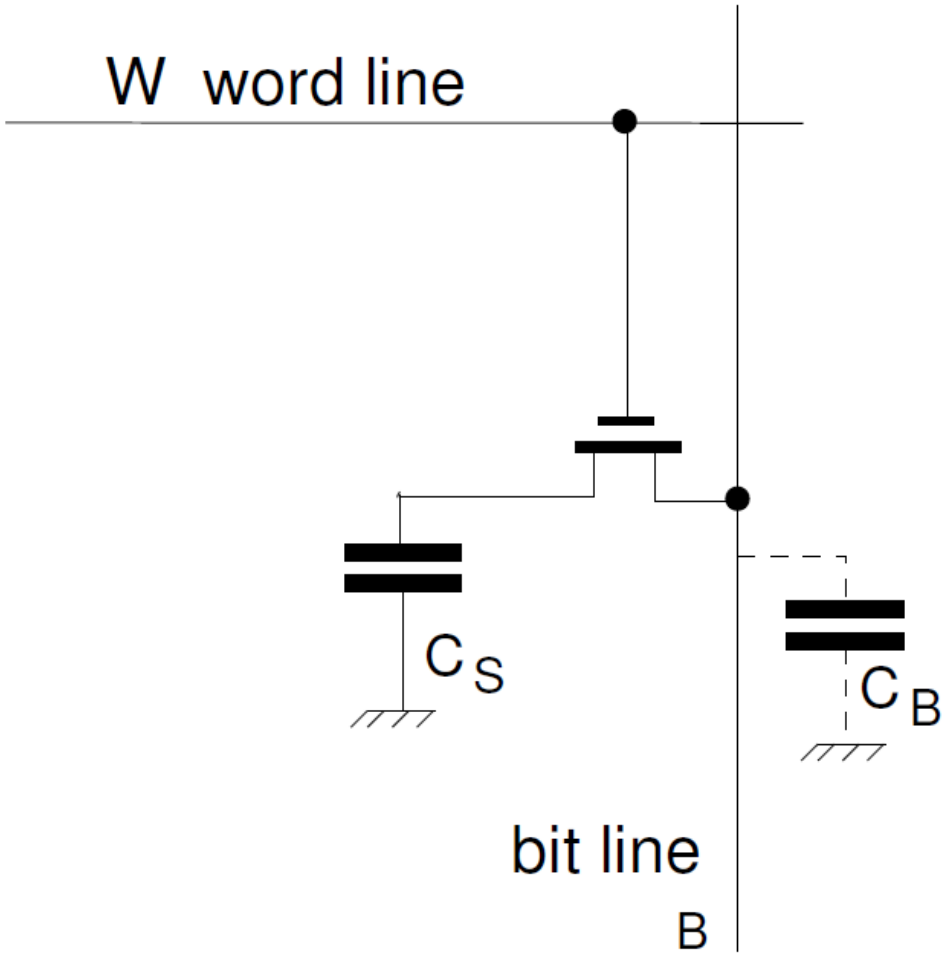


RAM dinamiche (DRAM)

LETTURA



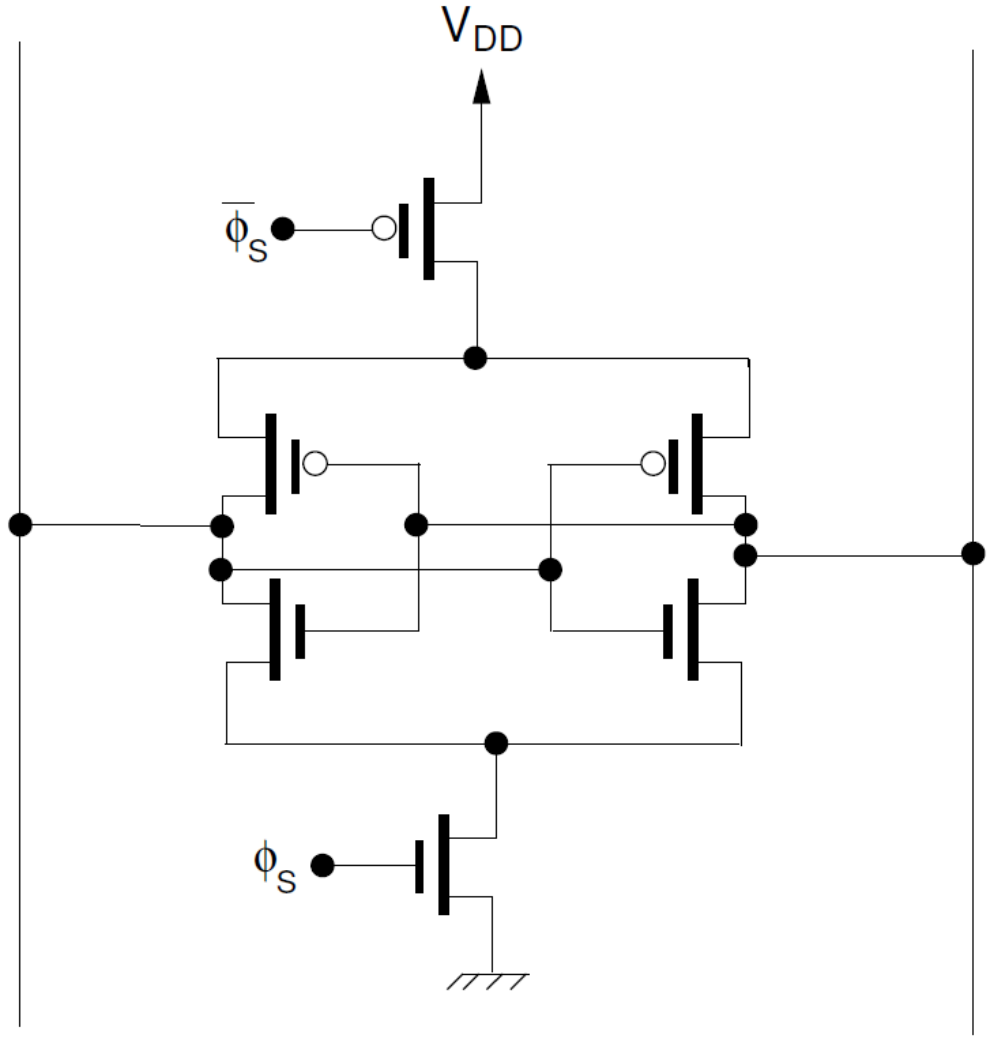
RAM dinamiche (DRAM)



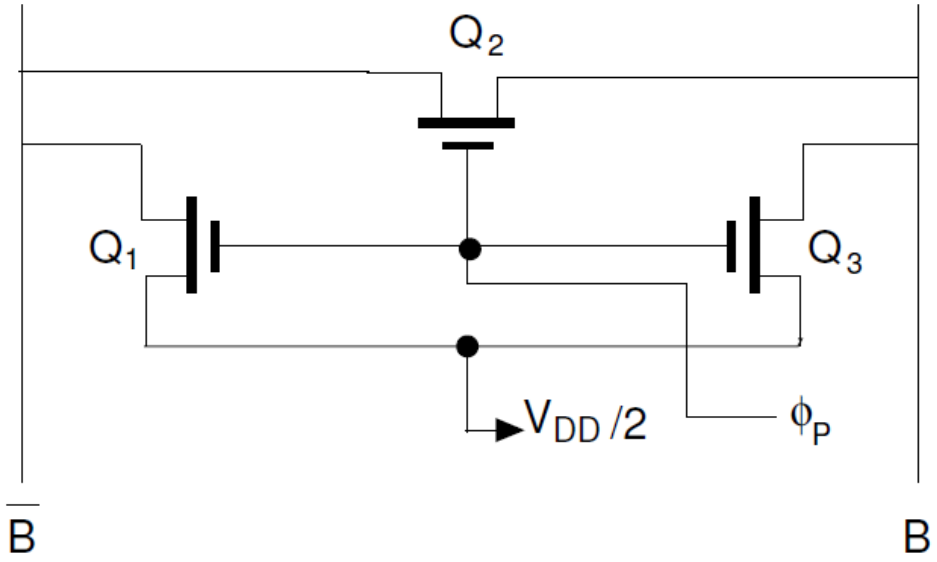
LETTURA

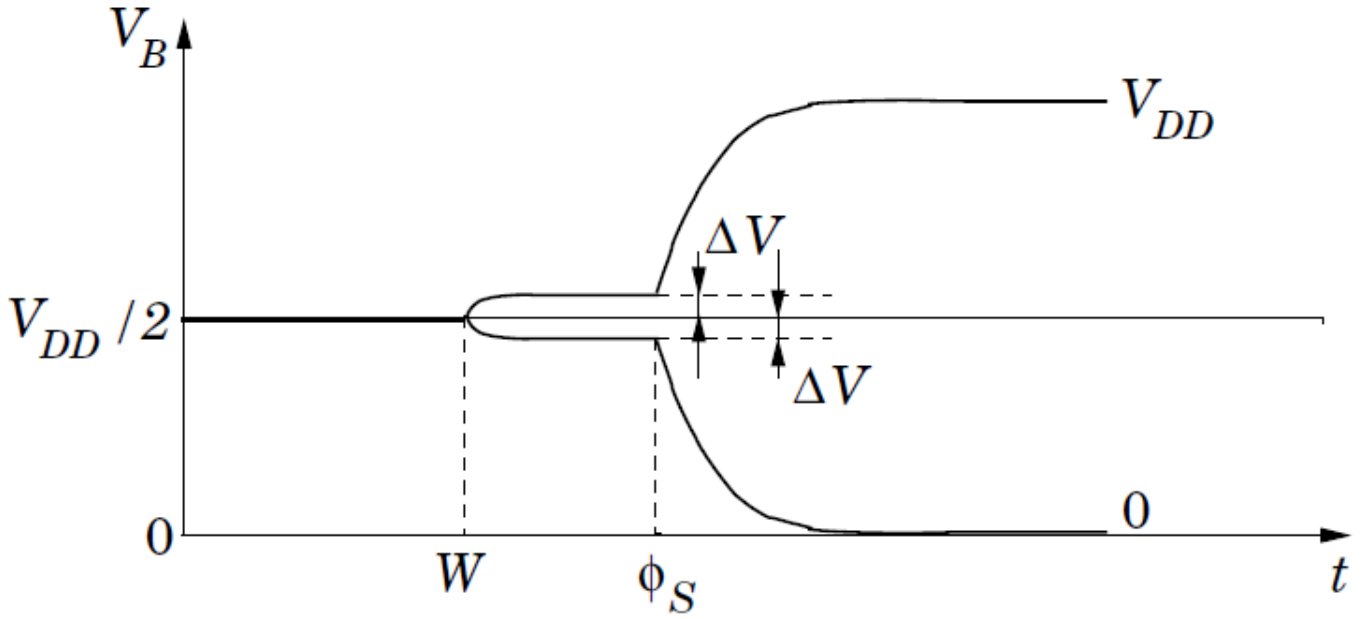
$$\Delta V \approx \frac{C_S}{C_B}\left(V_{CS} - \frac{V_{DD}}{2}\right)$$

Sense amplifier

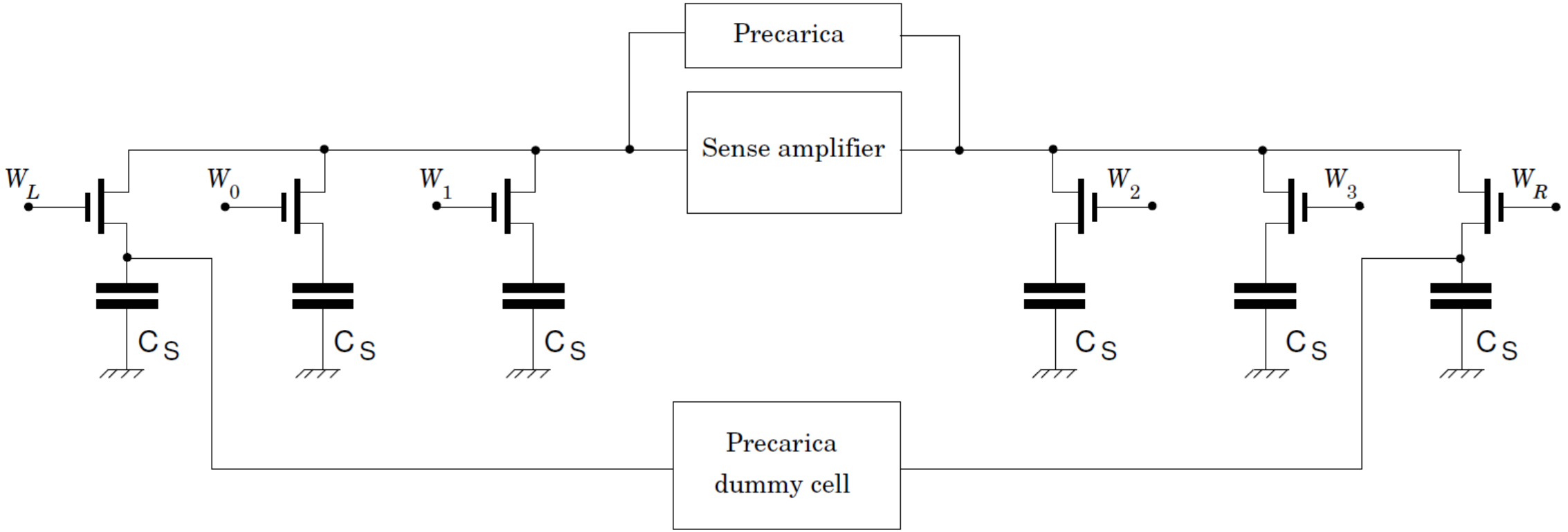


Circuito di precarica





Sense amplifier per DRAM



Decoder degli indirizza di riga

Ciascuna word line deve essere attivata soltanto se sul corrispondente blocco di indirizzi compare l'indirizzo associato. Questo risultato potrebbe essere ottenuto utilizzando una appropriata logica combinatoria a porte, ma risulterebbe piuttosto complicato. Sono pertanto stati progettati dei circuiti specifici per questo scopo, come quello che descriviamo nel seguito.

$$(000) \rightarrow W_0 = \overline{A_2}\,\overline{A_1}\,\overline{A_0} = \overline{A_2 + A_1 + A_0}$$

$$(001) \rightarrow W_1 = \overline{A_2}\,\overline{A_1}\,A_0 = \overline{A_2 + A_1 + \overline{A_0}}$$

$$(010) \rightarrow W_2 = \overline{A_2}\,A_1\,\overline{A_0} = \overline{A_2 + \overline{A_1} + A_0}$$

$$(011) \rightarrow W_3 = \overline{A_2}\,A_1\,A_0 = \overline{A_2 + \overline{A_1} + \overline{A_0}}$$

WIRED-NOR

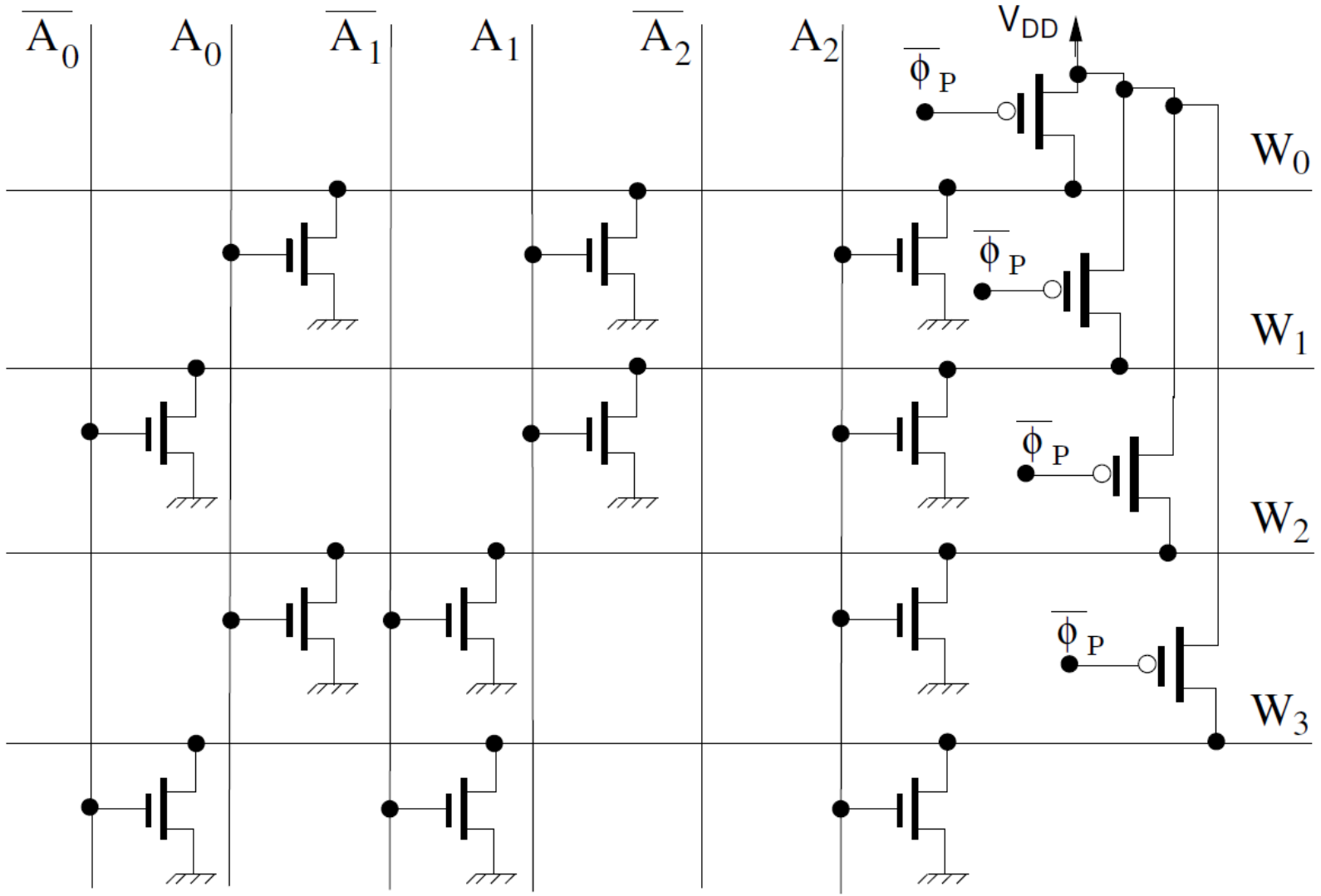
Decoder degli indirizza di riga

$$W_0 = \overline{A_2 + A_1 + A_0}$$

$$W_1 = \overline{A_2 + A_1 + \overline{A_0}}$$

$$W_2 = \overline{A_2 + \overline{A_1} + A_0}$$

$$W_3 = \overline{A_2 + \overline{A_1} + \overline{A_0}}$$



Multiplexer-Demultiplexer delle bit line