Compito di Reti Logiche – 9/1/2018

Esercizio 1 – una possibile soluzione

La tabella di figura contiene un ciclo di tre stati. È pertanto necessario inserire uno stato ponte. Ad esempio, codificando gli stati come S0=00, S1=01, S2=10, è possibile usare S0 come stato ponte nelle transizioni S1-S2. La tabella modificata è la seguente (si notino le celle in grassetto):

x_1x_0 / z1z0	00	01	11	10	z1z0
S0	--	S1	S0	S2	11
S1	S1	S1	S0	**S0**	01
S2	S2	**S0**	S0	S2	10

y_1y_0 \ x_1x_0	00	01	11	10	z1z0
00	--	01	00	10	11
01	01	01	00	00	01
11	--	--	--	--	--
10	10	00	00	10	10

a_1a_0

tabella di applicazione del latch SR

q	q'	s	r
0	0	0	-
0	1	1	0
1	0	0	1
1	1	-	0

y_1y_0 \ x_1x_0	00	01	11	10
00	--	0-	0-	10
01	0-	0-	0-	0-
11	--	--	--	--
10	-0	01	01	-0

s_1r_1

y_1y_0 \ x_1x_0	00	01	11	10
00	--	10	0-	0-
01	-0	-0	01	01
11	--	--	--	--
10	0-	0-	0-	0-

s_0r_0

$\overline{s_1} = x_0 + y_0$ -> $s_1 = \overline{x_0 + y_0}$

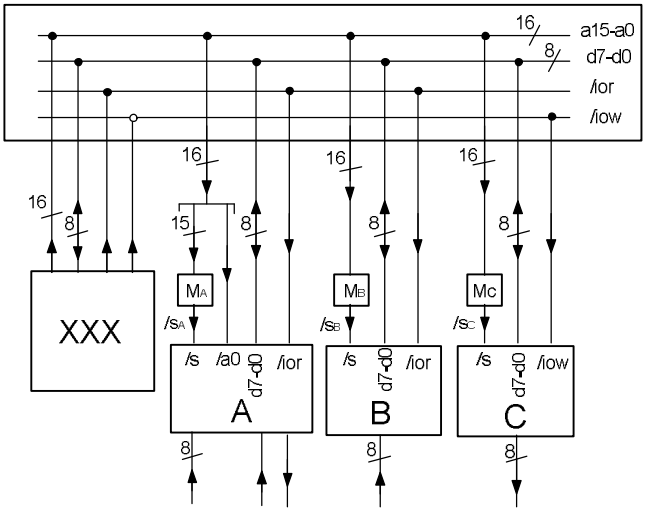
$\overline{r_1} = \overline{x_0}$ -> $r_1 = x_0$

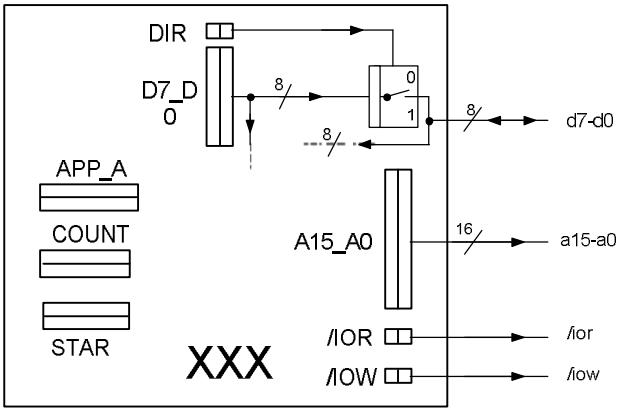
$\overline{s_0} = x_1 + y_1$ -> $s_0 = \overline{x_1 + y_1}$

$\overline{r_0} = \overline{x_1}$ -> $r_0 = x_1$

Per quanto riguarda le uscite, si ha: $z_0 = \overline{y_1}$, $z_1 = \overline{y_0}$

Esercizio 2 - una possibile soluzione:






```
    wire sA_=((a15_a0=='H0100)|(a15_a0=='H0101))?0:1;
    wire sB_=(a15_a0=='H0120)?0:1;
    wire sC_=(a15_a0=='H0140)?0:1;

module XXX(d7_d0, a15_a0, ior_, iow_, clock, reset_);
input         clock, reset_;
 inout  [7:0]  d7_d0;
 output [15:0] a15_a0;
 output        ior_, iow_;
 reg        IOR_, IOW_;  assign ior_=IOR_; assign iow_=IOW_;
 reg        DIR;
 reg [15:0] A15_A0;   assign a15_a0=A15_A0;
 reg [7:0]  D7_D0;    assign d7_d0 =(DIR==1)?D7_D0:'HZZ; //FORCHETTA
 reg [7:0]  APP_A;
 reg [6:0]  COUNT;
 reg [3:0]  STAR;
 parameter S0=0,S1=1,S2=2,S3=3,S4=4,S5=5,S6=6,S7=7,S8=8,S9=9,S10=10,S11=11;
 parameter Num_Periodi=100;
 always @(reset_==0) begin APP_A<='H00; DIR<=0; COUNT<=Num_Periodi;
                           IOR_<=1; IOW_<=1; STAR<=S0; end
 always @(posedge clock) if (reset_==1) #3
  casex(STAR)
   S0:  begin COUNT<=COUNT-1; A15_A0<='H0120; STAR<=S1; end
   S1:  begin COUNT<=COUNT-1; IOR_<=0; STAR<=S2; end
   S2:  begin COUNT<=COUNT-1; D7_D0<=d7_d0+APP_A; IOR_<=1; A15_A0<='H0140;
              DIR<=1; STAR<=S3; end
   S3:  begin COUNT<=COUNT-1; IOW_<=0; STAR<=S4; end
   S4:  begin COUNT<=COUNT-1; IOW_<=1; STAR<=S5; end
   S5:  begin COUNT<=COUNT-1; DIR<=0; A15_A0<='H0100; STAR<=S6; end
   S6:  begin COUNT<=COUNT-1; IOR_<=0; STAR<=S7; end
   S7:  begin COUNT<=COUNT-1; IOR_<=1; STAR<=(d7_d0[0]==0)?S6:S8; end
   S8:  begin COUNT<=COUNT-1; A15_A0<='H0101; STAR<=S9; end
   S9:  begin COUNT<=COUNT-1; IOR_<=0; STAR<=S10; end
   S10: begin COUNT<=COUNT-1; APP_A<=d7_d0; IOR_<=1; STAR<=S11; end
   S11: begin COUNT<=(COUNT==1)?Num_Periodi:COUNT-1;
              STAR<=(COUNT==1)?S0:S11; end
  endcase
endmoduleendmodule
```