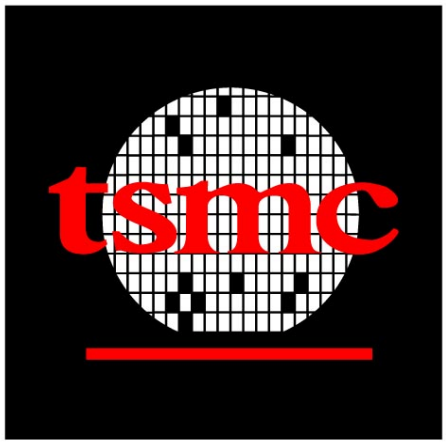

TSMC Universal Standard I/O Library General Application Note

Version 2.00
April 2008

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Revision History

Version	Date	Special Note
2.00	2008/04/03	1. Update the "Dedicated Power to Internal Macro PVDD1ANA/ PVDD2ANA" section in Chapter 2 2. Update the "POC Implementation" section and "Power Up Sequence" section in Chapter 3 3. Update the "Pull-Up/Down I/O Cell Usage" section in Chapter 4 4. Insert a note in Chapter 5 5. Update Chapter 7 contents on page 29, 47 6. Insert new sections on "I/O Ring" and "Dedicated Analog Power & Ground Cell" in Chapter 10. 7. Update Chapter 10 contents. 8. Update the "Open Drain Emulation" section in Chapter 11 9. Update the "Device Mapping between Spice Model Card and LVS/LPE Netlist " section, and insert a new section on "Floating NGATE/PGATE" in Chapter 13 10. Insert a new chapter (Chapter 14) on "Characterization Conditions"
1.90	2007/06/28	1. Update the "Dedicated Power/Ground to Internal Macro" section and insert "Analog Signal Transmission" section into Chapter 2 2. Update the "Power-Up Sequence" section in Chapter 3 3. Update the "Programmable Pins" section in Chapter 5 4. Update Chapter 7 5. Update the "Dummy Power Cell Insertion" section in Chapter 10 6. Update the device mapping table in Chapter 13
1.80	2005/12/20	1. Update the "Dedicated Power/Ground to Internal Macro" section in Chapter 2
1.70	2005/12/08	1. Update *Figure* 2.2 of Chapter 2 and *Figure* 10.1 of Chapter 10
1.60	2005/11/08	1. Update the "Adapter Cell" section of Chapter 7
1.50	2005/08/25	1. Update the "Dedicated Power/Ground to Internal Macro" section of Chapter 2 2. Update the "Power Up Sequence" section of Chapter 3 3. Update the "Non-CUP Wire Bond I/O" section and "Circuit Under Pad (CUP)" section of Chapter 7 4. Update the "Limited Power/Ground Bandwidth" section of Chapter 8
1.40	2005/07/12	1. Update the "Dedicated Power/Ground to Internal Macro" section of Chapter 2. 2. Insert a new paragraph on "High-Vt (Threshold Voltage) Implant" into Chapter 12.

1.30	2005/06/27	1. Update Table 7.3 and Table 7.5 in Chapter 7. 2. Update the content on PADxM/PADxMU for mixed-mode process with top two thick metals and top two large vias in Chapter 7. 3. Update Chapter 12.
1.20	2005/06/15	1. Update the “Limited Power/Ground Bandwidth” section of Chapter 8
1.10	2005/05/30	1. Insert a new section on “Adapter Cell” to guide you how to use TSMC universal standard I/O with TSMC specialty I/O into Chapter 7. 2. Update the bond pad options in “The Bond Pad Cell” section of Chapter 7. 3. Insert the content on “tape-out with top two thick metals for the mixed-mode process” into the bond pad library section of Chapter 7. 4. Insert a section on Direct Shrink to Half-Node Technology into Chapter 4 and Chapter 5 respectively.
1.00	2004/12/10	1. First release of Universal Standard I/O library general application note.

Table of Contents

Chapter 1 Introduction

Purpose

This *General Application Note* describes *Universal Standard I/O* functions, specifications, and usage of the *TSMC Universal Standard I/O Library*.

Related Documentation

For the library-dependent information, please refer to the *library release note* and *Databooks* packed within the document kit. Note that DC information is covered in the *Databooks* for every Universal Standard I/O library. For the silicon-proven libraries, please download the *Silicon Report* from TSMC Online.

Notes

Note 1: Please closely follow TSMC masking layers and bias documents described in the "Tape-Out Layer Information" of library release note. In addition, please refer to Chapter 12 for general tape-out information.

Note 2: The I/O library name that ends up with the character "V" indicates that this library is the Universal I/O library, featuring multi-bonding options, including the non-CUP wire bond, CUP (Circuit Under Pad), and RDL (Re-Distribution Layer) flip chip.

Note 3: For ESD/Latch-Up concern, the maximum resistance "R" of the power/ground metal bus from the bonded power cell / the bonded ground cell to any I/O cell cannot be greater than 1 Ohm for 90nm/65nm/45nm/40nm process technologies. Please refer to page 69 for details.

Note 4: The minimum capacitive load is 20pF between the "VDD" pin on the core side of PVDD1DGZ/CDG and the "VSS" pin on the core side of PVSS1DGZ/CDG. This requirement can also be applied to (PVDD1ANA & PVSS1ANA pair) and (PVDD2ANA & PVSS2ANA pair). Please insert the decoupling capacitor in case capacitive load is below 20pF. The ESD (HBM / MM / CDM) performance can be enhanced by following this requirement.

Particularly for small I/O domain, please place two PVDD1DGZ cells together and double bond them. If PVDD1ANA cells are also in use, please place two PVDD1ANA cells together and double bond them.

Note 5: Please do not use Apollo frame view (apf kit) to steam out the gds.

Chapter 2 Power Arrangement

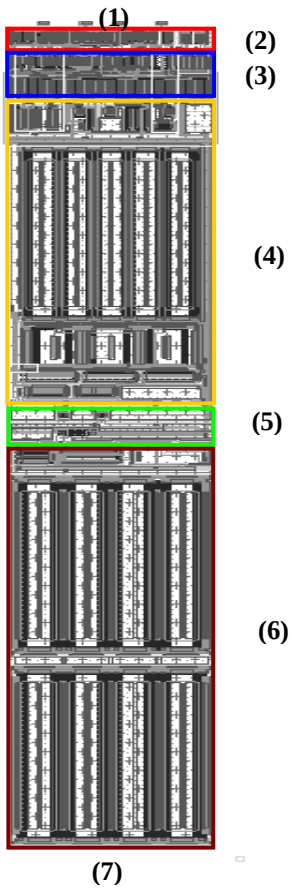
This chapter includes the following topics:

- I/O power rail structure
- Power/ground cells and LVS consideration
- Dedicated Power/Ground Cells to Internal Macro
- Analog Signal Transmission

I/O Power Rail Structure

This section provides information about the I/O power/ground rail configuration. Please make sure that the power rail of each I/O cell is connected by abutting with another I/O cell or with the P&R cells (Filler Cells / Corner Cells). Doing so can ensure a ESD discharge path for any combinations of the ESD stress modes.

Figure 2.1 illustrates a typical *TSMC Universal I/O* layout.



(1) Internal control and signal pins to the core logics

(2) Power rail ***VDD***: connects to the core power ring for the pre-driver

(3) Ground rail ***VSS***: connects to the core ground ring for the pre-driver

(4) Power rail ***VD33*** (or ***VDDPST***): connects to the I/O power ring for level-shifters and post-driver

(5) Double guard ring

(6) Ground rail ***VSSPST***: connects to the I/O ground ring for the post-driver

(7) I/O signal for connecting to the bonding pad

Figure 2.1 Typical TSMC Universal I/O Layout

Power/Ground Cells and LVS Consideration

The TSMC Universal I/O libraries include power and ground cells that supply different voltages to the core, pre-drivers, and post-drivers. The global text is attached to the pad to separate multi-power/ground routing and is used for Layout vs. Schematic (LVS) purposes. Table 2.1 describes the routing pin to the core side and the attached pad text for LVS.

Table 2.1 Pins Information for Power/Ground Cells

Power/Ground Cells	Connected to	Pin to core	Pad text for LVS
PVDD1DGZ / CDG	core cells + pre-drivers	VDD	VDD:
PVDD2 DGZ / CDG PVDD2POC	post-drivers	None	VD33: or VDDPST:
PVSS1DGZ / CDG	core cells + pre-drivers	VSS	VSS:
PVSS2DGZ / CDG	post-drivers	None	VSSPST:
PVSS3DGZ / CDG	all the transistors	VSS	VSS:

Note: The DGZ cell suffix is for the high-volt tolerant libraries, while the CDG cell suffix is for the non high-volt tolerant libraries.

Designers can consider two ground schemes when using TSMC Universal I/O library, and should use different power/ground cells and LVS SPICE netlist files for the corresponding set.

- The **separate ground scheme** separates the ground sources of (core cells + pre-drivers) and (post-drivers) as VSS and VSSPST to provide a clean ground to the core. Table 2.1 indicates that designers can use PVSS1xxx/PVSS2xxx ground cells for this scheme. The name of the SPICE netlist file for LVS is <*Library Name*>*_1_2.spi*.
- The **common ground scheme** provides only one ground source to all transistors (named VSS) to save the number of ground cells. PVSS3xxx is the ground cell that supplies the core cells, pre-drivers, and post-drivers. The name of the SPICE netlist file for LVS is <*Library Name*>*_3.spi*.

The **separate ground scheme** is suggested to provide a less-noisy ground source, since core and I/O grounds are separated. Even in the case of limited package pins, designers can use double bonding from adjacent chip (die) pads PVSS1xxx and PVSS2xxx to bond them to a single package pin and thus reduce the ground noise to the core area. Please refer to *Figure* 7.1 for the bonding pad method.

The **common ground scheme** is suggested only when the ground noise is not critical in the extremely pad-limited design.

There must be at least two kinds of power sources because the power supplies of the core and I/O cells are different. That is why TSMC does not provide a single power to supply both core cells and I/O cells.

For LVS, designers should use the SPICE netlist that corresponds to the target ground scheme. Table 2.2 shows the LVS files required for two different ground schemes.

Table 2.2 Power/Ground Schemes and the Corresponding SPICE Netlist for LVS Check

Power Supply	Separate Ground Scheme	Common Ground Scheme
Core Cells + Pre-drivers	PVDD1DGZ / CDG PVSS1DGZ / CDG	PVDD1DGZ / CDG PVDD2DGZ / CDG (PVDD2POC) PVSS3DGZ / CDG
Post-drivers	PVDD2DGZ / CDG (PVDD2POC) PVSS2DGZ / CDG	
LVS SPICE netlist	*<Library Name>_1_2.spi*	*<Library Name>_3.spi*

For guidance on the usage of PVDD2POC cell, please refer to Chapter 3 for details.

Attention 1: The purpose of I/O power & ground cells (PVDD2CDG/DGZ & PVSS2CDG/DGZ) is to supply the I/O pad ring. There is no pin on the phantom to connect to the core side, but there is a pad pin for bond pad connection. For front-end kits, such as Verilog and Synopsys views, phantoms are modeled as black boxes with no pins and no functions, which is consistent with back-end kits.

Attention 2: Since there are ESD protection devices within the power/ground cells, it is necessary to run LVS check using SPICE netlist.

The Dedicated Analog Power (PVDD1ANA / PVDD2ANA) / Analog Ground (PVSS1ANA / PVSS2ANA) to Internal Macro

The universal standard I/O library provides dedicated power/ground cells to internal macro for PLL/RAM/Voltage-Island applications. It is not necessary to place a power-cut cell (PRCUT) in between the digital I/O cells and the dedicated power/ground cells. In other words, these dedicated power/ground cells can share a common domain with the digital I/O cells. Please refer to *Figure* 2.6 for illustration.

The Dedicated Analog Power PVDD1ANA / PVDD2ANA to Internal Macro

- PVDD1ANA: The dedicated power supply to internal macro with core voltage.
- PVDD2ANA: The dedicated power supply to internal macro with I/O voltage.

Note 1: The PVDD1ANA / PVDD2ANA power cells are optimized for analog power supply.

Note 2: It is not necessary to place a power-cut cell (PRCUT) in between the dedicated power/ground cells and the digital I/O cells. Please refer to *Figure* 2.6 and "Separated Power Domain" of Chapter 10 for PRCUT usage information.

When using PVDD1ANA together with PVSS1ANA cell:

You need to adopt the PCLAMP cell from the corresponding universal analog I/O library, and do the following connections to enhance core ESD/Latch-Up protection.

Step 1: Connect from AVDD pin of PVDD1ANA analog power cell to VDDESD pin of PCLAMP cell. Connect from AVSS pin of PVSS1ANA analog ground cell to VSSESD pin of PCLAMP cell.

Step 2: Then connect from VDDESD and VSSESD rails of PCLAMP cell to internal core power rail and core ground rail respectively. For details on PCLAMP cell, please refer to Universal Analog I/O General Application Note.

Reminder: PCLAMP can only be used with PVDD1ANA & PVSS1ANA pair.

Analog Signal Transmission

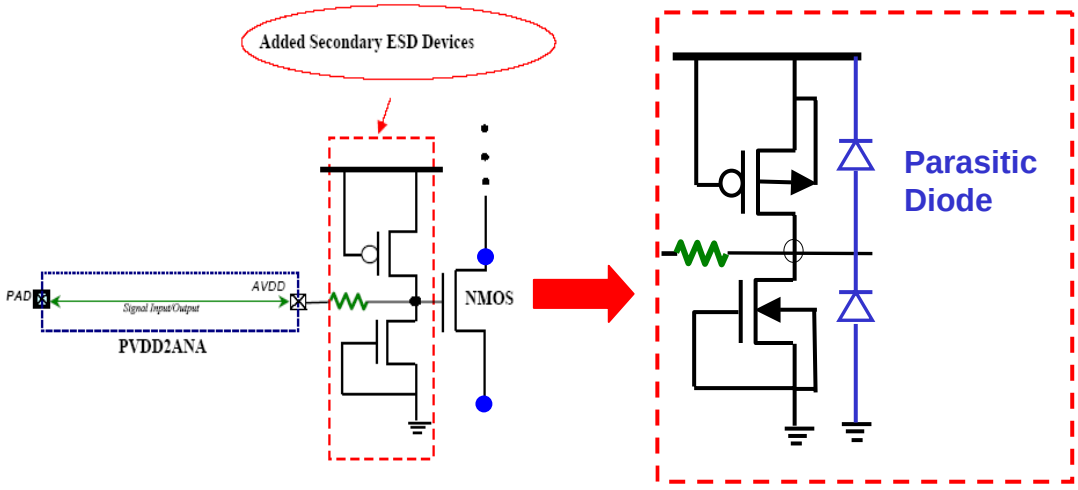
PVDD1ANA and PVDD2ANA are optimized for analog power supply, where PVDD1ANA is the core-voltage analog power supply; whereas PVDD2ANA is the I/O-voltage analog power supply. PVDD1ANA can never be used as core-voltage analog signal cell. However, PVDD2ANA might be used as I/O voltage analog signal cell.

For analog signal transmission:

1. PVDD1ANA can never be used as the core-voltage analog signal cell nor the I/O-voltage analog signal cell.
2. PVDD2ANA can be used as the I/O-voltage analog signal cell under certain applications, but can never be used as the core-voltage analog signal cell.

1st Condition: Connect the PVDD2ANA signal pin to the internal gate

It is required to implement your own secondary ESD protection device (with proper channel length) as specified in the ESD guidelines of TSMC Design Rule Manual, where a resistor in series with a PMOS protection device to power and an NMOS protection device to ground should be used as illustrated below.



- For internal signal connection, please avoid direct path to power or to ground through one gate oxide.

Figure 2.2 Secondary ESD Protection Device to Internal Gate

2nd Condition: Connect the PVDD2ANA signal pin to the drain side of internal thick device

It is required to implement your own secondary ESD protection device (with proper channel length) as specified in the ESD guidelines of TSMC Design Rule Manual, where a resistor in series with a PMOS protection device to power and an NMOS protection device to ground should be used as illustrated below.

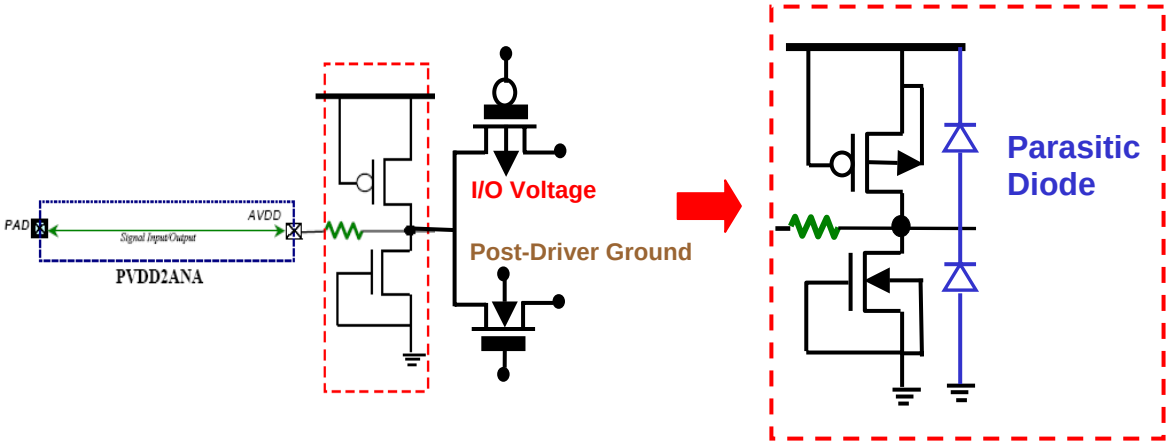


Figure 2.3 Secondary ESD Protection Device to The Drain Side of Internal Thick Device

If you do not implement the secondary ESD protection device, you need to ensure that the internal P & N transistors (as indicated in yellow) closely follow the ESD guidelines of TSMC Design Rule Manual.

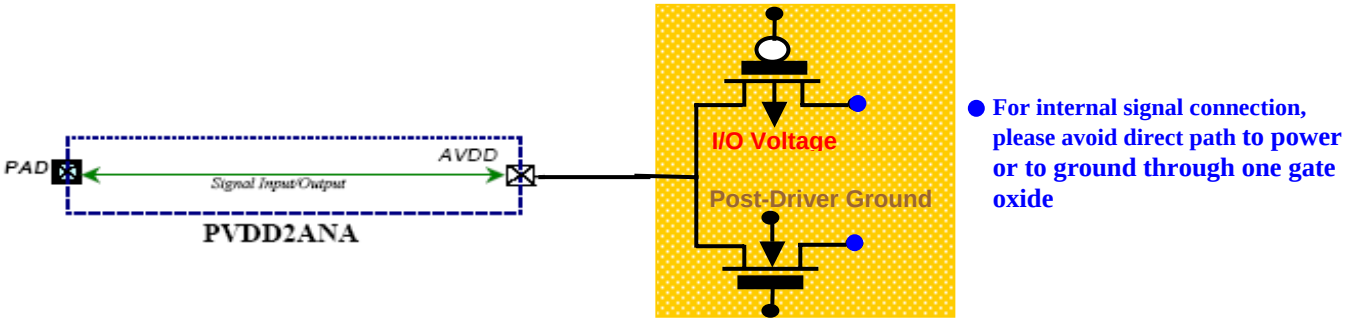


Figure 2.4 Internal P & N Transistor Need to Follow ESD Guidelines

Note: P & N transistors with drain side connected to the analog signal pin need to follow ESD guidelines, particularly the RPO ones as shown in Figure 2.5. Since P & N transistors in this case have to be regarded as ESD devices, please waive the associated DRC errors.

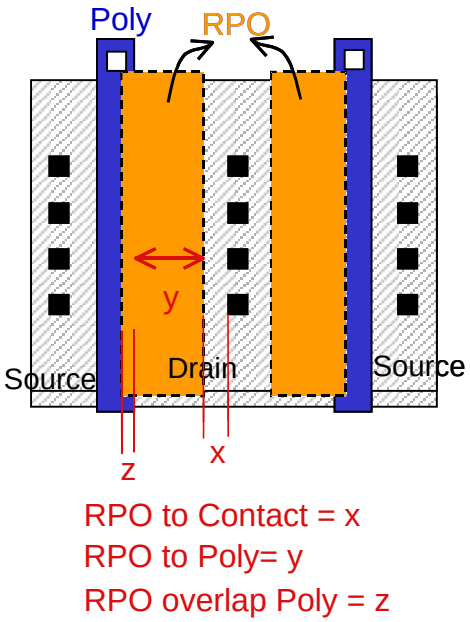


Figure 2.5 RPO Rules in ESD Guidelines (x, y; z varies, depending on the technology)

The Dedicated Analog Ground PVSS1ANA / PVSS2ANA to Internal Macro

- PVSS1ANA: The dedicated ground supply for PVDD1ANA.
- PVSS2ANA: The dedicated ground supply for PVDD2ANA

Attention 1: It is mandatory to use at least one core power cell PVDD1DGZ/CDG, one I/O power cell that features power-on control PVDD2POC, and one common-ground cell PVSS3DGZ/CDG within one domain.

Or

It is mandatory to use at least one group of core power **&** core ground cells PVDD1DGZ/CDG **&** PVSS1DGZ/CDG together with one group of I/O power cell that features power-on control **&** I/O ground cell PVDD2POC **&** PVSS2DGZ/CDG within one domain.

Attention 2: It is not necessary to place a power-cut cell between digital I/O and the dedicated power/ground cells to internal macro.

Attention 3: Please refer to Chapter of "Electrical Static Discharge (ESD) Considerations" for ESD protection scheme of the dedicated power/ground cells.

Application Examples

Example 1: Without PRCUT Power-Cut Cell

The analog power/ground cells can be placed in the digital domain for power/ground pin saving. Please refer to *Figure* 2.6 for illustration.

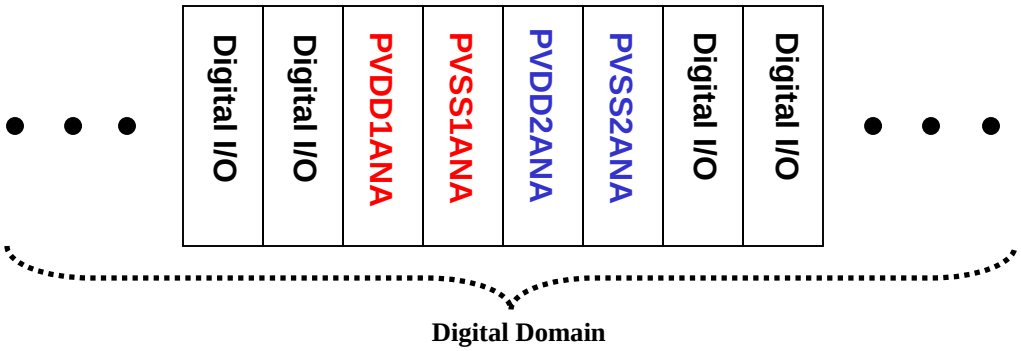


Figure 2.6 Using PVDDxANA/PVSSxANA Cells without Power-Cut Cell

Example 2: With PRCUT Power-Cut Cell

If customer has concern on coupling noise between metal lines, they can set up the isolated domain using PRCUT power-cut cells. Doing so requires **extra** digital power/ground pins in the isolated domain to supply ESD power/ground buses (i.e. VDD, VSS, VDDPST, and VSSPST). In other words, it is required to insert the following digital cells in addition to the analog power/ground cells:

- At least one digital core power cell PVDD1CDG/DGZ
- One and only one PVDD2POC that works as both post-driver power supply and POC signal generator.
- At least one PVSS3CDG/DGZ (common ground) **or** at least one PVSS1CDG/DGZ along with one PVSS2CDG/DGZ (separate grounds).

Attention: For full-chip LVS check, the digital ground cell type must be consistent across all digital domains. You can either use PVSS3CDG/DGZ in **each** digital domain or use PVSS1CDG/DGZ together with PVSS2CDG/DGZ in **each** digital domain.

The trade-off for example 2 is more pin counts. Please refer to *Figure* 2.7 for illustration.

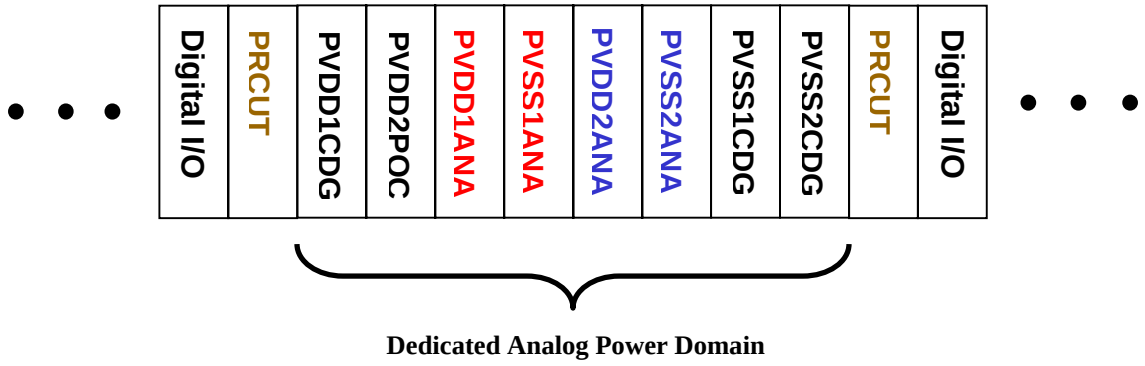


Figure 2.7 Using PVDDxANA/PVSSxANA Cells with Power-Cut Cell

Chapter 3 Power On Control System

This chapter covers information on the following topic:

- Power On Control (POC) usage
- POC implementation
- LVS consideration for the POC signal
- Power-up sequence
- Power-down sequence

Power On Control Usage

TSMC I/O libraries contain the Power On Control (POC) system to prevent I/O unknown state. An *unknown state* may cause high I/O crowbar current or bus contention when the I/O voltage is powered up before the core voltage.

The PVDD2POC cell features POC circuitry for POC signal generation:

- The **POC circuitry** is located within PVDD2POC cell, which plays the similar role to PVDD2DGZ / CDG cell for I/O-voltage power supply and for ESD protection between post-driver power rail and post-driver ground rail. PVDD2POC detects the “power-on” condition and generates a POC signal to the rest of the I/Os.
- The **POC signal** is distributed to other I/O buffers by cell abutment; no special POC routing is required.

For standard I/O cell, the POC signal can turn off the output NMOS and PMOS buffers when I/O power is on whereas core power remains off. For example, during the power up sequence, the I/O cell is set in the Hi-Z state or the input state.

Figure 3.1 illustrates that the POC signal generated by PVDD2POC cell is distributed through cell abutment, and the signal is not used in power pads where the POC rail just crosses the cell. Note that POC signal can be cut by inserting a power-cut (PRCUTx) cell as indicated in *Figure* 3.4.

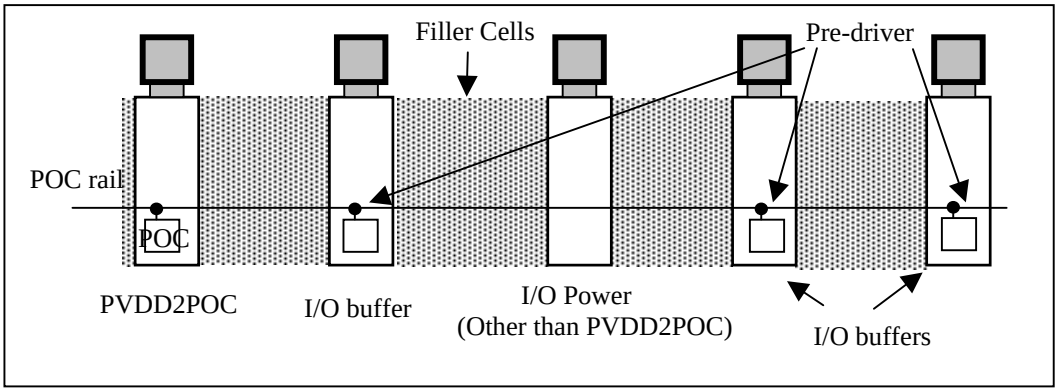


Figure 3.1 POC Usage in the I/O Ring

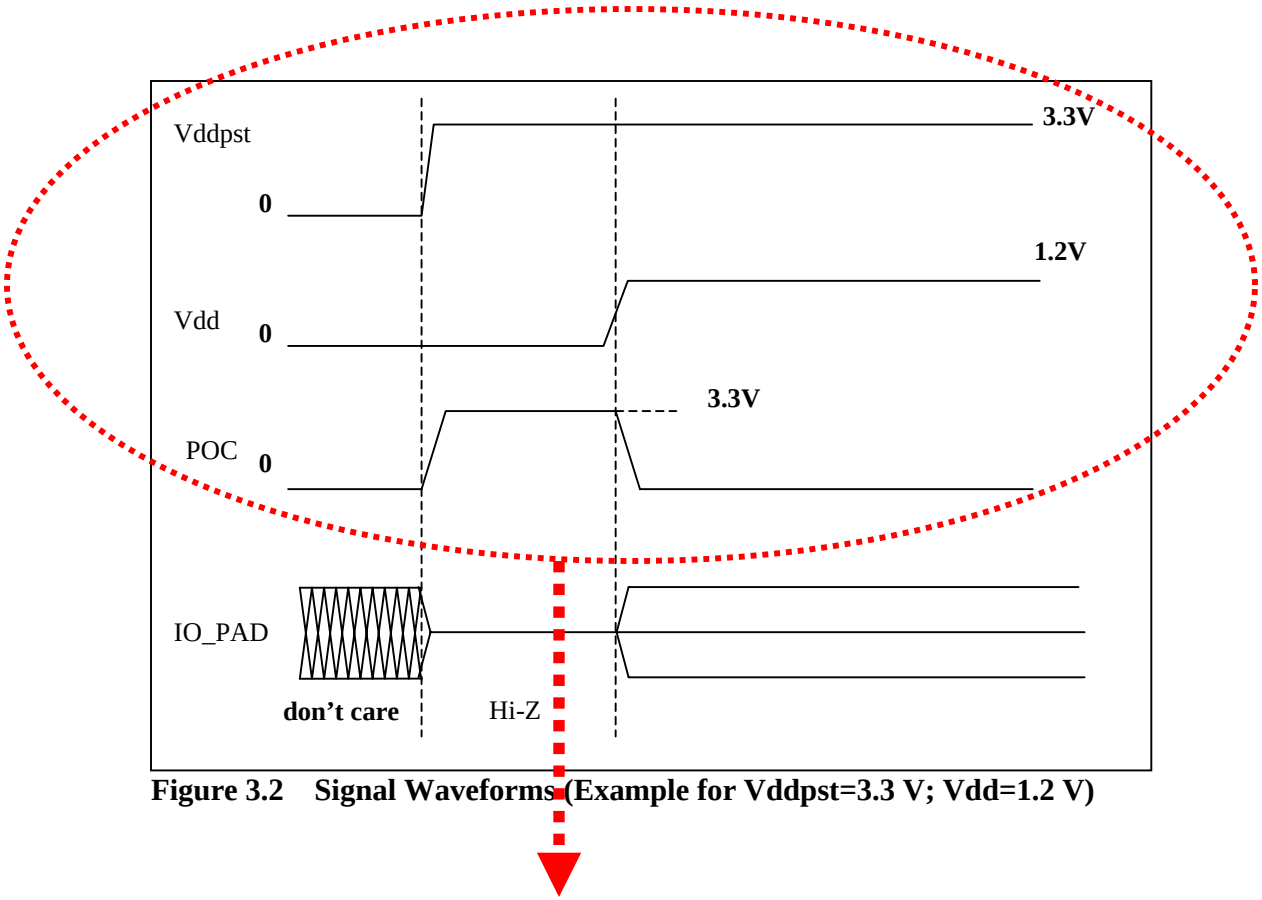


Figure 3.2 Signal Waveforms (Example for Vddpst=3.3 V; Vdd=1.2 V)

Note: Details on the relationship among VDD, VDDPST, and POC are addressed on the following page.

Use 0.13µm 1.2V/3.3V I/O as an example (please refer to *Figure* 3.3)

Note: The blue line corresponds to POC voltage (POC). The red line corresponds to the pre-driver voltage (VDD). The yellow line corresponds to the post-driver voltage (VDDPST).

- POC fully turns on while VDDPST reaches 0.5V (This value varies, depending on process technology.)
- POC goes off while VDD reaches its threshold point at 0.7V (This value varies, depending on process technology.)
- If VDD stays off while VDDPST is on first, POC stays on and there is NO crowbar leakage current at all time.
- In case VDDPST powers up first at "slow" rate, and VDD powers up afterwards at "fast" rate, our POC circuit can still work as long as VDDPST is greater than (pre-driver voltage VDD + one diode voltage) during power-up.
- POC is always on before VDD reaches its threshold point.
- Once VDD reaches its threshold point, POC is off. Then the state of the pad is controlled by "I" (Input) and OEN (Output Enable) pins.

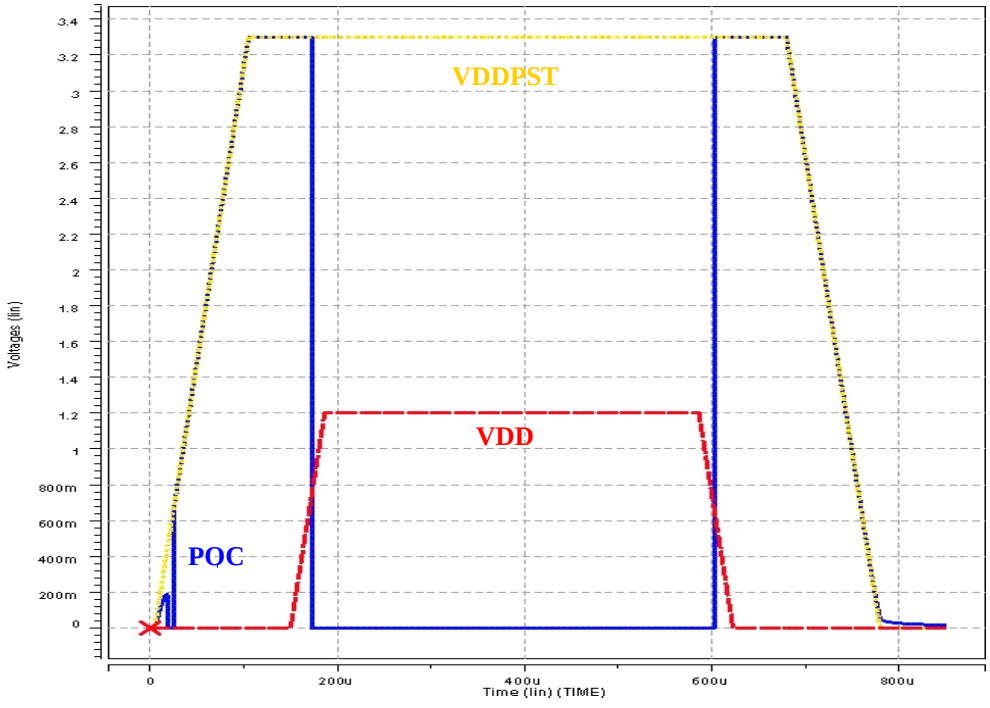


Figure 3.3 How PVDD2POC Cell of 1.2v/3.3V I/O Library Functions in the Power Up Process

POC Implementation

Warning: It is mandatory to use ONE and Only One PVDD2POC in each digital domain!

Note: PVDD2POC cell can be either bonded out (as a POC signal generator and the post-driver power supply), or not bonded out (as a filler cell).

It is mandatory to use ONE and Only One PVDD2POC in each digital domain that contains I/O buffers as illustrated in *Figure* 3.4. However, a digital domain composed of only power cells does not require POC signal. Implementation of PVDD2POC can be achieved by replacing one PVDD2DGZ / CDG with only one PVDD2POC in each power domain.

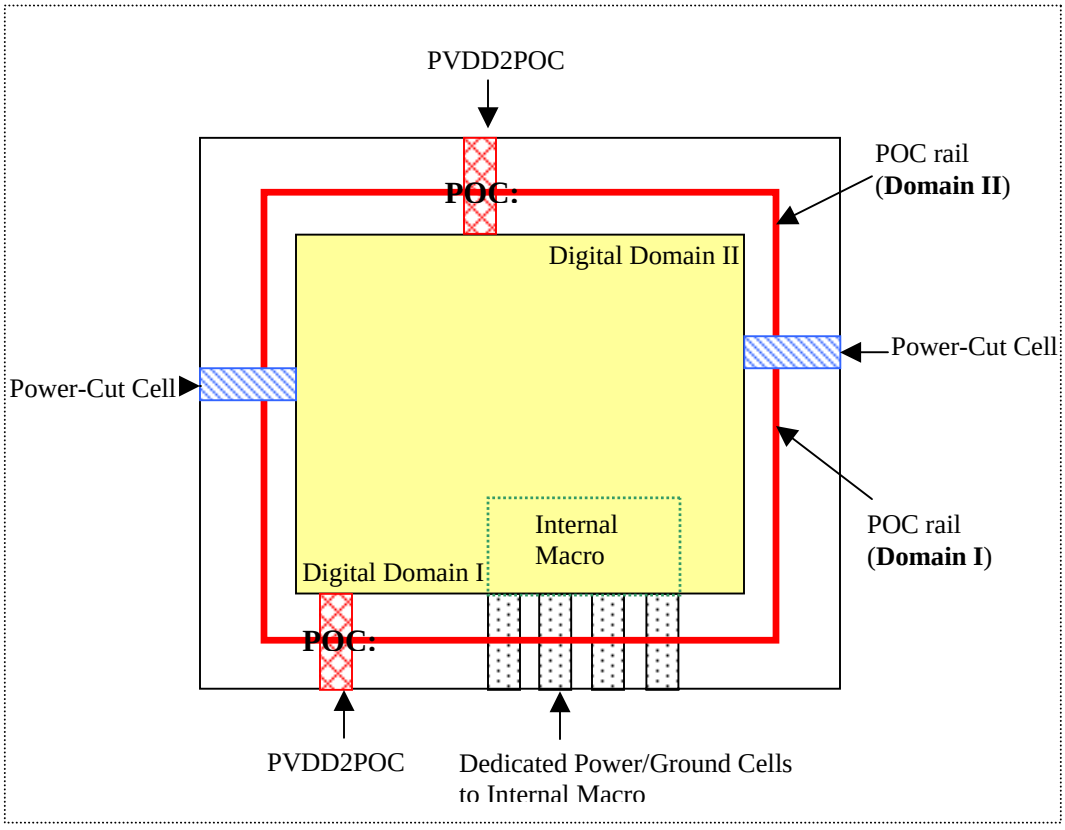


Figure 3.4 Example of Implementation of PVDD2POC

LVS Considerations for the POC Signal

For LVS purpose, it is necessary to put a "POC:" text on the top level of POC rail within the PVDD2POC cell. The number of added "POC:" text is the same as the number of PVDD2POC cell implemented on the chip. This has to be done in order to ensure a smooth LVS check.

If users do not implement one PVDD2POC cell per digital domain as instructed, it would lead to the floating node issue. Note that the POC rail is generally located in the pre-driver.

Power Up Sequence

- **Turn on the higher (I/O) voltage first and then the lower (core) voltage:** PVDD2POC cell would general POC signal to have the output NMOS and PMOS buffers off, so that the crowbar current in the post-driver fingers would not occur on the power-up stage.

- **Turn on the lower (core) voltage first and then the higher (I/O) voltage:** Turning on the core voltage prior to the I/O voltage is also allowed when the I/O control pins are set/reset to a fixed state. Customer can decide which voltage to turn on first based on the application.

Attention: If PVDD2ANA analog power cell exists in the domain, you need to ensure that the PVDD2ANA is powered up **after** the digital PVDD2CDG/DGZ power cell is on.

Power Down Sequence

There is no requirement on the power-down sequence. Customers can decide which voltage to be down first based on their application.

Attention: If the analog power cell (PVDD2ANA) exists in the domain, you need to ensure that the analog power cell is powered down **before** the digital power cells (PVDD1CDG/DGZ **&** PVDD2CDG/DGZ) are down.

Chapter 4 High-Voltage Tolerant I/O Cell Usage

Many of TSMC Universal I/O cells are high-voltage tolerant. Users can simply tell if the I/O library is high-volt tolerant by the library name prefix. If library name starts with "**tpz**", this library features high-volt input tolerance. For example, **tpz**n65lpgv2 reflects that this 65nm I/O library is high-volt input tolerant.

Because of the nature of high-voltage tolerant circuitry, there are some special notes that users must pay attention to beforehand.

- Programmable Pins
- Pull-up/down I/Os
- Output tri-state applications

Programmable Pins

The programmable pins of the high-volt tolerant I/O include:

OEN	(Output Enable) pin to enable the path from I → PAD
REN	Pull-up/Pull-down Resistor Enable

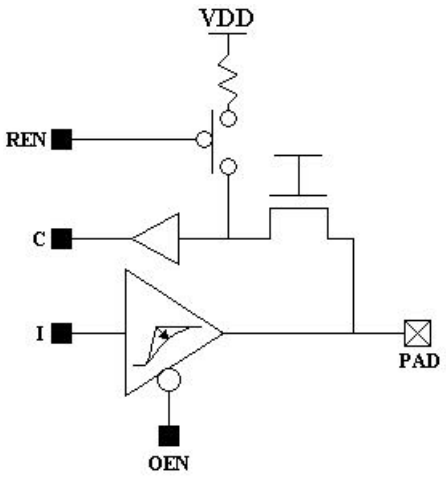


Figure 4.1 The Programmable Pins of High-Volt Tolerant I/O Cell (e.g. PRUWxDGZ)

To make the high-volt-tolerant I/O cell correctly function as expected, it is required to tie the programmable pins to low level (VSS) or high level (VDD) through a tie-high/tie-low cell available from the standard cell library.

Table 4.1 OEN Usage

Input		Output	Remarks
OEN	**I**	**PAD**	
1	X	Z	Output disable
0	0	0	Full swing output
0	1	1	

Table 4.2 REN Usage

REN	Remarks
1	Disable the Pull-up/Pull-down Resistor (not to pull the core)
0	Enable the Pull-up/Pull-down Resistor (to pull the core)

Pull-Up/Down I/O Cell Usage

Some of the TSMC high-volt tolerant universal standard I/O cells come with internal pull-up or pull-down. Because of the high-voltage tolerant architecture as shown in *Figure* 4.2, the internal pull is a weak pull, which can only pull the "core", but not the "PAD". Therefore, do not use them to pull the pad with external loads, or use these cells as drivers during switching. The pull-up/down resistance varies over a wide range depending on the process corner conditions. Please refer to the DC table of library databook for details.

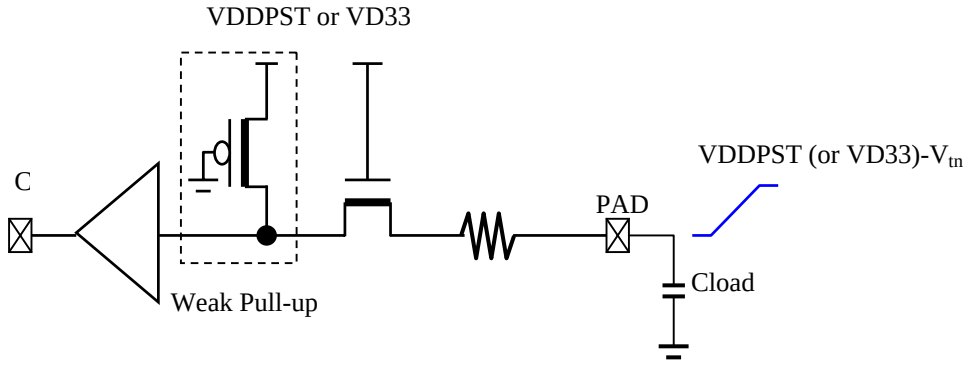


Figure 4.2 Weak Pull-Up in the High Voltage Tolerant Architecture

The main purpose of TSMC pull-up/down I/O is to tie the net on the "C" port (the port that connects the chip core) to a stable value when PAD is unconnected. This is useful for some pins such as "scan_in," which is used only during testing and not connected on the PCB. For this purpose, the unconnected pins of the "scan_in" can be pulled-up/down to avoid a floating net on the chip core.

For the reasons given in this section, the Verilog model for TSMC I/Os with pull-up/down is as follows:

When OEN=1 and no other driver is driving the "PAD" pin (pull-up/down situation), the model exhibits the following behavior:

- The effect of pull-up/down can't go through the "PAD" pin. The "PAD" pin remains in the "Z" state.
- The effect of pull-up/down can be seen on the "C" pin only after a 100 µs delay.

The purpose of this Verilog model behavior is to discourage designers from using the effect of pull-up/down during signal switching or the pull-up/down of external loads of chips. Electrically, the "PAD" pin would never reach the post-driver rail voltage (VD33 or VDDPST) for the high voltage tolerant architecture. A very long pull-up/down time for a "C" pin is set because the timing of the pull-up/down cannot be guaranteed due to process variations.

If pull-up/down is needed for the signal switching or for pull-up/down of an external load, it is recommended that you add "external" pull-up/down resistors on the PCB. The effect of this external pull-up/down should be modeled in the Verilog test bench (which normally models the chip environment). Note that electrically, the external pull-up resistor is preferred rather than the pull-down resistor.

Direct Shrinkage to Half-Node Technologies

The universal standard I/O can be directly shrunk to half-node technologies without any additional work. For example, 0.18µm universal standard I/O can be directly shrunk to 0.16µm technology, 0.13µm universal standard I/O can be directly shrunk to 0.11µm technology, 90nm universal standard I/O can be directly shrunk to 80nm technology, and 65nm universal standard I/O can be directly shrunk to 55nm technology. However, only a certain type of bond pads can support direct shrinkage to half-node technologies. For details, please refer to the bond pad library release note of each process technology.

Chapter 5 Regular I/O Cell Usage

Many of TSMC Universal I/O cells are not high-volt-tolerant. Users can simply tell if the I/O library is high-volt tolerant by the library name prefix. If the library name starts with "**tpd**", this library DOES NOT feature high-volt tolerance, and is categorized as a "**regular I/O library**". For example, **tpd**n90lpnv3 indicates that this 90nm I/O library is a regular I/O library.

Programmable Pins

The regular I/O cell comes with programmable pins to control the I/O as listed below:

DS	Drive Select	Tie to VDD or Ground
PE	Pull Enable	Tie to VDD or Ground
IE	(Input Enable) to enable the path from PAD → C	Tie to VDD or Ground
OEN	(Output Enable) to enable the path from I → PAD	Tie to VDD or Ground

Note: It is required to tie the control pin to power/ground through a tie-high/tie-low cell.

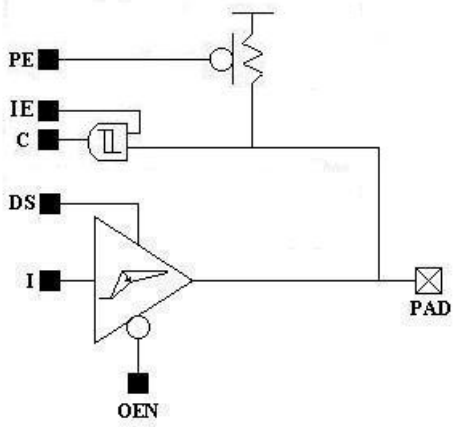


Figure 5.1 The Programmable Pins of Regular I/O Cell (e.g. PRUWxSCDG)

For example, by selecting the proper I/O cell and setting DS to the right value, user can achieve the driving strength ranging from 2mA up to 16mA. Please refer to the following tables for the functions of programmable pins.

Note 1: To make the regular I/O cell correctly function as expected, it is required to tie the programmable pins to low level (VSS) or high level (VDD) through a tie-low/tie-high cell available from the standard cell library.

Note 2: Regular I/O cannot support "fail-safe" application.

Note 3: The internal pull-up/down is a weak pull, which is designed to pull the "CORE", and takes a long while to pull the "PAD".

Table 5.1 Driving Strength of the I/O Cells

Regular I/O Cell (Example)	DS=0	DS=1
PDDW0204CDG	2 mA	4 mA
PDDW0812CDG	8 mA	12 mA

Similarly, the "DS" control pin is also included in other regular I/O cells.

Table 5.2 OEN Usage

Input		Output	Remarks
OEN	I	PAD	
1	X	Z	Output disable
0	0	0	Full swing output
0	1	1	

Table 5.3 Input Path (PAD→ C)

Input		Output	Remarks
IE	PAD	C	
0	X	0	Input disable
1	1	1	Input enable
1	0	0	

Table 5.4 Pull-Enable Usage (PAD → C Input Path)

PE	Remarks
0	Pull disable
1	Pull enable

Input Only Cells

If library does not include the input-only cell, setting the programmable pins to proper values can achieve the input-only purpose.

For example, by connecting the OEN pin of PDDW0204CDG cell (or PDDW0204SCDG cell if the Schmitt trigger input is required) to VDD through a tie-high cell, it can turn to the input-only cell. However, all the unused pins must also be tied to ground or VDD using a tie-low or tie-high cell.

Direct Shrinkage to Half-Node Technologies

TSMC linear universal standard I/O can be directly shrunk to half-node technologies without any additional work. For example, 0.18µm universal standard I/O can be directly shrunk to 0.16µm technology, 0.13µm universal standard I/O can be directly shrunk to 0.11µm technology, 90nm universal standard I/O can be directly shrunk to 80nm technology, and 65nm universal standard I/O can be directly shrunk to 55nm technology. However, only a certain type of bond pads can support direct shrinkage to half-node technologies. For details, please refer to the bond pad library release note of each process technology.

Chapter 6 Oscillator I/O Cell Usage

The oscillator I/O cells included in TSMC Universal I/O library are designed to oscillate with crystal samples from 2MHz to 30MHz in the fundamental mode. These cells are not designed to work in the KHz band or in overtone oscillation. For applications out of the 2-30 MHz range, please contact your TSMC regional FAE for further suggestions.

You should select the proper oscillator I/O cell according to your crystal specifications. The tank circuit for fundamental oscillation is provided only for reference.

This chapter provides information about the following topics:

- Selection of the oscillator I/O cell
- Oscillating tank circuits
- Pin order
- Back annotation

Selection of the Oscillator I/O Cell

There are four sets of oscillator I/O cell, PDXO01DG/PDXOE1DG, PDXO02DG/PDXOE2DG, PDXO03DG/PDXOE3DG, and PXOE1CDG/PXOE2CDG. Each set contains the cells with or without an enabling signal. The number in the cell name indicates the driving strength and signal gain (gm) level. To ensure the oscillation start up, the tank circuit must provide a negative resistance (-Re) at least **five times** greater than the equivalent series resistance (ESR) of the crystal sample. The greater the negative resistance is, the faster the crystal starts up. For the same load capacitance (CL), the higher gm provides larger negative resistance and thus can start up the crystal with higher ESR, but the power consumption is also higher. You should check the Drive Level (DL) specification of your sample to avoid damaging the parts.

To select the proper oscillator I/O cell, the specification of the applied crystal is crucial. The key parameters for start-up are CL and the maximum ESR at the target frequency. Reducing the CL can help increase the negative resistance of the tank circuit. But if CL is too small, the deviation from the target frequency increases because of the growing percentage of the capacitance variation. Therefore, there is a trade-off between the short start-up time and small frequency deviation in deciding the CL value.

The small ESR (with a higher price) also helps to reduce the start-up time. Once the CL and ESR are specified, you can refer to Table 6.1 (suitable for 0.25µm, 0.18µm, 0.15µm, 0.13µm, 90nm, and 65nm high-volt tolerant I/O libraries), and

Table 6.2 (suitable for 0.18µm, 0.13µm, and N90 regular I/O libraries) for selection guidance. These tables are for reference only, and are applicable in typical condition. If the start-up time is not critical, the smaller gm set is preferred for less power consumption.

Some conditions require a higher gm set, for example, when an application is start-up-time sensitive or the crystal gets much higher CL (or ESR) compared to that in Table 6.1. According to Table 6.1, if you have a 14.31818MHz crystal part with CL=12pF and the maximum ESR=80Ohm, set (I) is the first choice. However, if CL=20pF, then set (II) is recommended, especially when the start-up time is also a factor. If you are not sure whether your crystal part together with TSMC oscillator I/O can oscillate at the target frequency or not, please contact TSMC FAE for evaluation.

Table 6.1 Selection Guide of the Oscillator I/O for 0.25µm/0.18µm /0.15µm/0.13µm/N90/N65/N45 High-Volt Tolerant I/O Libraries

Target Freq (Hz)	2M~ 3M	3M~ 6M	6M~ 10M	10M~ 20M	20M~ 30M
CL (pF)	25	20	16	12	8
Maximum ESR (Ohm)	1K	400	100	80	40
Osc I/O Sets	**(I)**	**(I)**	**(I)**	**(I) (II)**	**(I)~(III)**

(I) is PDXO01DG/PDXOE1DG
(II) is PDXO02DG/PDXOE2DG
(III) is PDXO03DG/PDXOE3DG

Table 6.2 Selection Guide of the Oscillator I/O for 0.18µm/0.13µm/N90 Regular I/O Libraries

Target Freq (Hz)	2M~ 6M	6M~ 10M	10M~ 20M	20M~ 30M
CL (pF)	20	16	12	8
Maximum ESR (Ohm)	1K	160	90	40
Osc I/O Sets	**(I) (II)**	**(I) (II)**	**(I) (II)**	**(I) (II)**

(I) is PXOE1CDG
(II) is PXOE2CDG

Note that the only difference between PXOE1CDG and PXOE2CDG is that PXOE2CDG contains a feedback resistor Rf between XO and XI; whereas PXOE1CDG does not. To find out Rf value in PXOE2CDG cell, please refer to the LVS netlist.

Oscillating Tank Circuits

Figure 6.1 shows a reference tank circuit for crystal part that oscillates in fundamental mode. The circuit connects the oscillator I/O cell and some external components to ensure the oscillation start-up, and to keep it stable and precise.

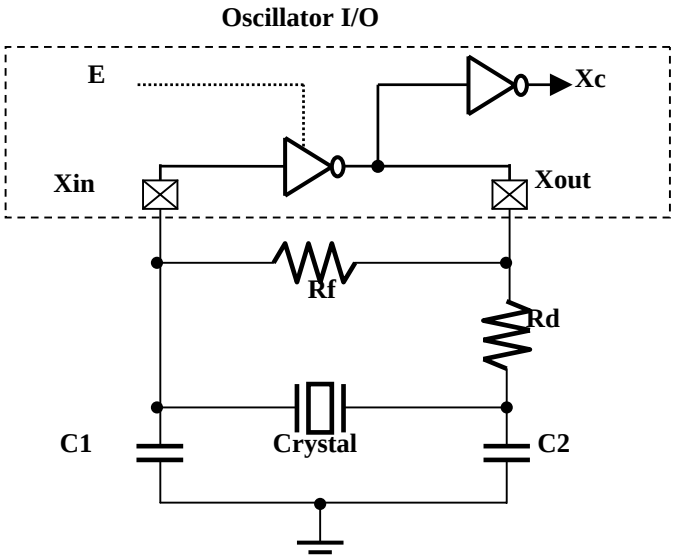


Figure 6.1 Tank Circuit for the Fundamental Mode Oscillation

Figure 6.1 shows several components that are critical to oscillation, where

- *Rf* represents the feedback resistor to bias the inverter in the high gain region. Rf cannot be too low, or the loop may fail to oscillate. Normally, an Rf of 1MOhm is sufficient for MHz band applications.
- *Rd* represents the damping resistor that helps increase stability, save power, and suppress the gain in the high frequency area. The trade-off for inserting Rd is the reduction of negative resistance. Therefore, Rd cannot be too large, or the loop could fail to oscillate. Sometimes users may drop Rd in high frequency applications to reduce production costs.
- *C1 and C2* are decided according to the crystal or resonator CL specification. In the steady state of oscillation, *CL* is defined as (C1 x C2)/(C1+C2). In fact, the I/O ports, the bond pad, and package pin all contribute the parasitic capacitance to C1 and C2. Therefore, we can rewrite CL to be (C1* x C2*)/(C1*+C2*), where C1*=(C1+$C_{in,\ stray}$) and C2*=(C2+$C_{out,\ stray}$). In this example, the required C1 and C2 would be reduced.

This tank circuit is for parallel resonance but not for series resonance. Since C1, C2, Rd, and Rf vary with the crystal specifications and the selected oscillator I/O

cell, there is no single set of component specifications for all applications. For reference values, please contact your TSMC regional FAE with your crystal specifications.

Pin Order

There are two pins labeled “XIN” and “XOUT” for each oscillator I/O cell, and the layout is symmetrical. Sometimes, the cell is mirrored and the pin order of “XIN” and “XOUT” is reversed. When this happens, LVS may not produce an appropriate warning. Although the mirrored oscillator I/O is functionally equivalent, problems could occur in the test mode (bypass mode) because the external clock signal is supposed to trigger “XIN,” not “XOUT”. To prevent this problem, check the pin order carefully when you are dropping text onto the corresponding I/O pin.

Back Annotation

For the oscillator I/O cells, the XC output is derived from the XOUT through an inverting buffer as *Figure* 6.1 shows. Hence, the delay paths are characterized for

(A) XIN → XOUT and (B) XOUT → XC

The path delay for XIN → XC is calculated by the delay of (A) + (B). This characterization is required because the XIN → XC delay depends on both the XOUT load and the XC load. Synopsys tools operate according to this model. That is, XIN → XOUT has one timing table and XOUT → XC has another timing table. If only one table (of XIN → XC) is used, the delay depends only on the XC load, but this is not the real case. Here is an example of a Standard Delay Format (SDF) output by Synopsys:

```
IOPATH  XIN  XOUT  (A1:A1:A1)  (A2:A2:A2)
IOPATH  XOUT  XC   (B1:B1:B1)  (B2:B2:B2)
```

The XIN → XC path delay would be (A2+B1:A2+B1:A2+B1) (A1+B2:A1+B2: A1+B2) when back annotated to Synopsys.

Verilog cannot specify delays from output to output. All delay paths must be from input to output. Therefore, the timing path in Verilog is modeled as XIN → XC instead of XOUT → XC. This causes a back-annotation problem when annotating delays with Synopsys SDF to Verilog. There would be a message: "`SDFA Error: Could not find path XOUT to XC`". The workaround to this problem is to modify the SDF output from Synopsys as shown

below. Users can annotate this SDF correctly in Verilog.

```
IOPATH  XIN  XOUT  (A1:A1:A1)  (A2:A2:A2)
IOPATH  XIN  XC  (A2+B1:A2+B1:A2+B1)  (A1+B2:A1+B2:A1+B2)
```

Bonding Pad Used with Oscillator Cell

Staggered Approach

It is required to connect the PADxN and PADxG to the oscillator I/O cell as shown in *Figure* 6.2.

Note: For universal I/O library, the bonding pads are available from a separate library, called the bond-pad library, where PADxG can be used as the outer bonding pad for staggered approach, while PADxN can be used either as the inner bonding pad for staggered approach or as the linear bonding pad for in-line approach.

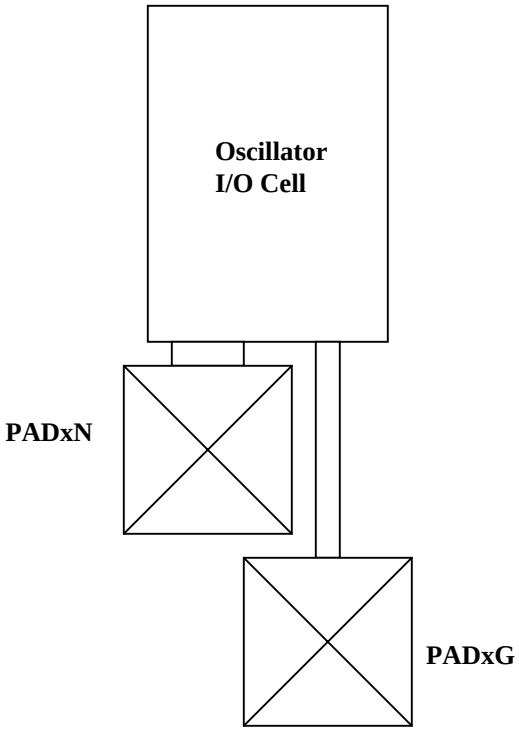


Figure 6.2 Oscillator Cell with Staggered Approach

Linear Approach

It is required to comply with the rule on minimum space between two CB defined in the bond pad design rule manual, slightly shifting two PADxN cells to left and right, and have them connected to the oscillator I/O cell as shown in *Figure* 6.3. It might be required to insert filler cells for in-line approach, depending on the pad-pitch of the bonding pad in use.

Note 1: For universal I/O library, the bonding pads are available from a separate library, called the bond-pad library, where PADxN can be used either as the inner bonding pad for staggered approach or as the linear bonding pad for in-line approach.

Note 2: Please refer to Chapter 7 for the bond-pad usage information.

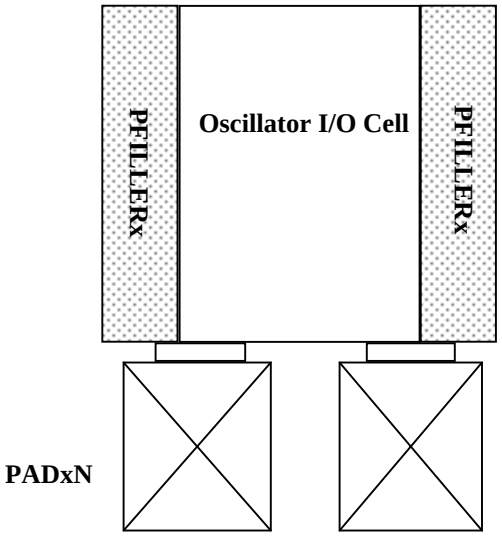


Figure 6.3 Oscillator Cell with Linear Approach

Chapter 7 Accessory Cell Usage

TSMC Universal I/O can be applied to design with different pad pitches by inserting filler cells (***PFILLERx***) in between the I/O cells. The pad pitch can be adjusted by using either the staggered or linear (in-line) bonding style together with inserting the appropriate number of filler cells. This kind of flexible bonding style has been registered by TSMC as ***EZBOND***™.

For the minimum bonding pitch, please refer to TSMC bond pad design rules that are compatible with ***ASE*** bonding rules. Due to the fact that the process and capability of each assembly house varies, please always consult your desired assembly house for their own design rule as well. TSMC will work with customers to resolve any design rule conflicts.

Since TSMC Universal I/O features multi-bonding options that includes the non-CUP Wire Bond, CUP (Circuit under Pad), and RDL (Re-Distribution Layout) Flip Chip, users can refer to Table 7.1 while selecting the back-end kits for the desired bonding options.

Table 7.1 Back-End Kit Directory Name for Different Bonding Options

Bond Pad Options	Universal I/O Back-End Kit	Bond Pad Library Back-End Kit
Non-CUP Wire Bond	mt or mt_2	wb
CUP Wire Bond	mt_2	cup
RDL Flip Chip	mt_2	fc

Attention 1: The library name suffix that contains the character "V" is called the Universal I/O library (e.g. tpz013lgv3), which features multi-bonding capability, including the non-CUP wire bond, CUP (Circuit Under Pad), and RDL Flip Chip. Since it is upon user's decision to choose the desired bonding style, please refer to the entire Chapter 7 for usage guidance.

Attention 2: The non-universal I/O cannot be directly abutted to universal I/O because of different power/ground rail location. To bridge between universal I/O and non-universal I/O, please use the adapter cell available from inter-connection library. Please refer to the last section of this Chapter for details.

Attention 3: All the bond pads for universal I/O library are available from the bond pad library with prefix "tpb", where tpbxxxgv is the bond-bad library for "staggered" universal I/O, and tpbxxxnv is the one for "linear" universal I/O. (For instance, the tpb013gv is the bond pad library dedicated to 0.13µm staggered universal I/O libraries.)

Attention 4: To use TSMC universal standard I/O for metal scheme that includes ultra thick metal "Mu":

- **For universal standard I/O**: Use the GDS under "mt_2" directory and insert dummy metals into the top 2 metal layers to fulfill the "Mu" requirement.
- **For bond pad**: TSMC bond pads cannot yet support "Mu" metal scheme (where u indicates ultra thick). Therefore, you need to modify the bond pad VIA size according to design rule manual followed by DRC / LVS check to ensure error free. It is necessary to change the data type to "Mu" before streaming out the GDS file. If needed, TSMC can modify it through customization service. Note that TSMC plans to provide the ultra-thick metal bond pad in the near future. Please refer to the bond pad library release note for guidance on bond pad selection.

TSMC offers a wide range of I/O bonding options, including the non-CUP Wire Bond, CUP (Circuit Under Pad), and RDL Flip Chip. Please refer to Table 7.2 for information covered in this chapter.

Table 7.2 Information Covered in Chapter 7

Chapter 7	**Non-CUP Wire-Bond I/O**	Staggered Bonding Style
		Linear Bonding Style
		How to Apply the Back-End Kits
	Circuit Under Pad (CUP) I/O	Staggered Bonding Style
		Linear Bonding Style
		How to Apply the Back-End Kits
	Flip Chip I/O	RDL Flip Chip
		How to Apply the Back-End Kits
	Filler Cell/Corner Cell/Power-Cut Cell	How to Use Filler/Corner/Power-Cut Cells
	Adapter Cell	How to Bridge between TSMC Universal Standard I/O and other TSMC IP

Non-CUP Wire-Bond I/O

Customer can apply either in-line bonding style or staggered bonding style to the non-CUP wire bond I/O.

Staggered Bond Style

Inner and outer pads are for staggered bonding. The outer pad PADxG / PADxGM is taller. The inner pad PADxN / PADxNM is shorter. These bonding pads are not embedded in the driving buffers because of the size difference. Users should attach the appropriate bonding pads to the I/O driving buffers with the PR boundary aligned with each other. These bonding pads are placed in the repeated sequence of inner and outer pads. The pattern is repeated until all the bonding pads are placed.

Note: **PADxGM** & **PADxNM** are the bond pads with top two thick metals and top two large VIAs for 0.13µm/0.15µm/0.18µm universal standard I/O. For 90nm & other advanced technologies, because of complex metallization options, you will not find **PADxGM** & **PADxNM** bond pads in the bond pad library. Instead, you can only see **PADxG** & **PADxN** bond pads under each specific back-end directory that is named by metallization options. For example, you can find **PADxG** & **PADxN** GDS from 9M_6X2Z directory, where 9M indicates 9 metal layer; 6X2Z indicates 6 metal layers with X metallization and top 2 metal layers with Z metallization.

Linear Bond Style

For linear (in-line) bonding, users can select PADxN/PADxNM based on target chip size and Electro Migration (EM) capacity. Please refer to Chapter 8 for details on EM.

Figure 7.1 shows how to realize EZBOND™ I/O using filler cells together with the non-CUP wire-bond I/O buffers. Note that more filler cells can be inserted to increase the bonding pad pitch.

(Continued on the following page)

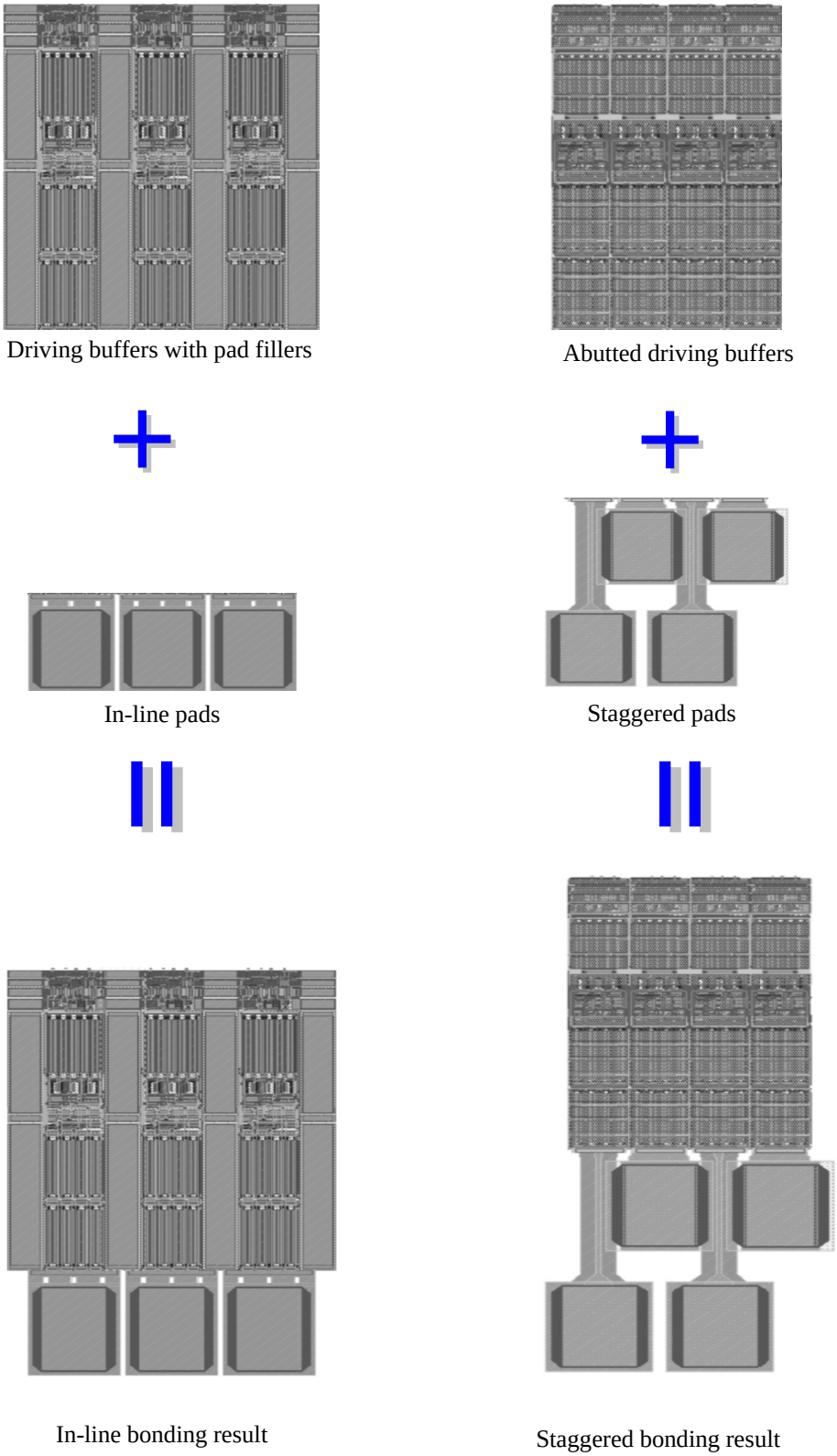


Figure 7.1 Flexible Bonding Style with Non-CUP Wire-Bond I/O

How to Apply the Back-End Kits

Universal I/O Back-End Kit Structure

Universal I/O features multi-bonding-style options, including the non-CUP wire bond, circuit under pad (CUP); RDL flip chip. To fulfill different types of bonding options, there are two directories under the back-end kits to meet different needs, which are mt (metal top) and mt_2 (metal top – 2), where "mt" directory is dedicated to the non-CUP wire bond application. As shown in Table 7.3, based on technology type, each "mt" directory offers a wide range of metal layer options within the back-end kits.

Table 7.3 "mt" Metal Layer Table (For Non-CUP Wire Bond)

Process	4lm	5lm	6lm	7lm	8lm	9lm	10lm
CL018	V	V	V				
CL015	V	V	V	V			
CL013	V	V	V	V	V		
CLN90	V	V	V	V	V	V	
CLN65	V	V	V	V	V	V	
CLN45		V	V	V	V	V	V
CLN40		V	V	V	V	V	V

The "mt_2" directory can be applicable to the non-CUP wire bond I/O with top 2 thick metals. All users have to do is adopt back-end kits from mt_2 directory and insert dummy metals in the top 2 metal layers. For example, to tape out with 6 metal layers in 90nm technology with top two thick metals, you need to access mt_2 directory and adopt the 6lm gds where metal 6 and metal 5 are empty. Then insert dummy metals as metal 5 and metal 6. As shown in Table 7.4, based on technology type, each "mt_2" directory offers a range of metal layer options within the back-end kits.

Table 7.4 "mt_2" Metal Layer Table (For Non-CUP Wire Bond with Top 2 Thick Metals)

Process	4lm	5lm	6lm	7lm	8lm	9lm	10lm
CL018		V	V				
CL015		V	V	V			
CL013		V	V	V	V		
CLN90		V	V	V	V	V	
CLN65		V	V	V	V	V	
CLN45		V	V	V	V	V	V
CLN40		V	V	V	V	V	V

Note: To tape out the non-CUP wire bond I/O with top 2 thick metals, it is required to insert the routing blockage layers in the top two metals.

Bond Pad Library Back-End Kit Structure

All the bond pads for universal I/O library are available from the bond pad library with the prefix “tpb”, where

- tpbxxxgv is the bond-pad library for “staggered” universal I/O
- tpbxxxnv is the bond-pad library for “linear” universal I/O.

(For instance, the tpb013gv is the bond pad library dedicated to 0.13µm staggered universal I/O library; whereas the tpb013nv is the bond pad library dedicated to 0.13µm linear universal I/O library.)

There are two types of bonding pads for non-CUP wire bond application:
(available from the “wb” directory)

- PADxN / PADxNM: used as inner pad for staggered approach or in-line pad for linear approach.
- PADxG / PADxGM: used as outer pad for staggered approach.
- For 0.13µm/0.15µm/0.18µm application with top two thick metals and top two large VIAs, it is required to use the bond pad with suffix “M”. For instance, you need to use PADxNM as an inner pad for staggered approach or in-line pad for linear approach. Similarly, you need to use PADxGM as the outer pad for staggered approach. **However, DO NOT mix PADxN with PADxNM; DO NOT mix PADxG with PADxGM at the same time.**
- For 90nm & other advanced technologies, because of complex metallization options, you will not find PADxGM & PADxNM bond pads in the bond pad library. Instead, you can only see PADxG & PADxN bond pads under each specific back-end directory that is named by metallization options. For example, you can find PADxG & PADxN GDS from 9M_6X2Z directory, where 9M indicates 9 metal layer; 6X2Z indicates 6 metal layers with X metallization and top 2 metal layers with Z metallization.

Figure 7.2 shows where to locate the non-CUP wire-bond bond pads for 0.13µm/0.15µm/0.18µm universal standard I/O library; *Figure* 7.3 shows where to locate the non-CUP wire-bond bond pads for 90nm or advanced universal standard I/O library.

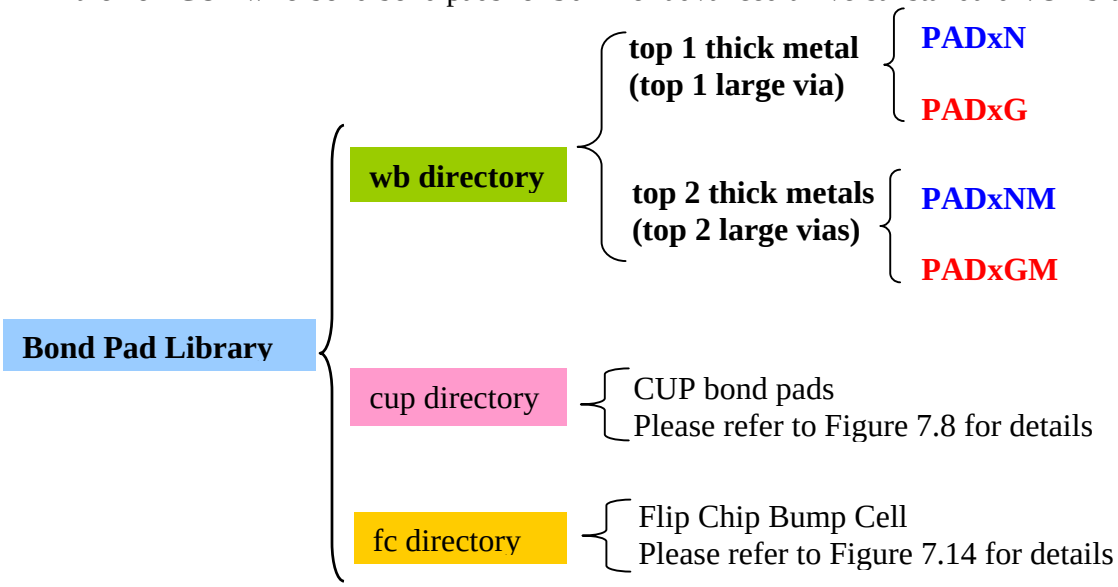


Figure 7.2 The Non-CUP Wire-Bond Bond Pads for 0.13µm/0.15µm/0.18µm Universal Standard I/O Library

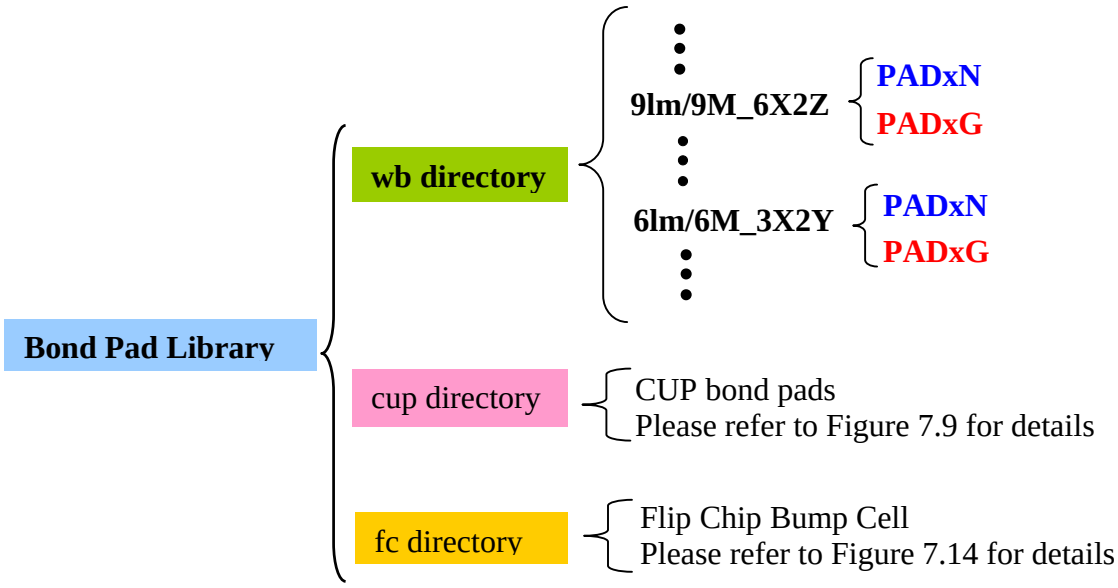


Figure 7.3 The Non-CUP Wire-Bond Bond Pads for 90nm/65nm/45nm/40nm Universal Standard I/O Library

Table 7.5 shows the tape-out layer option for the PADxN(M) / PADxG(M) cells.

Table 7.5 "WB" Metal Layer Table (For Non-CUP Wire Bond I/O)

Process	4lm	5lm	6lm	7lm	8lm	9lm	10lm
CL018	V	V	V				
CL015	V	V	V	V			
CL013	V	V	V	V	V		
CLN90	V	V	V	V	V	V	
CLN65	V	V	V	V	V	V	
CLN45		V	V	V	V	V	V
CLN40		V	V	V	V	V	V

For example, to tape out 6 layer metal gds with one top thick metal and one top large VIA in 0.13µm:

- For the I/O cell, use 6lm gds under "mt" directory within the gds kit.
- For the bond pad, use 6lm gds under "wb" directory within the gds kit.

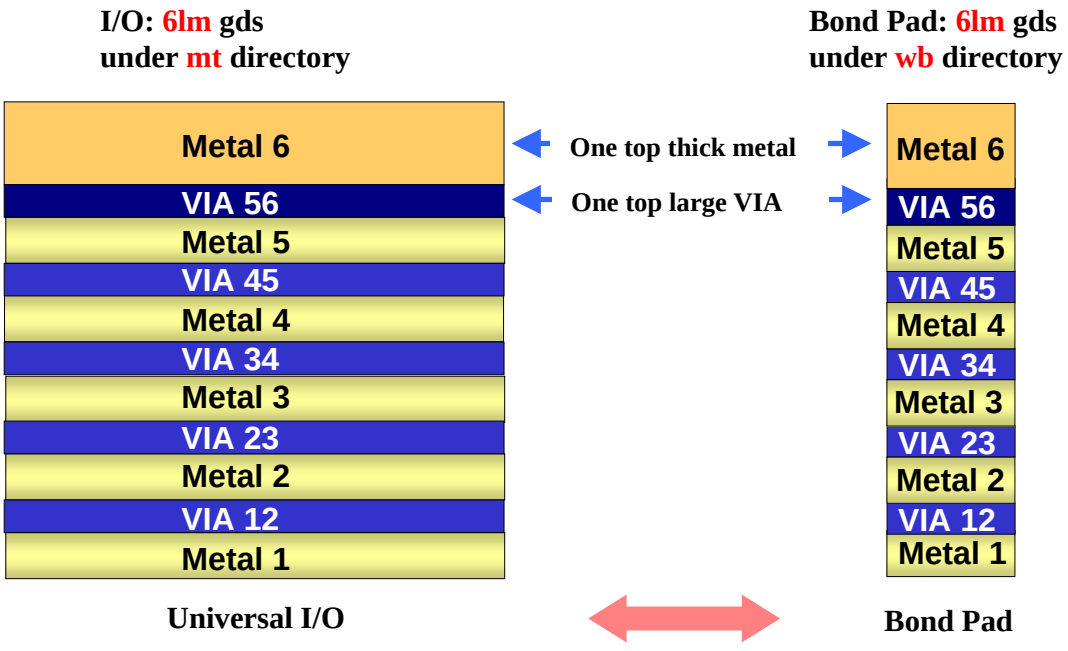


Figure 7.4 Illustration of GDS Kit Under "mt" and "wb" Directories for 0.18µm/0.15µm/0.13µm Non-CUP Wire Bond Application

For example, to tape out 6 layer metal gds with top two thick metals and top two large VIAs in 0.13µm:

- For the I/O cell, use 6lm gds under "mt_2" directory within the back-end kit, where 6lm gds only contains metal 1 to metal 4. Then insert dummy metals on top of metal 4 as metal 5 and 6.
- For the bond pad, use 6lm gds under "wb" directory within the back-end kit, and adopt the bond pad name with suffix "M", which indicates that this bond pad comes with top two thick metals and top two large VIAs.

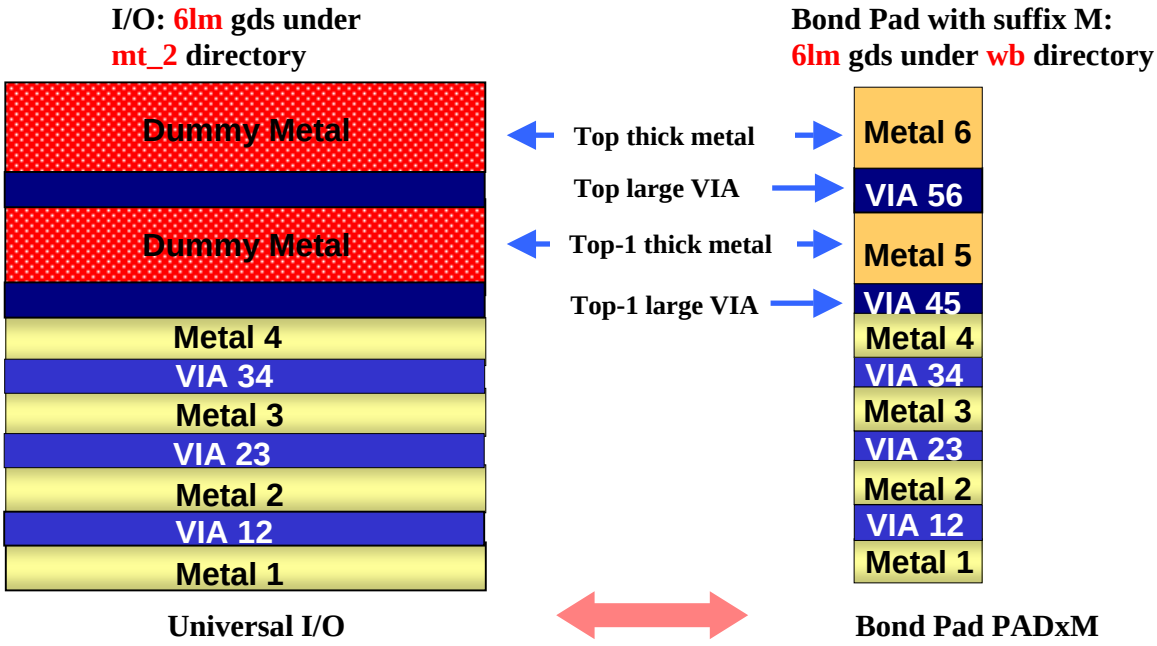


Figure 7.5 Illustration of GDS Kit Under "mt_2" and "wb" Directories for 0.18µm/0.15µm/0.13µm Non-CUP Wire Bond Application with Top Two Thick Metals

Note: For 90nm & other advanced technologies, because of complex metallization options, you would not find PADxGM & PADxNM bond pads in the bond pad library. Instead, you can only see PADxG & PADxN bond pads under each specific back-end directory that is named by metallization options. For example, you can find PADxG & PADxN GDS from 9M_6X2Z directory, where 9M indicates 9 metal layer; 6X2Z indicates 6 metal layers with X metallization and top 2 metal layers with Z metallization. Please refer to Figure 7.3 for illustration.

Circuit Under Pad (CUP)

This section provides information about the following topics:

- Circuit Under Pad (CUP) I/O usage.
- Features.
- Bonding type structures.

Circuit Under Pad (CUP) I/O Usage

CUP I/O is the I/O with bond pad over the I/O body itself. The pad pin is located close to the center of the I/O body for easier routing, signal integrity, and space saving purposes. It is required to place the CUP bond pad over the I/O body and have it connected to the pin. In addition, make sure that the PR boundary originates at the (0,0) coordinate.

Table 7.6 shows the minimal total number of layers for both Pad and I/O while using the CUP structure.

Table 7.6 Minimal Numbers of Layers by Technology

Technology	Minimal No. of Layers (Pad + I/O)
0.18 µm	5
0.15 µm	5
0.13 µm	5
N 90	5
N 65	5
N 45	6
N 40	6

Feature

Using the CUP I/O can substantially reduce the die size since the bonding pad does not take any extra space in addition to the I/O body itself.

Bonding Type Structures

Similar to the bonding pad structures of non-CUP wire bond I/O, CUP I/O also comes with the staggered bonding pad approach and linear bonding pad approach.

Note: If customers intend to implement universal I/O with CUP and Non-CUP Wire Bond applications on the same chip, I/O body needs to be based on “mt_2” structure for consistency. However, customers need to insert dummy metals in the top 2 layers of the non-CUP wire bond region.

Staggered Bond Style

Inner and outer pads are for staggered bonding. The inner pad PADxNU/PADxNMU is taller while the outer pad PADxGU/PADxGMU is shorter in phantom view. These bonding pads are not embedded in the driving buffers because of the size difference. Users should attach the appropriate bonding pads to the I/O driving buffers with the PR boundary aligned with each other at origin (0, 0). These bonding pads are placed in the repeated sequence of inner and outer pads. The pattern is repeated until all the bonding pads are placed.

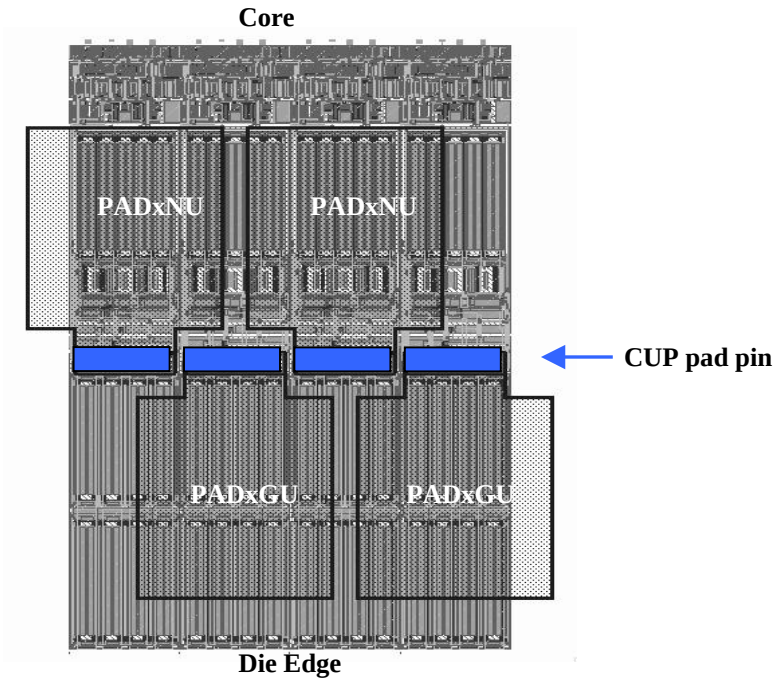


Figure 7.6 Staggered Bonding Approach Using CUP I/O

Linear Bond Style

For linear (in-line) bonding, users need to select PADxNU/PADxNMU. These bonding pads are not embedded in the driving buffers because of size difference. Users should attach the appropriate bonding pads to the I/O driving buffers with the PR boundary aligned with each other at origin (0, 0).

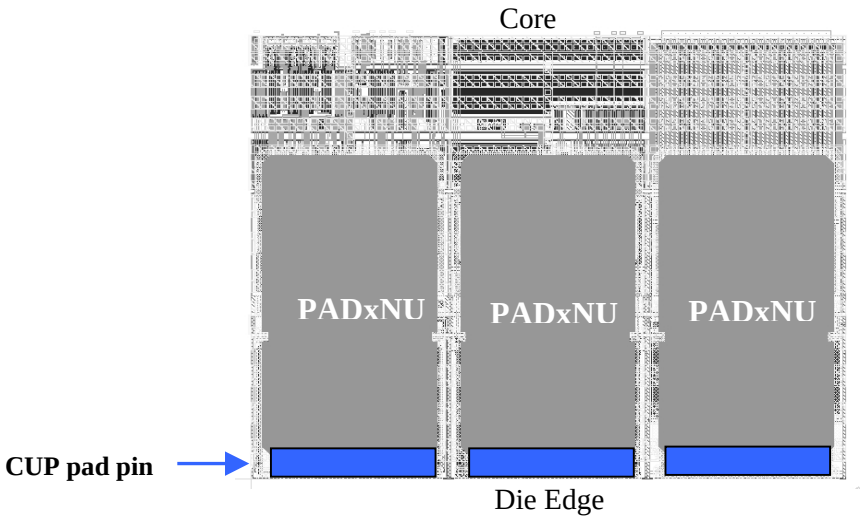


Figure 7.7 Linear Bonding Approach Using CUP I/O

How to Apply the Back-End Kits

Universal I/O Back-End Kit Structure

Universal I/O features multi-bonding-style options, including the non-CUP wire bond, circuit under pad (CUP); RDL flip chip. To fulfill different types of bonding options, there are two back-end directories to meet different needs, which are mt (metal top) and mt_2 (metal top – 2), where “mt_2” directory is suitable for the CUP I/O users. As shown in Table 7.7, based on technology type, each “mt_2” directory offers a wide range of metal layer options within the back-end kits.

Table 7.7 "mt_2" Metal Layer Table (For CUP I/O)

Process	4lm	5lm	6lm	7lm	8lm	9lm	10lm
CL018		V	V				
CL015		V	V	V			
CL013		V	V	V	V		
CLN90		V	V	V	V	V	
CLN65		V	V	V	V	V	
CLN45			V	V	V	V	V
CLN40			V	V	V	V	V

Note: For CUP I/O users, it is required to insert the routing blockage layers in the top two metals first, and then route the internal signal afterwards.

Bond Pad Library Back-End Kit Structure

All the bond pads for universal I/O library are available from the bond pad library with the prefix "tpb", where

- tpbxxxgv is the bond-bad library for "staggered" universal I/O
- tpbxxxnv is the bond-pad library for "linear" universal I/O.

(For instance, the tpb013gv is the bond pad library dedicated to 0.13µm staggered universal I/O library; whereas the tpb013nv is the bond pad library dedicated to 0.13µm linear universal I/O library.)

There are two types of bonding pads for CUP application:
(available from the "cup" directory)

- PADxNU / PADxNMU: used as inner pad (with respect to core) for staggered approach or in-line pad for linear approach.
- PADxGU / PADxGMU: used as outer pad (with respect to core) for staggered approach.
- For 0.13µm/0.15µm/0.18µm application with top two thick metals and top two large VIAs, it is required to use the bond pad with suffix "MU". For instance, use PADxNMU as an inner pad for staggered approach or in-line pad for linear approach. Similarly, use PADxGMU as the outer pad for staggered approach. **However, DO NOT mix PADxNU with PADxNMU; DO NOT mix PADxGU with PADxGMU at the same time.**
- For 90nm & other advanced technologies, because of complex metallization options, you cannot find PADxGMU & PADxNMU bond pads in the bond pad

library. Instead, you can only see PADxGU & PADxNU bond pads under each specific back-end directory that is named by metallization options. For example, you can find PADxGU & PADxNU GDS from 9M_6X2Z directory, where 9M indicates 9 metal layer; 6X2Z indicates 6 metal layers with X metallization and top 2 metal layers with Z metallization.

Figure 7.8 shows where to locate the CUP bond pads for 0.13µm/0.15µm/0.18µm universal standard I/O library; *Figure* 7.9 shows where to locate the CUP bond pads for 90nm or advanced universal standard I/O library.

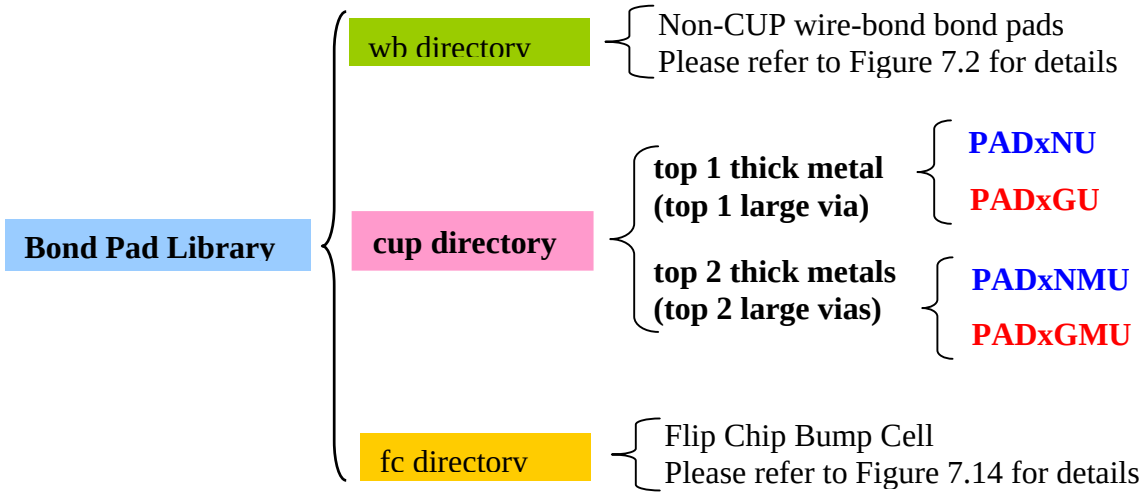


Figure 7.8 The CUP Bond Pads for 0.13µm/0.15µm/0.18µm Universal Standard I/O Library

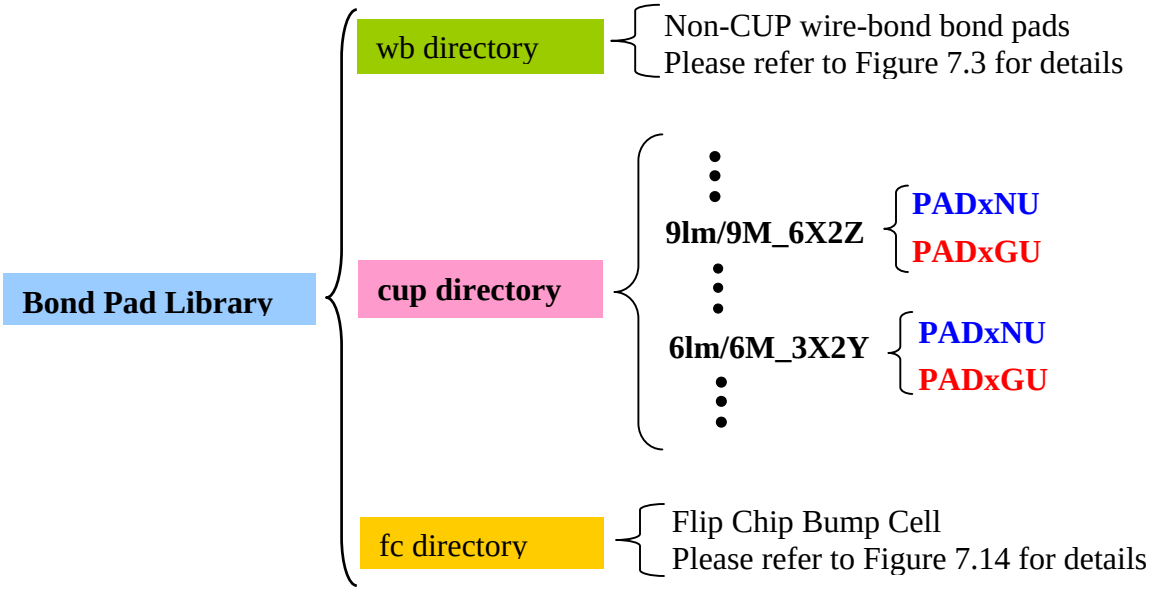


Figure 7.9 The CUP Bond Pads for 90nm/65nm/45nm/40nm Universal Standard I/O Library

Table 7.8 shows the tape-out layer option for the PADxN(M)U / PADxG(M)U cells.

Table 7.8 "CUP" Metal Layer Table (For CUP I/O)

Process	4lm	5lm	6lm	7lm	8lm	9lm	10lm
CL018		V	V				
CL015		V	V	V			
CL013		V	V	V	V		
CLN90		V	V	V	V	V	
CLN65		V	V	V	V	V	
CLN45			V	V	V	V	V
CLN40			V	V	V	V	V

For example, to tape out 6 layer metal gds with one top thick metal and one top large VIA in 0.13µm:

- For the I/O cell, use 6lm gds under "mt_2" directory within the gds kit, where 6lm gds contains metal 1 to metal 4.
- For the bond pad, use 6lm gds under "cup" directory within the gds kit, where 6lm gds contains metal 5 to metal 6.

Please refer to *Figure* 7.10 for illustration.

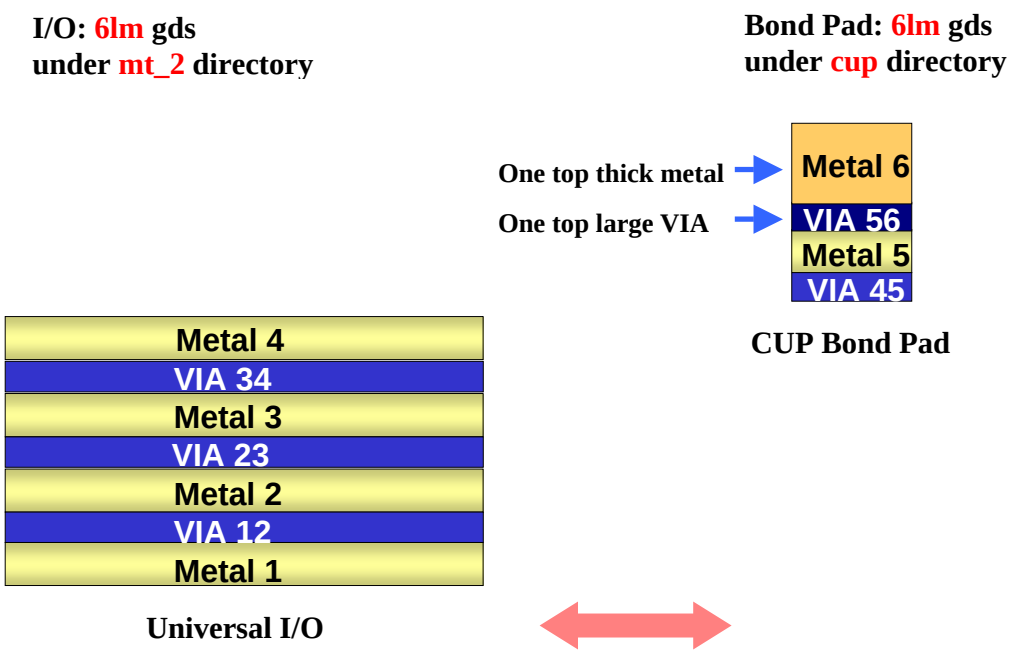


Figure 7.10 Illustration of GDS Kit Under "mt_2" and "cup" Directories for 0.18µm/0.15µm/0.13µm CUP Application

To tape out 6 layer metal gds with top two thick metals and top two large VIAs in 0.13µm:

- For the I/O cell, use 6lm gds under "mt_2" directory within the gds kit, where 6lm gds contains metal 1 to metal 4.
- For the bond pad, use 6lm gds under "cup" directory within the gds kit, where 6lm gds contains metal 5 to metal 6. It is required to adopt the bond pad name with suffix "M", which indicates that this bond pad comes with top two thick metals and top two large VIAs.

Please refer to *Figure* 7.11 for illustration.

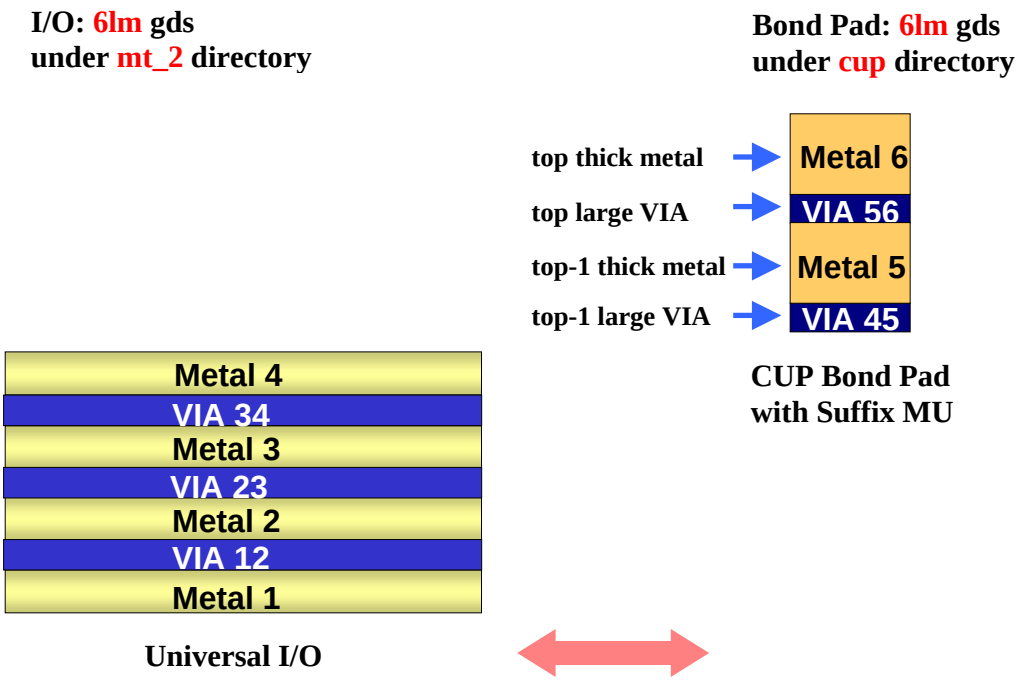


Figure 7.11 Illustration of GDS Kit Under "mt_2" and "cup" Directories for 0.18µm/0.15µm/0.13µm CUP Application with Top Two Thick Metals and Top Two Large VIAs

Note: For 90nm & other advanced technologies, because of complex metallization options, you will not find PADxGMU & PADxNMU bond pads in the bond pad library. Instead, you can only see PADxGU & PADxNU bond pads under each specific back-end directory that is named by metallization options. For example, you can find PADxG & PADxN GDS from 9M_6X2Z directory, where 9M indicates 9 metal layer; 6X2Z indicates 6 metal layers with X metallization and top 2 metal layers with Z metallization. Please refer to Figure 7.9 for illustration.

Flip Chip I/O

Flip Chip, the direct electrical connection of face down (hence "flipped") electronic components onto the substrate, with benefits in comparison with the non-CUP wire bond as follows:

- Reduce the required board area.
- Reduce the inductance and capacitance of connections and shortens the path, greatly improving the accuracy of impedance control.
- Provide excellent heat dissipating channel by using bumps.

This section provides information on the following topics:

Flip Chip	**RDL (Re-Distribution Layout) Flip Chip**	Double I/O Rings
		How to Apply the Back-End Kits

RDL (Re-Distribution Layout) Flip Chip

Double I/O Rings

To considerably reduce the die size, users may consider adopting the double I/O rings using the RDL flip chip option.

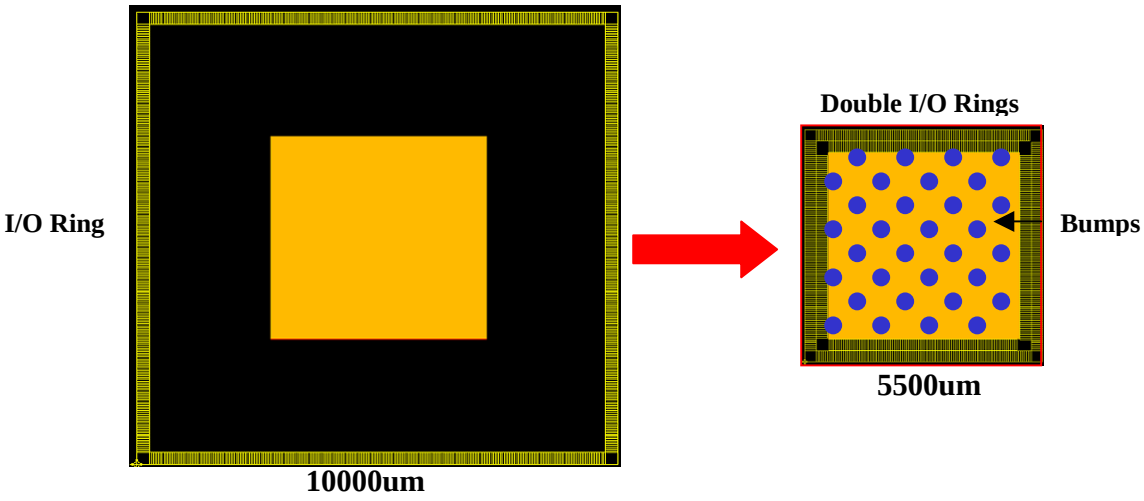


Figure 7.12 Illustration of Double I/O Rings Using the RDL Flip Chip I/O

Note 1: The back-end kits of universal I/O library for flip-chip application are available from “mt_2” directory.

Note 2: For place-and-route, it is required to closely follow the steps below to ensure signal integrity.

- **First**, route the I/O signal.
- **Second**, insert the routing blockage layers in the top two metals. (Note: By default, routing is not blocked in the top two metals.
- **Finally**, route the internal signal afterwards.

Note 3: At least one layer should be reserved for routing from the outer I/O ring to core. Please refer to *Figure* 7.13 for reference.

Note 4: Use MD and top two metals for RDL routing while completing RDL routing in one layer cannot be realized.
Reminder: For AP RDL, it is prohibited to use the wire-bond (i.e. CUP or non-CUP) bond pad together with the flip-chip bump cell at the same time. You can adopt either the AP layer of wire-bond bond pad or the AP layer of flip-chip bump for AP RDL.

Note 5: For latch-up prevention, it is required to closely follow the allowable spacing between the inner I/O ring and the outer I/O ring stated in the *TSMC Design Rule Manual*.

Note 6: The number of I/O power/ground cells and bumps should be based on SSO factors.

Note 7: The I/O power/ground bumps should be placed in groups for better package routability.

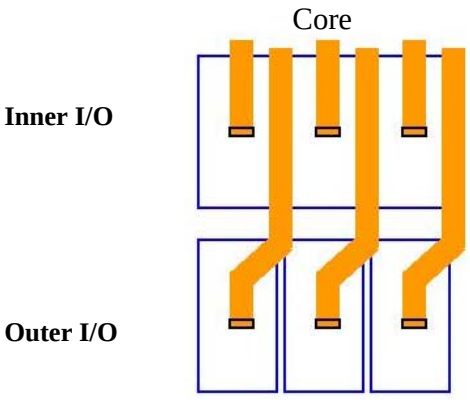


Figure 7.13 Illustration of Routing from the Double I/O Ring to Core

How to Apply the Back-End Kits

Universal I/O Back-End Kit Structure

Universal I/O features multi-bonding options, including the non-CUP wire bond, circuit under pad (CUP); RDL flip chip. To fulfill different types of bonding options, there are two back-end directories to meet different needs, which are mt (metal top) and mt_2 (metal top – 2), where "mt_2" directory is suitable for RDL flip-chip application. As shown in *Table* 7.9, based on technology type, each "mt_2" directory offers a range of metal layer options within the back-end kits.

Table 7.9 "mt_2" Metal Layer Table (For Flip-Chip I/O)

Process	4lm	5lm	6lm	7lm	8lm	9lm	10lm
CL018		V	V				
CL015		V	V	V			
CL013		V	V	V	V		
CLN90		V	V	V	V	V	
CLN65		V	V	V	V	V	
CLN45			V	V	V	V	V
CLN40			V	V	V	V	V

Bond Pad Library Back-End Kit Structure

All the bond pads for universal I/O library are available from the bond pad library with the prefix "tpb", where

- tpbxxxgv is the bond-bad library for "staggered" universal I/O
- tpbxxxnv is the bond-pad library for "linear" universal I/O.

(For instance, the tpb013gv is the bond pad library dedicated to 0.13µm staggered universal I/O library, whereas the tpb013nv is the bond pad library dedicated to 0.13µm linear universal I/O library.)

However, not all the bond-pad libraries offer "bump". If bump is offered, it is available from the "fc" directory within the back-end kits.

- PADxB: used as bump for flip-chip applications, where x is the UBM size.
- Please refer to the bond pad design rule manual to choose the bump cell with the desirable UBM width based on your application need.

Figure 7.14 shows where to locate the flip chip bump cell for universal standard I/O library.

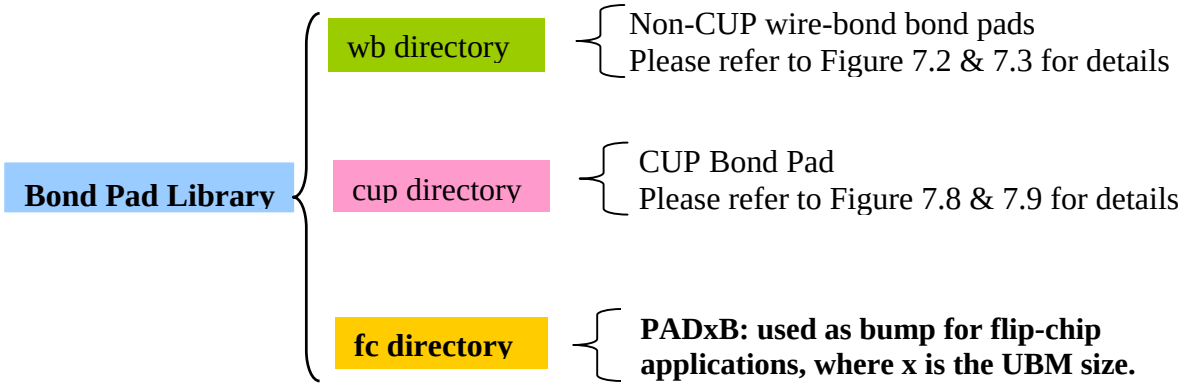


Figure 7.14 The Flip-Chip Bump Cell for Universal I/O Library

Note 1: Please refer to the library release note for bump cell selection and the required tape-out layers.

Note that the bump cells in some of the TSMC bond pad libraries (depending on process technology) are the "combo" bump, which includes the tape-out layers for AP RDL, MD RDL, and Ground-Up applications. As such, do not tape out the whole layers of TSMC combo bump, but closely follow the instructions in library release note and delete the unnecessary layers from GDS for your desired flip-chip application.

Note 2: It is required to run DRC & LVS checks before tape-out to ensure layer correctness.

Note 3: For AP RDL, it is prohibited to use the wire-bond (i.e. CUP or non-CUP) bond pad together with the flip-chip bump cell at the same time. You can adopt either the AP layer of wire-bond bond pad or the AP layer of flip-chip bump for AP RDL.

Filler Cell / Corner Cell / Power-Cut Cell

It is required to insert the fat fillers first and then the thin fillers afterwards. To avoid the metal-slot-rule violation, do not only use thin filler cells to fill large I/O spacing. For example, use one 20µm pitch filler cell (PFILLER20) and one 10µm pitch filler cell (PFILLER10) instead of using 6 “5µm pitch” filler cells (PFILLER5) to fill 30µm spacing. In addition, if spacing is larger than one cell pitch, you need to first insert core power cell PVDD1DGZ/CDG and I/O power cell PVDD2DGZ/CDG; then, insert filler cells to fill up the rest of spacing for ESD robustness.

Front-end kits, such as Verilog and Synopsys, contain no filler cells (PFILLERx), no power-cut cell (PRCUT), nor corner cells (PCORNERx). However, back-end kits, such as Apollo, Silicon Ensemble, and GDSII, do contain filler, power-cut cell, and corner cell. In back-end kits, these cells have power/ground bus connections, but no pins, transistors, nor functions. Please do not include these cells in your netlist for simulation, but instantiate them when doing the physical layout.

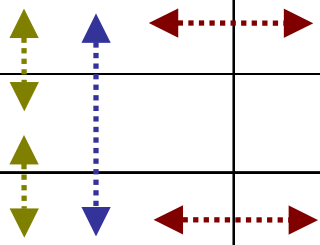
Note: For the power-cut cell (PRCUT) usage information, please refer to page 73 and 74 for details.

Adapter Cell

TSMC offers various types of adapter cells suitable for the following applications:

- To bridge between staggered universal standard I/O and TSMC specialty I/O.
- To bridge between linear universal standard I/O and TSMC specialty I/O
- To bridge between staggered universal standard I/O and staggered non-universal standard I/O
- To bridge between linear universal standard I/O and linear non-universal standard I/O
- To bridge between staggered universal standard I/O and linear universal standard I/O

Table 7.10 How to Bridge between Different Types of TSMC I/O Cells

Library Type	Universal I/O	Non-Universal I/O
Staggered		
Specialty I/O		
Linear		

Staggered universal standard I/O + PRADPT190/185 + PRADPT + PRADPT120/115 + linear universal standard I/O

Staggered universal standard I/O + PRBRIG190/185 + staggered non-universal standard I/O. Or linear universal standard I/O + PRBRIG120/115 + linear non-universal standard I/O

Staggered universal standard I/O + PRADPT190/185 + PRADPT + specialty I/O adapter cell + universal-based specialty I/O. Or linear universal standard I/O + PRADPT120/115 + PRADPT + specialty I/O adapter cell + universal-based specialty I/O

Note1: Please download the **tpi***nv** or **tpi***gv** bridge library (where *** is the technology code) for the interface adapter cells.

Note2: The **tpi***nv** is the bridge library for linear universal standard I/O; whereas the **tpi***gv** is the bridge library for staggered universal standard I/O.

How to Use TSMC Staggered Universal Standard I/O with TSMC Universal-Based Specialty I/O

- PRADPTx is the adapter cell to bridge between universal standard I/O with "x" µm cell height and PRADPT universal adapter cell. For example, PRADPT190 is the adapter cell to bridge between the universal standard I/O with 190µm cell height and the PRADPT cell.
- Both PRADPTx and PRADPT cells are provided in the "**tpi**" bridge library, where **tpi***gv** is the bridge library for staggered universal standard I/O.

  Note: * denotes technology code. For example, 013 is the technology code for 0.13µm process.

To bridge TSMC staggered universal standard I/O cell with TSMC specialty I/O cell, it is required to follow the steps as mentioned below:

Step 1: Turn on the cell view / layout view for PRADPTx adapter cell first, where "x" is the universal standard I/O cell height.

Step 2: For PRADPTx adapter cell, place the side whose bus height is compatible with the universal standard I/O bus height right next to the universal standard I/O cell as illustrated in *Figure* 7.15.

If you would like to insert filler cell between the Universal Standard I/O cell and the PRADPTx adapter cell, do not insert filler cell whose cell width is less than 1µm.

Figure 7.15 Place PRADPTx Cell Next To Universal Standard I/O Cell

Step 3: For PRADPTx adapter cell, place the other side right next to the PRADPT universal adapter cell as illustrated in *Figure* 7.16.

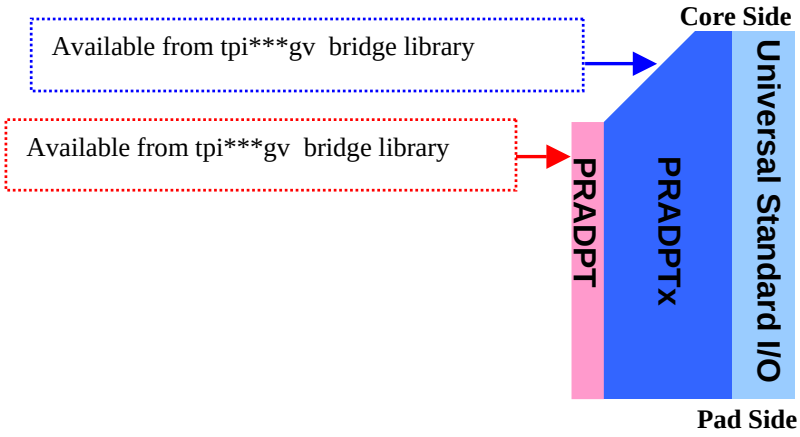


Figure 7.16 Place PRADPT Cell Next To The Other Side of PRADPTx Cell

Step 4: For how to place specialty I/O cells, please refer to specialty I/O application note for details.

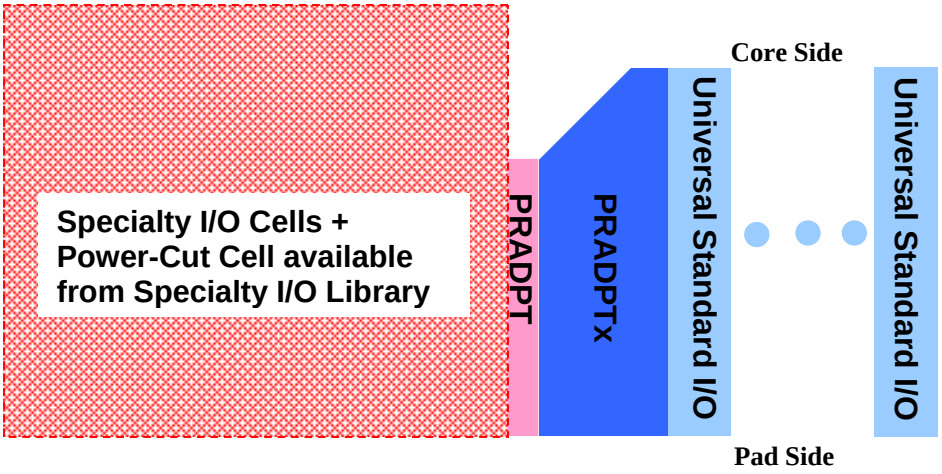


Figure 7.17 Place Cells from Specialty I/O Library

Note 1: Customer can also mirror the PRADPTx adapter cell from right to left to place Universal Standard I/O and Specialty I/O in an opposite direction, as illustrated in *Figure* 7.18.

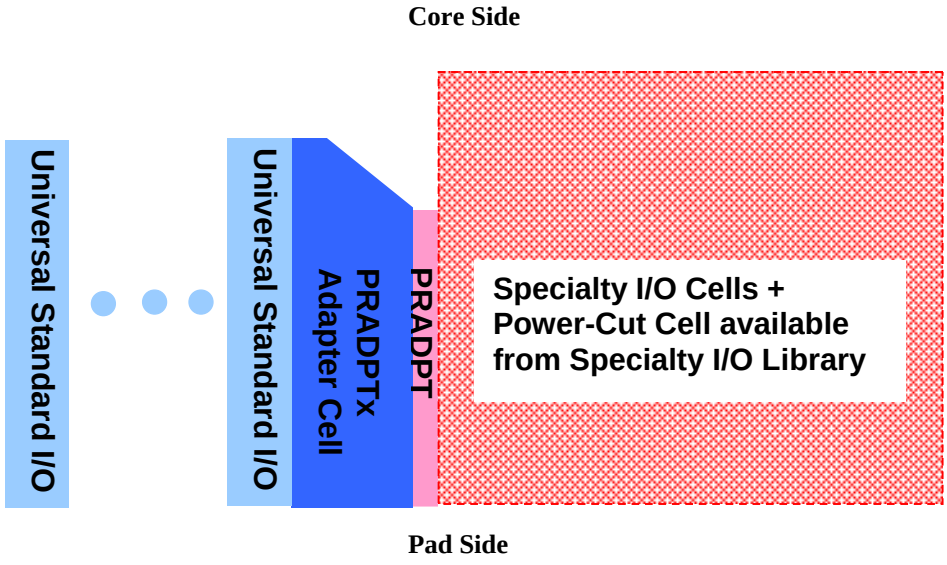


Figure 7.18 Mirror PRADPTx Cell to Place Universal Standard I/O and Specialty I/O in An Opposite Direction

Note 2: Placing the Universal Standard I/O Cell to the wrong side of PRADPTx adapter cell would result in DRC/LVS errors.

How to Use TSMC Linear Universal Standard I/O with TSMC Specialty I/O

- PRADPTx is the adapter cell to bridge between universal standard I/O with "x" µm cell height and PRADPT universal adapter cell. For example, PRADPT120 is the adapter cell to bridge between the universal standard I/O with 120µm cell height and the PRADPT cell.
- Both PRADPTx and PRADPT cells are provided in the "**tpi**" bridge library, where **tpi***nv** is the bridge library for linear universal standard I/O.

  Note: *** denotes the technology code. For example, 013 is the technology code for 0.13µm process

To bridge TSMC linear universal standard I/O cell with TSMC specialty I/O cell, it is required to follow the steps as mentioned below:

Step 1: Turn on the cell view / layout view for PRADPTx adapter cell first, where "x" is the universal standard I/O cell height.

Step 2: For PRADPTx adapter cell, place the right side next to the universal standard I/O cell as illustrated in *Figure* 7.19.

If you would like to insert filler cell between the Universal Standard I/O cell and the PRADPTx adapter cell, do not insert filler cell whose cell width is less than 1µm.

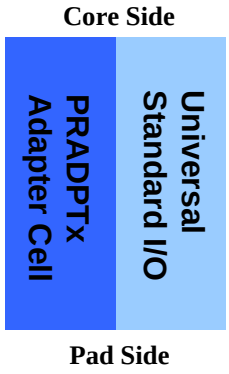


Figure 7.19 Place PRADPTx Cell Next To Universal Standard I/O Cell

Step 3: Place PRADPT universal adapter cell to the left side of PRADPTx cell as illustrated in *Figure* 7.20.

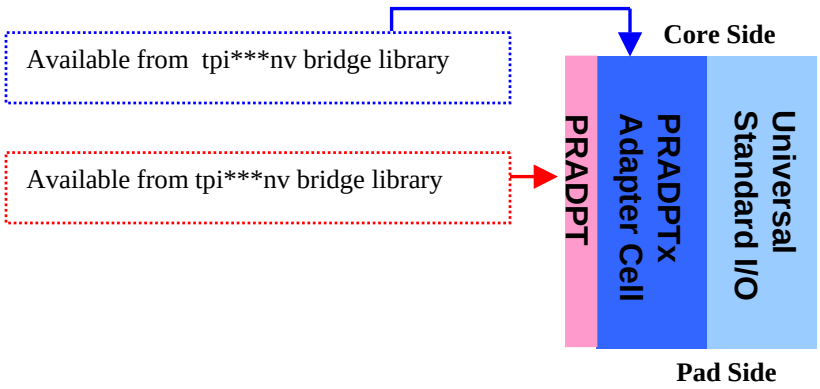


Figure 7.20 Place PRADPT Cell Next To The Other Side of PRADPTx Cell

Step 4: For how to place specialty I/O cells, please refer to specialty I/O application note for details. *Figure* 7.21 is an illustration.

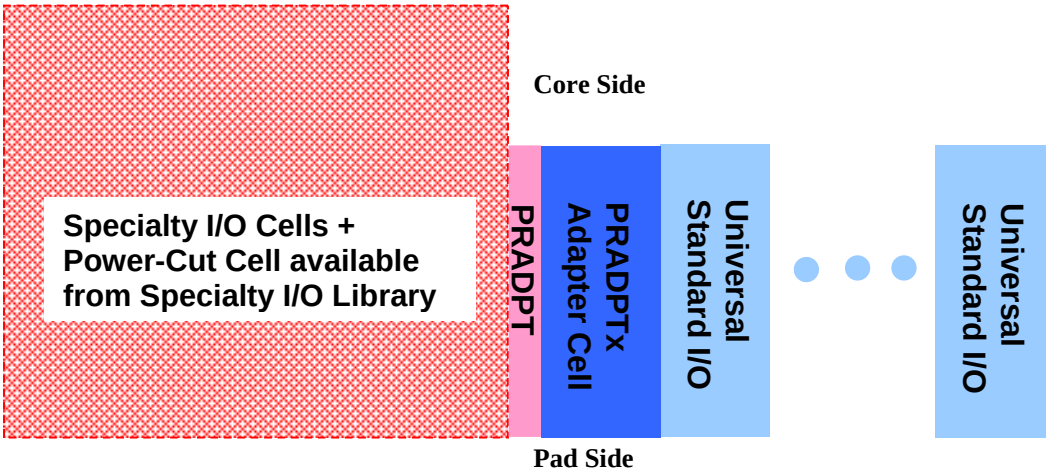


Figure 7.21 Place Cells from Specialty I/O Library

Note 1: Customer can also mirror the PRADPTx adapter cell from right to left to place Universal Standard I/O and Specialty I/O in an opposite way, as illustrated in *Figure* 7.22.

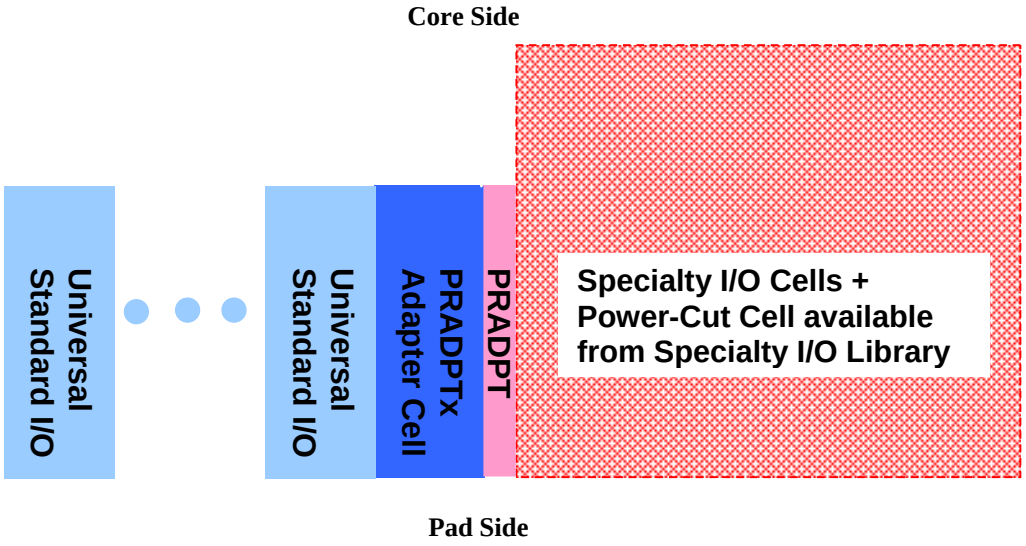


Figure 7.22 Mirror PRADPTx Cell to Place Universal Standard I/O and Specialty I/O in An Opposite Direction

Note 2: Placing the Universal Standard I/O Cell to the wrong side of PRADPTx adapter cell would result in DRC/LVS errors.

How to Bridge between TSMC Linear Universal Standard I/O and TSMC Staggered Universal Standard I/O

Step 1: Use PRADPT190/PRADPT185 from **tpi***gv** inter-connection library, and have its one side placed right next to staggered universal standard I/O cells.

Step 2: Use PRADPT120/PRADPT115 from **tpi***nv** inter-connection library, and have its one side right placed next to linear universal standard I/O cells.

Step 3: Have the other side of PRADPT120/PRADPT115 placed right next to the other side of PRADPT190/PRADPT185 as illustrated in *Figure* 7.23.

Note: *** denotes the technology code. For example, 013 is the technology code for 0.13µm process

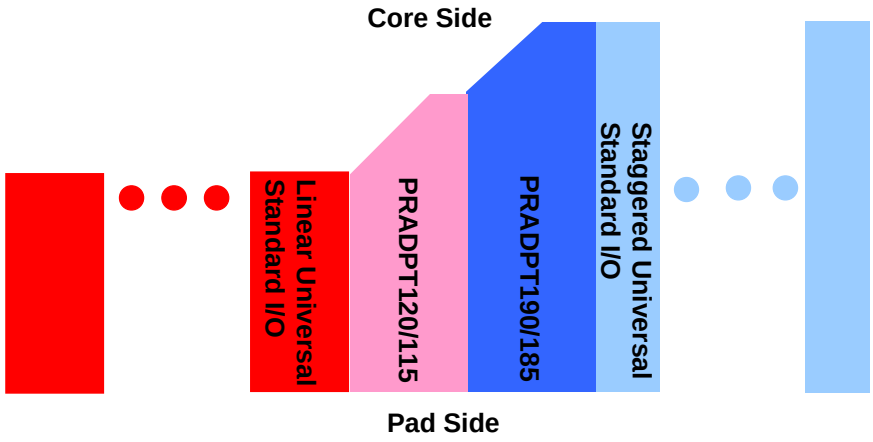


Figure 7.23 Use PRADPTx Cells to Bridge between Staggered Universal Standard I/O and Linear Universal Standard I/O

How to Bridge between TSMC Universal Standard I/O and The Corresponding Non-Universal Standard I/O

It is required to use PRBRIGyyy from **tpi***gv** or **tpi***nv** inter-connection library to bridge between universal standard I/O and the corresponding non-universal standard I/O, where yyy is the universal standard I/O cell height.

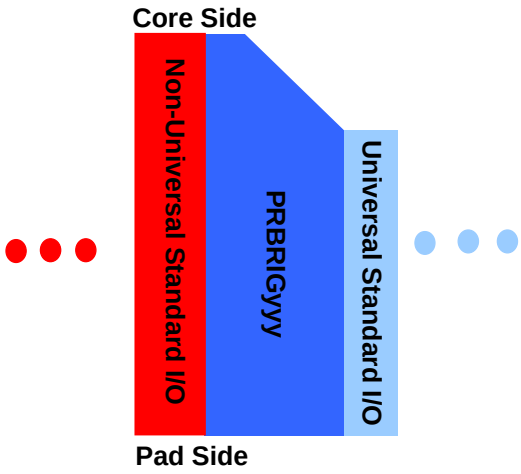


Figure 7.24 Use PRBRIGyyy Cell to Bridge between Universal Standard I/O and Non-Universal Standard I/O

Chapter 8 Electromigration Considerations

This chapter provides information about the following topics:

- Power/ground cells
- Bonding pads
- Limited power/ground bandwidth

Power/Ground Cells

The TSMC Universal I/O provides several sets of power/ground cells and bonding pads to supply current to the core and I/O areas.

Determining the Maximum Allowable Current

To determine the *maximum allowable current* that each power/ground cell and bonding pad can supply, you can compare the layout with the EM criteria set by the maximum current density (J_{max}) table in the *Design Rule* Manual. Layout with potential EM problems may occur in metal routing, in contact/via placement, and in the connecting port metal width.

Determining the Required Number of Power / Ground Cells

A table listing the maximum allowable current is provided in the release note for each I/O library. This data is useful for calculating the required number of power/ground cells that are necessary to supply enough current to the core and I/O areas according to the estimated power consumption. When designers calculate the number of power/ground cells for I/O areas, designers should consider the Simultaneously Switching Outputs (SSO) effect in addition to EM. For details about SSO, please refer to "Chapter 9 Simultaneously Switching Output Consideration."

Locating the EM Critical Point

EM is a reliability factor in chip manufacturing. EM may not cause chip failure immediately upon power up, but could degrade the performance over time. To locate a possible EM weak point, an EDA tool analysis of the current distribution

and EM criterion is highly recommended. Regardless, a layout review of the connecting ports to power/ground cells is necessary, especially for via number and metal width. Adding via arrays or stacked metal can help increase the maximum allowable current and thereby release the EM critical point.

Bonding Pads

In EZBOND™, there are staggered or linear bonding styles. If you use a staggered bonding style, you must take care of the EM capability of the outer bonding pads. These pads might become a bottleneck in the current path. For linear style bonding designs, in case the bonding pad designed only for the linear approach is not provided in the library, the inner bond pad set is recommended since the inner bond pad provides better EM capability. For the current supply capability for each of the bonding pads with different top metal layers, please refer to the EM table in the library release note.

EM Enhancement

Double/Triple Bonding

For some designs with a low-pin-count package, only one or a few pairs of power/ground pins are specified, and these pins cannot supply enough current, resulting in an EM problem. Because the package pin count is limited, it is suggested that you duplicate the power and ground cells on the pad ring and apply double or even triple bonding to the same power or ground pins of the package.

Figure 8.1 shows an example of duplicating and double bonding the core supplies. With this method, you may get the required current supply from the limited power/ground bandwidth and also take advantage of the reduced wiring inductance from double bonding.

For Non-CUP Wire Bond

Step 1: Adopt the I/O gds under “mt_2” back-end directory, where the top metal is up to the target total metal layer – 2.
Step 2: Adopt the bond pad gds under “wb” directory, where the top metal is up to the target total metal.
Step 3: Connect the top 2 metal lines from the bond pad to internal core **as** depicted in *Figure* 8.2.

For example, I/O 6lm gds under “mt_2” directory only covers from metal 1 to metal 4; the bond pad 6lm gds under “wb” directory covers from metal 1 to

metal 6. Then connect the metal lines in metal 5 and 6 from the bond pad to core for EM enhancement.

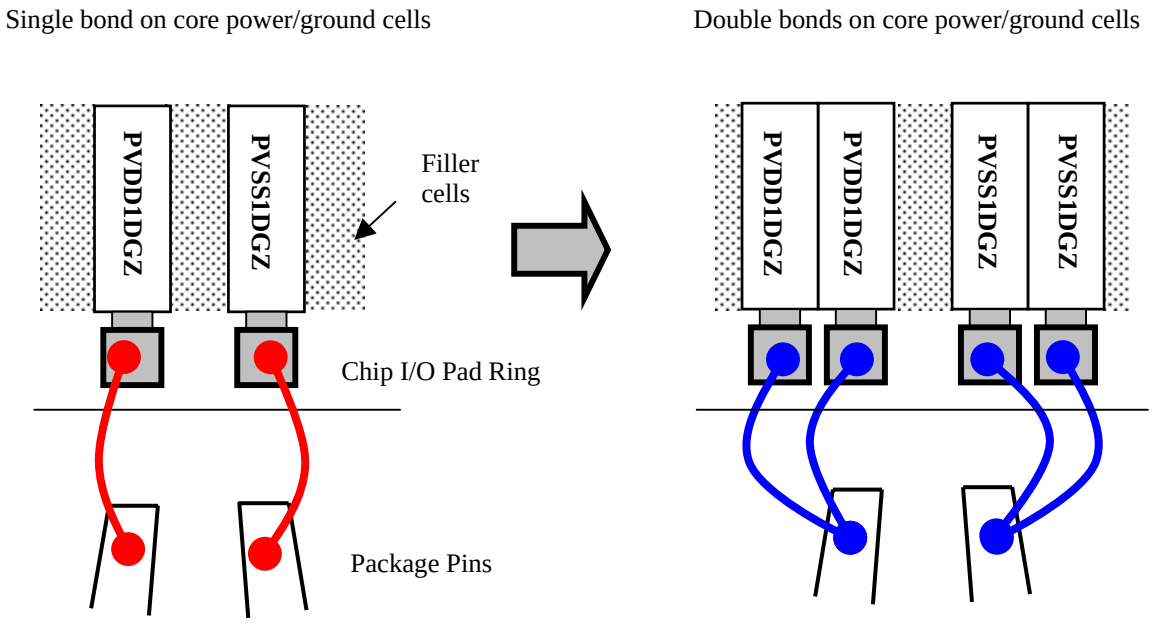


Figure 8.1 Duplicate the Power/Ground Cells and Apply the Double Bond Method to Improve EM

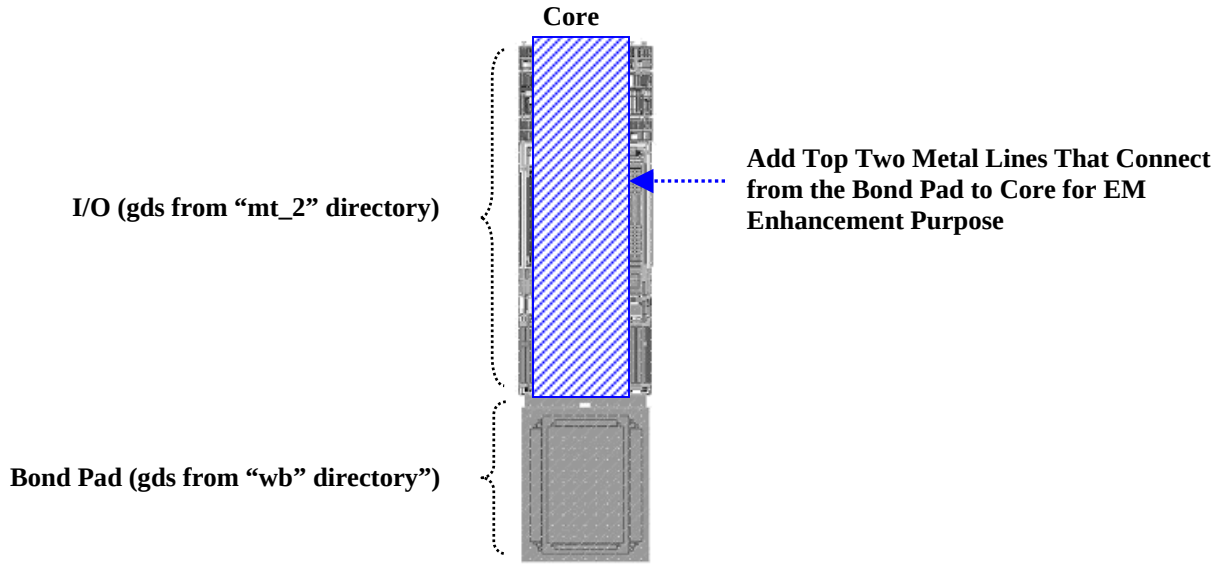


Figure 8.2 EM Enhancement through the Top Two Metal Lines

For CUP Wire Bond

Option 1: Connect top two metal lines between the inner CUP pad PADxNU and internal core for EM enhancement. Please refer to *Figure* 8.3 for illustration.

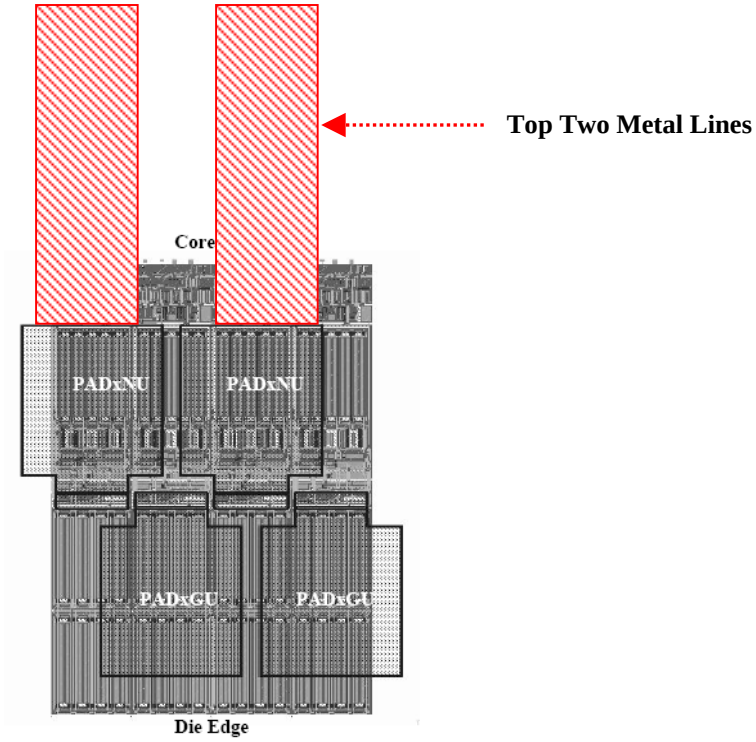


Figure 8.3 EM Enhancement through the Option 1 Approach

Option 2: Insert filler Cells on both sides of core power/ground cells, so that you can connect the top two metal lines between the CUP pad and internal core. Please refer to *Figure* 8.4 for illustration.

Taking N90 staggered universal standard I/O as an example, if you insert 15µm filler cells on both sides of PVDD1DGZ cell as well as connect the top two metals lines with 25.55µm width, EM can thus be enhanced by 89.59 mA @ 125 Celsius degree

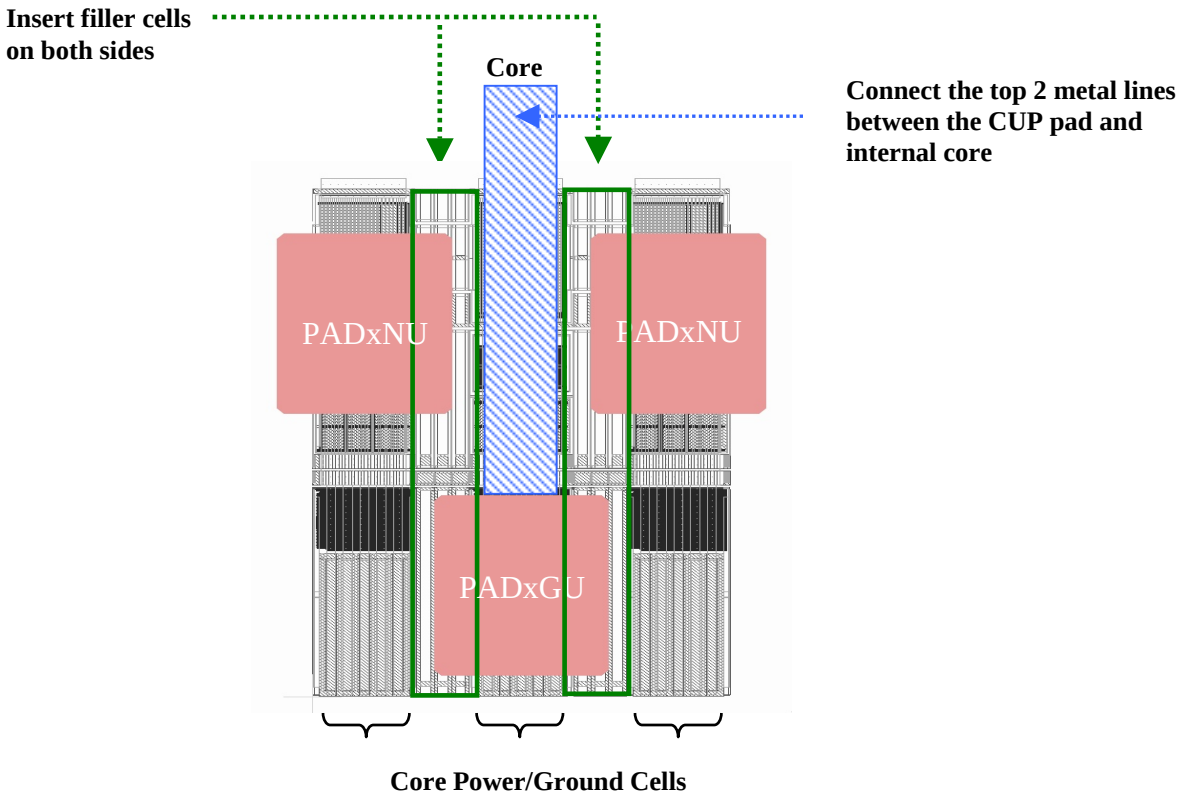


Figure 8.4 EM Enhancement through the Option 2 Approach

Option 3: Place two separate Power/Ground cells together. Then modify the CUP pad pin to which you can connect the CUP pad in the middle of two cells. Finally connect the top two metal lines between the CUP pad and internal core. Please refer to *Figure* 8.5 for illustration.

Compared with option 2, option 3 is preferable in terms of ESD robustness, as the core power/ground cells are implemented with ESD protection circuitry. Therefore, placing two power/ground cells together is more ESD robust than the filler-cell insertion approach.

Taking N90 staggered universal standard I/O as an example, if you place two separate PVDD1DGZ cells together with CUP pad pin modification as well as top two metal-line connection (e.g. 25.55 metal width), EM can thus be enhanced by 89.59 mA @ 125 Celsius degree. If the original total number of PVDD1DGZ cell to achieve the target EM is 150, you only need 25 pairs of PVDD1DGZ cells with “option-3” approach to reach the same EM target.

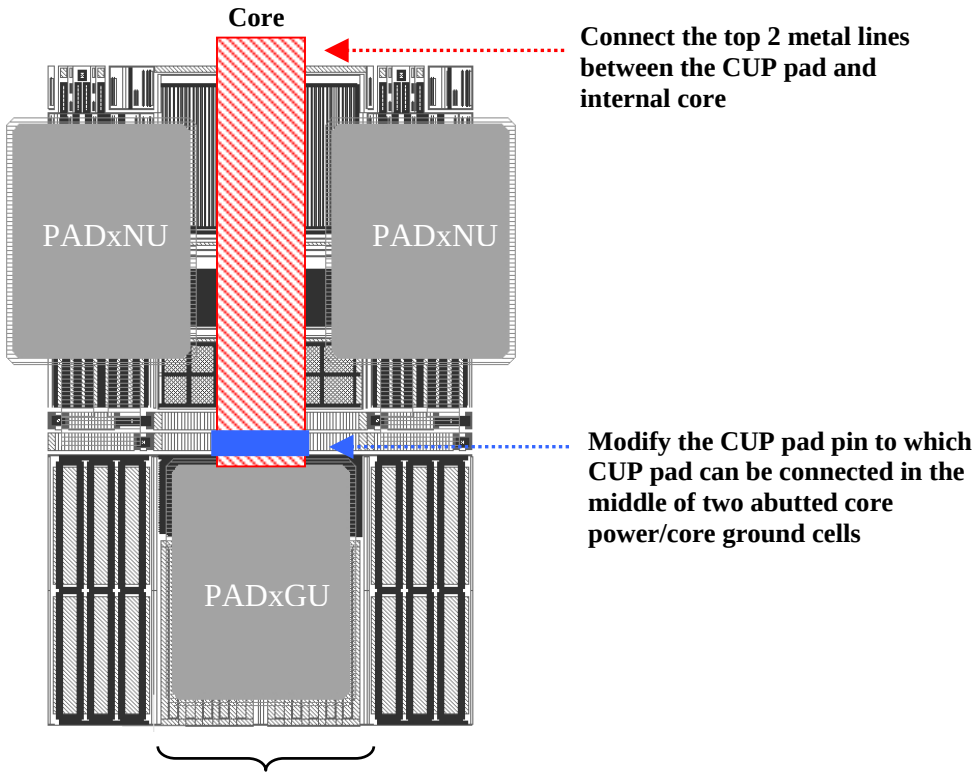


Figure 8.5 EM Enhancement through the Option 3 Approach

Chapter 9 Simultaneously Switching Output Considerations

This chapter provides information about the following topics:

- Terminology and definitions
- SSO simulation model
- Calculation for the required number of I/O power/ground cells
- Time to valid state

Terminologies and Definitions

Simultaneously Switching Output

Simultaneously Switching Output (SSO) means that a certain number of I/O buffers are switching at the same time and in the same direction (H → L, HZ →L or L → H, LZ → H), which results in noise on the power/ground lines. SSO occurs because of the large dI/dt value and the parasitic inductance of the bonding wire on the I/O power/ground cells.

Simultaneously Switching Noise

Simultaneously Switching Noise (SSN) is the noise produced by simultaneously switching output buffers. SSN changes the voltage levels of power/ground nodes, creating the so-called “Ground Bounce Effect." The Ground Bounce Effect is tested at the device output by keeping one stable output at low “0” or high “1," while all other device outputs switch simultaneously. The noise that occurs at the stable output node is called “Quiet Output Switching“ (QOS). If the input low voltage is defined as V_{il}, the QOS of V_{il} is considered the maximum noise that the system can endure.

Driving Index

Driving Index (DI) is the maximum number of copies of an I/O cell switching from high to low simultaneously without making the voltage on the quiet output “0” higher than a threshold value “V_{il}” when a single ground cell is applied. The QOS of “V_{il}” is a criterion in defining DI because “1” has more noise margin than “0”. For example, in an LVTTL specification, the margin of “V_{ih}” (2.0V) to

VD33 (3.3V) is 1.3V in a typical corner, which is higher than the margin of "V_{il}" (0.8V) to ground (0V).

Driving Factor

Driving Factor (DF) is the amount that the specific output buffer contributes to the SSN on the power/ground rail. The DF value of an output buffer is proportional to dI/dt, the derivative of the current on the output buffer. DF can be obtained as follows:

DF = 1/DI

Sum of Driving Factors

Sum of Driving Factors (SDF) accumulates the DF values of all the I/O cells within a group or a chip. SDF indicates the number of power/ground cell for I/O and counts those cells switching simultaneously.

- **SSO case**

  Required number of ground cells for I/O = SDF

  Required number of power cells for I/O = SDF / 1.1

- **Non-SSO case**

  The required number of power/ground cells for I/O is less than that for the SSO case in this section (SDF and SDF/1.1). As a general rule, use (SDF/1.6) and (SDF/1.5) respectively for the number of power and ground cells.

SSO Simulation Model

As *Figure* 9.1 shows, each power/ground net and output node is modeled with individual RLC circuits according to the package type.

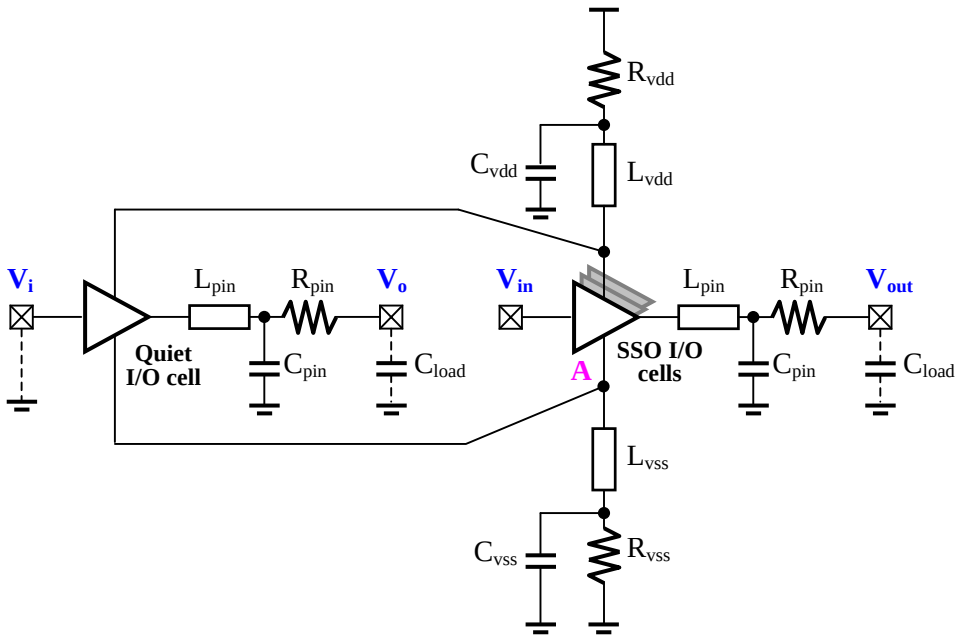


Figure 9.1 The Model for SSO Simulation

In the *Figure*, V_{in} represents the input node of several SSO I/O cells. When V_{in} toggles, all the SSO I/O cells are switching simultaneously and the change of the current (I) on L_{vss} could be high. Therefore, the noise of [L_{vss} * (dI/dt)] is generated at node A.

Meanwhile, another quiet I/O cell grounded to node A is transmitting a "0" through V_o at the same time. The "0" could be recognized as "1" if the noise at V_o is greater than V_{il} because of the raised reference voltage at node A. DI is the minimum number of SSO I/O cells that contribute noise of V_{il} at V_o. DF can be calculated from DI:

$$1/DI = DF$$

The largest SSN happens in the best process corner with the highest voltage and the lowest temperature. Thus, the corresponding DI is characterized based on those conditions. Users can find the corresponding DF table in the library databooks.

Calculation for the Required Number of I/O Power/Ground Cells

From the DF table in the library databook, users can calculate the required number of power/ground cells for I/O in SSO or non-SSO cases. The following provides an example of the calculation process.

1. **Check the DF value of each I/O cell type.**

   QOS of "V_{il}" is defined as the failure criterion in SSO simulation. If four copies of the I/O cell with one ground cell (Lvss) cause noise "V_{il}," the DI is 4 and the DF is 1/4 = 0.25. You can check the DF table in the library databook with the package wiring inductance (L_{vdd}, L_{vss}, L_{pin}).

2. **Calculate the SDF value of the whole chip**.

   After you determine the DF for each I/O cell type, you can sum the DF values to calculate the SDF. For example, consider a design with ten 2 mA buffers, six 8 mA buffers, and twenty-six 24 mA slew-rate-controlled buffers. The DF table indicates the corresponding DF of 2 mA, 8mA, and 24 mA cells as 0.012, 0.063, and 0.260 for a wiring inductance of 7.8 nH. The SDF is calculated as follows:

   10 x 0.012 + 6 x 0.063 + 26 x 0.260 = 7.258

3. **Obtain the required I/O power/ground cell number.**

   The number of power/ground cells for I/O depends on whether the case is SSO or non-SSO.

   SSO case:

   ground cell number = 7.258 → **8**

   power cell number = 7.258 / 1.1 = 6.598 → **7**

   Therefore, for I/O in SSO case, the required number of ground cells is eight and the required number of power cells is seven.

   Non-SSO case:

   ground cell number = 7.258 / 1.5 = 4.839 → **5**

   power cell number = 7.258 / 1.6 = 4.537 → **5**

   Therefore, in the non-SSO case, the required number of ground cells is five and the required number of power cells is five.

Time to Valid State

The SSN peak amplitude normally decreases over time. If a design with simultaneously switching outputs does not have enough power/ground cells for I/O because of a pin count restriction, sample the data after a period of time to ensure the correctness of the sampled data. This period of time is called the “time to valid state."

If the number of power/ground cells for I/O is not sufficient, refer to the TTVS tables in the library databook for information. These tables provide the timing required for SSO noise to settle down to an acceptable value (V_{il}). Note, however, that the tables are characterized with only one pair of I/O power/ground cells.

Tips to Reduce SSN

- Don’t use stronger output buffers than are necessary.
- Use slew-rate-controlled output cells wherever possible.
- Insert as many power and ground cells for I/O as possible. It is recommended to place the I/O power cell near the middle of the output buffers.
- Place noise-sensitive cells away from SSO I/Os.
- Consider using double bonding on the same or duplicated power/ground cells to reduce inductance.

Chapter 10 Electrostatic Discharge (ESD) Considerations

This chapter provides information about the following topics:

- ESD Network
- I/O Ring
- Dummy Power Cell Insertion
- Dedicated Analog Power & Ground Cell
- Separated Power Domains
- Tie High / Tie Low

ESD Network

The Electrical Static Discharge (ESD) clamping circuits of the *TSMC Universal I/O library* are embedded in each power/ground/IO cell to construct the I/O ring ESD protection scheme as shown in *Figure* 10.1.

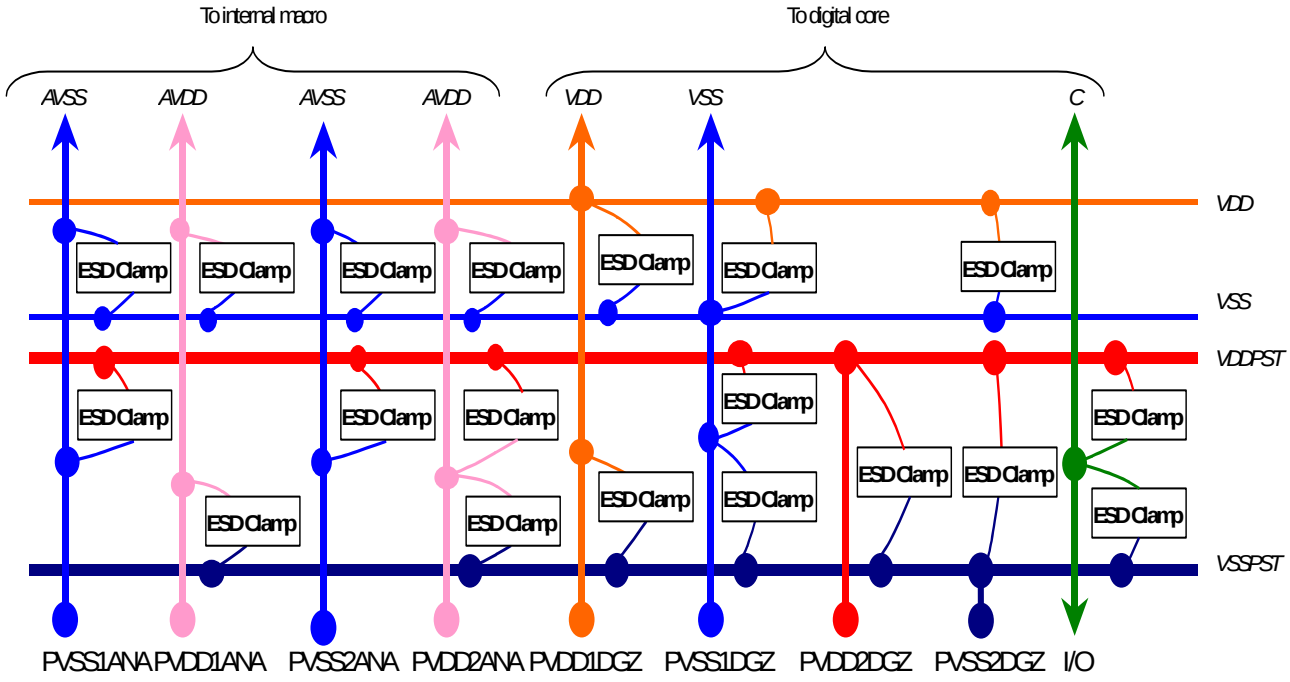


Figure 10.1 ESD Protection Scheme for Power/Ground/IO Cells

I/O Ring

To achieve robust ESD/Latch-Up performance, it is required to implement the I/O cells in a “ring” structure, ensuring that the global ESD bus (VSS, the pre-driver ground bus) is continuous throughout the entire I/O domains. If not, the ESD/Latch-Up protection level would be degraded.

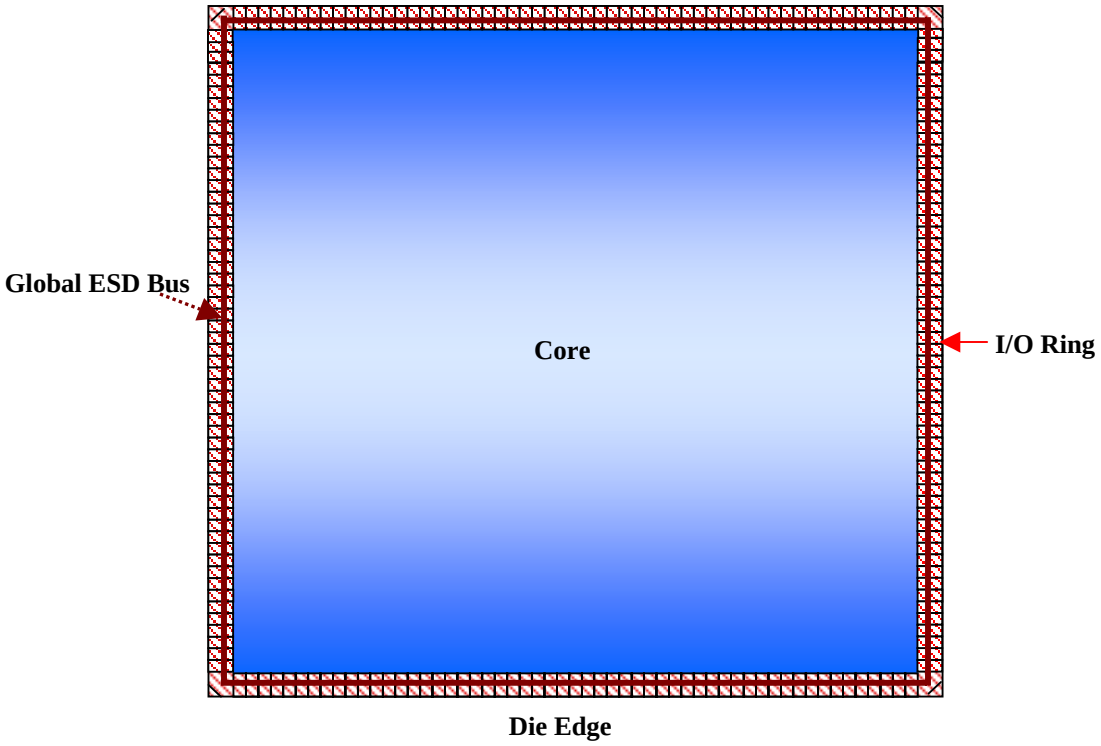


Figure 10.2 I/O Ring

Power Cell Insertion

The ESD test models include the Human Body Model (HBM), Machine Model (MM), and Charge Device Model (CDM). The HBM and MM include PD/PS (positive to V_{DD}/V_{SS}), ND/NS (negative to V_{DD}/V_{SS}), pin-to-pin (positive/negative), and power-to-ground (positive/negative) tests. Many of the test modes require the ESD discharge path from power (VDD) to ground (VSS) rail. To provide the shortest ESD path, it is strongly suggested to implement power cells that contains power clamp inside as many as possible if space is allowed. Moreover, **the maximum resistance "R" of the power/ground BUS line from any I/O cell to the "nearest" "bonded" power cell / to the "nearest" "bonded" ground cell is 1 Ohm for the advanced process technologies (90nm and below); 3 Ohm for 0.13um and above.** Please refer to *Figure* 10.3 for reference.

$R = R_{sheet} \times L / W$, where R_{sheet} is available in the spice model

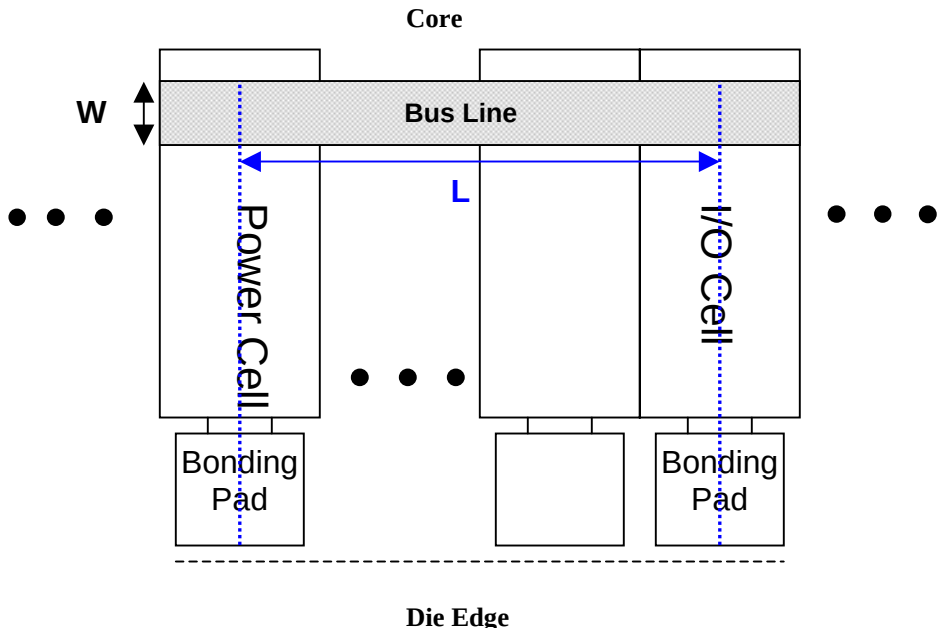


Figure 10.3 Illustration of Bus Resistance Calculation

Figure 10.4 indicates that dummy power cells act exactly like fat filler cells. The benefit to using dummy power cells is that they provide short ESD path; whereas filler cells do not. In the packaging phase, dummy power is not bonded, so the total pin count is not impacted. To construct robust ESD protection scheme for different ESD test models, it is highly recommended to insert dummy PVDD1DGZ/CDG and PVDD2DGZ/CDG cells. However, the only trade-off is the stand-by leakage current in the power cell.

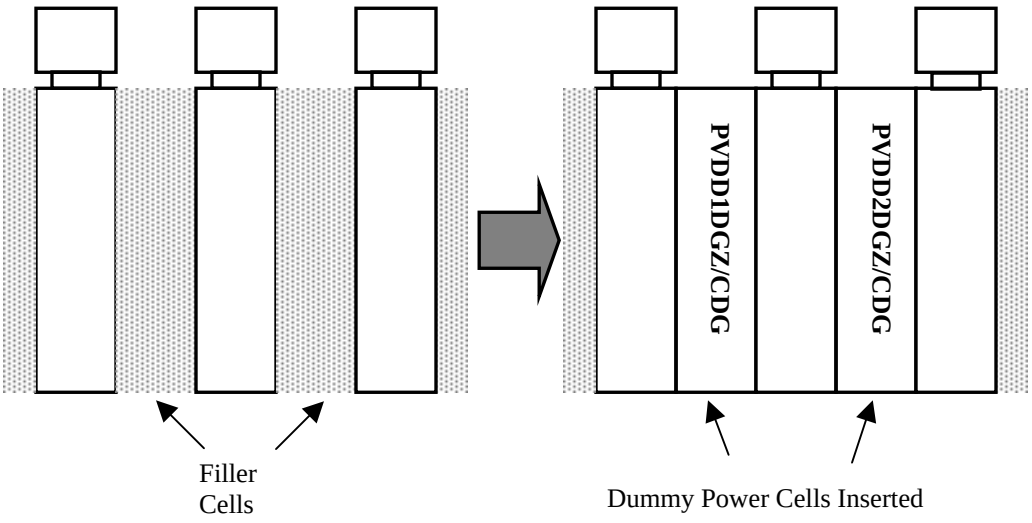


Figure 10.4 Add Dummy Power Cells for ESD Robustness

To achieve robust ESD/Latch-Up protection:

Note 1: For the I/O domain implemented with TSMC universal standard I/O cells, it is recommended to place **"at least"** TWO PVDD2DGZ/CDG digital I/O power cells, **"at least"** TWO PVDD1DGZ/CDG digital core power cells, and **"at least"** TWO PVSS1DGZ/CDG digital core ground cells together with TWO PVSS2DGZ/CDG digital I/O ground cells, or TWO PVSS3DGZ/CDG digital common ground cells in each domain. In particular for small digital I/O domain, it is recommended to place two PVDD1DGZ/CDG cells together and double bond them.

Note 2: The minimum capacitive load is 20pF between the "VDD" pin on the core side of PVDD1DGZ/CDG and the "VSS" pin on the core side of PVSS1DGZ/CDG. It is required to insert decoupling capacitor available from TSMC standard cell library in case capacitive load is below 20pF. The ESD (HBM / MM / CDM) performance can all benefit from this requirement.

Dedicated Analog Power & Ground Cell

Note 1: When using PVDD1ANA together with PVSS1ANA cell:

You need to adopt the PCLAMP cell from the corresponding universal analog I/O library, and do the following connections to enhance core ESD/Latch-Up protection.

Step 1: Connect from AVDD pin of PVDD1ANA analog power cell to VDDESD pin of PCLAMP cell. Connect from AVSS pin of PVSS1ANA analog ground cell to VSSESD pin of PCLAMP cell.

Step 2: Then connect from VDDESD and VSSESD rails of PCLAMP cell to internal core power rail and core ground rail respectively. For details on PCLAMP cell, please refer to Universal Analog I/O General Application Note.

Reminder: PCLAMP can only be used with PVDD1ANA & PVSS1ANA pair, but not with PVDD2ANA & PVSS2ANA pair.

Note 2: Similar to digital power/ground cell, the minimum capacitive load is 20pF between the "AVDD" pin on the core side of PVDD1ANA and "AVSS" pin on the core side of PVSS1ANA. Please refer to *Figure* 10.5 for illustration. This requirement can also be applied to PVDD2ANA and PVSS2ANA pair. The ESD (HBM / MM / CDM) performance can all benefit from this. It is required to insert the decoupling capacitor (available from TSMC standard cell library) in case capacitive load is below 20pF.

Note 3: In particular for small I/O domain, it is recommended to place two PVDD1ANA cells together and double bond them. Similarly, it is recommended to place two PVDD2ANA cells together and double bond them.

Note 4: PVDDxANA / PVSSxANA cannot be implemented alone in a domain without digital power and ground cells. It is required to have the ESD power bus and ground bus supplied by digital power cell and ground cell placement. For details, please refer to Chapter 2.

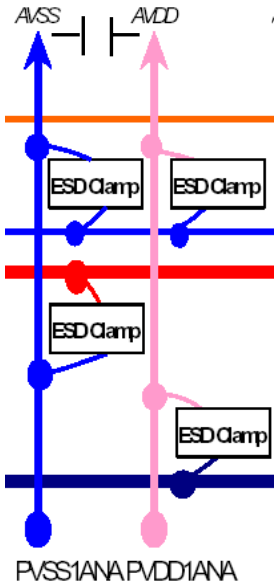


Figure 10.5 The Capacitive Load

Separated Power Domains

A mixed-voltage design can contain several I/O power domains with different voltages for either digital or I/O sections. TSMC provides a whole chip ESD protection scheme with the "power-cut cell" approach to connect different power domains.

Inside the power-cut cell (**PRCUT**), the pre-driver ground rails (VSS) are shorted, but the post-driver ground rails (VSSPST) and all the power buses as well as POC rails are left open. Please refer to *Figure* 10.6 as an example.

Note that the PRCUT cell must also be used to separate digital domains with different supplied voltages.

To realize the short ESD discharge path across different I/O domains, it is recommended to have the PVDD1DGZ/CDG cell placed near the power-cut cell. For details about the usage of power-cut cell between digital and analog power domains, please refer to the "TSMC Universal Analog I/O Application Note".

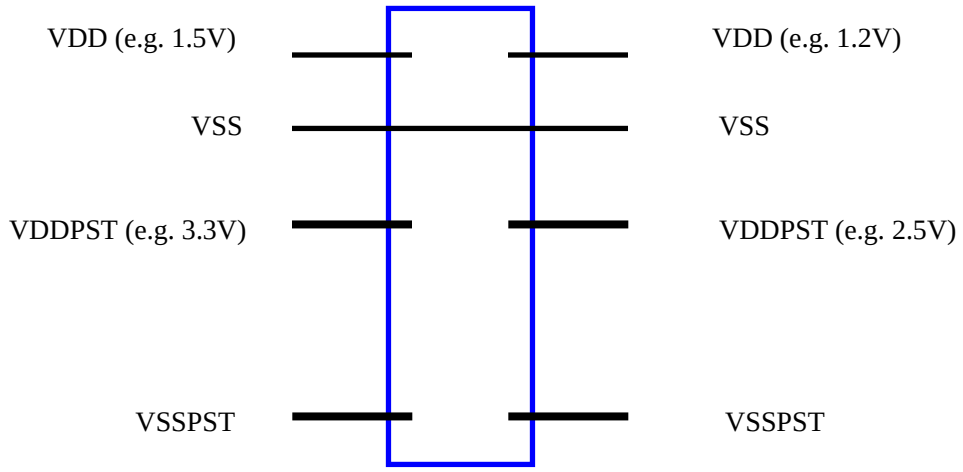


Figure 10.6 The Power-Cut Cell (PRCUT) Scheme

When to Use the Power-Cut Cell (PRCUT)

- Require two digital domains with different supplied voltage.
- Require a dedicated domain using Universal Standard I/O for noise concern.

Attention 1: It is mandatory to use at least one core power cell PVDD1xxx , one I/O power cell PVDD2POC that features power-on control, and one common-ground cell PVSS3xxx within one domain.

Or

It is mandatory to use one group of core power & ground cells PVDD1xxx & PVSS1xxx together with one group of I/O power that features power-on control & ground cells PVDD2POC & PVSS2xxx within one domain.

Attention 2: PRCUT cell is only offered in the universal standard I/O library.

Attention 3: PRCUT cell is not included in the LVS netlist since there is no device within the cell.

Tie High / Tie Low

For ESD robustness, do not directly tie the programmable pins (e.g. OEN) to power (VDD) / ground (VSS). Instead, connect a tie-high or tie-low cell between the programmable pins and power / ground.

Note: The tie-high / tie-low cell is available from the standard cell library.

Chapter 11 Open Drain Emulation

TSMC Universal I/O does not provide open drain I/O cells. However, users can emulate open drain behavior with the tri-state output I/O from high-volt-tolerant I/O library. *Figure* 11.1 shows that the input port (I) is tied to ground “0” through a tie-low protection cell, and the output signal is connected to enable port (OEN) to transfer a “0” or “Hi-Z” to the PAD. When OEN=”0," the output is enabled, and the PAD is equal to I as “0”. When OEN=”1”, the output is disabled (Hi-Z), and the PAD is pulled high by the external pull-up device.

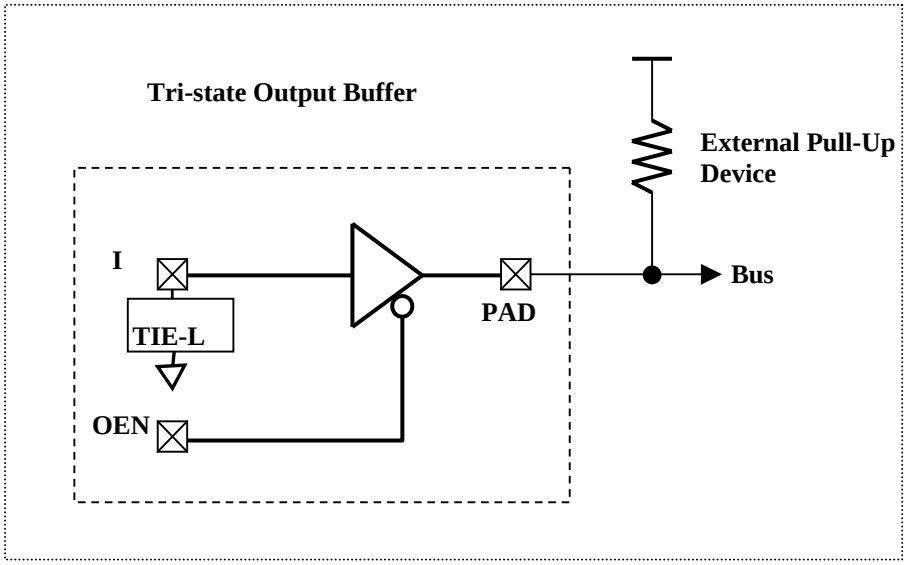


Figure 11.1 The Open Drain Emulation Diagram

- Note 1: It is required to tie the “I” pin to ground through a tie-low cell available from the standard cell library for ESD concern.
- Note 2: The other approach to emulate the open-drain behavior is to tie “I” and “OEN” together, with drawback of higher power consumption.

Note: Do not use regular (i.e. non-high-volt-input-tolerant) I/O for open drain emulation.

Chapter 12 Library Integration Notes

Integration of Library Tape-out Layers

To correctly tape out with TSMC I/O library, users must refer to the corresponding "*Masking Layers & Bias*" document at TSMC Online for the most updated mask tooling layers and operation/bias equations. The following sections include important notes that users must review prior to taping out a chip.

GDSII Number Mapping

For libraries from different vendors, the GDSII numbers defined for each process layer and dummy layers can be different. Therefore, it is required to comply with the definition in the technology-dependent "*GDS Layer Usage Description File*" that can be downloaded from TSMC Online.

Warning: The mixing or wrong mapping of GDSII layers could result in a serious mask problem and silicon failure.

OD Mask

According to the "*GDS Layer Usage Description File*," there are two methods for defining the OD region in GDSII: One method is to use DIFF; another, is to use (PDIFF+NDIFF). Different libraries may have their preferences and users must tape out all the GDSII layers related to an OD mask, or the chip may fail. It's suggested to tape out the OD layer with (DIFF or PDIFF or NDIFF) to ensure all the OD layout styles are included in the OD mask tooling.

ESD Mask

Different GDSII layers are defined for ESD implant, e.g. masks (110) and (111). Though the ESD implant is optional in process steps, the ESD mask (111) might be required for a specific I/O library to improve the ESD margin. Please make sure all the ESD-related GDSII layers are taped out correctly according to the "*Masking Layers & Bias*" table. Please also check the library release note for the special instruction on ESD mask, if any.

Poly Resistor

To ensure that the poly resistor and SPICE model match, users can tape out dummy layers (such as DMN2V, DMP2V, RHDMY or RH[⊗]) to ensure/avoid the LDD implant on the poly resistors. Users must check the "*Masking Layers & Bias*" table to tape out the corresponding dummy layer with the TSMC Universal I/O library.

Non LDD Device

To form Non-LDD implant, RHDMY or RH is used in 0.13µm, 90nm, and 65nm, but not in 0.15µm and 0.18µm technologies. For 0.15µm/0.18µm, it is required to insert NOT VARDMY into the general-purpose logic equation. Please check the 0.15µm/0.18µm library release note for the exact logic operation in detail.

GDSII Change to Mask Revision

Even minor changes of the GDSII layers may result in a major change of a mask set, especially in base layers of a process. For example, the modification of the OD2 GDSII layer not only changes the OD2 mask but also other masks, such as LDD, POLY, RPO, ESD, and so on, depending on the technology. Users must review the "*Masking Layers & Bias*" document to tape out all the masks related to the changing GDSII layers.

High-Vt (Threshold Voltage) Implant

Since the 0.13µm/90nm/65nm advanced process features high-Vt option, the 0.13µm/90nm/65nm universal standard I/O gds already contains high-Vt implant layer on core ESD protection devices to substantially reduce the core power stand-by leakage current. Please refer to the stand-by leakage current comparison table **("with high-Vt layer" versus "without high-Vt layer")** available from the library release note first; then decide whether to tape out this layer or not.

- To tape out the high-Vt layer, it is required to select it in the MT form
- If not, discard the high-Vt implant in the tape out MT form or remove it from the gds.

[⊗] DMN2V/DMP2V are used in 0.18um, 0.15um technologies to ensure LDD implant, but RHDMY/RH is used to avoid the LDD implant in 0.13um/90nm technology.

Chapter 13 Simulation Notes

This chapter conveys all the know-how to users who encounter issues while running simulation using TSMC Universal I/O library. The topics include:

- LPE Spice Netlist (applicable to the I/O power cell PVDD2x and to the I/O ground cell PVSS2x)
- Maximum Channel Length in Spice Model (applicable to ESD device in some of the old libraries)
- Device Mapping between Spice Model Card and LVS/LPE Netlist (applicable to 0.13µm, 0.15µm, 0.18µm, and 0.25µm I/O libraries)

LPE Spice Netlist

- For simulation using the parasitic extracted spice netlist (lpe_spice), please manually insert the post-driver power and ground pin names to the first line of PVDD2x and PVSS2x sub-circuits as follows, otherwise an error of "missing pin" would occur.

  Example 1: Post-driver Power Cell (PVDD2x)

  .subckt PVDD2CDG **VDDPST**

  …

  Example 2: Post-driver Ground Cell (PVSS2x)

  .subckt PVSS2CDG **VSSPST**

  …

- For digital I/O, some of the PVDD2x / PVSS2x cell names end up with "_18", or "_25", or "_33", the added pin names should also end up with "_18", or "_25", or "_33", otherwise an error of "missing pin" would occur.

  Example 3: Post-driver Power Cell (PVDD2x_33)

  . subckt PVDD2CDG_33 **VDDPST_33**

  …

Maximum Channel Length in Spice Model

Some of the ESD capacitance device channel length in the spice netlist exceeds the maximum device channel length (LMAX) defined in the spice model. To avoid encountering "missing device" issue while running simulation, users can take either of the following two approaches, where approach 1 is preferable.

- Approach 1: Partition device in the spice netlist, and each of partition is within the range of LMAX defined in the spice model:

  For example, the NMOS channel length in the spice netlist is defined as follows:

  M1 VSS NET VSS VSS N W=20 L=43

  We can partition the transistor in 3 parts, and each of the partition is covered by LMAX.

  M1 VSS NET VSS VSS N W=20 L=14

  M2 VSS NET VSS VSS N W=20 L=15

  M3 VSS NET VSS VSS N W=20 L=14

- Approach 2 (Not recommended): Extend the LMAX in the spice model to the value that can cover the device length in the spice netlist:

  For example, if the P-Channel length in the spice netlist is 6E-05 whereas the maximum P-Channel length defined in the spice model is 4E-05, users can extend the LMAX from 4E-05 to 6E-05 to cover the range.

  Note1: Only libraries with less advanced technology may come with the above issue.

  Note 2: Though approach 2 is easier than approach 1, approach 2 may result in "inaccuracy" issue.

Device Mapping between Spice Model Card and LVS/LPE Netlist

For 65nm 3.3v overdrive, 0.13µm, 0.15µm, 0.18µm, and 0.25µm I/O, since device name defined in the spice model card is different from that in the LVS/LPE netlist, user must modify the spice netlist following the mapping table below prior to running simulation.

However, for 45nm I/O, 65nm 2.5v I/O, and 90nm I/O, the device name of the spice model card is consistent with that of the LVS/LPE netlist. Therefore, there is no need to take any action on this matter.

Technology	Device Name in the Spice Model Card	Device Name in the LVS/LPE Netlist
45nm	The same as LVS/LPE netlist	The same as spice model card
65nm 2.5v I/O	The same as LVS/LPE netlist	The same as spice model card
65nm 2.5v I/O with 3.3v Over-Drive	NCH_33	NCH_25OD
	PCH_33	PCH_25OD
	NDIO_33	NDIO_25OD
	PDIO_33	PDIO_25OD
90nm	The same as LVS/LPE netlist	The same as spice model card
0.13µm 0.15µm 0.18µm	nch	N
	pch	P
	nch_25 nch_33 nch3	ND
	pch_25 pch_33 pch3	PD
	nch_na33 nanch3	NN
	DIO_esd33 DIO_esd25 ENDIO_3	DB

	NDIO_33 NDIO_25 NDIO_3	D2
	PDIO_33 PDIO_25 PDIO_3	D1
0.25µm	Nch	N
	Pch	P
	nch3	ND
	pch3	PD
	ech3	Y

Floating NGATE / PGATE

The NGATE / PGATE in the LVS / LPE netlist are the probing node for characterization purpose. Please keep NGATE / PGATE in the netlist as is (i.e. stay floating) for simulation accuracy.

Chapter 14 Characterization Conditions

The characterization conditions of TSMC standard I/O libraries in different PVT (Process Voltage Temperature) combinations are listed below. The condition coverage would vary, depending on the process technology.

Name	Description	Core Voltage	I/O Voltage	Temp	Process
LT	Low Tempeature	1.1*Vdd	1.1*Vddpst	-40	FF
BC	Best Case	1.1*Vdd	1.1*Vddpst	0	FF
TC	Typical Case	1.0*Vdd	1.0*Vddpst	25	TT
WC	Worst Case	0.9*Vdd	0.9*Vddpst	125	SS
WCL	Worst Case Low Temperature	0.9*Vdd	0.9*Vddpst	-40	SS
WCZ	Worst Case Zero Temperature	0.9*Vdd	0.9*Vddpst	0	SS
ML	Maximum Leakage	1.1*Vdd	1.1*Vddpst	125	FF

Note 1: WCL (Worst Case Low Temp) is for worst timing check-up because of the effect of temperature inversion. For instance, at 45nm and more advanced technologies, WCL could have worse timing than WC in some timing arc (e.g. input path). As such, sign-off for worst corner timing analysis should use WCL together with WC.

Note 2: WCZ (Worst Case Zero Temp) is an extensive condition to WCL (Worst Case Low Temp) for user's reference, as 0 is considered more realistic than -40 Celsius degree for certain applications.

Note 3: ML (Maximum Leakage) is primarily to check the worst leakage condition. ML is not included for 0.15µm and less advanced technologies, since the leakage of standard I/O cells is less critical. However, for 0.13µm and more advanced technologies, leakage of the standard I/O cells could be a critical factor, leading to a need for characterization.

Note 4: For re-characterization or customization request that requires modification on off-the-shelf I/O, unless specifically requested in Statement of Work (SOW) form, it would still be based on the characterization conditions of the original library.

Chapter 15 Contact Us

The TSMC Universal I/O libraries are released under the supervision of the TSMC standard quality assurance (QA) procedure. If you find any errors or encounter any problems with the library, please first refer to the *release notes* and *designkit.info* (packed as part of the deliverable kits) for the known issues. Also, make sure that the tool version, *Design Rule* manual, and DRC/LVS command files comply with the TSMC QA condition. For any further issues, please contact your library distributor or TSMC regional application engineer for immediate assistance.