L-3/T-1/CSE Date : 29/10/2019

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-1 B. Sc. Engineering Examinations 2018-2019

Sub : **CSE 305** (Comp. Architecture)

Full Marks : 210 Time : 3 Hours

The figures in the margin indicate full marks.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**.

You may choose to answers parts of some questions in the figures provided with the question script. In that case, you must securely attach that page to your answer script after having that duly signed by the honourable invigilator.

1. (a) Consider the single cycle datapath shown in Figure 1.A. Update the figure to implement the following MIPS instructions: bne, j, jr, jal, slt, lui. Briefly explain your updates. You can make the changes in Figure 1.A and have that page stapled with your script. The question page containing Figure 1.A must then be signed by the invigilator. **(30)**

   (b) Why are single cycle implementations not very efficient? **(5)**

2. (a) Consider the following code snippet: **(10)**

```
        beq $1, $2, TARGET # branch is/will be taken for this one
        lw $3, 40($4)
        add $2, $3, $4
        sw $2, 40($4)
TARGET: or $1, $1, $2
```

   Assume that branch decision is checked using the ALU zero signal (i.e., no separate hardware is placed to decide early). Now can an attempt to flush and stall the pipeline occur simultaneously? If yes, then will there be an issue? Explain with the help of a single cycle illustration. If there is an issue, you need to provide a solution. If there is no issue, you need to clearly explain why not.

   (b) Discuss what are the issues and how can they be handled in the following code snippet. Assume that using extra hardware branch decision is checked as early as possible. Use multicycle illustrations to explain. How many cycles will be needed to complete the code snippet? **(10)**

```
lw $1, 100($2)
add $1, $1, $2
beq $1, $2, TARGET
```

   (c) Discuss how a TLB miss is handled by MIPS architecture. Consider the pipelined datapath in Figure 2.c. that is capable of handling underfined instruction and overflow exceptions. Now, discuss how TLB miss exception may be handled there. You may update Figure 2.c if you feel necessary. You can make the changes in the question page containing Figure 2.c and have that stapled with your script. The question page must then be signed by the invigilator. **(15)**

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3. (a) With the help of a flowchart show how a real read or write request is processed in a system with a TLB interacting with an appropriate cache and virtual memory. **(8)**

(b) Consider a virtual memory system with 40-bit virtual byte address, 16KB pages and 36-bit physical byte address. All the virtual pages are in use and there are valid, protection, dirty and use bits. Disk addresses are not stored in the page table. There is a 2-way set associative TLB with a total of 256 TLB entries. Now answer the following questions: **(4+3+12=19)**

a. What is size of the page table?

b. What will be the size of the page table if we use the inverted page table concept?

c. With the help of an appropriate illustration show how the virtual-to-physical mapping is done. Assume a 16 KB direct-mapped cache with 16 words block.

(c) You have designed a processor with 16-entry TLB and 4 KB pages and have exhausted your budget for implementing the system. During trial you have found that programs are accessing at least 2MB of memory at a time. How would your system perform and why? Can you suggest how can you improve the system performance of the system if no more money is available? What if more money is available? **(8)**

4. (a) Consider three processors with different cache configurations and data as follows: **(4+3+12=19)**

Processor/Cache	Processor cycle time	Organization	Block size (Word)	Instruction Miss rate	Data Miss rate
1	420 ps	Direct-Mapped	1	4%	6%
2	420 ps	Direct-Mapped	4	2%	4%
3	310 ps	Two-way Set Associative	4	2%	3%

For these processors, one half of the instructions contain a data reference and cache miss penalty is 6+ block size in words. The CPI of this workload was measured on Processor I (i.e., with cache 1) and was found to be 2.0. Now, answer the following questions.

a. Which processor spends the most cycle on cache misses?

b. Which processor is the fastest and which one is the slowest?

c. For processor 3, show the cache organization and how the cache will be accessed with the help of a detailed illustration.

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Contd..... Q. No. 4

(b) Suppose you are working on a computer architecture with the following properties: **(4+6+6=16)**

a. 32-bit address

b. byte addressable RAM

c. 256KB cache

d. 64 words block

e. Random replacemet algorithm

f. Write-through scheme

Now answer the following questions:

a. What is the size of the cache?

b. What is the overhead if the cache is:

i. direct-mapped

ii. 2- way set associative

iii. fully associative

c. Consider the current value of $2 is 1000 in decimal. Assuming direct-mapped organization, find the cache address for the following load word instruction: lw $1, 18($2).

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) Draw the hardware block diagram and the flowchart of the sequential version of the multiplication algorithm. Also, draw the flowchart of the refined version of the algorithm. **(12)**

(b) Consider a 16-bit floating point representation system, where the exponent is 4 bits long. With this system, represent the floating point numbers $(-1.25)_{10}$ and $(0.375)_{10}$ into a bit string of length 16 using appropriate bias. **(8)**

(c) Determine the decimal value of the floating point number represented by the hexadecimal value $(DF80\ 7500)_{16}$ according to IEEE 754 single precision floating point format. **(5)**

(d) Design a 4-bit ALU with three selection variables S_0, S_1 and S_2 that performs the following operations on two 4-bit inputs (A and B): **(10)**

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Contd..... Q. No. 5(d)

S_2	S_1	S_0	Operation
0	0	0	Addition
0	0	1	Transfer A
0	1	0	Add 1's complement of B to A
0	1	1	Increment A
1	0	0	XOR
1	0	1	NOT
1	1	0	AND
1	1	1	OR

Draw the logic diagram of one typical stage of your designed ALU.

6. (a) What are the different addressing modes of MIPS? Describe and illustrate the calculation process for each addressing mode. **(15)**

(b) Suppose you have a 4-bit ALU and you are required to perform a division operation, where the dividend is 11001001 and the divisor is 1011. Show the division process step by step along with the value of each relevant register at each step. **(15)**

(c) How many instruction formats are there in MIPS? Write down the name of each instruction format along with the length of each field therein. **(5)**

7. (a) Consider the following MIPS assembly language code and assume that the code fragment is loaded at location 60000 in the memory: **(10)**

```
Loop:   sll  $t1,  $s2,  2
        add  $t1,  $t1,  $s6
        lw   $t0,  0 ($t1)

        beq  $t0,  $s5, Lp1
        j Exit
Lp1:    addi  $s2,  $s2,  1
        j  Loop
Exit:
```

Write down the MIPS machine code with appropriate decimal values for the above assembly code.

(b) Assume that a processor with 4 GHz clock rate is executing a program that requires the following instruction types. **(20)**

Contd 5

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Contd..... Q. No. 7(b)

Instructions	FP	INT	L/S	BRANCH
Instruction Count ($\times 10^6$)	160	110	10	16
CPI	2	1	5	2

(i) Calculate the execution time of the program.

(ii) If you want the program to run two times faster, then how much should you improve the CPI of **FP** instructions? Explain your finding.

(iii) If you want the program to run two times faster, then how much should you improve the CPI of **L/S** instructions? Explain your finding.

(iv) By how much is the execution time changed if the **CPI** of **INT** and **BRANCH** instructions are increased by 15% and the **CPI** of **FP** and **L/S** instructions are decreased by 20%?

(c) What is the use of Bias in floating point representation? Give the encoding of the floating point "infinity". **(5)**

8. (a) Consider the following C code which calculates a^b (a raised power b), **(20)**

```
int fun (int a, int b)
{
    if (b == 0)
        return 0,
    else if (b % 2 == 0)
        return fun (a*a, b/2);
    return fun (a* a, b/2)  *a;
```

Write down the equivalent MIPS assembly code for it. Use a minimal number of MIPS instructions.

(b) What are the steps of floating point addition? Describe with an example. Also, write down the condition of overflow and underflow during a floating point addition. **(10)**

(c) What is the problem in the following code snippet? How can you solve the problem? **(5)**

Address	Instruction
005000	beq $s0, $s1, 30500

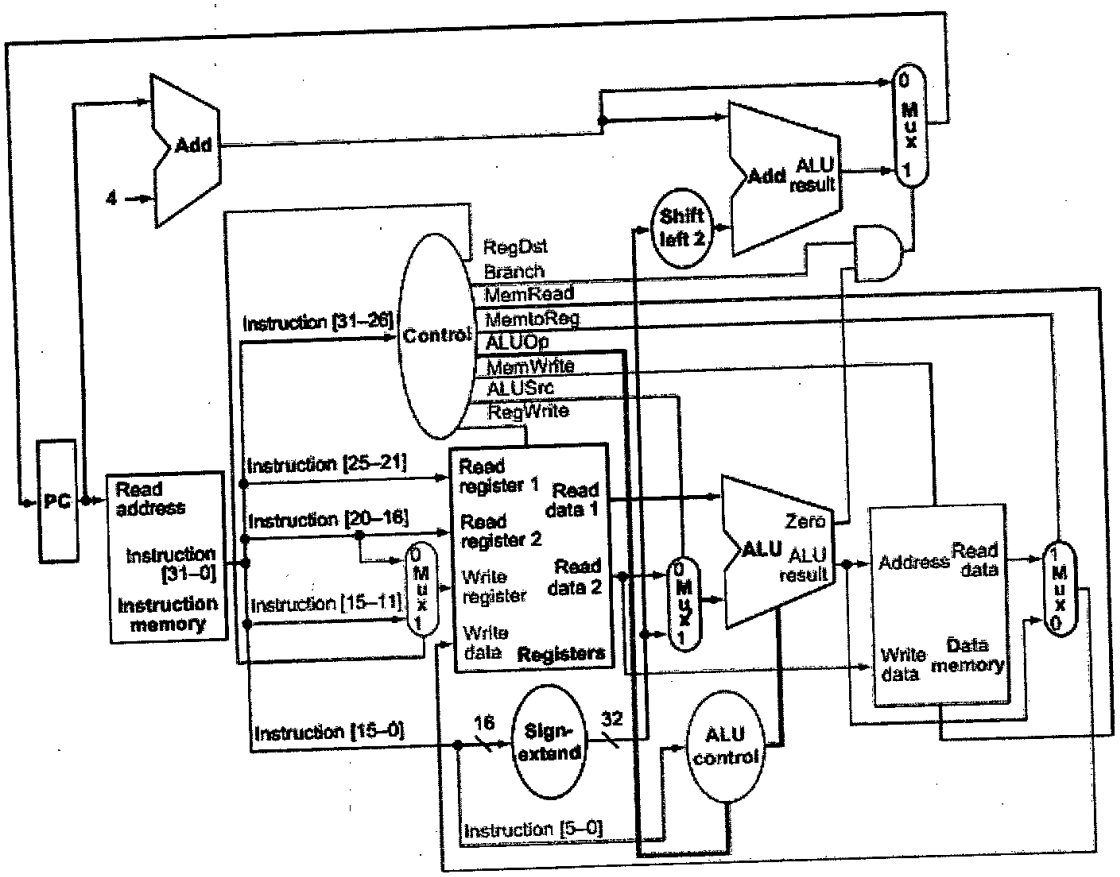
Add
4
M u x
0
1
Add
ALU result
Shift left 2
RegDst
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Instruction [31–26]
Control
PC
Read address
Instruction [31–0]
Instruction memory
Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Instruction [5–0]
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
16
Sign-extend
32
ALU
Zero
ALU result
ALU control
Address
Read data
Write data
Data memory

Figure 1.A

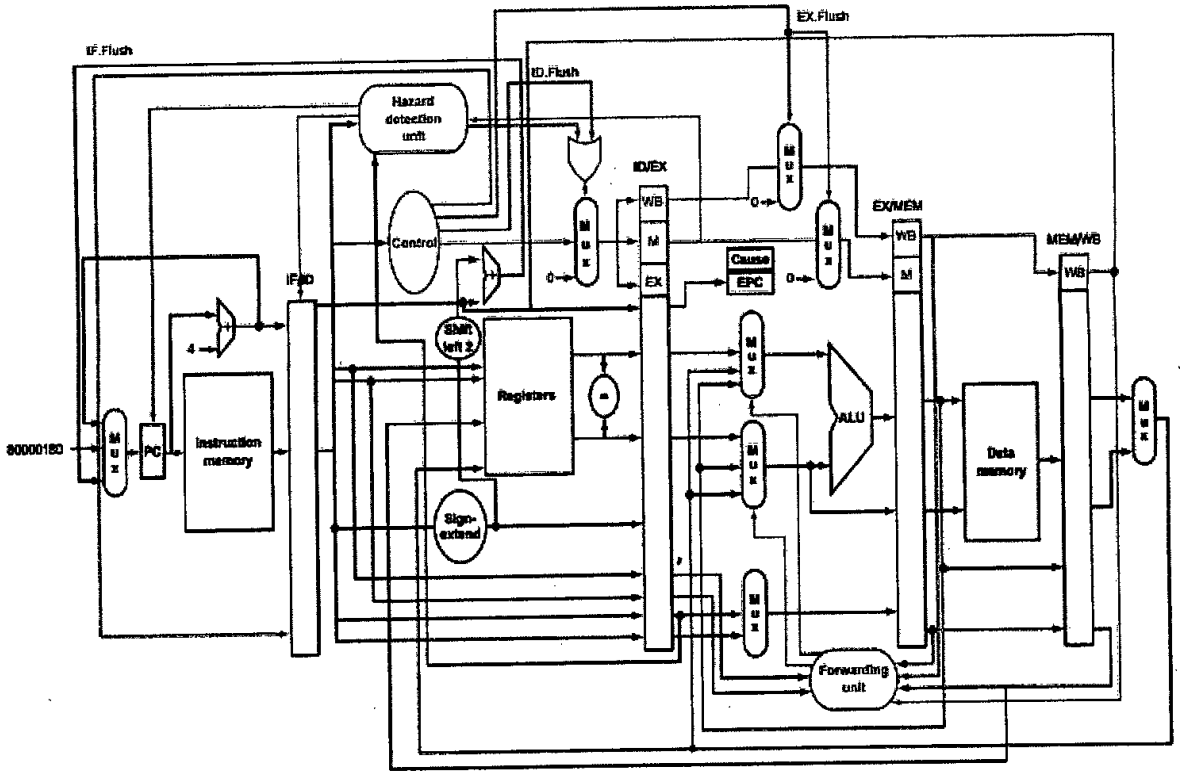
IF.Flush
EX.Flush
ID.Flush
Hazard detection unit
ID/EX
WB
M
EX
EX/MEM
MEM/WB
Control
Cause
EPC
IF/ID
4
Shift left 2
Registers
ALU
PC
Instruction memory
Data memory
Sign-extend
Forwarding unit
M u x

Fig 2.c

L-3/T-1/CSE **Date: 23/09/2018**

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USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**.

1. (a) Consider the following C code: **(10)**

A = B + C; D = A + E;

All the above are memory instructions. The base address is in register t0 and the offsets are A (0), B (4), C (8), D (12), E (16). How many cycles are required to execute the above? Can you reduce the number of cycles using code scheduling? If yes, what will be resulting number of cycles? Show each step.

(b) Consider the following set of instructions: **(15)**

add, lw, beq

Draw the complete single cycle data path (not pipelined) and control that can execute the above set of instructions.

(c) Consider the following information for load word (lw) instruction: **(5)**

Instr.	Instruction Fetch	Register read	ALU op	Memory access	Register write
lw	200 ps	100 ps	100 ps	200 ps	100 ps

Consider the following program:

lw $1, 100($0)

lw $2, 200($0)

lw $3, 300($0)

What is the speedup for the pipelined datapath over the single cycle datapath for this program? What will be the speedup if we add 3,000,000 more load word (lw) instructions?

(d) "Even with a perfect branch predictor, 1-cycle penalty for a taken branch". Why is that? How to solve this? **(5)**

2. (a) Briefly explain double data hazard with example. How MIPS detect hazard due to the use of load instruction and how MIPS stall the pipeline? **(10)**

(b) Design a complete forwarding unit with necessary equations for MIPS considering double data hazard. Draw the complete forwarding unit using the provided figure below. **(15)**

Contd P/2

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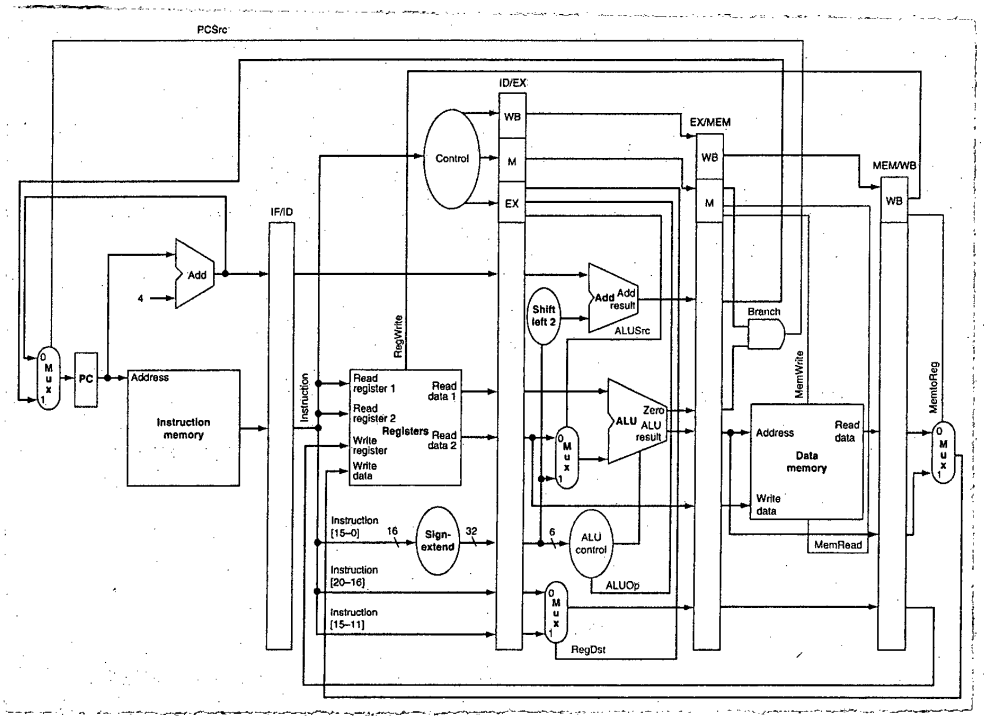
Contd... Q. No. 2(b)



(c) Give the MIPS codes for each of the following cases of data hazard for branches: **(5)**

(i) Needs one cycle stall to resolve

(ii) Needs two cycle stalls to resolve

(d) Consider the following code: **(5)**

```
outer:
    // some code
inner:
    // some code
    beq $t0, $zero, inner
    // some code
    beq $t1, $zero, outer
```

What is the problem with the above code if we use 1 bit branch predictor? How can you solve that?

3. (a) What are the three sources of cache misses? The specification of an ideal disk is as follows: **(10)**

sector size: 1 MB, rotational latency: 10000 rpm, average seek time: 5 ms, transfer rate: 100 MB/s, and controller overhead: 0.5 ms. What is the average read time for the disk? If the average seek time can be reduced to 2 ms, then how much improvement can be possible on average read time? **(10)**

Contd P/3

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Contd... Q. No. 3

(b) What is meant by spatial and temporal locality? Briefly explain write-through and write-back scheme for cache. How do write-through and write-back schemes handle write-miss? **(15)**

(c) Briefly explain how page table works with respect to virtual address, physical address, main memory and disk. **(5)**

(d) Assume the miss rate of an instruction cache is 3%, the miss rate of the data cache is 5%, and the frequency of all loads and stores is 40%. If a processor has a CPI of 2 without any memory stalls and the miss penalty is 200 cycles for all misses, determine how much faster a processor would run with a perfect cache that never missed. Also, determine the amount of execution time spent on memory stalls. **(5)**

4. (a) Suppose we have a processor with a base CPI of 1.0, assuming all references hit in the primary cache and a clock rate of 4 GHz. Assume a main memory that has an access time of 200 ns, including all the miss handling. Suppose the miss rate per instruction at the primary cache is 4%. How much faster will the processor be if we add a second level cache that has a 10 ns access time for either a hit or a miss and is large enough to reduce the miss rate to main memory to 1%? How much faster will the processor be if we add a third level cache that has a 40 ns access time for either a hit or a miss and is large enough to reduce the miss rate to main memory to 0.5%? **(10)**

(b) Assume there are three small caches, each consisting of four one-word blocks and uses LRU replacement policy. One cache is fully associative, the second is two-way set-associative, and the third is direct-mapped. Find the number of misses for each cache organization, given the following sequence of block addresses: **(15)**

- 1, 3, 5, 1, 3, 1, 3, 5, 3, 1, 5, 3

(c) What is meant by TLB? Why TLB is necessary in a virtual memory system? **(5)**

(d) Explain (with flow chart) the interaction between TLB and data cache for only write operation. **(5)**

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) Suppose there are three classes of instructions A, B and C in a particular instruction set architecture with CPIs 1.2, 2 and 2.5, respectively. The number of instructions from each class in two separate programs P1 and P2 are as follows: **(8+7=15)**

Contd P/4

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Contd... Q. No. 5(a)

Programs	Instruction Classes		
	A	B	C
P1	40	10	16
P2	12	13	40

(i) Which program will execute faster and by how much?

(ii) By how much should we improve the CPI of Instruction Class B to make P1 execute two times faster? Explain you finding.

(b) Consider a half precision floating point representation system where each floating point is represented by 16 bits in which the exponent is 4 bits long. Now convert the two floating points $(0.75)_{10}$ and $(1.25)_{10}$ into the mentioned representation system and then demonstrate the addition of them step by step along with the values of exponent and fraction fields at every step. **(15)**

(c) Determine the decimal value of the floating point represented by the hexadecimal value $(7F80\ 0005)_{hex}$ according to IEEE 754 single precision floating point format. **(5)**

6. (a) Design an ALU with three selection variables S_2, S_1 and S_0 that performs the following operations on two 4-bit inputs (A and B): **(25)**

S_2	S_1	S_0	**Operation**
0	0	0	Addition
0	0	1	Transfer A
0	1	0	Decrement A
0	1	1	Add 1's complement of B to A
1	0	0	XOR
1	0	1	AND
1	1	0	NOT
1	1	1	OR

Draw the logic diagram of one typical stage of your designed ALU.

(b) For each arithmetic operation listed in question 6(a), find out the conditions under which the output carry will be equal to 1. **(10)**

Contd P/5

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7. (a) The following C code segment can sort an array of integers in ascending order. Write down the equivalent MIPS assembly code for it. Assume appropriate registers for the variables. **(25)**

```
void swap(int v[], int k)
{
      int temp;
      temp = v[k];
      v[k] = v[k+1];
      v[k+1] = temp;
}

void sort (int v[], int n)
{
      int i, j;
      for (i = 0; i < n; i += 1) {
        for (j = i - 1; j >= 0 && v[j] > v[j + 1]; j -= 1){
           swap(v,j);
        }
      }
}
```

(b) Suppose you are required to jump to the instruction at address $(4000\ 0001)_{hex}$. Write down the MIPS assembly code for this task. **(10)**

8. (a) Suppose you have a 4-bit ALU and you are required to perform a division operation, where the dividend is 11010101 and the divisor is 1011. Show the division process step by step along with value of each relevant register at every step. **(15)**

(b) Write down the equivalent MIPS assembly code for the following function, written in C programming language. Assume appropriate registers for the variables. **(10)**

```
float convert (float cels)
{
      float ferh = (9.0 * cels) / 5.0;
      ferh = ferh + 32.0;
      return ferh;
}
```

(c) How many instruction formats are there in MIPS? Write down the name of each instruction format along with the length of each field in it. **(10)**

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USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this Section. Answer any **THREE**.

1. Consider a CPU which has PC, MAR, MDR, IR, ALU and Instruction Decoder. There are six general purpose registers R0, R1, R2, R3, R4, R5 and a temporary register TEMP inside the CPU. The CPU gets one input directly from the bus and the other input through a register Y. The output of the ALU is sent to the bus through a register Z. The ALU can perform ten arithmetic-logic operations and has a special input for Carry-in.

   (a) Draw a block diagram of single bus datapaths inside the CPU following the description above. **(10)**

   (b) Show step-wise control signals for executing the instruction

   Add (R3), R1

   which adds the contents of a memory location pointed to by Register **R3** to Register **R1**. Assume that the instruction is stored in memory and PC contains the address of the instruction. **(10)**

   (c) Design a control word for the CPU above such that the number of bits in the control word is significantly smaller than the number of control signals. **(10)**

   (d) What are the relative merits of horizontal and vertical microinstruction formats? **(5)**

2. Answer the following questions based on MIPS architecture shown in Figure 1.

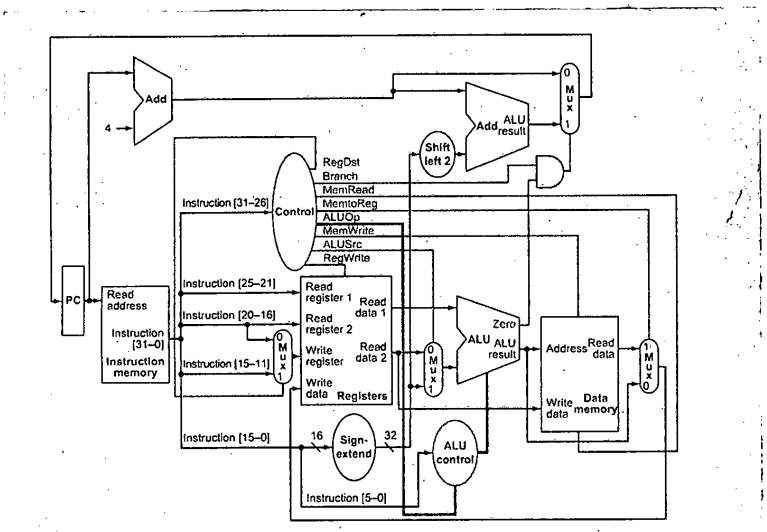

Figure 1: Figure for Question 2.

Contd P/2

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Contd ... Q. No. 2

(a) Write the functions of the control signals ALUSrc, ALUOp, RegDst, MemWrite and RegWrite. **(5)**

(b) Explain how the ALU control bits are set depending on the ALUOp control bits and the function codes for the R-type instruction. **(10)**

(c) Describe the datapaths for R-type instructions. **(10)**

(d) How is the content of the PC updated for the branch (beq) instruction? **(5)**

(e) What are the two inputs of the MUX at the input of the ALU? **(5)**

3. (a) What do you mean by the principle of locality of reference? Discuss the role of the principle of locality of reference in designing memory hierarchy. **(5)**

(b) Answer the following questions for a memory system that uses 32-bit address at the byte level, and a cache that uses a 64-byte line size. **(15)**

(i) Assume a direct cache with a tag field in the address of 20 bits. Show the address format and determine the number of addressable units, the number of blocks in main memory, and the number of lines in the cache.

(ii) Assume an associative cache. Show the address format and determine the number of addressable units, the number of blocks of main memory, the number of lines in the cache and the size of the tag.

(iii) Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the number of addressable units, the number of blocks in main memory, the number of lines in a set, the number of sets in the cache, and the number of lines in the cache.

(c) The access time of the cache M_1 of a single cache memory system is 6ns/bit during hit and that of the main memory M_2 is 900ns/bit during miss. Calculate the block transfer time and the access efficiency of the memory system at the hit ratio of 0.8. **(5)**

(d) Describe SISD, SIMD and MISD architectures with block diagrams. **(10)**

4. (a) What are pipeline hazards? Explain a structural pipeline hazard with a time-space diagram. What type of pipeline hazards occurs in the following code segment? How can it be overcome? **(10)**

```
lw    $t1, 0($t0)
lw    $t2, 4($t0)
add   $t3, $t1,$t2
sw    $t3, 12($t0)
lw    $t4, 8($t0)
add   $t5, $t1,$t4
sw    $t5, 16($t0)
```

Contd P/3

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Contd ... Q. No. 4

(b) Perform the necessary modification of the single-cycle data path in Figure 2 for pipeline implementation by inserting Pipeline Registers, Forwarding Unit and Hazard Detection Unit. Describe the modification step by step and draw the final modified datapath with all necessary control signals. **(15)**

(c) Compare the characteristics of typical CISC and RISC architectures. **(6)**

(d) Consider a bus-based shared memory multiprocessor system. It is constructed using processors with speed of 10^6 fetches/sec. and a bus with a peak bandwidth of 10^5 fetches/sec. The caches are designed to support a hit rate of 90%. **(4)**

(i) What is the maximum number of processors that can be supported by this system?

(ii) What hit rate is needed to support a 20-processor system?

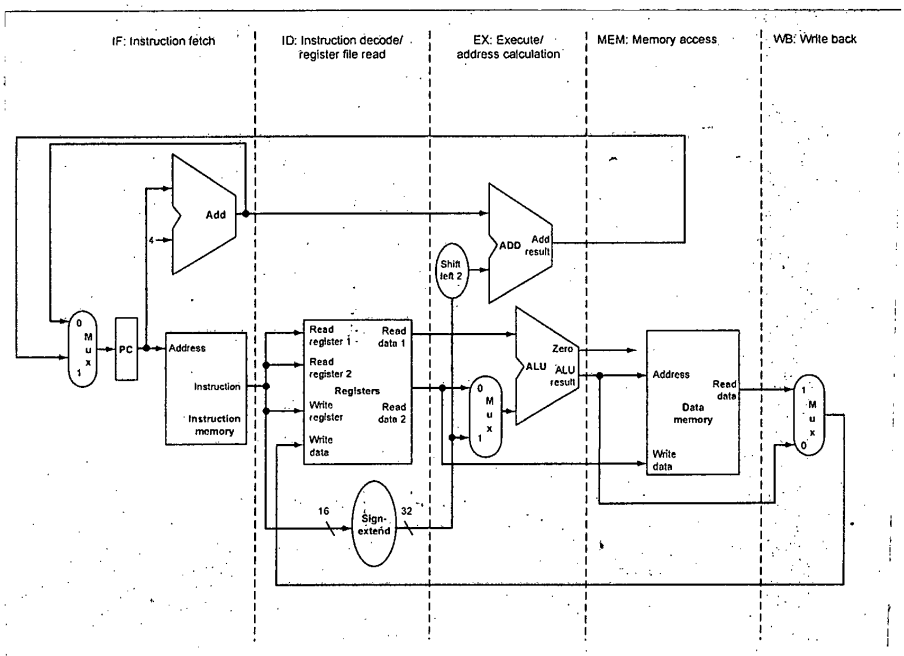

Figure 2: Figure for Question 4(b)

CSE 305

SECTION – B

There are **FOUR** questions in this Section. Answer any **THREE** questions.

5. (a) "Computer architectures have invented several great ideas in the last 60 years of computer design. These ideas are so powerful that they have lasted long after the first computer that used them, with newer architects demonstrating their admiration by imitating their predecessors." These ideas include: **(10)**

(i) Design for Moore's Law
(ii) Use abstraction to simplify design
(iii) Make the common case faster
(iv) Performance via parallelism
(v) Performance via pipelining
(vi) Performance via prediction
(vii) Hierarchy of memories
(viii) Dependability via redundancy

-You are given several design features of MIPS and other modern computing systems in the following. Now, please **identify** that which of the above great ideas are behind these design decisions.

(i) While implementing instructions at hardware level, it is possible to implement all the instructions as single cycle instructions. However, modern designers do not use this single-cycle design as it is inefficient. (hint: for single cycle implementation, the clock cycle must have the same length for every instruction and the longest instruction determine the clock cycle length.)

(ii) Modern computers use a technique called prefetching. "In prefetching, a block of data is brought into the cache before it is actually referenced. Many microprocessors use hardware perfectching to access the block needed in the future that may be difficult for software to notice".

(b) Lenovo x3650 M5 server containing a 32 cores (Intel Xeon E5-2699v4) obtained following results in SPEC test. Find the spec ratio for the computer. **(10)**

Program Name	Execution Time	Reference Time	Spec Ratios
perlbench	236	9770	
bzip2	375	9650	
gcc	208	8050	
mcf	133	9120	
gobmk	337	10490	
hmmer	105	9330	
sjeng	340	12100	
libquantum	2	20720	
h264ref	379	22130	
omnetpp	119	6250	
astar	195	7020	
xalancbmk	86	6900	
Spec ratui (Specint2006)	-	-	

Contd P/5

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Contd ... Q. No. 5

(c) Assume a processor with 3 GHz clock rate is executing a program that requires following instructions, **(15)**

Instructions →	FP	INT	L/S	BRANCH
Instruction Count ($\times 10^6$)	40	80	90	15
CPI	1	1	3	2

(i) Calculate the execution time of the program.

(ii) By how much must we improve the CPI of **FP** instructions if we want the program to run two times faster?

(iii) By how much is the execution time program changed (improved or degraded) if the **CPI** of **INT** and **FP** instruction is increased by 20% and the **CPI** of **L/S** and Branch is reduced by 10%?

6. (a) A simple MIPS assembly code snippet and it's corresponding MIPS machine code is given below. Note that, the former one is not complete. Please complete it with appropriate MIPS assembly code. **(10)**

	sll	1000	0	00000	10000	01111	00010	000000
	add	1004	0	01111	10001	01111	00000	100000
	lw	1008	35	01111	01000	00000	00000	000000
	bne	1012	5	01000	10111	00000	00000	000001
	addi	1016	8	10000	10000	00000	00000	000001
	j	1020	2	00000	00000	00000	00011	111010

(b) What support does MIPS instruction set architecture provide for synchronization? Explain with an example. **(10)**

(c) The following four design principles have been guiding the instruction-set designers to find a balance between the number of instructions needed to execute a program, the number of clock cycles needed by an instruction, and the speed of the clock. **(15)**

(i) Simplicity favors regularity

(ii) Smaller is faster

(iii) Good design demands good compromise

(iv) Make the common case faster

- You are given several design features of MIPS instruction-set architecture in the following. Now, please identify that which of the above principles are behind these design decisions.

Contd P/6

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Contd ... Q. No. 6(c)

(i) keeping instruction immediate value in a range of 16-bits

(ii) always requiring three register operands in arithmetic instructions

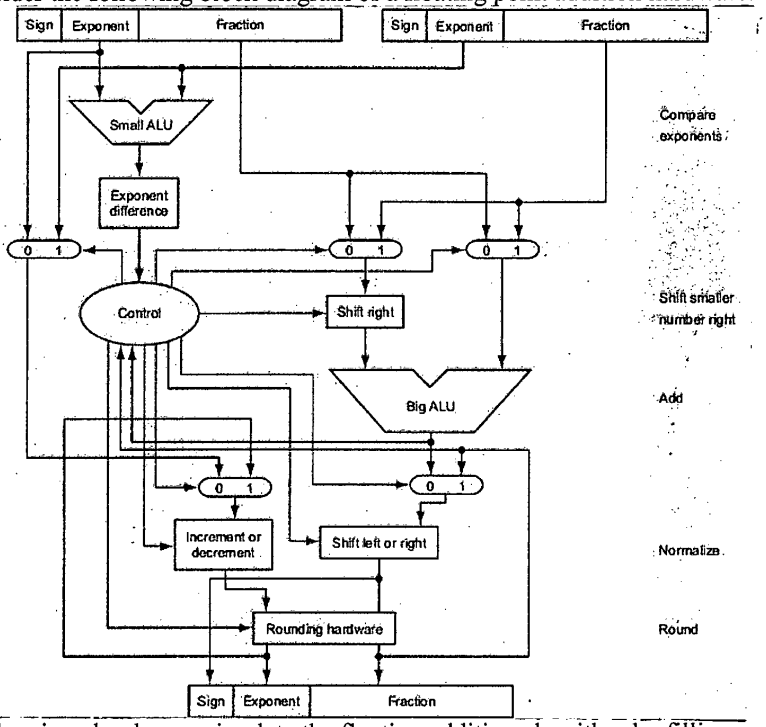
(iii) using PC-relative addressing for conditional branching

(iv) keeping 32 registers rather than many more

(v) keeping the register fields in the same place in each instruction format

7. (a) Please draw the illustrations of he five MIPS addressing modes. Also give an example instruction for each of the five addressing modes. **(10+10)**

(b) Consider the following block diagram of a floating point addition hardware. **(15)**



-Using the given hardware, simulate the floating addition algorithm by filling up the following tables. The two numbers for addition are, $-(0.25)_{10}$ and $(0.625)_{10}$

	$-(0.25)_{10}$	$(0.625)_{10}$
Binary		
Step1: Exponent Matching		
Step2: Significand Addition		
Step3: Normalization		=
Step4: Rounding		

Contd P/7

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8. (a) The following table illustrates the various combinations of two operands for binary addition-subtraction. Please identify the overflow conditions in that table. Then, formulate the overflow boolean variable as a logical function of various input variables (You don't need to simplify the function). **(5+5)**

O	S_A	S_B	S_R	V
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Here,

$$\text{Operation, } O = \begin{cases} 0, & A + B \\ 1, & A - B \end{cases}$$

$$\text{Sign bit of Operand A, } S_A = \begin{cases} 0, & A \geq 0 \\ 1, & A < 0 \end{cases}$$

$$\text{Sign bit of Operand B, } S_B = \begin{cases} 0, & B \geq 0 \\ 1, & B < 0 \end{cases}$$

$$\text{Sign bit of Result R, } S_R = \begin{cases} 0, & R \geq 0 \\ 1, & R < 0 \end{cases}$$

$$\text{Overflow, } V = \begin{cases} 1, & \text{Overflow occurred} \\ 0, & \text{No overflow possible} \end{cases}$$

Contd P/8

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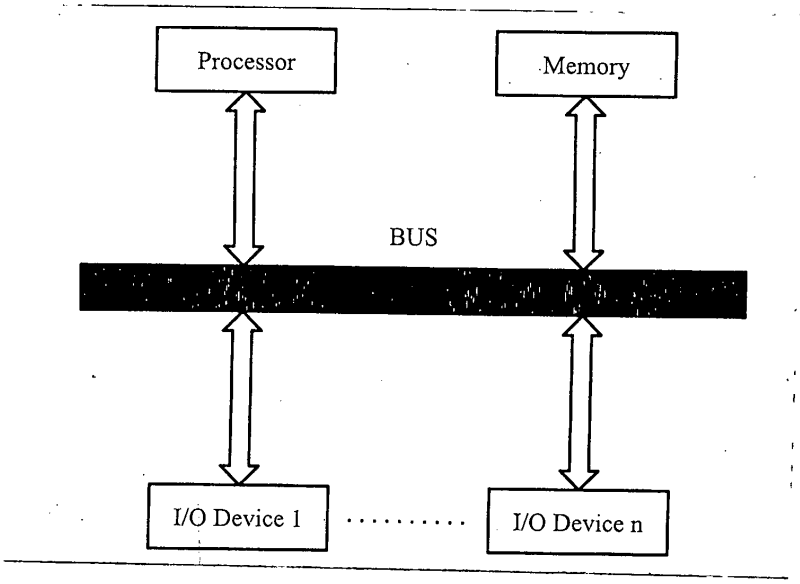
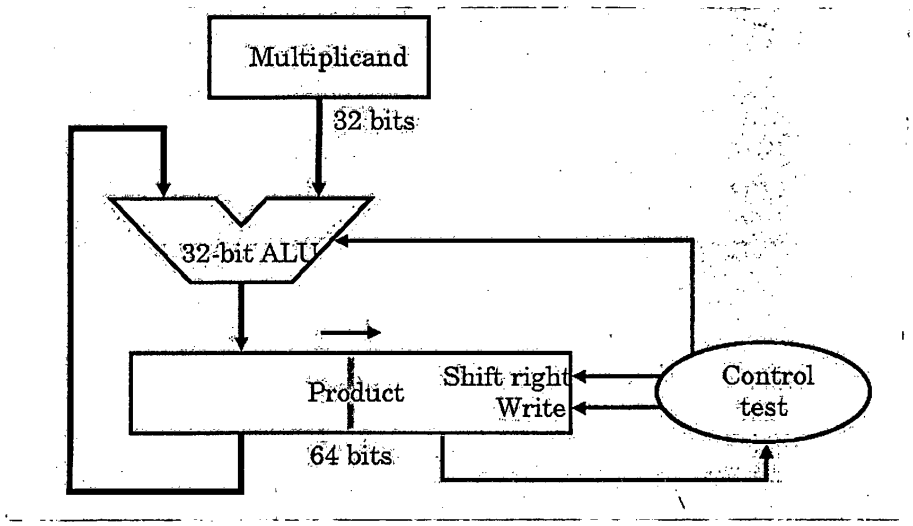
Contd ... Q. No. 8

(b) In the following figure, a single bus computer architecture was drawn where, various devices like processor, memory, and I/O devices are connected with each other via a single BUS. Please note that, these devices do not operate at a similar rate. Then, how can you redesign this single bus computer architecture so that these devices can interact with each other smoothly using this single bus. Just draw your redesigned single bus computer architecture. **(10)**



(c) Consider the following multiplication hardware. **(15)**



-Using the given hardware, simulate the unsigned multiplication algorithm by filling up the following tables for Multiplicand, 0110 and Multiplier, 0110.

Contd P/9

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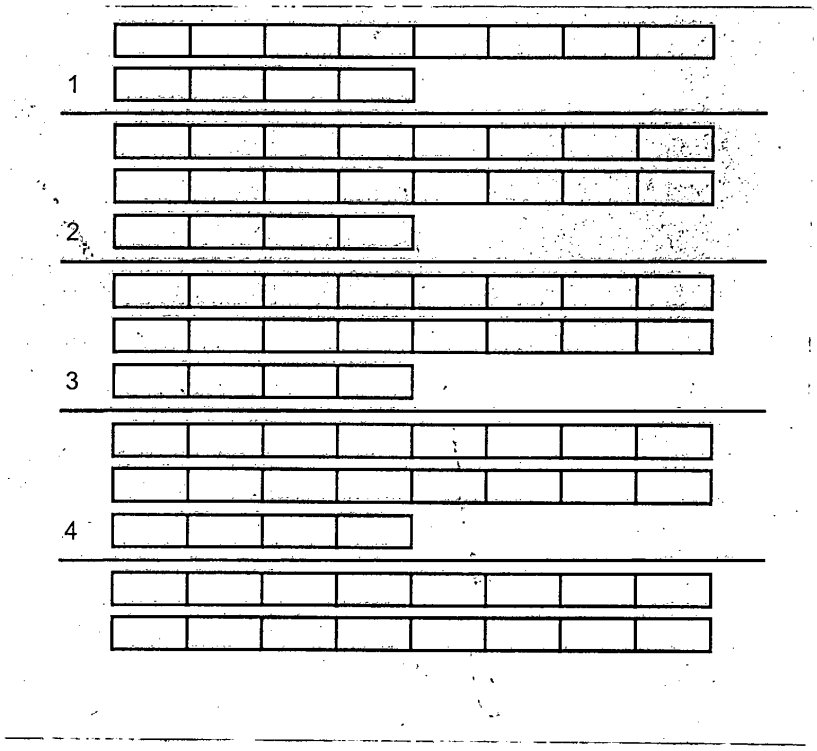
Contd ... Q. No. 8(c)



L-3/T-1/CSE Date : 26/01/2016

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-1 B. Sc. Engineering Examinations 2014-2015

Sub : **CSE 305** (Computer Architecture)

Full Marks : 210 Time : 3 Hours

The figures in the margin indicate full marks.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**.

1. (a) Describe SISD, SIMD, MIMD and MISD architectures with block diagrams. **(10)**

   (b) Consider a bus-based shared memory multiprocessor system. It is constructed using processors with speed of 10^6 fetches/sec, and a bus with a peak bandwidth of 10^5 fetches/sec. The caches are designed to support a hit rate of 90%. **(4)**

   (i) What is the maximum number of processors that can be supported by this system?

   (ii) What hit rate is needed to support a 20-processor system?

   (c) Compare the characteristics of typical CISC and RISC architectures. **(8)**

   (d) Show the time-space diagram for pipelining in a superscalar processor. Briefly describe the architecture of a typical superscalar RISC processor with necessary block diagrams. Mention the differences between a superscalar processor and a VLIW processor. **(3+8+2)**

2. (a) List out the key characteristics of computer systems. What do you mean by the principle of locality of reference? Discuss the role of the principle of locality of reference in designing memory hierarchy. **(6+3+3)**

   (b) Write short notes on (i) flash storage and (ii) holographic data storage. **(4+4)**

   (c) Answer the following questions for a memory system that uses 32-bit address at the byte level, and a cache that uses a 64-byte line size. **(15)**

   (i) Assume a direct cache with a tag field in the address of 20 bits. Show the address format and determine the number of addressable units, the number of blocks in main memory, and the number of lines in the cache.

   (ii) Assume an associative cache. Show the address format and determine the number of addressable units, the number of blocks of main memory, the number of lines in the cache and the size of the tag.

   (iii) Assume a four-way set-associative cache with a tag field in the address of 9 bits. Show the address format and determine the number of addressable units, the number of blocks in main memory, the number of lines in a set, the number of sets in the cache, and the number of lines in the cache.

Contd P/2

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3. (a) What are pipeline hazards? Explain a structural pipeline hazard with a time-space diagram. What type of pipeline hazards occurs in the following code segment? How can it be overcome? **(10)**

```
lw    $t1,  0($t0)
lw    $t2,  4($t0)
add   $t3,  $t1, $t2
sw    $t3,  12($t0)
lw    $t4,  8($t0)
add   $t5,  $t1, $t4
sw    $t5,  16($t0)
```

(b) Briefly describe different dynamic branch prediction techniques for dealing with control hazards. **(10)**

(c) Perform the necessary modification of the single-cycle data path in Figure 1 for pipeline implementation by inserting pipeline registers and a forwarding unit. Describe the modification step by step and draw the final modified datapath with all necessary control signals. **(15)**

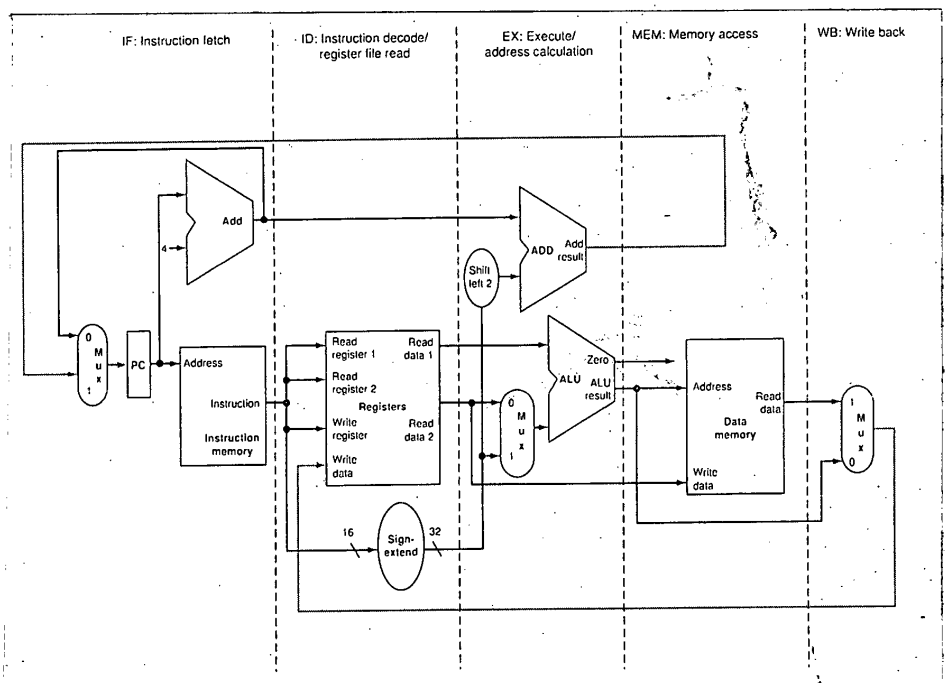

Figure 1: Figure for Question 3(c)

4. (a) Show the components of an I/O module using a block diagram and describe the functions of each component. **(8)**

(b) Describe the operation of a vector interrupt structure with daisy chain interface for detecting and managing interrupting I/O devices. **(10)**

Contd P/3

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Contd ... Q. No. 4

(c) Mention the advantages of DMA transfer over programmed I/O and interrupt-driven I/O. Briefly describe a DMA transfer structure with necessary diagrams. **(4+8)**

(d) The access time of the cache M_1 of a single cache memory system is 6ns/bit during hit and that of the main memory M_2 is 900ns/bit during miss. Calculate the block transfer time and the access efficiency of the memory system at the hit ratio 0.8. **(5)**

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) "Computer architects have invented several great ideas in the last 60 years of computer design. These ideas are so powerful that they have lasted long after the first computer that used them, with newer architects demonstrating their admiration by imitating their predecessors". These ideas include: **(20)**

    1. Design for Moore's Law
    2. Use abstraction to simplify design
    3. Make the common case faster
    4. Performance via parallelism
    5. Performance via pipelining
    6. Performance via prediction
    7. Hierarchy of memories
    8. Dependability via redundancy

    You are given several design features of MIPS and other modern computing systems in the following. Now, please **identify** that which of the above great ideas are behind these design decisions.

    1. In MIPS datapath, there is an adder which computes the value of **(PC+4)**, where PC means Program Counter. For branch addressing the MIPS address is actually relative to this **(PC+4)** rather than **(PC)**. This form of branch addressing is called PC-relative addressing.
    2. In the past, most PCs (personal computers) and server systems used separate SRAM (static random access memory) chips for either their primary, secondary, or even tertiary caches. Today, all levels of caches are integrated onto the processor chip, so the market for separate SRAM chips has nearly evaporated.
    3. A fast multiplication hardware, "unrolls the loop" by using 31 adders rather than using a single 32-bit adder 31 times.
    4. Procedures or Functions allow programmers to concentrate on just one portion of the task at a time, parameters act as an interface between the procedure and the rest of the program and data, since they can pass values and return results.
    5. Modern computers use a technique called prefetching. In prefetching, a block of data is brought into the cache before it is actually referenced. Many microprocessors use hardware prefetching to access the block needed in the future that may be difficult for software to notice.

Contd P/4

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Contd ... Q. No. 5

(b) Assume a processor with 2 GHz clock rate is executing a program that requires the following instructions. **(15)**

Instructions	FP	INT	L/S	BRANCH
Instruction Count ($\times 10^6$)	160	110	10	16
CPI	2	1	5	2

(i) Calculate the execution time of the program.

(ii) By how much must we improve the CPI of **FP** instructions if we want the program to run two times faster?

(iii) By how much must we improve the CPI of **L/S** instructions if we want the program to run two times faster?

6. (a) A simple recursive C function and it's corresponding MIPS assembly code is given below. Note that, the later one is not complete. Please complete it with appropriate expressions. **(15)**

```
int recurseSum(int n){
   if(n<1) return 0;
   else return n+recurseSum(n-1);
}
```

```
recurseSum:
[    ] $t0, $a0, 1
beq $t0, $zero, Recurse
add $v0, $zero, $zero
jr [    ]
Recurse:
addi $sp, $sp, [    ]
sw $ra, [    ]
sw [    ], 0($sp)
addi $a0, $a0, -1
jal recurseSum
lw [    ], 0($sp)
lw $ra, [    ]
[    ]
add [    ], $a0, $v0
jr [    ]
```

(b) What support does MIPS instruction set architecture provide for synchronization? **(5)**

(c) A simple MIPS assembly code snippet and it's corresponding MIPS machine code are given below. Note that, the later one is not complete. Please complete it with appropriate decimal values. **(15)**

```
Loop:   sll $t1, $s2, 2
        add $t1, $t1, $s6
        lw $t0, 0($t1)
        beq $t0, $s5, L1
        j Exit
L1:     addi $s2, $s2, 1
        j Loop
Exit:
```

6000	0	0	18	9		0
6004	0				0	32
6008	35			0		
6012	4	8	21			
6016						
6020	8	18	18	1		
6024	2					
6028						

Contd P/5

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7. (a) Please draw the illustrations at the five MIPS addressing modes. **(15)**

(b) MIPS instruction set architecture supports *beq* and *bne* instructions, however, does not support other branching instructions like *blt*, *bge*, etc. What is the reason behind this design decision? How could you program these instructions (*blt*, *bge*, etc.) in MIPS instructions? **(5+5)**

(c) What is the problem in the following code snippet? How can you solve this problem? **(5+5)**

Address	Instruction
005000	`beq, $s0, $s1, 30500`

8. (a) The following table illustrates the various combinations of two operands for binary addition-subtraction. Please identify the overflow conditions in that table. Then, formulate the overflow boolean variable as a logical function of various input variables (You don't need to simplify the function). **(8+4)**

O	S_A	S_B	S_R	V
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Here,

$$\text{Operation, } O = \begin{cases} 0, & A + B \\ 1, & A - B \end{cases}$$

$$\text{Sign bit if Operand A, } S_A = \begin{cases} 0, & A \geq 0 \\ 1, & A < 0 \end{cases}$$

$$\text{Sign bit of Operand B, } S_B = \begin{cases} 0, & B \geq 0 \\ 1, & B < 0 \end{cases}$$

$$\text{Sign bit of Result R, } S_R = \begin{cases} 0, & R \geq 0 \\ 1, & R < 0 \end{cases}$$

$$\text{Overflow, } V = \begin{cases} 0, & \text{Overflow occured} \\ 1, & \text{No overflow possible} \end{cases}$$

Contd P/6

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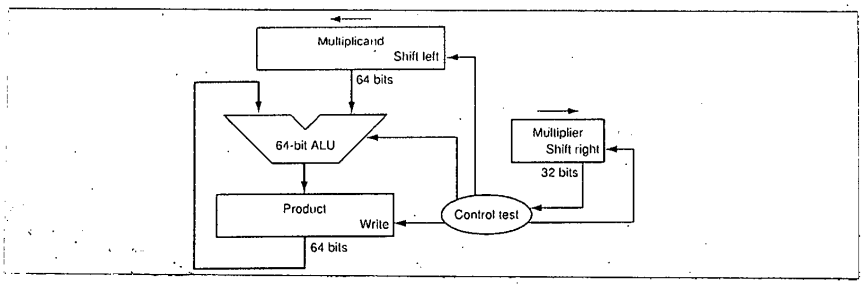
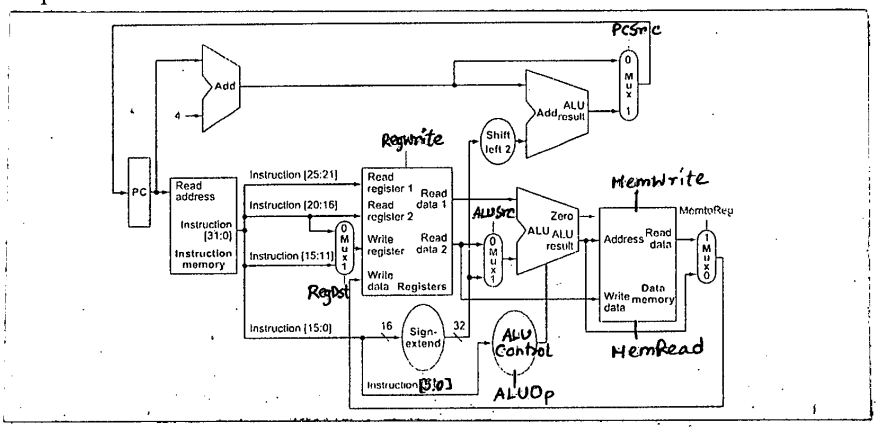
Contd ... Q. No. 8

(b) In the following figure, a multiplication hardware is given. Now draw the flowchart of a the sequential version of multiplication algorithm for this hardware. Please note that, this simple hardware is not register-optimized, therefore, draw a register-optimized refined version of this hardware. **(8+5)**



(c) A simple MIPS datapath and its respective control signals are illustrated below. Please design the control bits corresponding to the instruction "`beq rs, rt, address`" for this datapath. **(10)**



Control Signal	0	1
RegDst	Write register address = rt	Write register address = rd
RegWrite	-	Write register
ALUSrc	ALU Second Operand = Read data 2	ALU Second Operand = lower 16-bit of instruction
MemRead	-	Read data from memory
MemWrite	-	Write data into memory
MemtoReg	Register Write Data from ALU	Register Write Data from data memory
PCSrc	PC=PC+4	PC=branch target
ALUOP1	not dependent on function	dependent on function
ALUOP0	addition	subtraction

L-3/T-1/CSE Date : 05/07/2015

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-1 B. Sc. Engineering Examinations 2013-2014

Sub : **CSE 305** (Computer Architecture)

Full Marks : 210 Time : 3 Hours

The figures in the margin indicate full marks.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**.

1. (a) State the principle of temporal locality and the principle of spatial locality. **(3+3)**

   (b) Assume a two-way set associative cache with four blocks. The current state of the cache is empty. Assuming an LRU replacement policy, how many hits does the address sequence 0, 2, 4, 0, 2, 4, 0, 2, 4 exhibit? Show the state of the cache after every address access. **(9)**

   (c) State three conditions required for a cache/memory to be coherent. **(9)**

   (d) What is the limitation of a processor that does not have a TLB but uses the virtual memory technique? **(5)**

   (e) What is the size of the tag field for a direct-mapped cache with 2^n blocks and the following configuration: 32-bit byte address and the block size: 2^m words (Assume 1 word = 4 bytes). **(6)**

2. (a) Suppose a single shared memory processor has 20 GB of main memory. Five clustered computers each have 4 GB. The OS occupies 1 GB. How much more space is there for users with shared memory? **(5)**

   (b) Determine the total network bandwidth and dissection bandwidth for ring and fully connected topologies. Assume that the number of processor is P. **(8)**

   (c) Differentiate UMA shared memory multiprocessor from NUMA shared memory multiprocessor. **(5)**

   (d) A virtual memory system has the following parameters: **(7)**

   Virtual address (bits): 32
   Physical DRAM installed: 4 GB
   Page size: 8 KB
   PTE size (byte): 4

   How many page table entries are needed? How much physical memory is needed for storing the page table?

   (e) Write down the procedure to handle a TLB page miss. **(10)**

3. (a) Write down the steps for the addition of two binary floating point numbers. **(10)**

   (b) Show the IEEE 754 binary representation of the number -0.75_{ten} in single precision. **(10)**

   (c) Draw a block diagram of hardware organization and corresponding flowchart for the multiplication of two 32-bit binary unsigned integer numbers, where there is no separate multiplier register. **(15)**

Contd P/2

CSE 305

4. (a) Why does RAID 0 improve disk performance? **(5)**

(b) Write down the steps of handling an interrupt. **(12)**

(c) What happens if the interrupt enable bit of the Cause register is not set when handling an interrupt? What value could the interrupt mask value take to accomplish the same thing? **(3+3)**

(d) What is "DMA stale data problem"? How can it occur in a system with caches? **(12)**

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) What is Moore's Law? What do you mean by response time and throughput? **(6)**

(b) Consider two different implementations of the same instruction set architecture. There are four classes of instructions, A, B, C and D. The clock rate and CPI of each implementation are given in the following table: **(15)**

Implementation	Clock Rate	CPI Class A	CPI Class B	CPI Class C	CPI Class D
P1	3 GHz	1	2	3	4
P2	2 GHz	2	2	2	2

Given a program with 200 instruction divided into classes as follows:

10% class A, 20% class B, 50% class C and 20% class D.

(i) Find the clock cycles required in both cases.

(ii) Which implementation is faster?

(iii) What is the global CPI for each implementation?

(c) What do you mean by Amdahl's law? Write down the equation. Suppose a sample program takes 100 seconds to complete. The division operation accounts for 80 seconds. How much improvement in division operations' performance can give 4x overall improvement? **(8)**

(d) Consider the following information for two different computers. **(6)**

Computer	Number of Instructions	Clock Rate	CPI
A	10 Billion	4 GHz	1
B	8 Billion	4 GHz	1.1

(i) Which one has the highest MIPS rating?

(ii) Which one is faster?

6. (a) What are the four design principles used for MIPS instruction set design? What are the steps for starting a Java application? **(8)**

(b) Write down the MIPS code and corresponding machine code for the following C code. **(12)**

A [3] = A [1] – A [2];

Consider the base address of A is in Ss0. The op-code for load word is 35, and for store word is 43. The (op-code, function-code) for addition is (0, 32), and for subtraction is (0, 34). Registers St0 to $t7 are numbered from 8 to 15, and $s0 to Ss7 are numbered from 16 to 23.

Contd P/3

CSE 305

Contd ... Q. No. 6

(c) Write down the MIPS code for the following C procedure: **(12)**

```
int sum (int n)
{
        if (n <=0) return 0;
        else return n + sum (n – 1);
}
```

Consider n in $a0 and result in Sv0.

(d) If branch target is too far to encode with 16-bit offset, hoe does the assembler rewrite the following code: **(3)**

```
beq $s0, Ss1, L1
```

7. (a) Briefly describe the two instructions used for synchronization in MIPS. Write down the MIPS code to do the following atomically: **(8)**

A [0} = X

Consider the base address of A is in $s1 and X is in Ss2.

(b) Describe MIPS addressing modes. **(4)**

(c) Consider the following set of instruction: **(14)**

add, sw, beq

Draw the complete single cycle datapath (not pipelined) and control that can execute the above set of instructions.

(d) What are the five states of MIPS pipeline? Consider the following information for load word (lw) instruction **(9)**

Instruction	Instruction Fetch	Register read	ALU op	Memory access	Register write
lw	200 ps	100 ps	200 ps	200 ps	100 ps

Consider the following program:

```
lw $1, 100(S0)
lw $2, 200(S0)
lw $3, 300(S0)
```

What is the speedup for the pipelined datapath over the single cycle datapath for this program? What will be the speedup if we add 1,000,000 more load word (lw) instructions?

8. (a) Draw the complete MIPS pipelined datapath and control for load word (lw) instruction with pipelined registers. **(15)**

(b) Consider the following MIPS code: **(7)**

```
add $s0, St0, $t1
sub $t2, $s0, St3
lw $s1, 20($t1)
sub $t4, $s1, St2
```

How many data hazards are there? Describe the techniques to eliminate data hazards in the above code.

Contd P/4

CSE 305

Contd ... Q. No. 8

(c) What do you mean by data hazard for branches? Give examples with MIPS code for each of the following cases of data hazards for branches: **(9)**

(i) Needs no stall to resolve

(ii) Needs one cycle stall to resolve

(iii) Needs two cycle stalls to resolve

(d) Consider the following code: **(4)**

```
outer:
        // some code
inner:
        // some code
beq $t0, $zero, inner
// some code
beq $t1, $zero, outer
```

What is the problem with the above code if we use 1 bit branch predictor? How you can solve that? Explain

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CE 314
12+3

L-3/T-1/CSE **Date : 10/05/2014**

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-1 B. Sc. Engineering Examinations 2012-2013

Sub : **CSE 305** (Computer Architecture)

Full Marks : 210 Time : 3 Hours

The figures in the margin indicate full marks.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this section. Answer any **THREE**.

1. (a) What is a jump address table? Discuss with an appropriate example how Case/Switch Statements can be implemented with a jump address table. (15)

   (b) How you can create a 32 bit constant in MIPS Assembly Language? (5)

   (c) Consider the following MIPS assembly language code and assume that the code fragment is loaded at location 80000 in the memory. What should be the values of the immediate fields of *bne* instruction and *j* instruction? (8)

```
Loop:   s11 $t1,$s3,2
        add $t1,$t2,$s6
        Lw $t0, o($t1)
        bnr $to,$s5, Exit
        addi $s3, $s3, 1
        j Loop
Exit:
```

   (d) Explain why the assembler might have problems directly implementing the branch instruction in the following code fragment. How can this problem be fixed? (7)

```
Here: beq $s0, $s2, there
...
...
there: add $s0, $s0, $s0.
```

2. Consider the single cycle datapath in Figure 2 which is constructed for *add, sub, and, or, lw, sw, beq*. Now, implement the following instructions in the datapath: *bne, j, jr, jal.* You need to clearly explain your implementation and mention the values of the control lines (including any additional control lines you have introduced) for the new instructions. (35)

   [You may modify Figure 2 (separate sheet) and attach the update figure with your answer script after having it signed by the respected invigilator.]

Contd P/2

CSE 305

3. (a) Present and explain a microprogram for the control unit of the multicycle implementation illustrated in Figure 3. (17)

(b) Modify the implementation of Figure 3 so that it can handle the **Underfined Instruction Exception** and the **Overflow Exception.** (8)

[You may modify Figure 3 (separate sheet) and attach the updated figure with your answer script after having it signed by the respected invigilator.]

(c) Which stage should you detect the **overflow exception** in so as to ensure that the offending instruction does not change the content of the destination register? Justify your answer. (5)

(d) Your friend claims that the *PCWriteCond* signal can be safely replaced by *PCSource[0]*. Do you agree with him? Justify your answer. (5)

4. (a) Discuss how you can detect data hazards and solve those with the help of a forwarding unit. (17)

(b) Present a scenario when you cannot solve a data hazard with the help of a forwarding unit. Suggest what to do in this case. (13)

(c) What is a branch hazard? (5)

SECTION – B

There are **FOUR** questions in this section. Answer any **THREE**.

5. (a) What is the average time to read or write a 512-byte sector for a typical disk rotating at 15,000 RPM? The seek time is 4 ms, the transfer rate is 100 MB/sec, and the controller overhead is 0.2 ms. Assume that the disk is idle so that there is no waiting time. (10)

(b) What is the purpose of using RAID organization? Briefly describe the concept of different RAID levels with diagrams. (2+18)

(c) Differentiate between NAND and NOR flash memories. (5)

6. (a) Consider a computer running program with CPU times shown in the following table: (3+3+3)

FP intr.	INT instr.	Load/Store instr.	Branch intr.	Total Time
50sec	80sec	50sec	30sec	210sec

(i) By how much (in %) is the total time reduced if the time for FP operations is reduced by 20%?

(ii) Assume that the time for INT operations is improved. By how much (in %) is the time for INT operations is reduced if the total time is reduced by 20%?

(iii) Can the total time be reduced by 20% by reducing only the time for branch instructions?

Contd P/3

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(b) What is the disadvantages of using virtually addressed cache? (6)

(c) "The TLB acts as a cache of the page table for the entries that map to physical pages only" – Do you agree or disagree? Explain. (7)

(d) A program accesses 2 cache blocks, one that begins at memory address 0x1000 and another one that begins at memory address 0x2000. Memory accesses alternate between these two blocks and each block is accessed 100 times.

If the program is run on a system with a 1 KB direct-mapped cache with 32 blocks, how many cache misses will occur? (13)

How many of these misses will be compulsory and conflict misses. Mention the reason behind classifying a miss as a compulsory or a conflict miss. Note that there will be no capacity miss as the total amount of data accessed by the program is less than the capacity of the cache.

7. (a) State the advantages of using write back cache. (6)

(b) If a cache has a capacity of 16 KB and a line length (block size) of 128 bytes, how many sets does the cache have if it is 2-way, 4-way and 8-way set associative? (9)

(c) Consider a processor with following parameters: (12)

Base CPI, no memory stalls: 2.0

Processor speed: 1 GHz

Main memory access time: 100 ns

First-level cache miss rate per instruction: 4%

Second level cache, direct-mapped speed: 10 cycles

Global miss rate with second-level cache, direct mapped: 4%

Second level cache, eight-way set associative speed: 20 cycles

Global miss rate with second-level cache, eight-way set associative: 1.6%

Calculate the CPI for the processor using (i) only a first-level cache, (ii) both a first-level cache and a second-level direct-mapped cache, (iii) both a first level cache and a second-level eight-way set associative cache.

(d) Briefly discuss interleaved memory organization. (4)

(e) Differentiate between fine-grain and coarse-grain multithreading. (4)

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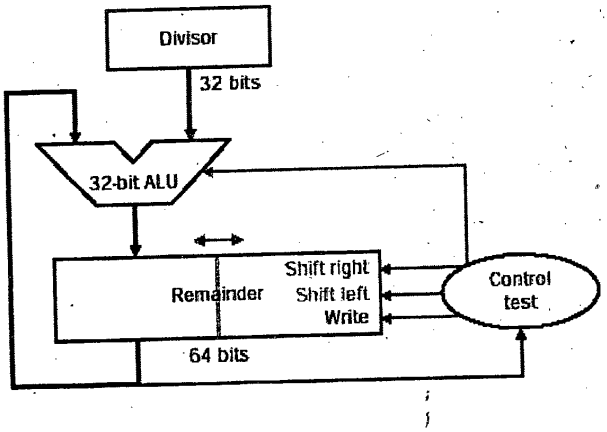
8. (a) What is the purpose of using biased notation for representing exponents of floating point numbers? (5)

(b) Draw the flowchart showing the execution steps of the division operation for the division hardware organization given below: (12)



(c) Describe the steps of DMA transfer. (8)

(d) Discuss crossbar network and Omega network with diagrams. (10)

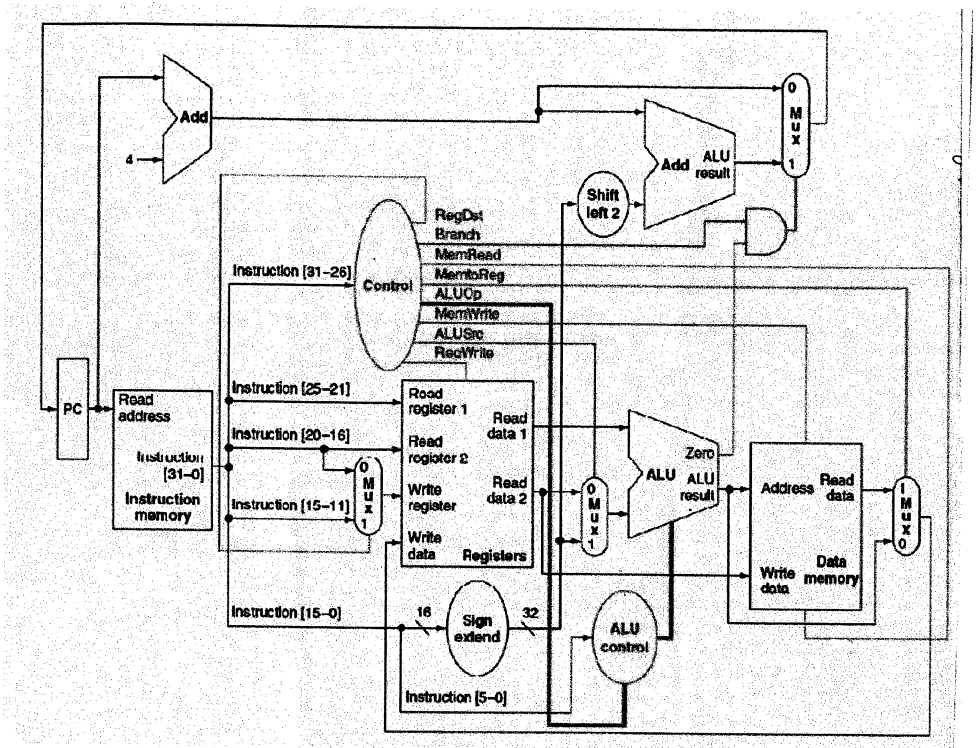

Add
4
0
M
u
x
1
Add
ALU result
Shift left 2
RegDst
Branch
MemRead
MemtoReg
ALUOp
MemWrite
ALUSrc
RegWrite
Instruction [31–26]
Control
PC
Read address
Instruction [31–0]
Instruction memory
Instruction [25–21]
Instruction [20–16]
Instruction [15–11]
Instruction [15–0]
Instruction [5–0]
Read register 1
Read register 2
Write register
Write data
Read data 1
Read data 2
Registers
ALU
Zero
ALU result
Address
Read data
Write data
Data memory
16
Sign extend
32
ALU control

Figure – 2

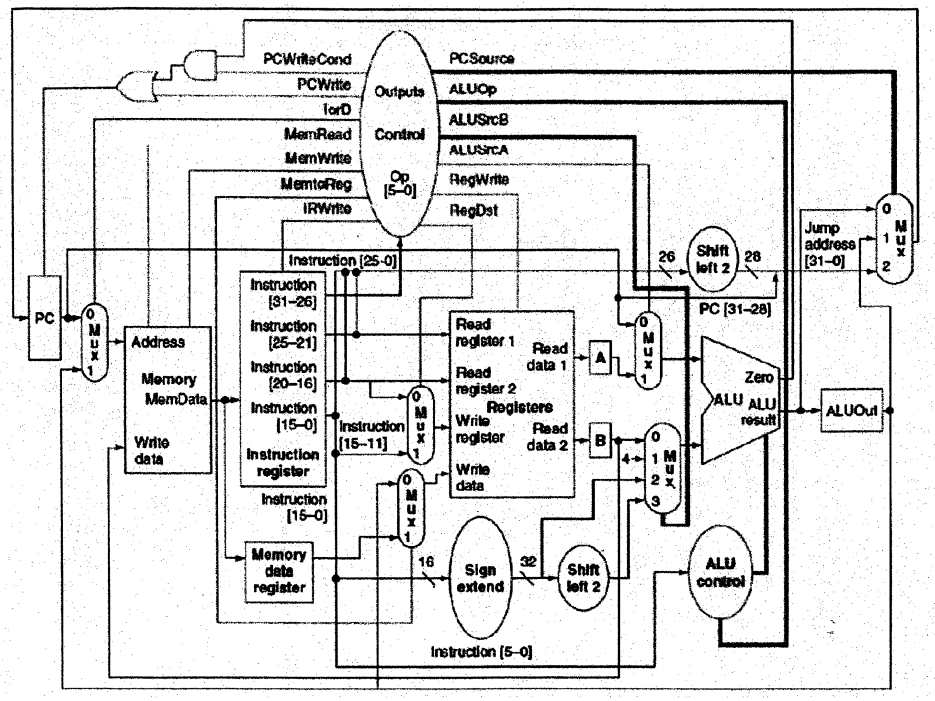

PCWriteCond
PCWrite
IorD
MemRead
MemWrite
MemtoReg
IRWrite
Outputs
Control
Op
[5–0]
PCSource
ALUOp
ALUSrcB
ALUSrcA
RegWrite
RegDst
Instruction [25-0]
26
Shift
left 2
28
PC [31–28]
Jump
address
[31–0]
PC
Address
Memory
MemData
Write
data
Instruction
[31–26]
Instruction
[25–21]
Instruction
[20–16]
Instruction
[15–0]
Instruction
register
Instruction
[15–0]
Instruction
[15–11]
Read
register 1
Read
register 2
Registers
Write
register
Write
data
Read
data 1
Read
data 2
A
B
4
Zero
ALU
ALU
result
ALUOut
Memory
data
register
16
Sign
extend
32
Shift
left 2
ALU
control
Instruction [5–0]

Figure-3

L-3/T-1/CSE

Date : 27/07/2013

BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY, DHAKA

L-3/T-1 B. Sc. Engineering Examinations 2011-2012

Sub : **CSE 305** (Computer Architecture)

Full Marks : 210 Time : 3 Hours

The figures in the margin indicate full marks.

USE SEPARATE SCRIPTS FOR EACH SECTION

SECTION – A

There are **FOUR** questions in this Section. Answer any **THREE**.

1. (a) What are the components of a computer? Mention the task of each of these components. **(7.5)**

   (b) Briefly describe ISA classes with examples and block diagrams. **(10)**

   (c) Suppose we have two implementations of the same instruction set architecture Computer A has a clock cycle time of 250 ps and a CPI of 2.0 for some program, and computer B has a clock cycle time of 500 ps and a CPI of 1.2 for the same program. Which computer is faster for this program and by how much? (Show all steps of calculations.) **(7)**

   (d) Suppose a program runs in 10 seconds and the program spends 50% of its time executing floating point instructions. We improve the floating point unit by a factor of five. How big is the speedup? **(6)**

   (e) What are the problems with measuring performance in terms of MIPS (million instructions per second)? **(4.5)**

2. (a) What are the MIPS design principles? Mention one use of each of these design principles in MIPS ISA. **(4+4)**

   (b) Which instructions and registers are used in procedure call in MIPS hardware? What are the purpose of using these registers and instructions? **(7.5)**

   (c) If branch target is too far to encode with 16-bit offset, how does the assembler rewrite the following code: BEQ $s0, $s1, L1? **(3.5)**

   (d) Describe MIPS addressing modes. **(10)**

   (e) Give three examples of complexity of IA-32. **(6)**

3. (a) Consider the following set of instructions: ADD, SW, JUMP. Draw the single cycle datapath and control that can execute the above set of instructions. Minimize the number of hardware used as much as possible, i.e., there should be no redundant hardware in your design. (Note that explanation is not required.) **(15)**

   (b) Write the purpose of using ALU unit for R-type, load/store, and branch instructions. **(6)**

   (c) Briefly describe the properties of hard-wired and microprogrammed control unit design. **(6)**

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Contd ... Q. No. 3

(d) Consider the following MIPS instructions: **(8)**

(i) LW $6, 36($1)

(ii) ADD $5, $5, $5

What do these instructions perform in EX and MEM stages. Assume that the pipelined datapath has 5 stages: IF (Instruction Fetch), ID (Instruction decode and register file read), EX (Execution op address calculation), MEM (Data memory access), and WB (Write Back).

IF/ID

4. (a) What are the values stored in IF/D and ID/EX pipeline registers? **(6)**

(b) What is a pipeline hazard? What are the different types of pipeline hazards? **(2+6)**

(c) Give an example of double data hazard. **(3)**

(d) Consider the following sequence of instructions: **(4)**

LW $1, 40($6)

ADD $6, $2, $2

SW $6, 50($1)

Eliminate

Assume that there is no forwarding in this pipelined processor. Estimate data hazards with "nop" instruction.

(e) Consider the following repeating pattern of branch outcome: T, T, NT, T. What is the accuracy of the two-bit predictor for this sequence of branch outcomes? What is the accuracy of the two-bit predictor in steady state if this pattern is repeated forever? Assume that the 2-bit predictor starts off in the bottom left state (predict not taken) of the figure given below. **(7)**

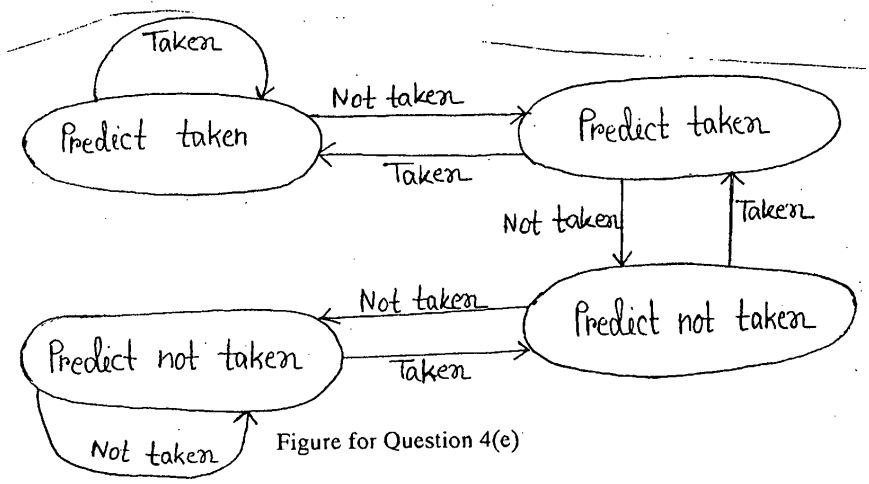

Figure for Question 4(e)

(f) Why does the MIPS implementation use EPC and Cause registers for processing an exception? What is an imprecise exception? **(4+3)**

Contd P/3

CSE 305

SECTION – B

There are **FOUR** questions in this Section. Answer any **THREE**.

5. (a) Draw the flow diagram of floating point addition. Also write down the condition of overflow or underflow during a floating point addition. **(8+2)**

   (b) What are the 'direct mapped', 'set associative', and 'fully associative' cache schemes? **(6)**

   (c) Assume there are three small coaches, each consisting of 4 one-word blocks. One each is fully associative, another one is 2-way set associative, and the third one is direct mapped. Find the number of misses for each cache organization given the following sequence of block addresses: 0, 4, 0, 2, 6, 8. **(15)**

   (d) What is a 'spit cache'? How is it different from the multilevel cache system? **(2+2)**

   Split

6. (a) Draw diagrams of the first and refined versions of the multiplication hardware. Discuss the improvement of the refined version over the first version. **(5+5+5)**

   (b) Assume the miss rate of an instruction cache is 2% and the miss rate of a data cache is 4%. If a processor has a CPI of 6 without any memory stalls, determine how much faster a processor would run with a perfect cache that never misses. Assume a main memory access time of 100 ns (including all the miss handling) and the processor clock rate is 4 GHz. **(10)**

   (c) Write down the steps to handle a cache miss. **(5)**

   (d) Discuss the components of disk data access time. **(5)**

7. (a) (i) What do you understand by the 'virtual memory' scheme? **(3)**

   (ii) Explain the purpose of a 'page table' and a 'page table register' in this scheme. **(4+2)**

   (iii) Draw the mapping from a 32-bit virtual address to a 30-bit physical address using a page table. **(6)**

   (iv) With a 32-bit virtual address, 4 kB pages and 4 bytes per page table entry, compute the total size of a page table. **(5)**

   (b) Draw the state diagram of a simple cache controller. **(10)**

   (c) What are the 'synchronous' and the 'asynchronous' bus system? **(5)**

8. (a) Assuming a cache of 16k blocks, a 4-word block size and a 32 bit address, find the total number of tag bits for a 4-way set associative cache. Also find the total size of the cache. [byte offset = 2 bits, 1 word = 32 bits, and $1k = 2^{10}$]. **(10)**

   (b) Briefly describe the 'shared memory multiprocessor' and the 'message passing multiprocessor' systems. **(6+6)**

Contd P/4

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Contd ... Q. No. 8

(c) Suppose a single shared memory processor has 20 GB of main memory. Five clustered computers occupy 4 GB each and the OS occupies 2 GB. How much more space is there for users with shared memory? **(8)**

(d) What are processor memory bus and back-plane bus? **(5)**
