Nandini Singhal

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Work Experience

July 2018 - Current

Software Engineer @ Microsoft R&D, Bangalore | Full-Stack Developer

- Developed a one-stop Partner app in a 2-member team for Microsoft Partners using React Native for android and iOS. Was involved in writing several API's for app functionalities like OCR recognition, raising support tickets, viewing events, blogs, developing partner competencies and many more.
- Currently working on Partner finder search using Azure search which handles a million requests every day. Developing the entire backend for partner referrals workflow and working on deploying services and webjobs on Azure.
- Also developed monitoring dashboards to monitor requests, failures, latencies for every API and dependencies, across datacenters and deployment environments.
- **Winner of the PACE-IDC Hackathon**: Project on using actionable messages which can authenticate and authorize users to perform actions on an external platform (like approve expenses) directly from within email / chat.

April 2018 - July 2018

Intern @ IST Austria | Prof. Dan Alistarh

Project: "Memory Tagging for Reducing Synchronization in Concurrent Data Structures"

- Implemented several data structures showing that tagging can enable fast, scalable, and arguably simple concurrent data structure designs, such as lists, binary search trees, balanced search trees, and range queries.
- New hardware operations were implemented by simulation over MIT Graphite and applications were developed to test these hardware operations to improve performance.

Jan 2018 - April 2018

Intern @ MPI-SWS, Germany | Prof. Viktor Vafeiadis

Project: "Verifying Concurrent Queue Algorithms under Weak Memory Model."

- Understood various memory models at the Software (Release-Acquire and Relaxed Memory Models) and Hardware (ARM, x86, POWER) level.
- Formally verified Herlihy-Wing Queue, Elimination Queue under WMM.

March 2017 - July 2017

Polly Labs (LLVM Compiler) | Dr. Michael Kruse, Inria & Dr. Tobias Grosser, ETH Zurich

Project: "Finer Statement Granularity in Polly for better Optimizability" (Patches)

- Creating polyhedral statements that contain only a subset of the instructions in a basic block. This allows loop distribution, without introducing excessive scalar dependences.
- Proposed a heuristic for efficient splitting of basic blocks into polyhedral SCoP statements.
- Performing experiments on various benchmarks like SPEC CPU 2006, LLVM test-suite to understand the impact of having finer granularity of statements.

Jan 2017 - *Dec 2017*

Research Assistantship at IITH | funded by 'Board of Research in Nuclear Sciences' (BRNS)

Project: "An Efficient Software Framework for High Performance Computing Systems"

- Development of Software Transactional Memory (STM) Library consisting of multiple version algorithms which enable concurrent threads to execute seamlessly (without using locks).
- Testing of these libraries on highly concurrent benchmarks like STAMP and Synchrobench.
- Tools and Languages Used: C++, Pthreads, OpenMP, Intel Parallel Studio XE

Jan 2015 - *Dec 2016*

Research Assistantship at IITH | funded by 'ANURAG, DRDO Lab'

Project: "An Efficient Middleware for Multi-Core Systems using Software Transactional Memory Systems"

- Development of STM Library consisting of single version algorithms like (BTO, SGT, MVTO) which enable concurrent threads to execute seamlessly.

July 2016

Summer Intern at Samsung Research & Development Institute Delhi

- Developed command line programs to reset any USB device in Linux. Understanding of Linux USB stack & Wrote a simple Linux USB Device driver.
- Deployed a Tizen TV video application for Indian Channel Serial using Youtube API.

June 2013- June 2014

Internship at Indian Institute of Technology Bombay (IITB) | Guide: Prof. Uday Khedker

- Integrated Priority and Temporal view with the existing Logical view in FreeMind, an open source Mind-Mapping tool making it user friendly.
- Languages Used: Java, HTML, CSS

Education

December 2017	M.Tech. in Computer Science & Engineering **Indian Institute of Technology Hyderabad** Thesis: "Exploiting Concurrency in Graph Algorithms" | Advisor: Prof. Sathya Peri	GPA: 9.81/10 Institute Silver Medal
June 2014	Bachelor in Engineering (B.E.) in Computer Science & Engineering **College of Engineering Manjari, University of Pune** Thesis: "Integrating various views in Mind Mapping Tool" | Advisor: Prof. Uday Khedker, Indian Institute of Technology Bombay	Percentage: 74 Institute Topper (Univ. Top 10)

Achievements

- 2019 Winner of the Microsoft PACE-IDC Hackathon 2019 held over the duration of 3 days.
- 2018 Awarded Institute Silver Medal for highest CGPA of graduating batch 2018.
- 2016 Awarded complete travel grant to attend LLVM Developer's Meeting in San Jose and IPDPS in Chicago.
- 2015 was Awarded a prize by IIT Hyderabad for Academic Performance as a part of IIT Hyderabad Excellence Awards for the academic year 2015-16.
- 2014 'Gaurav Chinh' Award by Pune District Education Association for Academic Performance in B.E.
- 2014 98.9 Percentile in GATE 2014.
- 2013 Top 2% score in the 10^{th} National IT Aptitude Test by NIIT.
- 2013 Secured 1^{st} Position in 'Blind Coding' in Serendipity organized by PDEA's COEM.
- 2009 Awarded 2^{nd} Best Entry Award and won a cash prize of Rs 15000/- in National Essay Competition organized by Oil India Limited.
- 2009 Awarded 3^{rd} Position in the 17^{th} All India Essay Competition conducted by NAVA & Grihini.
- 2008 Awarded 'The Late Tehmie Irani Prize' in Secondary Examination by ICSE Board.

Publications

Submitted	"**Memory Tagging: Minimalistic Synchronization for Scalable Search Data Structures**", guided by Prof. Dan Alistarh.
Published	"**A Pragmatic Non-blocking Concurrent Directed Acyclic Graph**", guided by Prof. Sathya Peri; in Proc. of the 7^{th} International Conference on Networked Systems (NETYS), 2019. (link)
Published	"**A Simple and Practical Concurrent Non-blocking Unbounded Graph with Reachability Queries**", guided by Prof. Sathya Peri; in Proc. of the 20^{th} International Conference on Distributed Computing and Networking (ICDCN), 2019. (link)
Published	"**Practical Multi-threaded Graph Coloring Algorithms for Shared Memory Architecture**", guided by Prof. Sathya Peri & Prof. Subrahmanyam Kalyanasundaram; in Proc. of the 18^{th} International Conference on Distributed Computing and Networking (ICDCN), 2017. (link)

Posters

"**Dynamic Acyclicity of Concurrent Graph Objects**" as a Poster in EuroSys Doctoral Workshop 2017. (pdf)

"**Reducing the Computational Complexity of RegionInfo Pass in LLVM**" as a Poster & Lightning talk in 10^{th} US LLVM Developer's Meeting, San Jose 2016. (Video | pdf)

"**Multi-threaded Graph Coloring Algorithms for Shared Memory Architecture**" in Research Colloquia of Xerox Research Centre India (XRCI) Open 2016 and PhD Forum of IPDPS 2016.