CMP SCI 635: Modern Computer Architecture

Memory Errors in Modern Systems

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Date: 24th Sept, 2019

Paper: 6 – Memory [Sridharan15]

Strengths:

1. The conclusions of this research are applicable to super-computer centres, any kind of large data centre and compute clusters. Which makes this practical as this kind of industries will actually face these issues by 2020, giving them a buffer to ensure that the current systems are ready for the increase in hardware scale.

2. Points to the Fault versus Error rate fallacy, which might ensure that fault rate proves itself as a more useful metric when we are thinking about hardware resiliency. Gives reason about why the fault leading to an error doesn't mean that error entirely depends on a particular hardware fault only.

Weaknesses:

1. Doesn't mention the case where the 2 DRAMs of a rank which are used for storage of check bits fail. How does that gets detected and corrected?

2. It is not specified how the SRAM faults are related to faults in smaller structures like TLB, L2 cache and L3 cache. How does cache bit flips matter in case of SRAM? Is it when the cache write-backs are performed and the wrong data/ flipped bits are written as is? Then it's more of a fault in caches and SRAM drivers only have to detect and correct the flips.

Questions/Assertions:

1. For the particle strikes in SRAM, where does the alpha particle originate from? Is that the same phenomena we had discussed in the "Wearout Lecture" where the decrease in size of transistors make positive charges pushed so far apart that they do not come back and the electron flow gets disrupted? Does this change the memory bit states?

2. How does this particle strike affect DRAM? The charge is going to go down during every refreshed cycle anyway. Does that make any difference if some alpha particles are exciting the electrons?

3. Shouldn't the "Intermittent Faults" be grouped with "Transient Faults" as the observation of their occurrences aren't time-bound or definite? While, anything that's behaving in same manner at every test fault generated will be the "Permanent or Hard Faults".

4. "*[For Cielo, this includes 12 months of data from July 2011 to November 2012.] …in the case of both systems, time periods where the system was not in a consistent state or was in a transition state were excluded.*" What does system being in "transition state" means?

5. How does the rate of permanent faults can decrease? Doesn't it only stay constant or increases?

6. Is only talking about fault rate helpful? Even if a hardware has as low as 1 FIT fault rate, it could be generating thousands of errors, it all comes down to which component has failed, in that case, the severity of the fault can only be known by the error rate. Sure, faults show hardware resilience in better way, but it will only be noticeable and worth the effort if the fault is actually a big one and generating thousands of errors.