CMP SCI 635: Modern Computer Architecture

Characterizing Flash Memory: Anomalies, Observations, and Applications

Name: Kunjal Panchal Date: 31th Oct, 2019 Student ID: 32126469

Paper: 15 – Secondary Storage [Grupp09]

Strengths:

1. Although it is possible for storage systems to directly access raw flash, the storage system must be aware of the complexities involved in doing so, in particular, the inability to update data in place. Using an FTL allows file systems and SSDs to maintain the block interface of disks without sacrificing the tighter integration and control over how the flash is managed.

2. One basic hardware characteristics of flash memory is that it has an erase-before-write architecture. That is, to update a location in flash memory, the location must first be erased before new data can be written to it. The memory portion for erasing differs in size from that for reading or writing, resulting in the major performance degradation of the overall flash memory system. FTL successfully deals with this.

Weaknesses:

1. Virtualizing flash as a new layer below the file system introduces inefficiency because the FTL block interface does not allow for the communication of file system block de-allocations. Delaying block de-allocations results in copying out more data during cleaning and wear levelling than is necessary.

2. For FTLs, the inability to overwrite in place, together with the granularity of erase, often necessitates the copy out of live data pages from an erase block before it can be reused.

Questions/Assertions:

1. Static wear levelling in flash drives keeps the cold data moving around to distribute the wear-out effect equally. And is used on all flash controllers for a long time. But in general, keeping static data on flash drives is not a good idea. Flash drives have terrible data retention. Theoretically, if you write to it a lot, older data will get shifted around. Is there any true fix for this problem? Can TLC be used here?

2. Why there are not many consumer SLC drives for quite a while now?

3. Even if I didn't use the device, would it eventually lose charge and the data would be lost, in case of flash drives? Just about after 10 years too?

4. As the feature size of flash memory cells reaches the minimum limit, further flash density increases are driven by greater levels of MLC, possibly 3-D stacking of transistors, and improvements to the manufacturing process. The decrease in endurance and increase in incorrectable bit error rates that accompany feature size shrinking can be compensated by improved error correction mechanisms.

5. Flash memories have been demonstrated to be a reliable and flexible integrated circuit to be used in many new applications that could be covered neither by EEPROM's, because of their low density and high cost, nor by EPROM's, which do not support in-system reprogramming.