

**ILLINOIS INSTITUTE OF TECHNOLOGY
ECE429-V03**

Project Report

**CASE STUDY OF THE 32-BIT PIPELINED CPU
DESIGN WITH NEW ALU ARCHITECTURE**

Report

by

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INTRODUCTION

ASIC design flow encompasses design conception, chip optimization, logical/physical implementation, design validation and verification, and design validation and verification. The functionality of the logic defined in VHDL/Verilog code as RTL (register-transfer-level) is logically synthesized into a gate-level netlist that only incorporates interlinked standard cells in the basic cell-based ASIC design cycle. In this project, we are producing the RTL description of the 32-bit pipelined processor and use the Synopsys Design Compiler logic synthesis tool to execute logical synthesis. We are also executing all the same process for the test bench which will have other commands too from the new test bench “tb_test.v”.

This project's 32-bit pipelined processor handles data with a word length of 32 bits and may execute several instructions at the same time. Externally controlled signals include the clock signal, instruction signals for addressing the memory file, choosing the Arithmetic Logic Unit (ALU) operands, and describing the ALU action. As a result, the major goal of this project is to learn how a pipelined CPU works and to verify that the aforementioned external signals are synchronized over the crucial delay route of the circuit, which will be used to establish the processor's minimum running duration.

THEORY

1. Carry Ripple Adder(CRA)

The CRA is built by cascading n-bit full adders. The carry of the process is rippled through the design. i.e. the carry is passed to the next adder in chain and this is carried on continuously for the rest of the adders until the adding operation or the number of bits is complete. The block diagram for CRA is given in *figure1*.

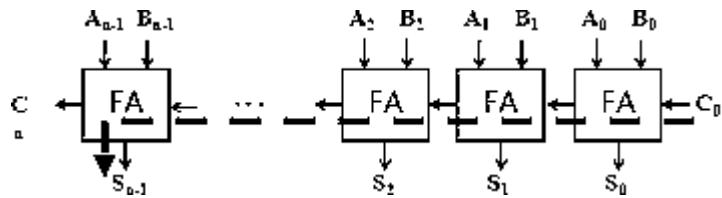


Figure 1 Block diagram of Carry Ripple Adder

2. Carry Lookahead Adder(CLA)

The ripple carry design is transformed into the carry Lookahead design by reducing the carry logic across predetermined groups of bits of the adder to two-level logic. The principle of producing and propagating carries is the foundation of a carry look-ahead adder. When both operands to be added are '1', a carry is formed, and it will propagate if and only if one of the operands is '1'. Figure 2 shows the block diagram and formulae for computing the carry bits.

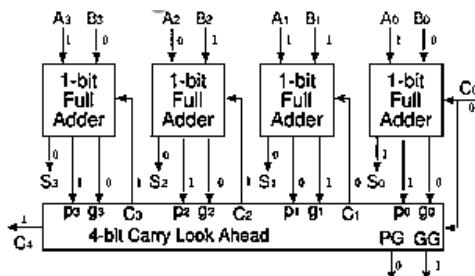


Figure 2 Block diagram of the Carry Lookahead adder

3. Carry Skip Adder(CSA)

In the Carry Skip Adder, the operands are divided into blocks of r bits blocks. Within each block, a ripple carry adder can be utilized to produce the sum bits and a carryout bit for the block. Each group generates “Group Carry-Propagate” =1 if all $p_i=1$ in each group. Its block diagram is given in figure 3.

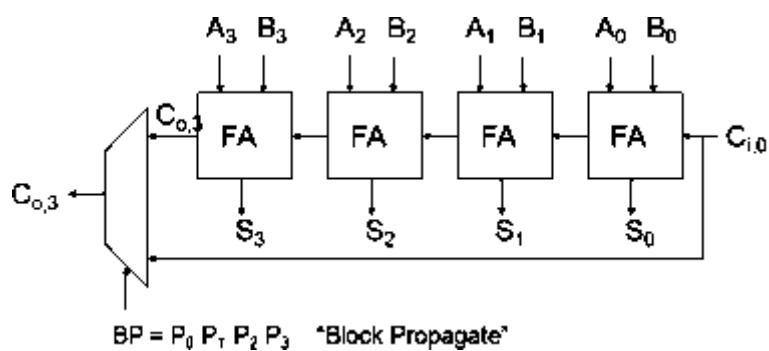


Figure 3 Block diagram of the Carry Skip Adder

4. Carry Select Adder (CSeA)

The CSeA adds two n-bit values together to get the (n+1)-bit total. Ripple carry adders and multiplexers are used to construct it. Like the Carry Skip Adder, the Carry Select Adder separates the operands to be added into r bit blocks. The block diagram is shown in figure 4.

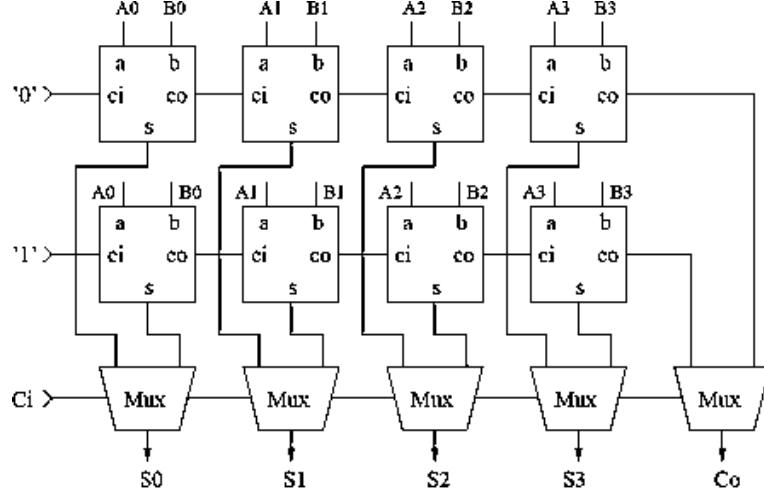


Figure 4 Block diagram of the Carry Select Adder

5. Structure of the 4-bit comparator

The Structure of the 4-bit comparator is given in figure

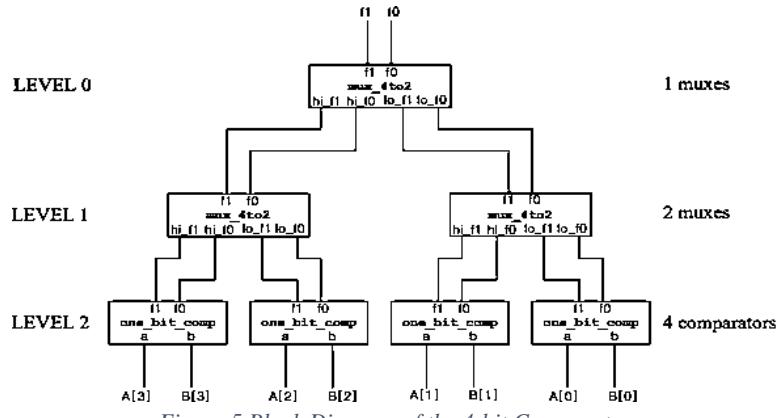


Figure 5 Block Diagram of the 4-bit Comparator

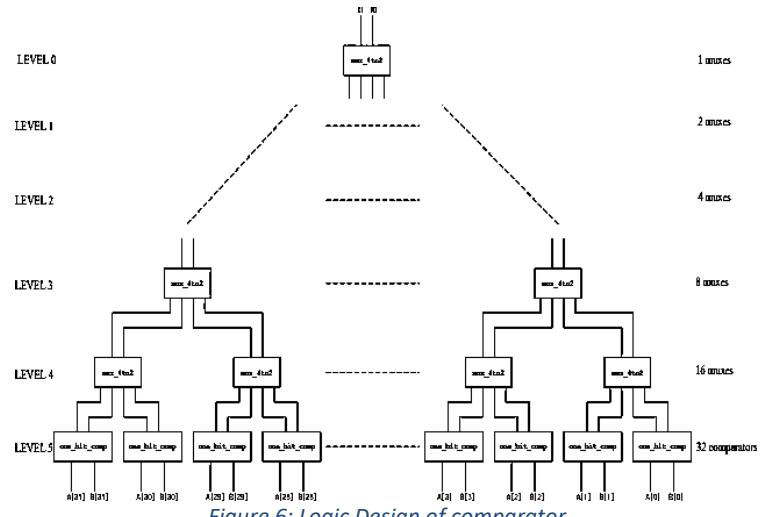


Figure 6: Logic Design of comparator

IMPLEMENTATIONS AND RESULT

1. Carry Ripple Adder (CRA)

```
Loading native compiled code: ..... Done
Design hierarchy summary:
      Instances  Unique
Modules:       6569    30
Primitives:    7351     6
Registers:    2166    14
Scalar wires: 3536     -
Expanded wires: 1198    41
Vectored wires: 6     -
Always blocks: 2156    4
Initial blocks: 3     3
Cont. assignments: 1     6
Pseudo assignments: 43    43
Writing initial simulation snapshot: worklib.stimulus:v
loading snapshot worklib.stimulus:v ..... Done
celium> source /apps/cadence/XCELIUM1803/tools/xcelium/files/xmsimrc
celium> run
msim: *W,SHMPOPT: Some objects excluded from $shm_probe due to optimizations.
      File: ./tb_cpu.v, line = 28, pos = 11
      Scope: stimulus
      Time: 0 FS + 0

imulation complete via $finish(1) at time 501 NS + 0
/tb_cpu.v:30    #1 $finish;
```

Figure a : RTL Simulation for CRA

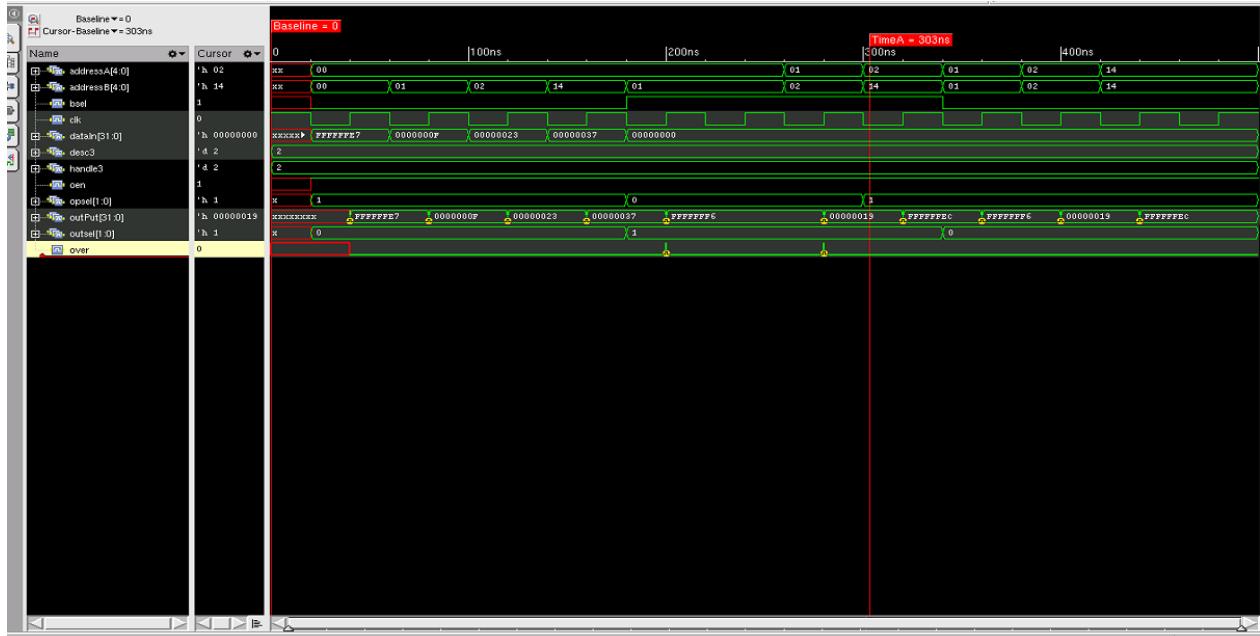


Figure b : Simvision Result for CRA

```

Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
          Instances   Unique
Modules:        14411      34
UDPs:           1628       4
Primitives:     25293      6
Timing outputs: 14411      19
Registers:      1638       18
Scalar wires:   16269      -
Expanded wires: 46          5
Always blocks:  1           1
Initial blocks: 3           3
Pseudo assignments: 9          9
Timing checks:  9769      1625
Simulation timescale: 10ps

Writing initial simulation snapshot: worklib.AOI21X1:v
Loading snapshot worklib.AOI21X1:v ..... Done
xcelium> source /apps/cadence/XCELIUM1803/tools/xcelium/files/xmsimrc
xcelium> run
Simulation complete via $finish(1) at time 501 NS + 0
./tb_cpu.v:30  #1 $finish;
xcelium> exit
asrinival@saturn.ece.iit.edu:~%

```

Figure c: Logic Synthesis of CRA

```

Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
          Instances   Unique
Modules:        14486      34
UDPs:           1628       4
Primitives:     25368      6
Timing outputs: 14486      19
Registers:      1638       18
Scalar wires:   16344      -
Expanded wires: 46          5
Always blocks:  1           1
Initial blocks: 3           3
Pseudo assignments: 9          9
Timing checks:  9769      1625
Simulation timescale: 10ps

Writing initial simulation snapshot: worklib.AOI21X1:v
oading snapshot worklib.AOI21X1:v ..... Done
celium> source /apps/cadence/XCELIUM1803/tools/xcelium/files/xmsimrc
celium> run
imulation complete via $finish(1) at time 501 NS + 0
/tb_cpu.v:30  #1 $finish;
celium> exit
srinival@saturn.ece.iit.edu:~%

```

Figure d: Place and Route

```

-----[redacted]-----
report_power consumed time (real time) 00:00:00 : peak memory (603M)
1
encounter >> reportGateCount -limit 0
Gate area 2.8158 um^2
[0] cpu Gates=15759 Cells=14477 Area=44375.6 um^2
encounter >> [redacted]

```

Figure e: Gate count from Encounter

```

Total Power
-----
Total Internal Power: 2.581 53.87%
Total Switching Power: 1.947 40.64%
Total Leakage Power: 0.2628 5.486%
Total Power: 4.791

report_power consumed time (real time) 00:00:03 : peak mem
Output file is power_final
*****
* Encounter script finished      *
* Results:                      *
* -----                         *
* Layout: final.gds2            *
* Netlist: final.v              *
* Timing: timing.rep.5.final   *
* Area: area.final              *
* Power: power.final            *
*                               *
* Type 'win' to get the Main Window *
* or type 'exit' to quit          *
*                               *
*****encounter 1> reportGateCount -limit 0
Gate area 2.8158 um^2
[0] cpu Gates=15749 Cells=14466 Area=44346.5 um^2
encounter 2> ■

```

Figure f: Encounter report of CRA

```

xterm
-----
Total Internal Power: 2.581 53.87%
Total Switching Power: 1.947 40.64%
Total Leakage Power: 0.2628 5.486%
Total Power: 4.791

Group           Internal   Switching   Leakage   Total   Percentage
Power          Power       Power       Power    Power (%) 
-----
Sequential      1.207     0.1075    0.08928   1.404   29.3
Macro          0          0          0          0          0
IO              0          0          0          0          0
Combinational   1.32      1.246     0.1716    2.738   57.14
Clock (Combinational) 0.05438  0.5932    0.001874  0.6495  13.56
Clock (Sequential) 0          0          0          0          0
Total          2.581     1.947     0.2628    4.791   100

Rail           Voltage   Internal   Switching   Leakage   Total   Percentage
                   Power       Power       Power    Power (%) 
-----
vdd             1.1        2.581     1.947     0.2628   4.791   100

Clock           Internal   Switching   Leakage   Total   Percentage
                   Power       Power       Power    Power (%) 
-----
clk             0.05438   0.5932    0.001874  0.6495  13.56
Total          0.05438   0.5932    0.001874  0.6495  13.56

-----
* Power Distribution Summary:
*   Highest Average Power: clk_14_I32 (INVX8): 0.009632
*   Highest Leakage Power: mb/ram/mer2/11/me31/qout_reg (DFFPOSX1): 5.498e-05
*   Total Cap: 1.80592e-10 F
*   Total instances in design: 14466
*   Total instances in design with no power: 0
*   Total instances in design with no activity: 0
*
*   Total Fillers and Decap: 0

report_power consumed time (real time) 00:00:00 : peak memory (567M)
1
encounter 3> ■

```

Figure g: Power Report

timing.rep (~/Desktop/Project/CRA) - gedit

File Edit View Search Tools Documents Help

New Open Save Print... Undo Redo Cut Copy Paste Find Replace

cpu_CRA.v x encounter.conf x timing.rep.5.final x timing.rep x

```

a/l3/f247/U2/Y (XNOR2X1)          0.00      3.71 r
a/l3/f247/U2/Y (XOR2X1)           0.07      5.78 r
a/l3/f256/U5/Y (XNOR2X1)          0.06      5.84 r
a/l3/f256/U2/Y (XOR2X1)           0.07      5.91 r
a/l3/f265/U5/Y (XNOR2X1)          0.06      5.97 r
a/l3/f265/U2/Y (XOR2X1)           0.07      6.04 r
a/l3/f274/U5/Y (XNOR2X1)          0.06      6.11 r
a/l3/f274/U2/Y (XOR2X1)           0.07      6.18 r
a/l3/f283/U5/Y (XNOR2X1)          0.06      6.24 r
a/l3/f283/U2/Y (XOR2X1)           0.07      6.31 r
a/l3/f292/U5/Y (XNOR2X1)          0.06      6.37 r
a/l3/f292/U2/Y (XOR2X1)           0.07      6.44 r
a/l3/h301/U2/Y (XOR2X1)           0.04      6.48 f
a/U26/Y (AOI22X1)                 0.03      6.52 r
U220/Y (BUFX2)                   0.04      6.56 r
U65/Y (AND2X1)                   0.07      6.62 r
U1794/Y (INVX1)                  0.10      6.73 f
mb/ram/mer12/m0/m31/U3/Y (AOI22X1) 0.05      6.78 r
U3794/Y (INVX1)                  0.02      6.80 f
mb/ram/mer12/ll/me31/qout_reg/D (DFFP0SX1) 0.00      6.80 f
data arrival time                6.80

clock clk (rise edge)            33.00     33.00
clock network delay (ideal)      0.00      33.00
mb/ram/mer12/ll/me31/qout_reg/CLK (DFFP0SX1) 0.00      33.00 r
library setup time               -0.06     32.94
data required time               32.94
-----  

data required time               32.94
data arrival time                -6.80
-----  

slack (MET)                      26.14

```

1

Ln 1, Col 1 INS

Figure h: Timing Report

timing.rep.5.final (~/Desktop/Project/CRA) - gedit

File Edit View Search Tools Documents Help

New Open Save Print... Undo Redo Cut Copy Paste Find Replace

cpu_CRA.v x encounter.conf x timing.rep.5.final x

```

#####
# Generated by: Cadence Encounter 10.13-s292_1
# OS: Linux x86_64(Host ID saturn.ece.iit.edu)
# Generated on: Sat Dec 4 16:20:25 2021
# Design: cpu
# Command: report_timing -nworst 10 -net > timing.rep.5.final
#####
Path 1: MET Setup Check with Pin mb/ram/mer15/ll/me30/qout_reg/CLK
Endpoint: mb/ram/mer15/ll/me30/qout_reg/D (^) checked with leading edge of
'clk'
Beginpoint: m0pd/bb/me2/qout_reg/Q          (v) triggered by leading edge of
'clk'
Other End Arrival Time      0.352
- Setup                      4.953
+ Phase Shift                33.000
= Required Time              28.398
- Arrival Time               10.940
= Slack Time                 17.458
    Clock Rise Edge          0.000
    + Clock Network Latency (Prop) 0.363
    = Beginpoint Arrival Time  0.363

-----
+
|             Pin          | Edge | Net       | Cell   | Delay | Arrival
| Required |          |       |          |        |        | Time
| Time   |          |       |          |        |        |
|       |          +---+---+---+---+---+---+
+-----+
| m0pd/bb/me2/qout_reg/CLK | ^  | clk_L4_N58 |        |        | 0.363
| 17.821 |          | v  | B[2]      | DFFP0SX1 | 0.244 | 0.607
| m0pd/bb/me2/qout_reg/Q  | v  | B[2]      | AND2X1  | 0.101 | 0.708
| 18.065 |          |       |          |        |        |
|       |          +---+---+---+---+---+---+

```

Ln 1, Col 1 INS

Figure i: Timing.final for CRA

```

#####
# Generated by: Cadence Encounter 10.13-s292_1
# OS: Linux x86_64(Host ID saturn.ece.iit.edu)
# Generated on: Sat Dec 4 20:08:30 2021
# Design: cpu
# Command: report_timing -nworst 10 -net > timing.rep.5.final
#####
Path 1: MET Setup Check with Pin mb/ram/mer11/ll/me31/qout_reg/CLK
Endpoint: mb/ram/mer11/ll/me31/qout_reg/D (^) checked with leading edge of
'clk'
Beginpoint: m0pd/bb/mel/qout_reg/Q (v) triggered by leading edge of
'clk'
Other End Arrival Time 0.333
- Setup 4.161
+ Phase Shift 17.000
= Required Time 13.172
- Arrival Time 11.147
= Slack Time 2.025
    Clock Rise Edge 0.000
    + Clock Network Latency (Prop) 0.288
    = Beginpoint Arrival Time 0.288

-----
+
| Required | Pin | Edge | Net | Cell | Delay | Arrival
| Time | | | | | | |
+-----+
| 2.313 | m0pd/bb/mel/qout_reg/CLK | ^ | clk_L4_N0 | | | 0.288
| 2.563 | m0pd/bb/mel/qout_reg/Q | v | B[1] | DFFPOSX1 | 0.250 | 0.538
| 2.653 | U1924/B | v | B[1] | AND2X1 | 0.089 | 0.628
| 2.653 | u1924/v | v | ~12/a1[1] | AND2X1 | 0.112 | 0.740

```

Figure j: Timing report for maximum frequency

```

xterm
      Instances Unique
Modules: 6569 30
Primitives: 7351 6
Registers: 2186 14
Scalar wires: 3536 -
Expanded wires: 1198 41
Vectorized wires: 6 -
Always blocks: 2156 4
Initial blocks: 3 3
Cont. assignments: 1 6
Pseudo assignments: 43 43
Writing initial simulation snapshot: worklib.stimulus;v
Loading snapshot worklib.stimulus;v ..... Done
xcelsim> source /apps/cadence/XCELUM1803/tools/xcelium/files/xmelsimrc
xcelsim> run
xmsim: *W,SHMPOPT: Some objects excluded from $shm_probe due to optimizations.
      File: ./tb_test.v, line = 29, pos = 11
      Scope: stimulus
      Time: 0 FS + 0
Simulation complete via $finish(1) at time 501 NS + 0
./tb_test.v:31 #1 $finish;
xcelsim> exit
asrinival@saturn.ece.iit.edu:"% "

```

Figure k: RTL for new test_bench

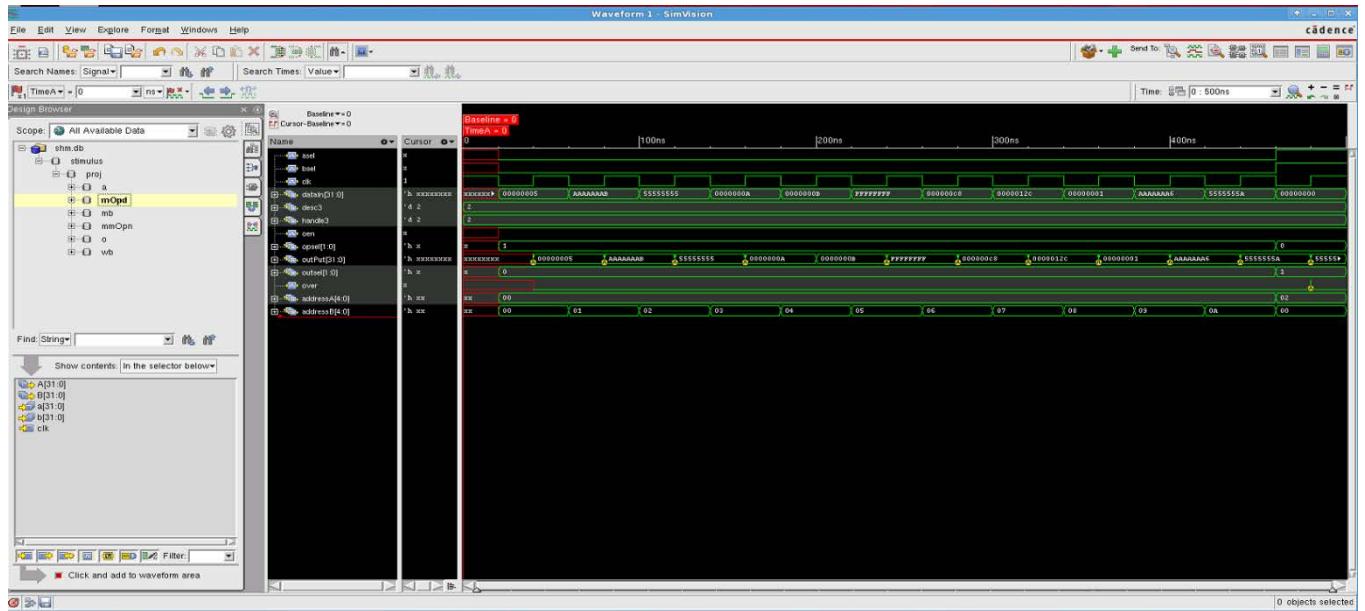


Figure 1: Simvision for tb_test

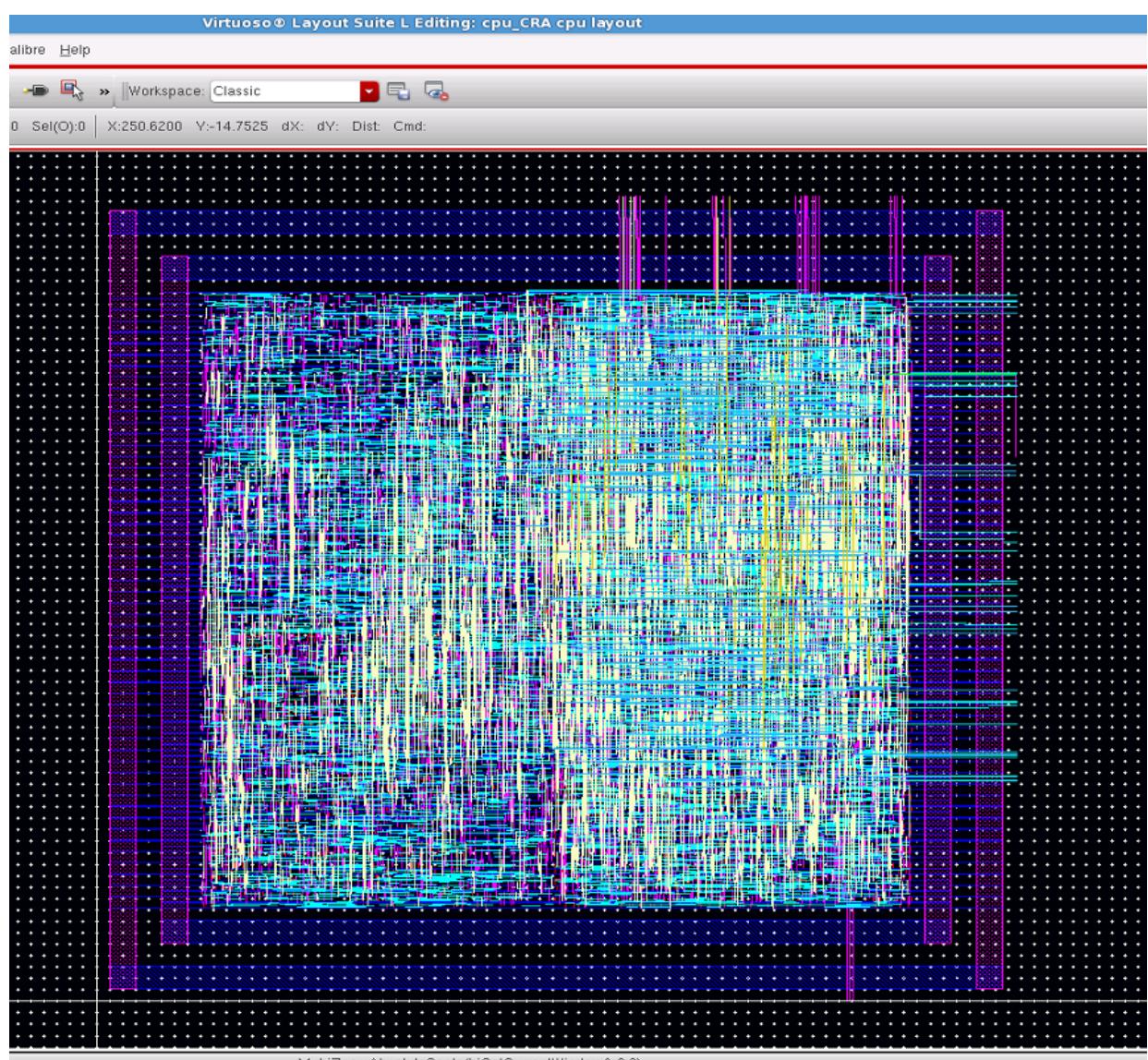


Figure m: Layout

cell.rep (~/Desktop/Project/CRA) - gedit

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New Open Save Print... Undo Redo Cut Copy Paste Find Replace

cell.rep x

o/tr/t4/b1	TBUFX2	gscl45nm	3.754400	"	
o/tr/t5/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t6/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t7/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t8/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t9/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t10/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t11/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t12/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t13/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t14/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t15/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t16/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t17/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t18/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t19/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t20/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t21/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t22/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t23/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t24/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t25/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t26/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t27/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t28/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t29/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t30/b1	TBUFX2	gscl45nm	3.754400	n	
o/tr/t31/b1	TBUFX2	gscl45nm	3.754400	n	
wb/bd/me0/qout_reg	DFFP0SX1	gscl45nm	7.978100	n	
wb/bd/me1/qout_reg	DFFP0SX1	gscl45nm	7.978100	n	
wb/bd/me2/qout_reg	DFFP0SX1	gscl45nm	7.978100	n	
wb/bd/me3/qout_reg	DFFP0SX1	gscl45nm	7.978100	n	
wb/bd/me4/qout_reg	DFFP0SX1	gscl45nm	7.978100	n	
Total 14382 cells			48598.829885		
1					

Ln 1, Col 1 INS

Figure n: Cell report for CRA

2. Carry Lookahead Adder (CLA)

```

WORKLIB.stimulus:v <0x19f0146c>
    streams: 13, words: 17668
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
      Instances Unique
Modules:       6607   33
Primitives:    7187    6
Registers:    2166   14
Scalar wires: 3692    -
Expanded wires: 1198   41
Vectored wires: 6    -
Always blocks: 2156   4
Initial blocks: 3    3
Cont. assignments: 11   15
Pseudo assignments: 43   43
Writing initial simulation snapshot: worklib.stimulus:v
Loading snapshot worklib.stimulus:v ..... Done
xcelium> source /apps/cadence/XCELIUM1803/tools/xcelium/files/xmsimrc
xcelium> run
xmsim: *W,SHMPOPT: Some objects excluded from $shm_probe due to optimizations.
      File: ./tb_cpu.v, line = 28, pos = 11
      Scope: stimulus
      Time: 0 FS + 0

Simulation complete via $finish(1) at time 501 NS + 0
./tb_cpu.v:30 #1 $finish;
xcelium> exit
asrinival@saturn.ece.iit.edu:~%

```

Figure o: RTL for CLA

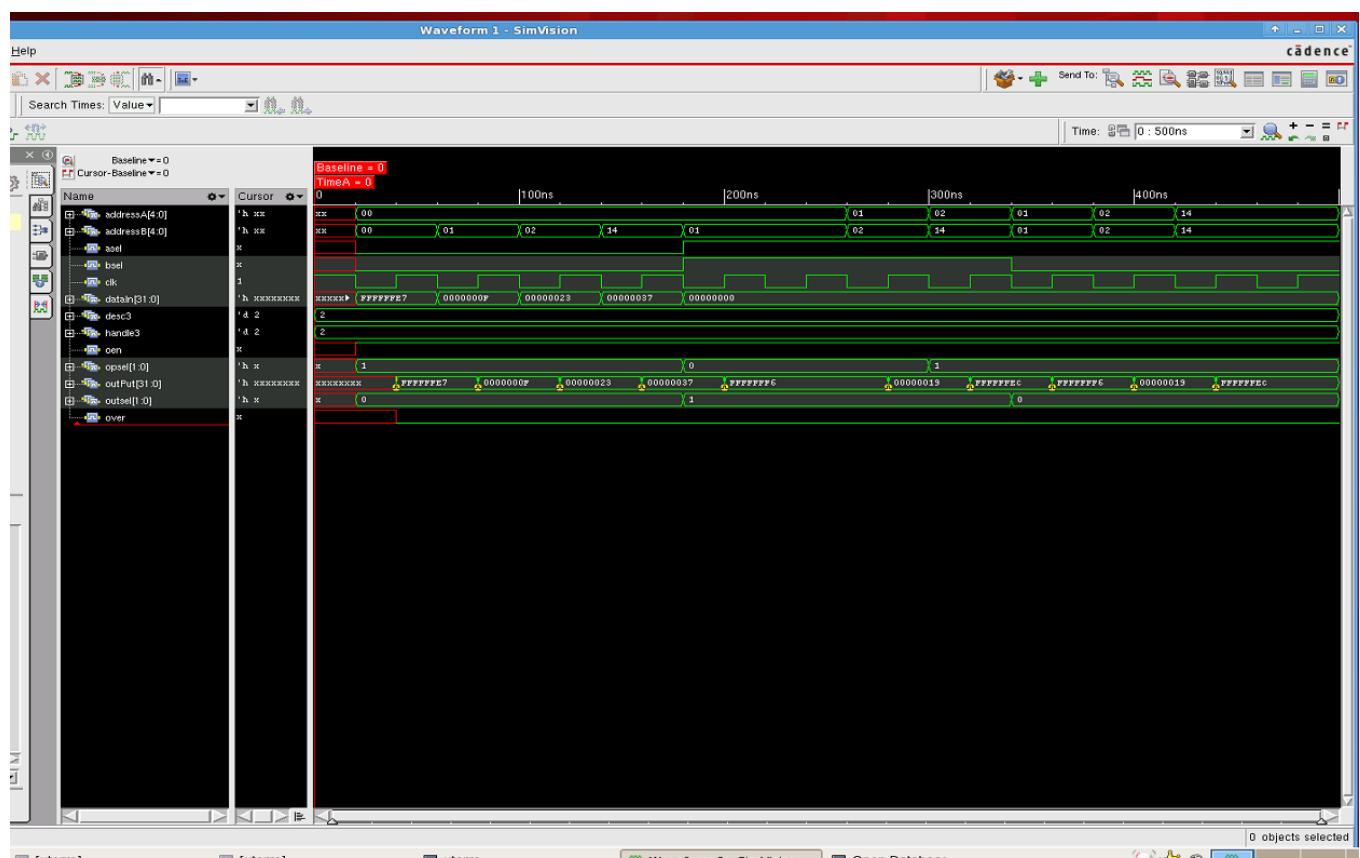


Figure p: Simvision output for tb_cpu

```

        streams: 0, words: 0
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
          Instances Unique
Modules:           14379   34
UDPs:             1628    4
Primitives:       25226    6
Timing outputs:  14379   19
Registers:        1638   18
Scalar wires:     16237   -
Expanded wires:    46     5
Always blocks:    1      1
Initial blocks:   3      3
Pseudo assignments: 9      9
Timing checks:    9769  1625
Simulation timescale: 10ps
Writing initial simulation snapshot: worklib.BUFX4:v
Loading snapshot worklib.BUFX4:v ..... Done
xcelium> source /apps/cadence/XCELIUM1803/tools/xcelium/files/xmsimrc
xcelium> run
Simulation complete via $finish(1) at time 501 NS + 0
./tb_cpu.v:30 #1 $finish;
xcelium> exit
asrinival@saturn.ece.iit.edu:~%

```

Figure q: Logic Synthesis

Total	0.05267	0.604	0.002096	0.6587
13.84				
<hr/>				
*	Power Distribution Summary:			
*	Highest Average Power:	clk_L4_I28 (INV8):		
*	0.009625			
*	Highest Leakage Power:	mb/ram/mer2/l1/me31/qout_reg (DFFPOSX1):		
*	5.490e-05			
*	Total Cap:	1.80425e-10 F		
*	Total instances in design:	14446		
*	Total instances in design with no power:	0		
*	Total instances in design with no activity:	0		
*	Total Fillers and Decap:	0		
<hr/>				

Figure r: encounter Power report

timing.rep (~/Desktop/Project/CLA) - gedit

The screenshot shows a Gedit window displaying a timing report named "timing.rep". The report lists various logic elements and their timing parameters. The columns represent setup time, hold time, and arrival time respectively. The report includes clock information and slack calculations.

a/l3/f2308/U2/Y (XOR2X1)	0.00	5.57	r
a/l3/f247/U5/Y (XNOR2X1)	0.07	5.64	r
a/l3/f247/U2/Y (XOR2X1)	0.06	5.71	r
a/l3/f256/U5/Y (XNOR2X1)	0.07	5.78	r
a/l3/f256/U2/Y (XOR2X1)	0.06	5.84	r
a/l3/f265/U5/Y (XNOR2X1)	0.07	5.91	r
a/l3/f265/U2/Y (XOR2X1)	0.06	5.97	r
a/l3/f274/U5/Y (XNOR2X1)	0.07	6.04	r
a/l3/f274/U2/Y (XOR2X1)	0.06	6.11	r
a/l3/f283/U5/Y (XNOR2X1)	0.07	6.18	r
a/l3/f283/U2/Y (XOR2X1)	0.06	6.24	r
a/l3/f292/U5/Y (XNOR2X1)	0.07	6.31	r
a/l3/f292/U2/Y (XOR2X1)	0.06	6.37	r
a/l3/h301/U2/Y (XOR2X1)	0.07	6.44	r
a/U26/Y (AOI22X1)	0.04	6.48	f
U219/Y (BUFX2)	0.03	6.52	r
U64/Y (AND2X1)	0.04	6.56	r
U1729/Y (INVX1)	0.07	6.62	r
mb/ram/mer12/m0/m31/U3/Y (AOI22X1)	0.10	6.73	f
mb/ram/mer12/ll/me31/qout_reg/D (DFFPOSX1)	0.05	6.78	r
data arrival time	0.02	6.80	f
	0.00	6.80	f
		6.80	
clock clk (rise edge)	33.00	33.00	
clock network delay (ideal)	0.00	33.00	
mb/ram/mer12/ll/me31/qout_reg/CLK (DFFPOSX1)	0.00	33.00	r
library setup time	-0.06	32.94	
data required time		32.94	

data required time		32.94	
data arrival time		-6.80	

slack (MET)		26.14	
1			

Figure s: Timing report

timing.rep.5.final (~/Desktop/Project/CLA) - gedit

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timing.rep.5.final x

```
#####
# Generated by: Cadence Encounter 10.13-s292_1
# OS: Linux x86_64(Host ID saturn.ece.iit.edu)
# Generated on: Sat Dec 4 18:00:47 2021
# Design: cpu
# Command: report_timing -nworst 10 -net > timing.rep.5.final
#####
Path 1: MET Setup Check with Pin mb/ram/mer30/ll/me31/qout_reg/CLK
Endpoint: mb/ram/mer30/ll/me31/qout_reg/D (^) checked with leading edge of
'clk'
Beginpoint: m0pd/bb/me1/qout_reg/Q (v) triggered by leading edge of
'clk'
Other End Arrival Time 0.344
- Setup 4.498
+ Phase Shift 33.000
= Required Time 28.846
- Arrival Time 10.925
= Slack Time 17.921
    Clock Rise Edge 0.000
    + Clock Network Latency (Prop) 0.333
    = Beginpoint Arrival Time 0.333

+-----+
+-----+-----+-----+-----+-----+
| Required | Pin | Edge | Net | Cell | 
| Time | | | | | |
+-----+-----+-----+-----+-----+
| 18.254 | m0pd/bb/me1/qout_reg/CLK | ^ | clk__L4_N9 | | 
| 18.502 | m0pd/bb/me1/qout_reg/Q | v | B[1] | DFFP0SX1 | 
| 18.556 | U1882/B | v | B[1] | AND2X1 | 
| 11.000 | v | .. | ~12/61[11] | AND2V1 |
```

Figure t: Final Timing report

```
* type 'help' to get started
* or type 'exit' to quit
*****
encounter 1> reportGateCount -limit 0
Gate area 2.8158 um^2
[0] cpu Gates=15744 Cells=14446 Area=44333.4 um^2
encounter 2>
```

Figure u: Gate count from encounter

```

Generating native compiled code:
    worklib.stimulus:v <0x19f0146c>
        streams: 13, words: 34978
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
          Instances Unique
Modules:      6607   33
Primitives:   7187   6
Registers:   2166  14
Scalar wires: 3692   -
Expanded wires: 1198  41
Vectored wires: 6   -
Always blocks: 2156   4
Initial blocks: 3   3
Cont. assignments: 11  15
Pseudo assignments: 43  43
Writing initial simulation snapshot: worklib.stimulus:v
Loading snapshot worklib.stimulus:v ..... Done
xcelium> source /apps/cadence/XCELIUM1803/tools/xcelium/files/xmsimrc
xcelium> run
xmsim: *W,SHMPOPT: Some objects excluded from $shm_probe due to optimizations.
      File: ./tb_test.v, line = 29, pos = 11
      Scope: stimulus
      Time: 0 FS + 0

Simulation complete via $finish(1) at time 501 NS + 0
./tb_test.v:31 #1 $finish;
xcelium> exit
asrinival@saturn.ece.iit.edu:~%

```

Figure v: RTL for tb_test

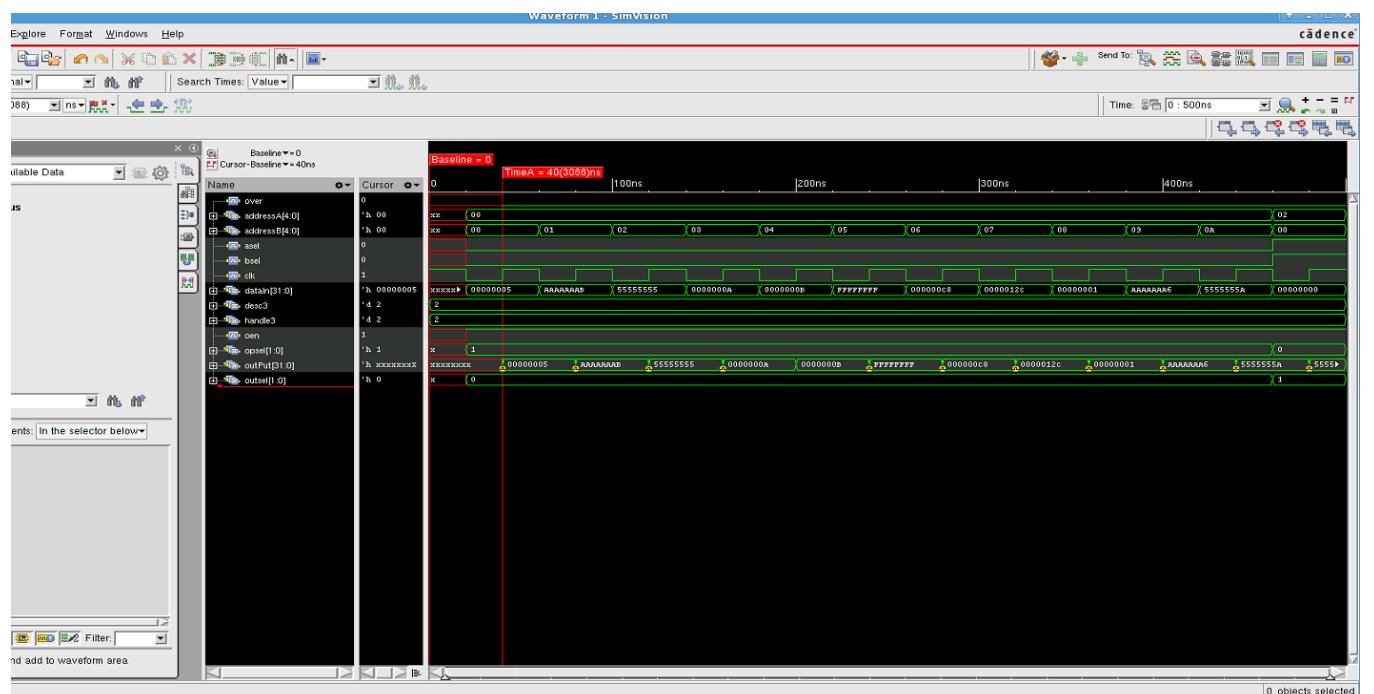


Figure w: Simvision for tb_Test

```
timing.rep.5.final (~/Desktop/Project/CLA) - gedit
File Edit View Search Tools Documents Help
New Open Save Print... Undo Redo Cut Copy Paste Find Replace
timing.rep.5.final x
#####
# Generated by: Cadence Encounter 10.13-s292_1
# OS: Linux x86_64(Host ID saturn.ece.iit.edu)
# Generated on: Sat Dec 4 20:28:35 2021
# Design: cpu
# Command: report_timing -nworst 10 -net > timing.rep.5.final
#####
Path 1: MET Setup Check with Pin mb/ram/mer24/l1/me31/qout_reg/CLK
Endpoint: mb/ram/mer24/l1/me31/qout_reg/D (^) checked with leading edge of
'clk'
Beginpoint: m0pd/bb/me2/qout_reg/Q (v) triggered by leading edge of
'clk'
Other End Arrival Time 0.350
- Setup 4.314
+ Phase Shift 17.000
= Required Time 13.036
- Arrival Time 11.086
= Slack Time 1.949
    Clock Rise Edge 0.000
    + Clock Network Latency (Prop) 0.357
    = Beginpoint Arrival Time 0.357

+-----+
+
|           Pin          |   Edge |           Net          |   Cell | Delay | Arrival
| Required |           |           |           |           |           |
| Time     |           |           |           |           |           |
|          |-----+-----+-----+-----+-----+
+-----+
| m0pd/bb/me2/qout_reg/CLK | ^ | clk_L4_N39 |           |           | 0.357
| 2.306 |           |           |           |           |
| m0pd/bb/me2/qout_reg/Q  | v | B[2]   | DFFPOSX1 | 0.290 | 0.647
| 2.596 |           |           |           |           |
| U1892/B |           | v | B[2]   | AND2X1  | 0.092 | 0.739
| 2.688 |           |           |           |           |
| U1892/V |           | v | B[2]   | AND2X1 | 0.120 | 0.850
```

Figure x: Timing report for maximum frequency

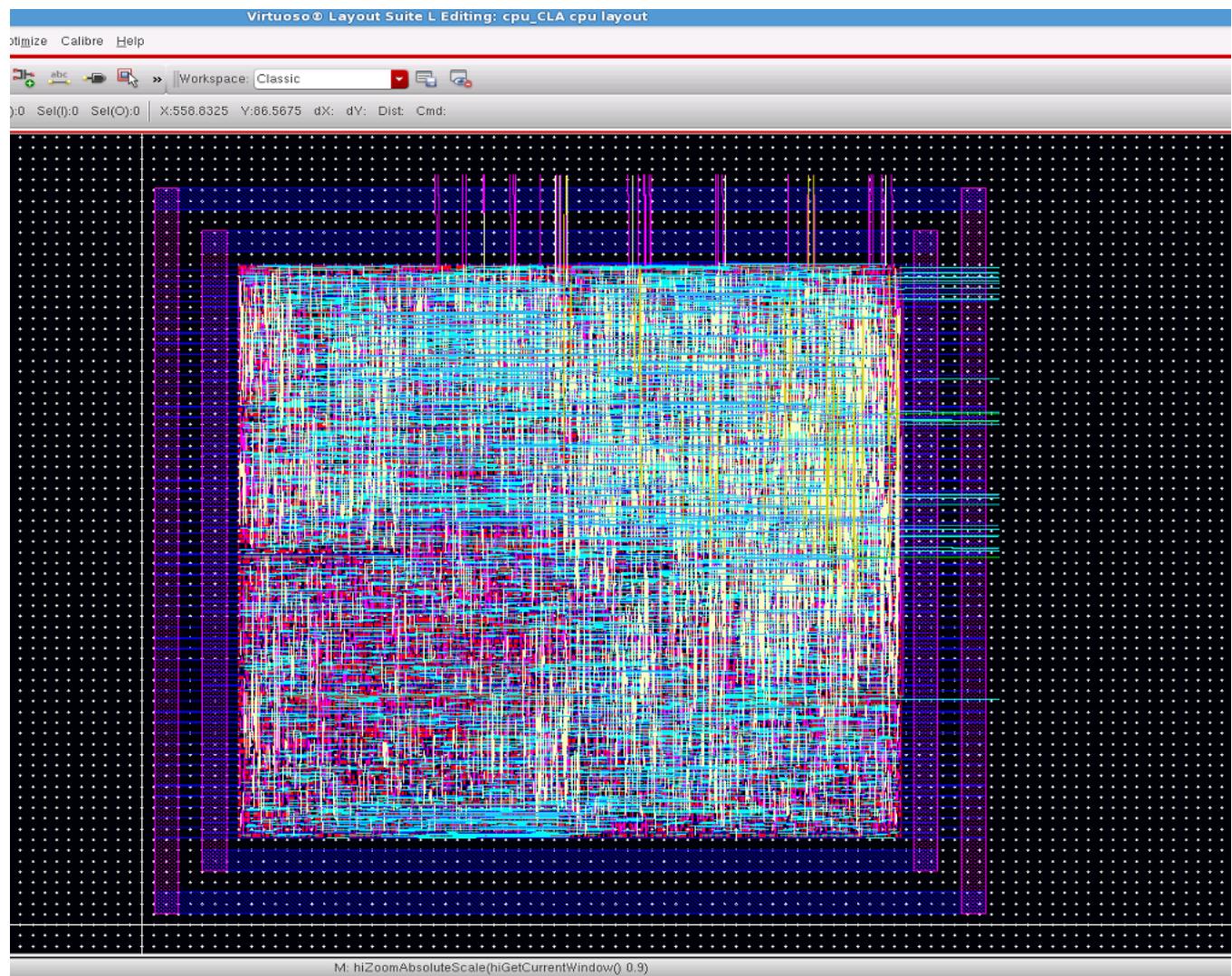


Figure y: Layout of CLA

3. Carry Skip Adder (CSA)

```

streams: 13, words: 17668
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
          Instances Unique
Modules:           6575   31
Primitives:        7347    6
Registers:         2166   14
Scalar wires:      3570    -
Expanded wires:    1198   41
Vectored wires:    6      -
Always blocks:     2156   4
Initial blocks:    3      3
Cont. assignments: 10     12
Pseudo assignments: 43     43
Writing initial simulation snapshot: worklib.stimulus:v
DEFINE OSU_stdcells /apps/FreePDK45/osu_soc/lib/freepdk45_cells
|
xmsim: *W_DLCLAP (./cds.lib,8): cds.lib Same file has different definitions for library 'library OSU_stdcells
from /home/asrinival/Desktop/Project/CSA/cds.lib line 8, redefines
library OSU_stdcells from same file line 7 defined earlier.' (continuing with last specified path).
Loading snapshot worklib.stimulus:v ..... Done
xcelium> source /apps/cadence/XCELIUM1803/tools/xcelium/files/xmsimrc
xcelium> run
xmsim: *W_SHMPOPT: Some objects excluded from $shm_probe due to optimizations.
      File: ./tb_cpu.v, line = 28, pos = 11
      Scope: stimulus
      Time: 0 FS + 0

Simulation complete via $finish(1) at time 501 NS + 0
./tb_cpu.v:30 #1 $finish;
xcelium> exit
asrinival@saturn.ece.iit.edu:~%
```

Figure z: RTL for CSA

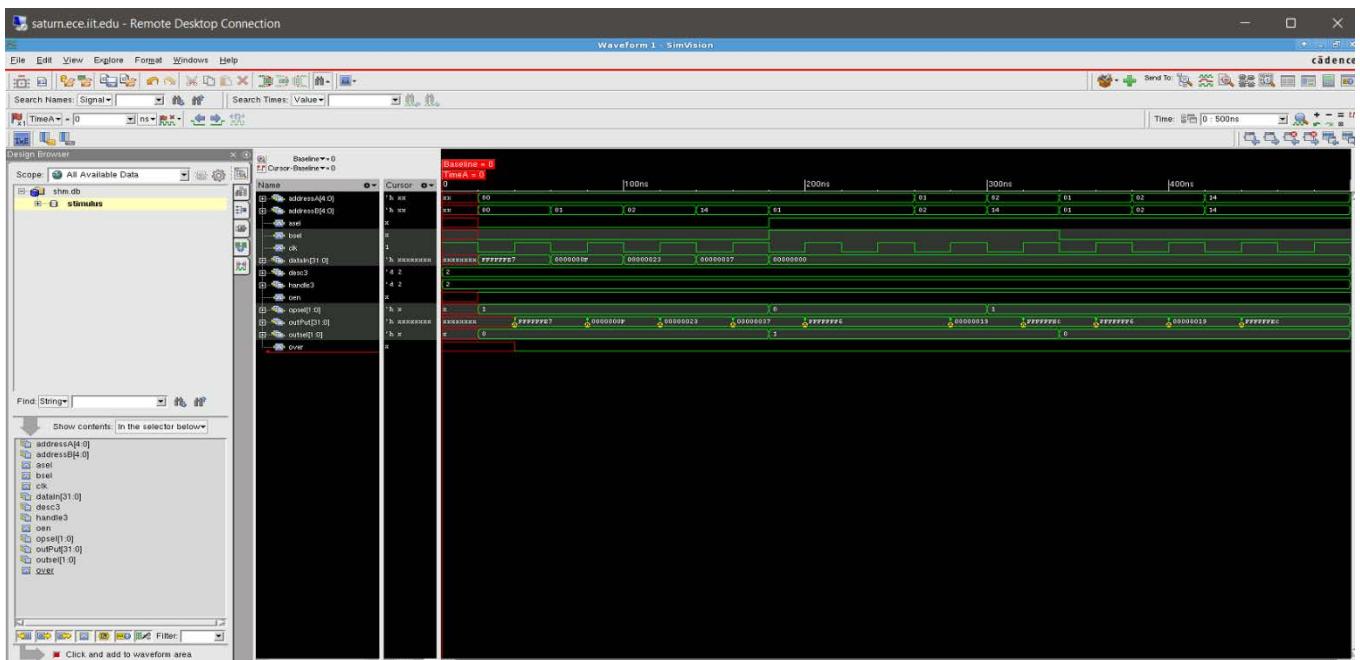


Figure aa: Simvision for tb_cpu

```

worklib.DFFSR:v <0x5559ea95>
    streams: 0, words: 0
worklib.DFFNEGX1:v <0x3a46602b>
    streams: 0, words: 0
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
          Instances   Unique
Modules:           14499     34
UDPs:             1628      4
Primitives:       25424      6
Timing outputs:  14499     19
Registers:        1638     18
Scalar wires:    16357      -
Expanded wires:   46       5
Always blocks:   1         1
Initial blocks:  3         3
Pseudo assignments: 9       9
Timing checks:   9769    1625
Simulation timescale: 10ps
Writing initial simulation snapshot: worklib.AOI21X1:v
DEFINE OSU_stdcells /apps/FreePDK45/osu_soc/lib/freepdk45_cells
|
xmsim: *W,DLCLAP (./cds.lib,8): cds.lib Same file has different definitions for library 'library OSU_stdcells
from /home/asrinival/Desktop/Project/CSA/cds.lib line 8, redefines
    library OSU_stdcells from same file line 7 defined earlier.' (continuing with last specified path).
Loading snapshot worklib.AOI21X1:v ..... Done
xcelium> source /apps/cadence/XCELIUM1803/tools/xcelium/files/xmsimrc
xcelium> run
Simulation complete via $finish(1) at time 501 NS + 0
./tb_cpu.v:30 #1 $finish;
xcelium> exit
asrinival@saturn.ece.iit.edu:~% █

```

Figure bb: Logic Synthesis

```

-----
-----
*      Power Distribution Summary:
*      Highest Average Power:          clk_L4_I7 (INVX8):
0.009491
*      Highest Leakage Power: mb/ram/mer2/l1/me31/qout_reg (DFFPOSX1):
5.498e-05
*      Total Cap: 1.81192e-10 F
*      Total instances in design: 14565
*      Total instances in design with no power: 0
*      Total instances in design with no activity: 0
*      Total Fillers and Decap: 0
-----
report_power consumed time (real time) 00:00:00 : peak memory (593H)
1
encounter 5> █

```

Figure cc: Power report

cell.rep (~/Desktop/Project/CSA) - gedit

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cell.rep x

```

o/c17/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t4/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t5/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t6/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t7/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t8/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t9/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t10/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t11/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t12/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t13/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t14/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t15/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t16/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t17/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t18/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t19/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t20/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t21/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t22/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t23/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t24/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t25/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t26/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t27/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t28/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t29/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t30/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t31/b1 TBUFX2 gscl45nm 3.754400 n
wb/bd/me0/qout_reg DFFPOSX1 gscl45nm 7.978100 n
wb/bd/me1/qout_reg DFFPOSX1 gscl45nm 7.978100 n
wb/bd/me2/qout_reg DFFPOSX1 gscl45nm 7.978100 n
wb/bd/me3/qout_reg DFFPOSX1 gscl45nm 7.978100 n
wb/bd/me4/qout_reg DFFPOSX1 gscl45nm 7.978100 n
-----
Total 14479 cells 48878.063377
1

```

Ln 1, Col 1 INS ..

Figure dd: Cell report for CSA

```

*****
encounter 1> reportGateCount -limit 0
Gate area 2.8158 um^2
[0] cpu Gates=15848 Cells=14565 Area=44626.2 um^2
encounter 2> ■

```

Figure ee: Gate count report

timing.rep (~/Desktop/Project/CSA) - gedit

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timing.rep.5.final timing.rep

```

a/l3/f2308/U2/Y (XOR2X1)          0.07    5.64 r
a/l3/f247/U5/Y (XNOR2X1)         0.06    5.71 r
a/l3/f247/U2/Y (XOR2X1)          0.07    5.78 r
a/l3/f256/U5/Y (XNOR2X1)         0.06    5.84 r
a/l3/f256/U2/Y (XOR2X1)          0.07    5.91 r
a/l3/f265/U5/Y (XNOR2X1)         0.06    5.97 r
a/l3/f265/U2/Y (XOR2X1)          0.07    6.04 r
a/l3/f274/U5/Y (XNOR2X1)         0.06    6.11 r
a/l3/f274/U2/Y (XOR2X1)          0.07    6.18 r
a/l3/f283/U5/Y (XNOR2X1)         0.06    6.24 r
a/l3/f283/U2/Y (XOR2X1)          0.07    6.31 r
a/l3/f292/U5/Y (XNOR2X1)         0.06    6.37 r
a/l3/f292/U2/Y (XOR2X1)          0.07    6.44 r
a/l3/h301/U2/Y (XOR2X1)          0.04    6.48 f
a/U26/Y (AOI22X1)                0.03    6.52 r
U222/Y (BUFX2)                  0.04    6.56 r
U67/Y (AND2X1)                  0.07    6.62 r
U1832/Y (INVX1)                 0.10    6.73 f
mb/ram/mer12/m0/m31/U3/Y (AOI22X1) 0.05    6.78 r
U3835/Y (INVX1)                 0.02    6.80 f
mb/ram/mer12/ll/me31/qout_reg/D (DFFP0SX1) 0.00    6.80 f
data arrival time               6.80

clock clk (rise edge)           33.00   33.00
clock network delay (ideal)     0.00    33.00
mb/ram/mer12/ll/me31/qout_reg/CLK (DFFP0SX1) 0.00    33.00 r
library setup time              -0.06   32.94
data required time              32.94
-----
data required time              32.94
data arrival time               -6.80
-----
slack (MET)                    26.14

```

1

Ln 1, Col 1 INS

Figure ff: Timing report

```

#####
# Generated by: Cadence Encounter 10.13-s292_1
# OS: Linux x86_64(Host ID saturn.ece.iit.edu)
# Generated on: Sat Dec 4 21:02:48 2021
# Design: cpu
# Command: report_timing -nworst 10 -net > timing.rep.5.final
#####
Path 1: MET Setup Check with Pin mb/ram/mer11/ll/me31/qout_reg/CLK
Endpoint: mb/ram/mer11/ll/me31/qout_reg/D (^) checked with leading edge of
'clk'
Beginpoint: m0pd/bb/me1/qout_reg/Q      (v) triggered by leading edge of
'clk'
Other End Arrival Time      0.309
- Setup                      3.945
+ Phase Shift                33.000
= Required Time              29.364
- Arrival Time               11.046
= Slack Time                 18.318
    Clock Rise Edge          0.000
    + Clock Network Latency (Prop) 0.309
    = Beginpoint Arrival Time  0.309

-----
+
|             Pin          | Edge | Net       | Cell    | Delay | Arrival
| Required |          | |          |          | |       |
| Time    |          | |          |          | |       |
|          |          +-----+-----+-----+-----+-----+
+-----+
| m0pd/bb/me1/qout_reg/CLK | ^  | clk_L4_N0 |          |        | 0.309
| 18.628 |          | v  | B[1]     | DFFP0SX1 | 0.216 | 0.525
| 18.844 |          | v  | B[1]     | AND2X1  | 0.169 | 0.694
| 19.013 |          | v  | B[1]     | AND2X1  | 0.142 | 0.827
| 19.100 |          | v  | B[1]     | AND2X1  | 0.142 | 0.827

```

Ln 1, Col 1 INS

Figure gg: final timing report

cell.rep (~Desktop/Project/CSA) - gedit

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cell.rep x

o/tr/t1/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t4/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t5/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t6/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t7/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t8/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t9/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t10/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t11/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t12/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t13/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t14/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t15/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t16/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t17/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t18/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t19/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t20/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t21/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t22/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t23/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t24/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t25/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t26/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t27/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t28/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t29/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t30/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t31/b1	TBUFX2	gscl45nm	3.754400	n
wb/bd/me0/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me1/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me2/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me3/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me4/qout_reg	DFFPOSX1	gscl45nm	7.978100	n

Total 14479 cells 48878.063377
1

Figure hh: Cell report for tb test

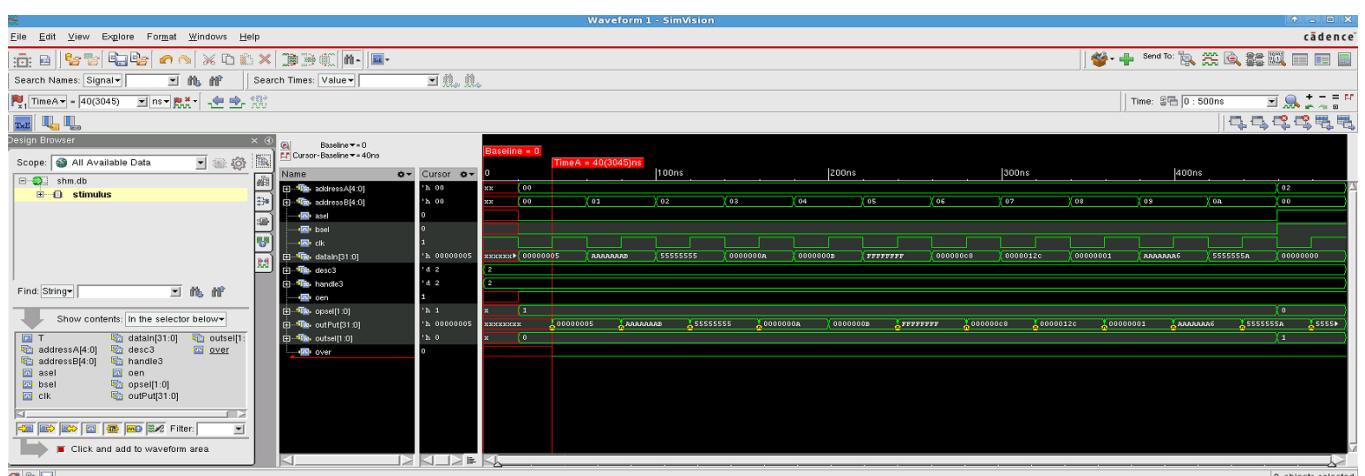


Figure ii: simvision for tb test

New Open Save Print... Undo Redo Cut Copy Paste Find Replace

timing.rep x

```

a/l3/f2308/U2/Y (XOR2X1) 0.00 5.57 r
a/l3/f247/U5/Y (XNOR2X1) 0.07 5.64 r
a/l3/f247/U2/Y (XOR2X1) 0.06 5.71 r
a/l3/f247/U2/Y (XOR2X1) 0.07 5.78 r
a/l3/f256/U5/Y (XNOR2X1) 0.06 5.84 r
a/l3/f256/U2/Y (XOR2X1) 0.07 5.91 r
a/l3/f265/U5/Y (XNOR2X1) 0.06 5.97 r
a/l3/f265/U2/Y (XOR2X1) 0.07 6.04 r
a/l3/f274/U5/Y (XNOR2X1) 0.06 6.11 r
a/l3/f274/U2/Y (XOR2X1) 0.07 6.18 r
a/l3/f283/U5/Y (XNOR2X1) 0.06 6.24 r
a/l3/f283/U2/Y (XOR2X1) 0.07 6.31 r
a/l3/f292/U5/Y (XNOR2X1) 0.06 6.37 r
a/l3/f292/U2/Y (XOR2X1) 0.07 6.44 r
a/l3/h301/U2/Y (XOR2X1) 0.04 6.48 f
a/U26/Y (A0I22X1) 0.03 6.52 r
U222/Y (BUFX2) 0.04 6.56 r
U67/Y (AND2X1) 0.07 6.62 r
U1832/Y (INVX1) 0.10 6.73 f
mb/ram/merl2/m0/m31/U3/Y (A0I22X1) 0.05 6.78 r
U3835/Y (INVX1) 0.02 6.80 f
mb/ram/merl2/ll/me31/qout_reg/D (DFFP0SX1) 0.00 6.80 f
data arrival time 6.80

clock clk (rise edge) 33.00 33.00
clock network delay (ideal) 0.00 33.00
mb/ram/merl2/ll/me31/qout_reg/CLK (DFFP0SX1) 0.00 33.00 r
library setup time -0.06 32.94
data required time 32.94
-----
```

data required time 32.94
 data arrival time -6.80

slack (MET) 26.14

1

Ln 1, Col 1 INS

Figure jj: timing report for tb_test

New Open Save Print... Undo Redo Cut Copy Paste Find Replace

timing.rep.5.final x

```

#####
# Generated by: Cadence Encounter 10.13-s292_1
# OS: Linux x86_64(Host ID saturn.ece.iit.edu)
# Generated on: Sat Dec 4 21:19:26 2021
# Design: cpu
# Command: report_timing -nworst 10 -net > timing.rep.5.final
#####
Path 1: MET Setup Check with Pin mb/ram/merl1/ll/me31/qout_reg/CLK
Endpoint: mb/ram/merl1/ll/me31/qout_reg/D (^) checked with leading edge of
'clk'
Beginpoint: m0pd/bb/me1/qout_reg/Q (v) triggered by leading edge of
'clk'
Other End Arrival Time 0.309
- Setup 3.945
+ Phase Shift 33.000
= Required Time 29.364
- Arrival Time 11.046
= Slack Time 18.318
  Clock Rise Edge 0.000
  + Clock Network Latency (Prop) 0.309
  = Beginpoint Arrival Time 0.309

+-----+
|           Pin          | Edge | Net      | Cell    | Delay | Arrival
| Required |          |       |          |         |       |
| Time   |          |       |          |         |       |
|-----+-----+-----+-----+-----+-----+
| m0pd/bb/me1/qout_reg/CLK | ^   | clk_L4_N0 |         |       | 0.309
| 18.628 |          | v   | B[1]     | DFFP0SX1 | 0.216 | 0.525
| m0pd/bb/me1/qout_reg/Q | v   | B[1]     | AND2X1  | 0.169 | 0.694
| 18.844 |          | v   | B[1]     | AND2X1  | 0.142 | 0.027
| U1980/B |          | v   | B[1]     | AND2X1  | 0.142 | 0.027
| 19.013 |          | v   | B[1]     | AND2X1  | 0.142 | 0.027
| U11000/v |          | v   | B[1]     | AND2X1  | 0.142 | 0.027
|-----+
```

>Loading file '/home/asrinival/Desktop/Project/CSA/timing.rep.5.final'...

Ln 1, Col 1 INS

Figure kk: Final timing report for tb_test

```

*          Total Fillers and Decap:    0
-----
report_power consumed time (real time) 00:00:00 : peak memory (583M)
1
encounter 2> reportGateCount -limit 0
Gate area 2.8158 um^2
[0] cpu Gates=15848 Cells=14565 Area=44626.2 um^2
encounter 3>

```

Figure II: gatecount report for tb_test

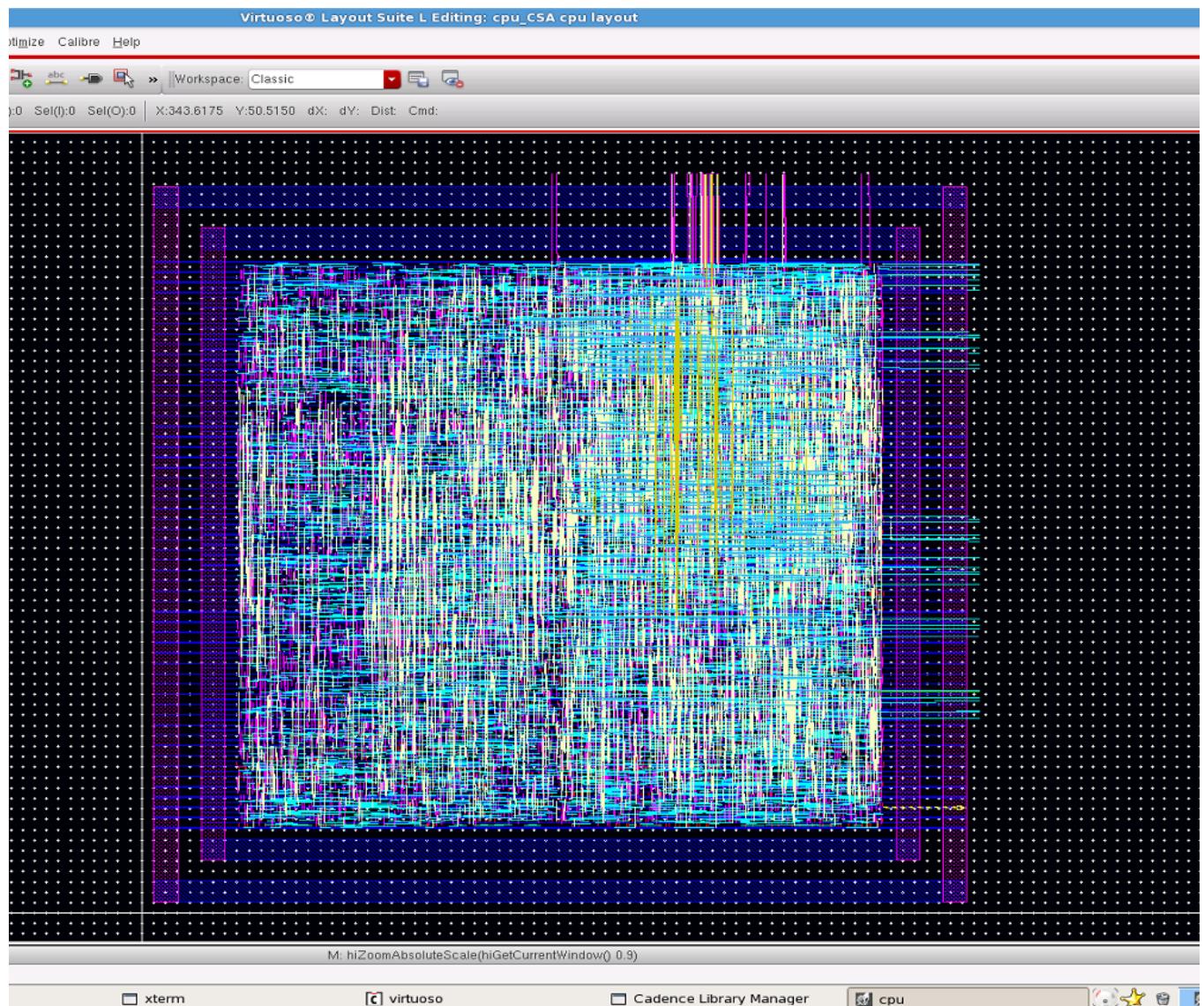


Figure mm: layout of CSA

4. Carry Select Adder (CSeA)

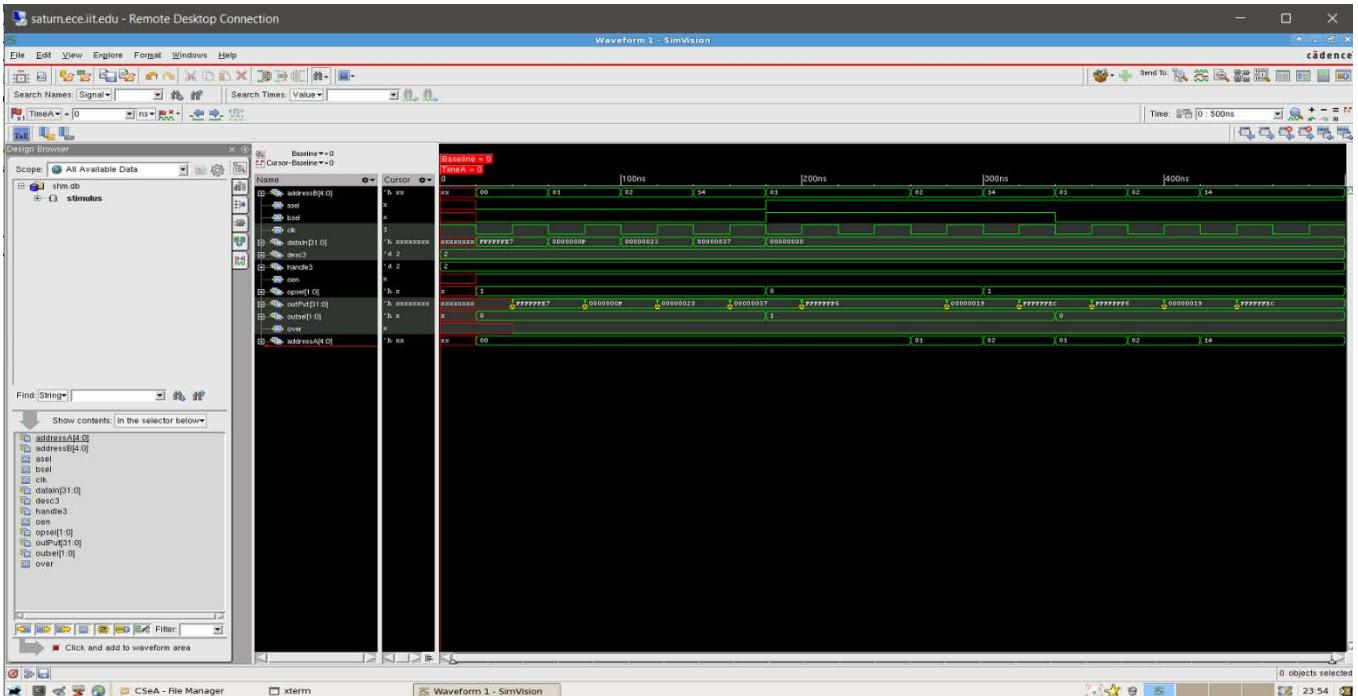


Figure nn: Simvision for CSeA

```

saturn.ece.iit.edu - PuTTY

Design hierarchy summary:
      Instances  Unique
Modules:          14598    34
UDPs:            1628     4
Primitives:      25648     6
Timing outputs:  14598    19
Registers:       1638    18
Scalar wires:    16456    -
Expanded wires:  46      5
Always blocks:   1       1
Initial blocks:  3       3
Pseudo assignments:  9      9
Timing checks:   9769   1625
Simulation timescale: 10ps

Writing initial simulation snapshot: worklib.AOI21X1:v
DEFINE OSU_stdcells /apps/FreePDK45/osu_soc/lib/freepdk45_cells

kmsim: *W,DLCLAP (./cds.lib,8): cds.lib Same file has different definitions for
library 'library OSU_stdcells from /home/asrinival/Desktop/Project/CSeA/cds.lib
line 8, redefines
library OSU_stdcells from same file line 7 defined earlier.' (continuing with
last specified path).
DEFINE OSU_stdcells /apps/FreePDK45/osu_soc/lib/freepdk45_cells

```

Figure oo: RTL for tb_cpu

```

saturn.ece.iit.edu - PuTTY

Design hierarchy summary:
      Instances  Unique
Modules:          14680      34
UDPs:            1628       4
Primitives:      25730       6
Timing outputs:  14680      19
Registers:       1638      18
Scalar wires:    16538      -
Expanded wires:   46        5
Always blocks:   1         1
Initial blocks:  3         3
Pseudo assignments: 9        9
Timing checks:   9769     1625
Simulation timescale: 10ps

Writing initial simulation snapshot: worklib.AOI21X1:v
DEFINE OSU_stdcells /apps/FreePDK45/osu_soc/lib/freepdk45_cells
|
xmsim: *W,DLCRAP (./cds.lib,8): cds.lib Same file has different definitions for
library 'library OSU_stdcells from /home/asrinival/Desktop/Project/CSeA/cds.lib
line 8, redefines
    library OSU_stdcells from same file line 7 defined earlier.' (continuing with
last specified path).
DEFINE OSU_stdcells /apps/FreePDK45/osu_soc/lib/freepdk45_cells
|

```

Figure pp: logic synthesis

```

-----
*      Power Distribution Summary:
*      Highest Average Power:           clk_L4_I26 (INVX8):
0.009877
*      Highest Leakage Power: mb/ram/mer2/l1/me31/qout_reg (DIFFPOSXL):
5.498e-05
*      Total Cap:      1.84055e-10 F
*      Total instances in design: 14660
*      Total instances in design with no power: 0
*      Total instances in design with no activity: 0
*      Total Fillers and Decap: 0
-----
```

Figure qq: Power report

cell.rep (~/Desktop/Project/CSeA) - gedit

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New Open Save Print... Undo Redo Cut Copy Paste Find Replace

cell.rep x

o/tr/t4/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t5/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t6/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t7/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t8/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t9/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t10/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t11/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t12/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t13/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t14/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t15/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t16/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t17/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t18/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t19/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t20/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t21/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t22/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t23/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t24/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t25/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t26/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t27/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t28/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t29/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t30/b1	TBUFX2	gscl45nm	3.754400	n
o/tr/t31/b1	TBUFX2	gscl45nm	3.754400	n
wb/bd/me0/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me1/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me2/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me3/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
wb/bd/me4/qout_reg	DFFPOSX1	gscl45nm	7.978100	n
Total 14577 cells			49150.726672	
1				

Ln 1, Col 1 INS

Figure rr: cell report of CSeA

```
=====
encounter 1> reportGateCount -limit 0
Gate area 2.8158 um^2
[0] cpu Gates=15933 Cells=14660 Area=44864.6 um^2
encounter 2>
```

Figure ss: Gate count report

New Open Save Print... Undo Redo Cut Copy Paste Find Replace

timing.rep.5.final

```
#####
# Generated by: Cadence Encounter 10.13-s292_1
# OS: Linux x86_64 (Host ID saturn.ece.iit.edu)
# Generated on: Sun Dec 5 00:08:12 2021
# Design: cpu
# Command: report_timing -nworst 10 -net > timing.rep.5.final
#####
Path 1: MET Setup Check with Pin mb/ram/mer18/ll/me31/qout_reg/CLK
Endpoint: mb/ram/mer18/ll/me31/qout_reg/D (^) checked with leading edge of
'clk'
Beginpoint: m0pd/bb/me1/qout_reg/Q (v) triggered by leading edge of
'clk'
Other End Arrival Time 0.319
- Setup 4.060
+ Phase Shift 33.000
= Required Time 29.259
- Arrival Time 11.114
= Slack Time 18.144
    Clock Rise Edge 0.000
    + Clock Network Latency (Prop) 0.314
    = Beginpoint Arrival Time 0.314

+-----+
+-----+-----+-----+-----+-----+-----+-----+
| Required | Pin | Edge | Net | Cell | Delay | Arrival |
| Time | | | | | | |
+-----+-----+-----+-----+-----+-----+-----+
| 18.458 | m0pd/bb/me1/qout_reg/CLK | ^ | clk_L4_N14 | | | 0.314
| 18.709 | m0pd/bb/me1/qout_reg/Q | v | B[1] | DFFP0SX1 | 0.251 | 0.564
| 18.770 | U2014/B | v | B[1] | AND2X1 | 0.062 | 0.626
| 18.770 | U2014/B | v | B[1] | AND2X1 | 0.111 | 0.727

```

Ln 1, Col 1 INS

Figure tt: Timing report

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timing.rep (~/Desktop/Project/CSEA) - gedit

New Open Save Print... Undo Redo Cut Copy Paste Find Replace

timing.rep

```
a/l3/f2308/U2/Y (XOR2X1) 0.00 5.64 r
a/l3/f247/U5/Y (XNOR2X1) 0.07 5.71 r
a/l3/f247/U2/Y (XOR2X1) 0.06 5.78 r
a/l3/f256/U5/Y (XNOR2X1) 0.07 5.84 r
a/l3/f256/U2/Y (XOR2X1) 0.06 5.91 r
a/l3/f265/U5/Y (XNOR2X1) 0.07 5.97 r
a/l3/f265/U2/Y (XOR2X1) 0.06 6.04 r
a/l3/f274/U5/Y (XNOR2X1) 0.07 6.11 r
a/l3/f274/U2/Y (XOR2X1) 0.06 6.18 r
a/l3/f283/U5/Y (XNOR2X1) 0.07 6.24 r
a/l3/f283/U2/Y (XOR2X1) 0.06 6.31 r
a/l3/f292/U5/Y (XNOR2X1) 0.07 6.37 r
a/l3/f292/U2/Y (XOR2X1) 0.06 6.44 r
a/l3/h301/U2/Y (XOR2X1) 0.04 6.48 f
a/U26/Y (AOI22X1) 0.03 6.52 r
U243/Y (BUFX2) 0.04 6.56 r
U74/Y (AND2X1) 0.07 6.62 r
U1844/Y (INVX1) 0.10 6.73 f
mb/ram/mer12/m0/m31/U3/Y (AOI22X1) 0.05 6.78 r
U3884/Y (INVX1) 0.02 6.80 f
mb/ram/mer12/ll/me31/qout_reg/D (DFFP0SX1) 0.00 6.80 f
data arrival time 6.80

clock clk (rise edge) 33.00 33.00
clock network delay (ideal) 0.00 33.00
mb/ram/mer12/ll/me31/qout_reg/CLK (DFFP0SX1) 0.00 33.00 r
library setup time -0.06 32.94
data required time 32.94

data required time 32.94
data arrival time -6.80

slack (MET) 26.14
```

1

Ln 1, Col 1 INS

Figure uu: timing report

```

xmvlog_cg: *W,DLCLAP (../cds.lib,9): cds.lib Same file has different definitions
for library 'library OSU_stdcells from /home/asrinival/Desktop/Project/CSeA/cds.
lib line 9, redefines
    library OSU_stdcells from same file line 8 defined earlier.' (continuing with last specified path).
        worklib.stimulus:v <0x19f0146c>
            streams: 13, words: 34978
        Building instance specific data structures.
        Loading native compiled code: ..... Done
    Design hierarchy summary:
        Instances Unique
    Modules: 6607 31
    Primitives: 7507 6
    Registers: 2166 14
    Scalar wires: 3571 -
    Expanded wires: 1230 49
    Vectored wires: 6 -
    Always blocks: 2156 4
    Initial blocks: 3 3
    Cont. assignments: 9 11
    Pseudo assignments: 43 43
    Writing initial simulation snapshot: worklib.stimulus:v
    DEFINE OSU_stdcells /apps/FreePDK45/osu_soc/lib/freepdk45_cells
|

```

Figure vv: RTL for tb_test

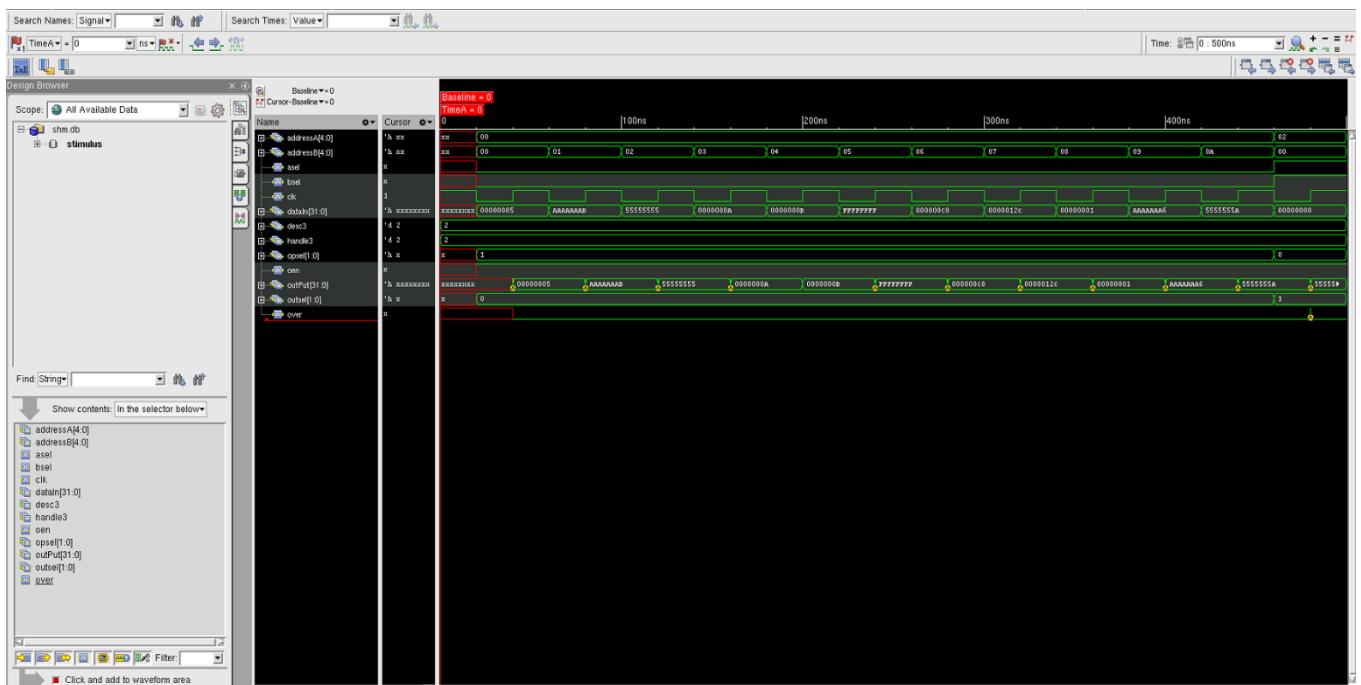


Figure ww: simvision for tb_test

```

-----
* Power Distribution Summary:
* Highest Average Power: clk_L4_I26 (INVX8):
0.009877
* Highest Leakage Power: mb/ram/mer2/ll/me31/qout_reg (DFFPOSX1):
5.498e-05
* Total Cap: 1.84055e-10 F
* Total instances in design: 14660
* Total instances in design with no power: 0
* Total instances in design with no activity: 0
* Total Fillers and Decap: 0
-----
reportPower consumed time (real time) 00:00:00 : peak memory (563M)
1
encounter 3> ■

```

Figure xx: Power report for tb_test

```

#####
# Generated by: Cadence Encounter 10.13-s292_1
# OS: Linux x86_64(Host ID saturn.ece.iit.edu)
# Generated on: Sun Dec 5 00:22:44 2021
# Design: cpu
# Command: report_timing -nworst 10 -net > timing.rep.5.final
#####
Path 1: MET Setup Check with Pin mb/ram/mer18/ll/me31/qout_reg/CLK
Endpoint: mb/ram/mer18/ll/me31/qout_reg/D (^) checked with leading edge of
'clk'
Beginpoint: m0pd/bb/me1/qout_reg/Q (v) triggered by leading edge of
'clk'
Other End Arrival Time 0.319
- Setup 4.060
+ Phase Shift 33.000
= Required Time 29.259
- Arrival Time 11.114
= Slack Time 18.144
    Clock Rise Edge 0.000
    + Clock Network Latency (Prop) 0.314
    = Beginpoint Arrival Time 0.314

+-----+
+-----+-----+-----+-----+-----+-----+-----+
| Required | Pin | Edge | Net | Cell | Delay | Arrival |
| Time | | | | | | |
+-----+-----+-----+-----+-----+-----+-----+
| 18.458 | m0pd/bb/me1/qout_reg/CLK | ^ | clk_L4_N14 | | | 0.314
| 18.709 | m0pd/bb/me1/qout_reg/Q | v | B[1] | DFFPOSX1 | 0.251 | 0.564
| 18.770 | U2014/B | v | B[1] | AND2X1 | 0.062 | 0.626
| 18.770 | U2014/V | v | B[1] | AND2X1 | 0.111 | 0.727

```

Figure yy: Timing final report for tb_test

a/l3/f2508/U5/Y (XNOR2X1)	0.00	5.57 r
a/l3/f2308/U2/Y (XOR2X1)	0.07	5.64 r
a/l3/f247/U5/Y (XNOR2X1)	0.06	5.71 r
a/l3/f247/U2/Y (XOR2X1)	0.07	5.78 r
a/l3/f256/U5/Y (XNOR2X1)	0.06	5.84 r
a/l3/f256/U2/Y (XOR2X1)	0.07	5.91 r
a/l3/f265/U5/Y (XNOR2X1)	0.06	5.97 r
a/l3/f265/U2/Y (XOR2X1)	0.07	6.04 r
a/l3/f274/U5/Y (XNOR2X1)	0.06	6.11 r
a/l3/f274/U2/Y (XOR2X1)	0.07	6.18 r
a/l3/f283/U5/Y (XNOR2X1)	0.06	6.24 r
a/l3/f283/U2/Y (XOR2X1)	0.07	6.31 r
a/l3/f292/U5/Y (XNOR2X1)	0.06	6.37 r
a/l3/f292/U2/Y (XOR2X1)	0.07	6.44 r
a/l3/h301/U2/Y (XOR2X1)	0.04	6.48 f
a/U26/Y (AOI22X1)	0.03	6.52 r
U243/Y (BUFX2)	0.04	6.56 r
U74/Y (AND2X1)	0.07	6.62 r
U1844/Y (INVX1)	0.10	6.73 f
mb/ram/mer12/m0/m31/U3/Y (AOI22X1)	0.05	6.78 r
U3884/Y (INVX1)	0.02	6.80 f
mb/ram/mer12/ll/me31/qout_reg/D (DFFPOSX1)	0.00	6.80 f
data arrival time		6.80
clock clk (rise edge)	33.00	33.00
clock network delay (ideal)	0.00	33.00
mb/ram/mer12/ll/me31/qout_reg/CLK (DFFPOSX1)	0.00	33.00 r
library setup time	-0.06	32.94
data required time		32.94

data required time		32.94
data arrival time		-6.80

slack (MET)		26.14

1

Ln 1, Col 1

INS

Figure zz: timing report tb_test

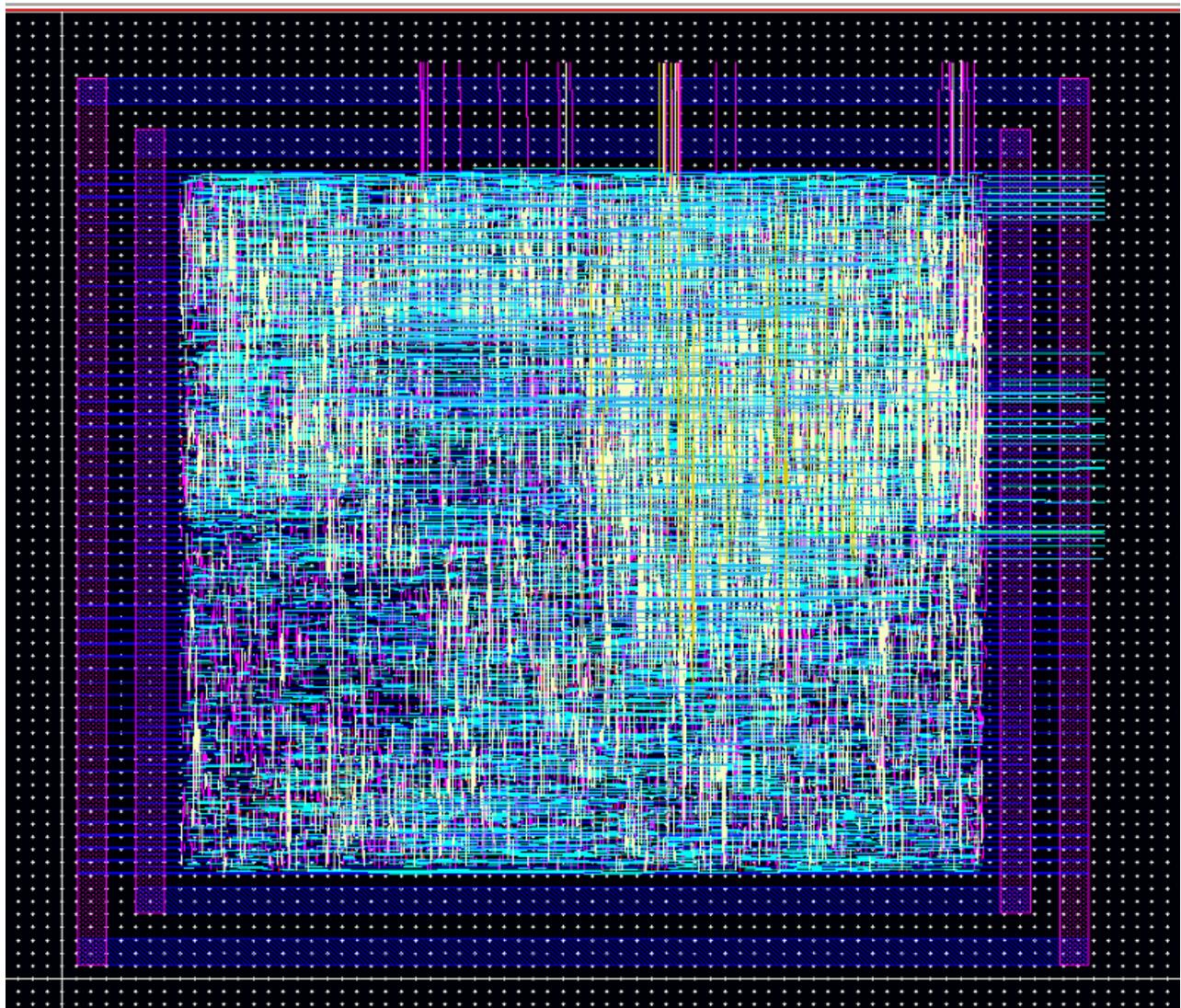


Figure aaa: Layout of CSeA

Case ii: Comparator:

```

worklib.dreg:v <0x60a2e9c9>
    streams: 2, words: 264
worklib.stimulus:v <0x49aa807b>
    streams: 13, words: 42067
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
      Instances Unique
Modules:       6672   37
Primitives:    7187    6
Registers:    2293   18
Scalar wires: 3819    -
Expanded wires: 1199   41
Vectored wires: 7    -
Always blocks: 2220   6
Initial blocks: 3    3
Cont. assignments: 12   16
Pseudo assignments: 43   43
Writing initial simulation snapshot: worklib.stimulus:v
Loading snapshot worklib.stimulus:v ..... Done
xcelium> source /apps/cadence/XCELIUM1803/tools/xcelium/files/xmsimrc
xcelium> run
xmsim: *W,SHMPOPT: Some objects excluded from $shm_probe due to optimizations.
      File: ./tb_test_comp.v, line = 28, pos = 11
      Scope: stimulus
      Time: 0 FS + 0

Please check Select Lines!
Please check Select Lines!
Simulation complete via $finish(1) at time 1001 NS + 0
./tb_test_comp.v:30 #1 $finish;
xcelium> exit
asrinival@saturn.ece.iit.edu:~%
```

Figure bbb: RTL for Comparator

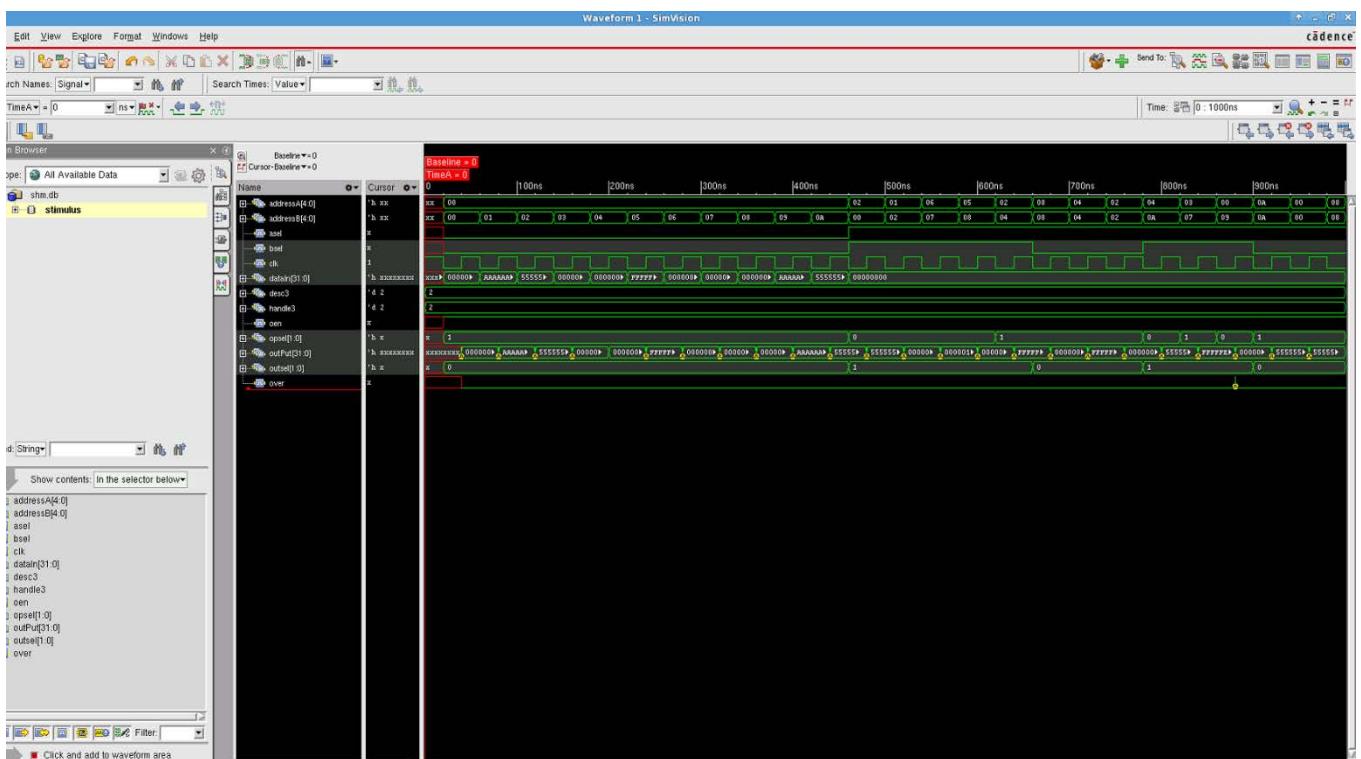


Figure ccc: Simvision output for Comparator

```
saturn.ece.iit.edu - PuTTY
    streams: 0, words: 0
worklib.cpu:vh <0x64411389>
    streams: 0, words: 0
worklib.stimulus:v <0x11362d78>
    streams: 13, words: 42067
worklib.DFFSR:v <0x5559ea95>
    streams: 0, words: 0
worklib.DFFNEGX1:v <0x3a46602b>
    streams: 0, words: 0
Building instance specific data structures.
Loading native compiled code: ..... Done
Design hierarchy summary:
      Instances Unique
Modules:          14744   34
UDRs:            1660    4
Primitives:       25753    6
Timing outputs:  14744   19
Registers:        1670   18
Scalar wires:     16634   -
Expanded wires:   47      5
Always blocks:    1       1
Initial blocks:   3       3
Pseudo assignments: 9      9
Timing checks:    9930  1659
Simulation timescale: 10ps
Writing initial simulation snapshot: worklib.BUFX4:v
Loading snapshot worklib.BUFX4:v ..... Done
xcelium> source /apps/cadence/XCELIUM1803/tools/xcelium/files/xmsimrc
xcelium> run
Simulation complete via $finish(1) at time 1001 NS + 0
./tb_test_comp.v:30 #1 $finish;
xcelium> exit
asriniv@saturn.ece.iit.edu:~%
```

Figure ddd: Logic Synthesis for comparator

```
* ****
encounter 1> reportGateCount -limit 0
Gate area 2.8158 um^2
[0] cpu Gates=16058 Cells=14810 Area=45216.1 um^2
encounter 2>
```

Figure eee: gate count report

timing.rep.5.final (~/Desktop/Project/comparator) - gedit

File Edit View Search Tools Documents Help

New Open Save Print... Undo Redo Cut Copy Paste Find Replace

timing.rep.5.final x

```
#####
# Generated by: Cadence Encounter 10.13-s292_1
# OS: Linux x86_64(Host ID saturn.ece.iit.edu)
# Generated on: Sun Dec 5 13:59:13 2021
# Design: cpu
# Command: report_timing -nworst 10 -net > timing.rep.5.final
#####
Path 1: MET Setup Check with Pin a/l3/rc31/qout_reg/CLK
Endpoint: a/l3/rc31/qout_reg/D (^) checked with leading edge of 'clk'
Beginpoint: m0pd/bb/mel/qout_reg/Q (v) triggered by leading edge of 'clk'
Other End Arrival Time 0.321
- Setup 2.924
+ Phase Shift 33.000
= Required Time 30.397
- Arrival Time 10.082
= Slack Time 20.315
Clock Rise Edge 0.000
+ Clock Network Latency (Prop) 0.322
= Beginpoint Arrival Time 0.322
+-----+
| Pin | Edge | Net | Cell | Delay | Arrival | Required |
|     |     |    |      |       | Time   | Time    |
+-----+
| m0pd/bb/mel/qout_reg/CLK | ^ | clk_L4_N11 | DFFPOSX1 | 0.243 | 0.322 | 20.637 |
| m0pd/bb/mel/qout_reg/Q | v | B[1] | AND2X1 | 0.156 | 0.565 | 20.880 |
| U2020/B | v | B[1] | AND2X1 | 0.136 | 0.721 | 21.036 |
| U2020/Y | v | a/l3/p1[1] | AND2X1 | 0.000 | 0.856 | 21.172 |
| U1370/B | v | a/l3/p1[1] | AND2X1 | 0.056 | 0.857 | 21.172 |
| U1370/Y | v | a/l3/f02/n3 | AND2X1 | 0.000 | 0.912 | 21.227 |
| U1371/A | v | a/l3/f02/n3 | INVX1 | 0.000 | 0.912 | 21.228 |
| U1371/Y | ^ | n747 | INVX1 | 0.004 | 0.916 | 21.232 |
| a/l3/f02/U3/C | ^ | n747 | OAI21X1 | 0.000 | 0.917 | 21.232 |
| a/l3/f02/U3/Y | v | a/l3/c0[1] | OAI21X1 | 0.126 | 1.042 | 21.358 |
| U1482/A | v | a/l3/c0[1] | INVX1 | 0.000 | 1.042 | 21.358 |
| U1482/Y | ^ | n2216 | INVX1 | 0.107 | 1.149 | 21.464 |
| a/l3/f03/U2/A | ^ | n2216 | XOR2X1 | 0.000 | 1.149 | 21.465 |
| a/l3/f03/U2/Y | v | a/l3/ps0[2] | XOR2X1 | 0.048 | 1.197 | 21.512 |
| U1018/A | v | a/l3/ps0[2] | AND2X1 | 0.000 | 1.197 | 21.512 |
+-----+
```

Ln 1, Col 1 INS

Figure fff: Timing final report

Here the maximum frequency can be found by adding the setup time and arrival time and use the formula $1/T$ to report the frequency. Here we have setup time 2.924 and arrival time is 10.082 so total time is $T = 13.006$ then the frequency is $1/T = 76.88$ Mhz.

timing.rep			
a/l3/f2011/U2/Y (XOR2X1)	0.06	5.21	r
a/l3/f2110/U5/Y (XNOR2X1)	0.07	5.28	r
a/l3/f2110/U2/Y (XOR2X1)	0.06	5.34	r
a/l3/f2110/U2/Y (XOR2X1)	0.06	5.40	r
U1428/Y (XOR2X1)	0.05	5.45	r
U1427/Y (XOR2X1)	0.07	5.52	r
a/l3/f2308/U5/Y (XNOR2X1)	0.06	5.59	r
a/l3/f2308/U2/Y (XOR2X1)	0.07	5.66	r
a/l3/f247/U5/Y (XNOR2X1)	0.06	5.72	r
a/l3/f247/U2/Y (XOR2X1)	0.07	5.79	r
a/l3/f256/U5/Y (XNOR2X1)	0.06	5.85	r
a/l3/f256/U2/Y (XOR2X1)	0.07	5.92	r
a/l3/f265/U5/Y (XNOR2X1)	0.06	5.98	r
a/l3/f265/U2/Y (XOR2X1)	0.07	6.06	r
a/l3/f274/U5/Y (XNOR2X1)	0.06	6.12	r
a/l3/f274/U2/Y (XOR2X1)	0.07	6.19	r
a/l3/f283/U5/Y (XNOR2X1)	0.06	6.25	r
a/l3/f283/U2/Y (XOR2X1)	0.07	6.32	r
a/l3/f292/U5/Y (XNOR2X1)	0.06	6.38	r
a/l3/f292/U2/Y (XOR2X1)	0.05	6.43	f
U1863/Y (AND2X1)	0.03	6.47	f
a/l3/rc31/qout_reg/D (DFFPOSX1)	0.00	6.47	f
data arrival time		6.47	
<hr/>			
clock clk (rise edge)	33.00	33.00	
clock network delay (ideal)	0.00	33.00	
a/l3/rc31/qout_reg/CLK (DFFPOSX1)	0.00	33.00	r
library setup time	-0.06	32.94	
data required time		32.94	
<hr/>			
data required time		32.94	
data arrival time		-6.47	
<hr/>			
slack (MET)		26.48	

Figure ggg: timing report

cell.rep (~/Desktop/Project/comparator) - gedit

File Edit View Search Tools Documents Help

New Open Save Print... Undo Redo Cut Copy Paste Find Replace

cell.rep x

```

o/tr/t4/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t5/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t6/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t7/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t8/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t9/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t10/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t11/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t12/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t13/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t14/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t15/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t16/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t17/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t18/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t19/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t20/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t21/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t22/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t23/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t24/b1 TBUFX2 gscl45nm 3.754400 n
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o/tr/t26/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t27/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t28/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t29/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t30/b1 TBUFX2 gscl45nm 3.754400 n
o/tr/t31/b1 TBUFX2 gscl45nm 3.754400 n
wb/bd/me0/qout_reg DFFP0SX1 gscl45nm 7.978100 n
wb/bd/me1/qout_reg DFFP0SX1 gscl45nm 7.978100 n
wb/bd/me2/qout_reg DFFP0SX1 gscl45nm 7.978100 n
wb/bd/me3/qout_reg DFFP0SX1 gscl45nm 7.978100 n
wb/bd/me4/qout_reg DFFP0SX1 gscl45nm 7.978100 n

```

Total 14727 cells 49485.806870
1

Ln 1, Col 1 INS

Figure hhh: Cell report

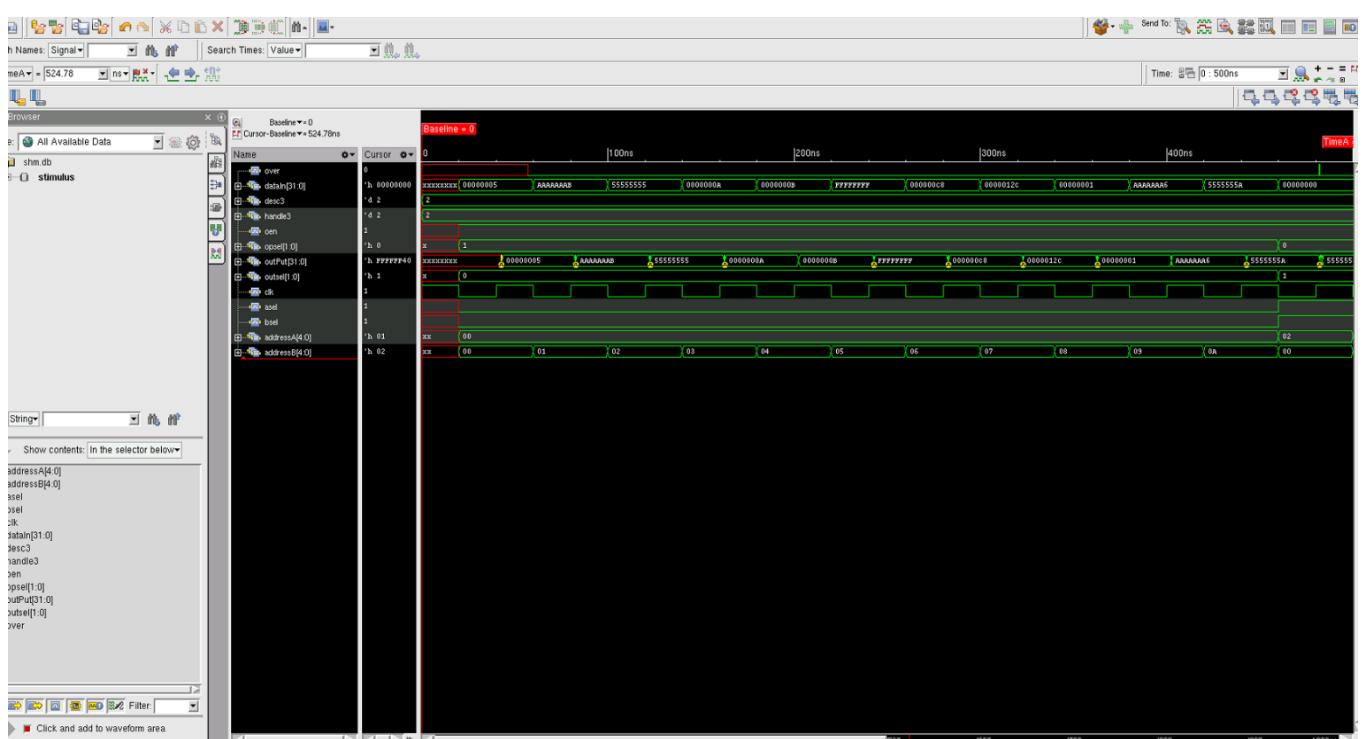


Figure iii: simvision after place and route

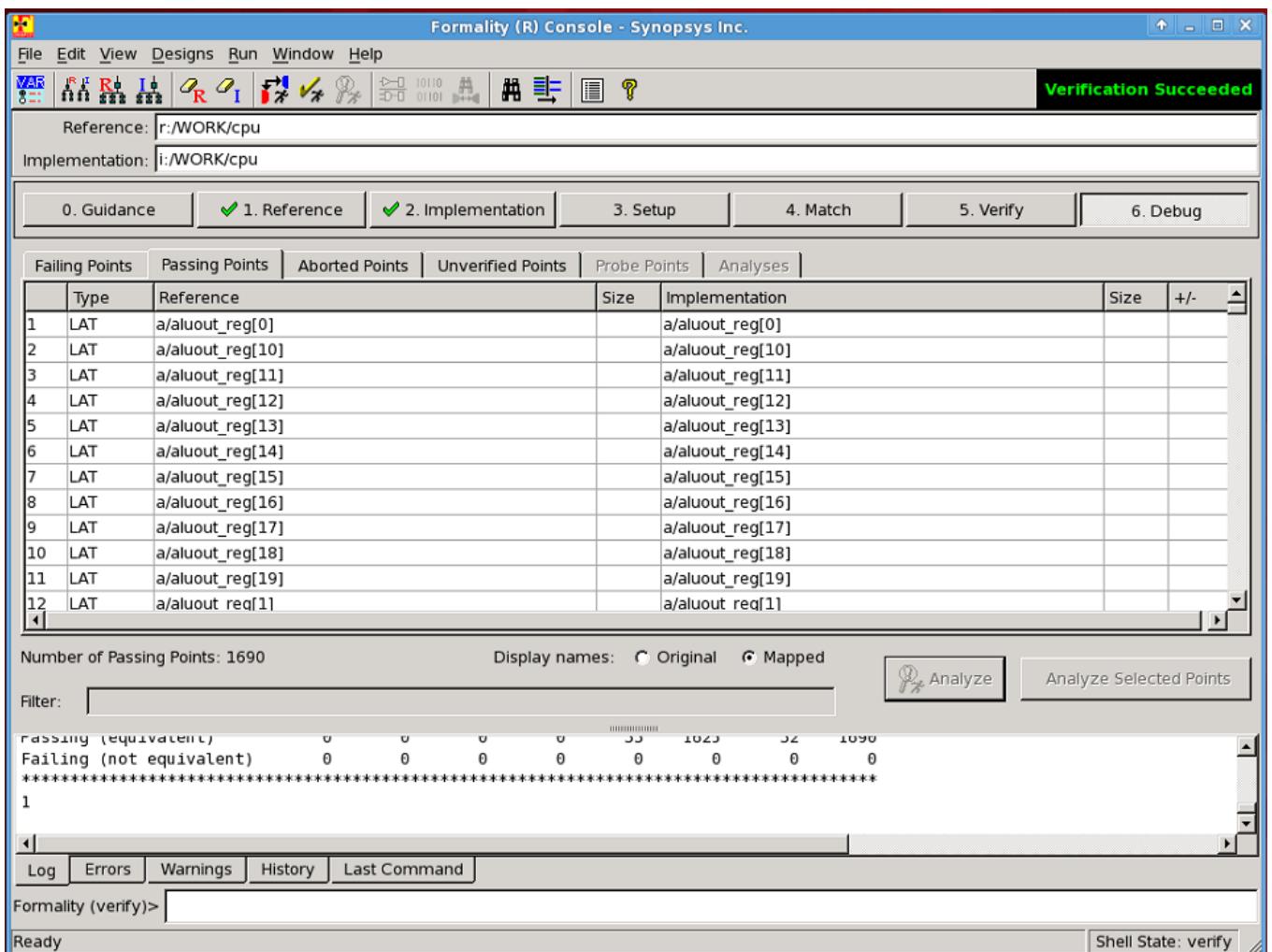


Figure jjj: Formal Verification

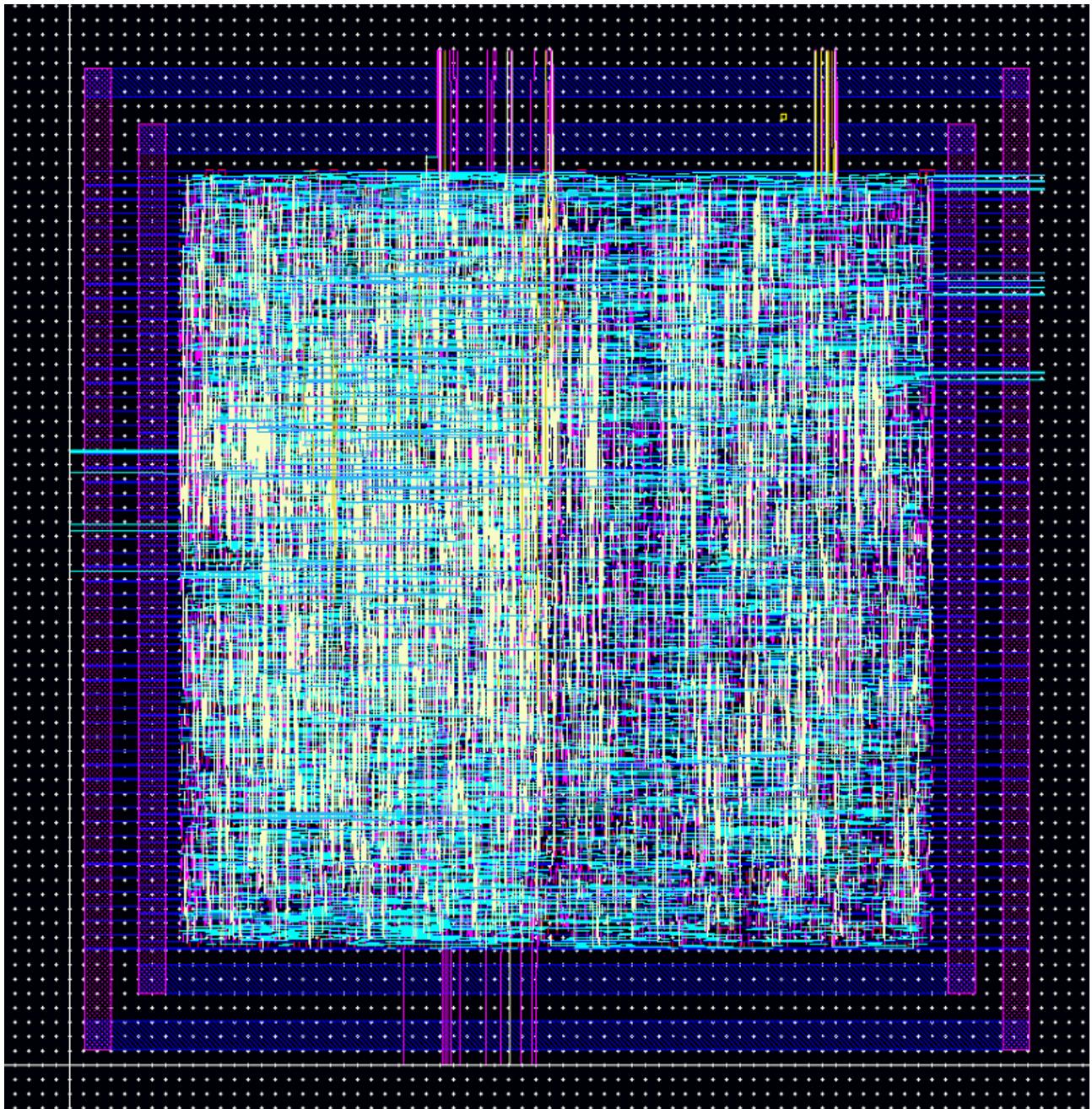


Figure kkk: Layout of comparator

CONCLUSION

Thus the overall CPU case studies were performed and the comparator is also synthesized based on ASIC flow.