NYU-ECE 6403 : Folded Cascode OTA Design

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Note: Zoom in to see the plots clearly

Contents

1 Introduction

Designing a CMOS OPAMP that achieves both a high DC gain and a high unity gain frequency presents a significant challenge. Traditionally, the design process involves manually calculating and evaluating equations derived from the behavioral characteristics of NMOS and PMOS transistors, followed by simulations using software like Cadence. Given the importance of high gain in the system, a Operational Transconductance Amplifier (OTA) topology has been selected for the design, as it offers several advantages over other alternatives. Numerous approaches exist for designing a two-stage operational amplifier, and the choice depends on the specific requirements and constraints of the application. In this design, a manual calculation approach has been employed.

The following document is organized into six sections, each addressing specific aspects of an OTA (Operational Transconductance Amplifier) design project. In Section 2, the OTA Specifications are thoroughly discussed, outlining the desired performance requirements and design constraints of the amplifier. Section 3 focuses on Hand Calculation, providing a step-by-step analysis and calculation of key parameters such as gain, bandwidth, and power consumption. Moving on to Section 4, Cadence Simulation, a detailed simulation using the Cadence software is performed to validate the hand calculations and evaluate the amplifier's performance under realistic conditions. Section 5 presents the Results obtained from the Cadence simulations, providing a comprehensive comparison and analysis of the data. Finally, in Section 6, the Conclusion summarizes the findings of the project and offers insights into potential improvements or further work that could be pursued.

2 OTA Specifications

The OTA specifications and the design parameters is as shown in table 1 and 2 respectively.

Table 1: OTA Design Specifications

Specification	**Value**
Gain	> 70 dB
ω_{3dB}	> 10 kHz
Slew Rate	> 30 V/μs
Phase Margin	$> 60^\circ$
Power Consumption	< 200 μW

Table 2: OTA Design Parameters

Parameter	**Value**
V_{DD}	1.2 V
C_L	2 pF

Also, we assume the ICMR for the design to be 0.6V

3 Hand Calculation

This section describes the Hand calculations for obtaining the intial values of W/L for all transistors. The OTA configuration is as shown in figure 1. M1 and M2 are the differential pair. M9 and M10 acts as current mirrors.

3.1 Determination of Process Parameters

Before going to the hand calculation we have to find the process parameters of the transistor models. The values are found in Assignment 3 and is as shown in tab 3

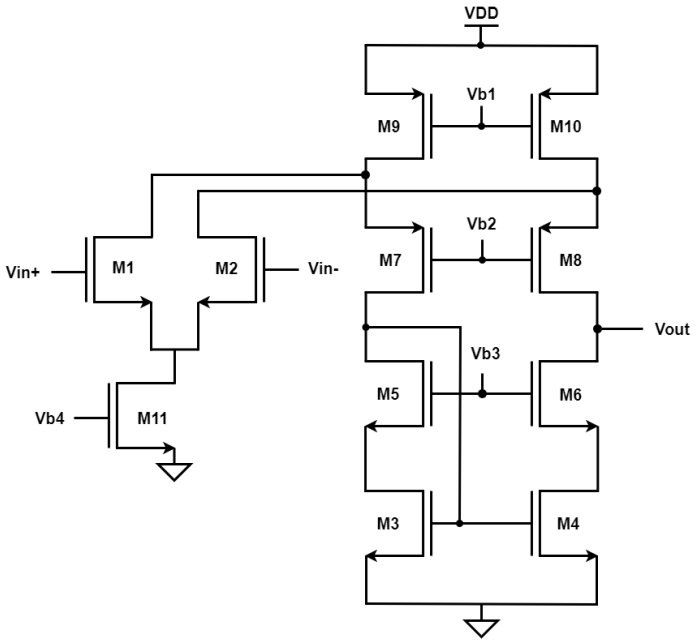

Figure 1: Cascode OTA Design

Table 3: Process parameters for NMOS and PMOS models

Parameter	**NMOS**	**PMOS**
V_{th}	0.322 V	0.302 V
μC_{ox}	265 $\mu A/V$	126 $\mu A/V$

3.2 Equations

The equations which can be used for the hand calculation is given in table 4

Table 4: Useful Equations

Parameter	**Equation**
g_m	$\frac{2I_D}{V_{ov}}$
A_v	$g_{m1}\left[(g_{m6}r_{o6}r_{04})\,//\,(g_{m8}r_{o8}\,(r_{o1}//r_{o10}))\right]$
Slew Rate	$\frac{I_D}{C_L}$
GBW	$\frac{g_{m1}}{C_L}$
W/L	$\frac{2I_D}{\mu C_{ox}V_{ov}^2}$

3.3 Folded Cascode Design

Consider current drawn from VDD is I_D. Therefore the current going through each of the transistors can be taken as $M_{9,10,11} = I_D/2$ and $M_{1-8} = I_D/4$.

Given the power should be less than $200\mu W$ therefore,

$$\begin{aligned} P = I_D \times V_{DD} &< 200\,\mu W \\ \implies I_D &< 167\,\mu A \end{aligned} \tag{1}$$

Also, Slew rate should be less than $30\,V/\mu s$,

$$\begin{aligned} SL = \frac{I_D}{C_L} &> 30\,\mu/V \\ \implies I_D &> 60\,\mu A \end{aligned} \tag{2}$$

From equation 2 & 1 we get,

$$60\,\mu A < I_D < 167\,\mu A \tag{3}$$

taking Gain as 70dB (≈ 3200) and BW as $2\pi 10 \times 10^3$, we get $GBW \approx 201 \times 10^6\ rad/s$. Using equation for GBW we get,

$$\begin{aligned} GBW = \frac{gm_1}{C_L} &> 198.69 \times 10^6 \\ \implies gm_1 &> 0.4\,mS \end{aligned} \tag{4}$$

$$\tag{5}$$

Taking $gm_1 = 7.5\,mS$ we get,

$$\begin{aligned} gm_1 = \frac{2V_{ov1}}{I_{D1}} &= 7.5\,mS \\ \implies V_{ov1} &= 0.01\,V \qquad (6) \\ \implies V_{GS1} = V_{ov1} + V_{thn} &= 0.332\,V \qquad (7) \end{aligned}$$

Choosing $I_D = 150\,\mu A$. We know,

$$|V_{ov10}| + |V_{ov8}| + V_{ov6} + V_{ov4} = 0.6\,V \tag{8}$$

Keeping in mind the V_{ov} for pmos should be higher than nmos and for the transistors carrying higher current. Therefore choosing $|V_{ov10}| = 0.3\,V$, $|V_{ov8}| = 0.15\,V$ and $V_{ov6} = V_{ov4} = 0.075\,V$

For calculating the ICMR (V_{cm}) value, we connect the output terminal to V_{in-} therefore,

$$V_{GS1} + V_{ov11} = 0.45\,V \implies V_{ov11} = 0.118V \tag{9}$$

Since we know the current going through each transistor and their V_{ov}, (W/L) can be easily found using equation in table 4.The calculated W/L values of each transistor is as shown in tab 5.

3.4 Finding values of bias voltages

Assuming all the transistos are working at the edge of saturation V_{b1}, V_{b2}, V_{b3} and V_{b4} is calculated as follows,

$$V_{b1} = V_{DD} - V_{thp} - V_{ov9} = 0.6\,V \tag{10}$$
$$V_{b2} = V_{DD} - V_{thp} - V_{ov9} - V_{ov7} = 0.45\,V \tag{11}$$
$$V_{b3} = V_{ov3} + V_{thn} + V_{ov5} = 0.47\,V \tag{12}$$
$$V_{b4} = V_{ov11} + V_{thn} = 0.44\,V \tag{13}$$
$$\tag{14}$$

3.5 Current Mirror Design

From the previous section, $V_{b4} = 0.44\,V$ and taking $Rb = 1M\Omega$ we get,

$$I_{D12} = \frac{V_{DD} - V_{b4}}{Rb} = 76\,\mu A \tag{15}$$

Also, we know $I_{D11} = I_D/2 = 75\,\mu A$. Since $V_{ov11} = V_{ov12}$ we get,

$$\left(\frac{W}{L}\right)_{12} = \frac{I_{D12}}{I_{D11}} \times \left(\frac{W}{L}\right)_{11} \tag{16}$$

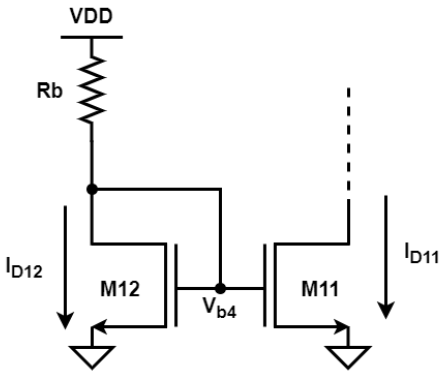

Figure 2: Current Mirror

Table 5 shows, the (W/L) of all transistors along with their choosen threshold voltage.

Table 5: Calculated values of (W/L) for $I_D = 150\,\mu A$

Transistor	$V_{ov}V$	**Current** μA	**W/L**
M1,M2	0.01	37.5	2830
M3,M4	0.075	37.5	50.3
M5,M6	0.075	37.5	50.3
M7,M8	0.15	37.5	26.5
M9,M10	0.3	75	6.5
M11	0.44	75	40.7
M12	0.44	7.6	4.1

4 Cadence Simulation

The circuit shown in 1 is drawn in Cadence along with the load capacitance and ideal voltage sources for biasing the transistors and is as shown in figure 3. Taking all lenght as $1\mu m$, the circuit is first simulated with the initial values of W/L given in table 5. Note that the output obtained using this initial values will be really different from what we expect. This is because the software uses more sophisticated (BSIM4) transistor models whereas the hand calculation uses simple transistor models.

First, we do Dc simulation for finding out the power, this is further discussed in Section 5.3. Starting with the initial values we obtained a power if less that 100 μW which is very much less than expected.Therefore we increase the current keeping the same V_{ov} and do the calculations discussed in the previous section to get the corresponding (W/L) ratio untill we get close to power margin. We found

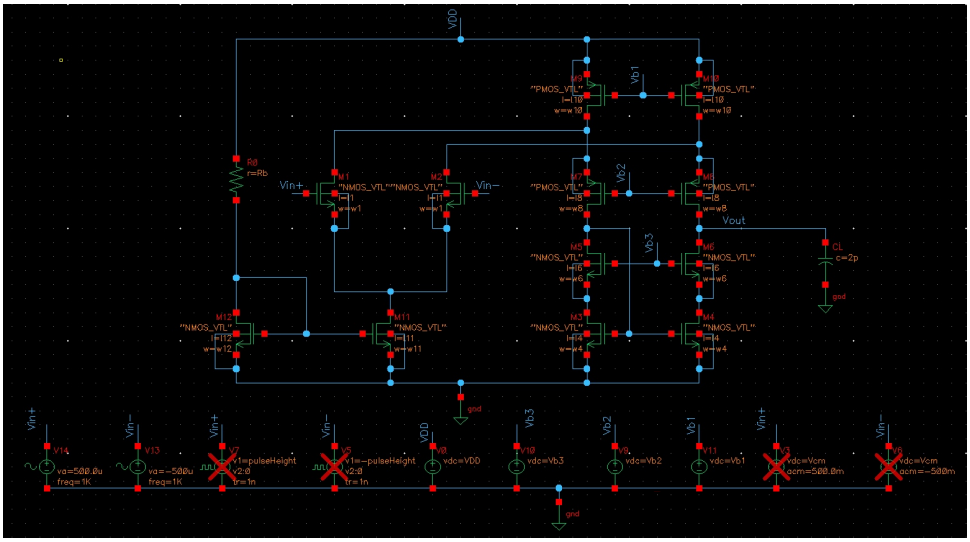

Figure 3: OTA Schematic in Cadence

that for a current of 200 μA we get a power of 196 μW. The corresponding values of W/L is as shown in table 6

Table 6: Calculated values of (W/L) for $I_D = 200\,\mu A$

Transistor	$V_{ov}V$	**Current** μA	**W/L**
M1,M2	0.01	50	3773
M3,M4	0.075	50	67
M5,M6	0.075	50	67
M7,M8	0.15	50	35.3
M9,M10	0.3	100	8.8
M11	0.44	100	54.1
M12	0.44	7.6	4.1

Now we do AC simulation to obtain the gain, bandwidth. We try changing the width of each transistor till we get the required specifications. Some of the points to keep in mind while changing the width is as below,

- By changing the width of W1 and W2 we can change the gain of the amplifier.
- W5-8 can be changed to change the gain as well as the bandwidth. Note that when we increase gain, bandwidth will reduce. We have to set a proper width such that we get both bandwidth and gain within the specifications.
- we can change the bias current by changing the width of M11, which in trun effect the slew rate.

Section 5 goes through the final results obtained. The final values of (W/L) obtained through iteration is as shown in table 7.

Table 7: Final values of (W/L)

Transistor	**W/L**
M1,M2	33
M3,M4	20
M5,M6	20
M7,M8	20
M9,M10	9
M11	33
M12	0.146

5 Results

This section shows the simulation results for the final W/L ratios given in table 7. The ADEL window for simulation is as shown in figure 4. In the output section the ADEL window we are plotting the bode plot, calculating the bandwidth (row 2), gain (row 3), phase margin (row 4) and power (row 6).

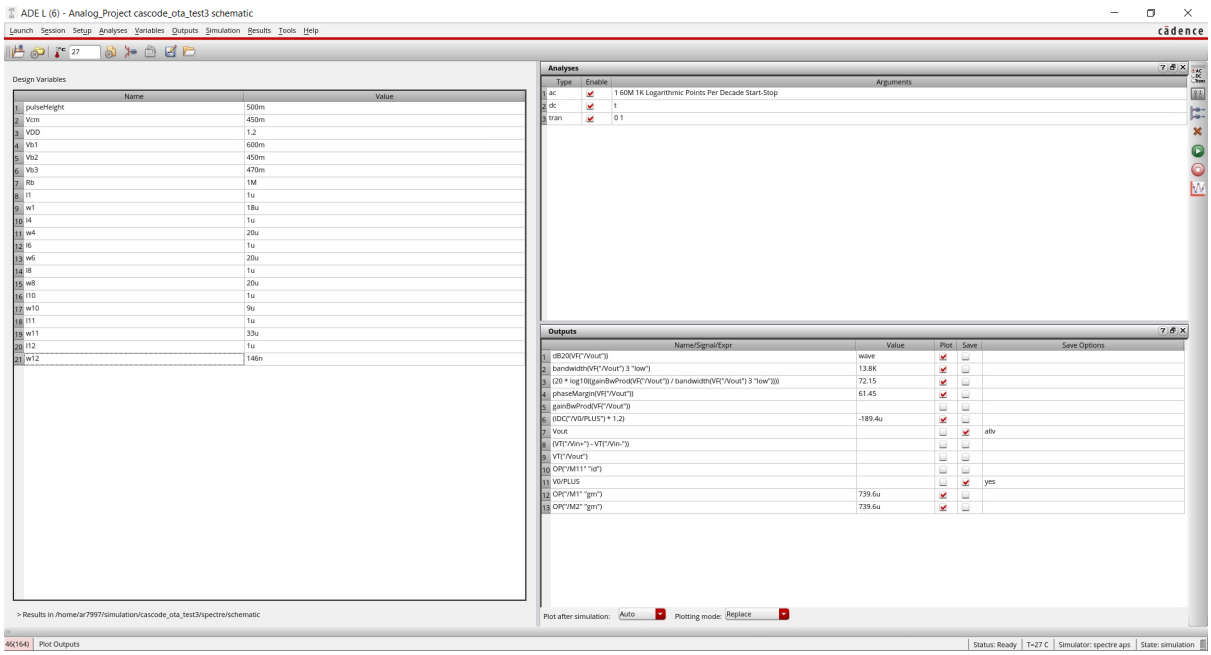

Figure 4: ADEL window after AC simulation

5.1 AC Simulations

The bode plot is as shown in figure 5.

5.1.1 OTA Gain

It is clear from figure 4 that we obtained a gain of 72.15dB, which is greated than required gain of 70dB

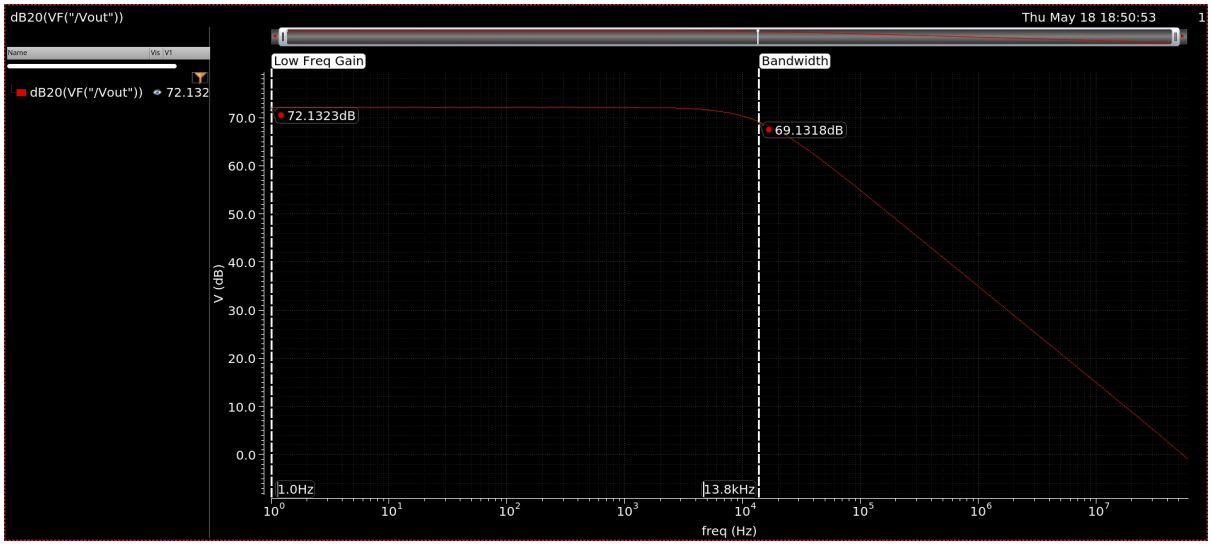

Figure 5: Bode plot showing low frequency gain of 72dB and 3dB bandwidth of 13.8kHz

5.1.2 3dB Bandwidth

The bandwidth is calculated using the function 'bandwidth'provided by the cadence calculator. It is clear from figure 4 that we obtained a 3dB bandwidth of 13.8kHz.

5.1.3 Phase Margin

The bandwidth is calculated using the function 'phaseMargin'provided by the cadence calculator. It is clear from figure 4 that we obtained a phase margin of 61.45^o.

5.2 Slew Rate

To calculate the slew rate we connect the negative input terminal to the output of the OTA and apply a pulse signal of 1V. We do transient simulation for the output and measure the slope when the output starts rising. The slope measurement is as shown in figure 6. It is clear that we obtained a slew rate greated than $30\,V\mu s$

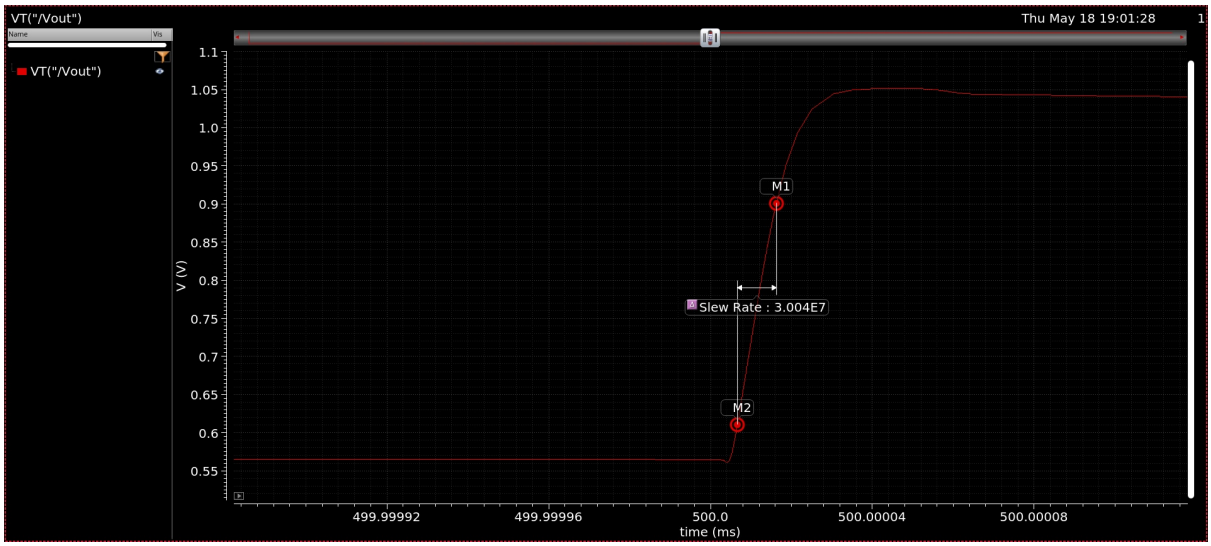

Figure 6: Slew rate calculation, slew rate is given by the slope of the rising edge.

5.3 Power Consumption

To measure the power consumed by the OTA we perform DC simulation. The power is given by the current drawn from VDD multiplied by VDD.The power output is as shown in figure 4. The power consumed is nearly equal to 189.4 μW which is less than the required value.

5.4 Noise Analysis

The input noise spectrum of the OTA is obtained using cadence and is as shown in figure 7 and noise summary obtained is as shown in figure 8. It is seen that the input differential pair contributes the most amount of the noise nearly 21.7%, which is as expected.

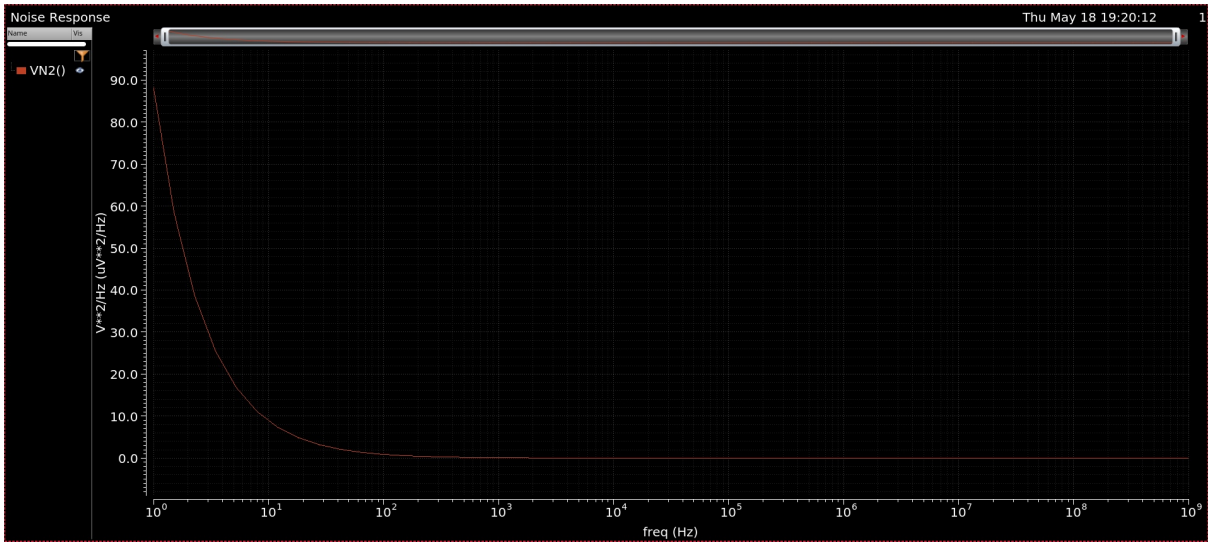

Figure 7: Input Noise Spectrum of the Designed OTA

Device	Param	Noise Contribution	% Of Total
/M1	fn	5.9113e-05	21.71
/M2	fn	5.9085e-05	21.70
/M9	fn	4.29603e-05	15.77
/M10	fn	4.29082e-05	15.76
/M4	fn	1.91867e-05	7.05
/M3	fn	1.91325e-05	7.03

Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Summarized Noise = 0.000272334
Total Input Referred Noise = 0.000164049
The above noise summary info is for noise data

Figure 8: Noise Summary of the designed OTA

5.5 Transient Simulation

Transient simulation is performed using 'vsin' from analogLib as the voltage source. The output is as shown in figure 9. Let us see if this matches with the gain we obtained through AC analysis,

$$Gain = \frac{V_{p-p,out}/2}{V_{in+}} = \frac{653.6/2}{0.1} = 3268 \text{ or } 70.2dB$$

Which is as expected.

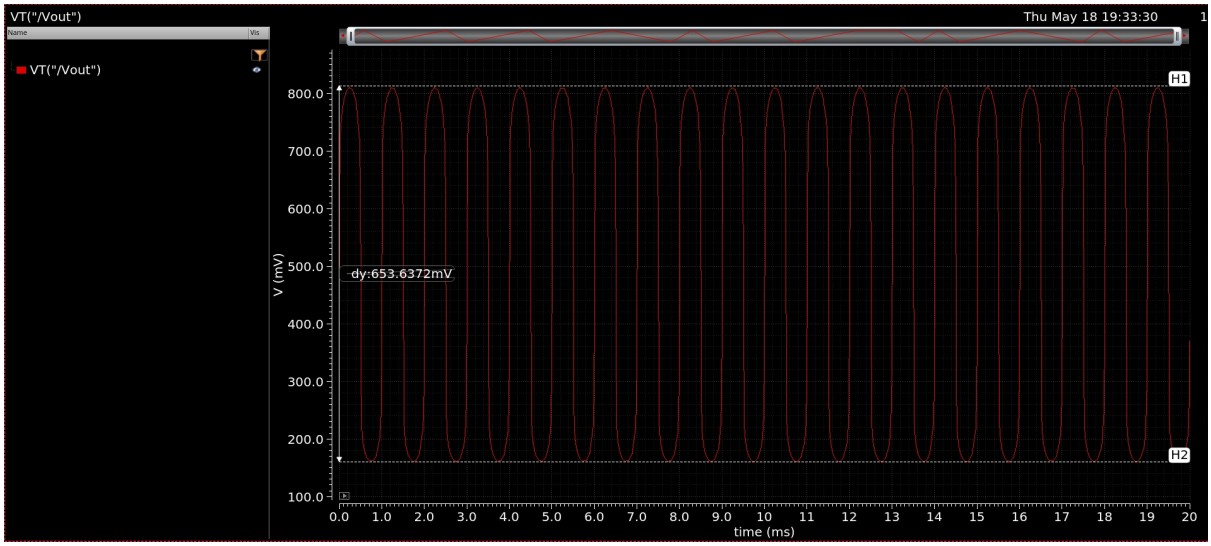

Figure 9: Output obtained for transient simulation with sin wave of frequency 1kHz

6 Conclusion

An overview of a general approach to design a folded cascode OTA has been described in this report. The procedure presented follows a pencil-and- paper method wherein the general equations obtained from behavioral characteristics of CMOS transistors are used to determine various design parameters of the transistor, to meet the prescribed system constraints. Necessary simulations and schematic diagrams implemented in Cadence have been added to the report. As for the future scope of the project optimized designs for lower power dissipation and higher gain bandwidth product can be obtained with fine tuning of the trade-offs involved in the design. The obtained specifications and given specifications are shown in table 8. It is clear that the designed Cascode OTA meets all the specifications.

Specification	**Given Value**	**Obtained Value**
Gain	$> 70dB$ dB	72.15dB
ω_{3dB}	$>$ 10 kHz	13.8kHz
Slew Rate	$>$ 30 V/μs	$\approx 30V/\mu s$
Phase Margin	$> 60°$	61.45°
Power Consumption	$<$ 200 μW	$189.4\mu W$

Table 8: Comparison b/w required and obtained value.