NYU-ECE 6403 : 2 Stage Amplifier Design

Aswin Raj K (N121801008, ar7997)

DEPARTMENT OF ELECTRICAL ENGINEERING

Note: Zoom in to see the plots clearly

Contents

1 Introduction

Designing a CMOS OPAMP that achieves both a high DC gain and a high unity gain frequency presents a significant challenge. Traditionally, the design process involves manually calculating and evaluating equations derived from the behavioral characteristics of NMOS and PMOS transistors, followed by simulations using software like Cadence. Given the importance of high gain in the system, a two-stage Operational Transconductance Amplifier (OTA) topology has been selected for the design, as it offers several advantages over other alternatives. Numerous approaches exist for designing a two-stage operational amplifier, and the choice depends on the specific requirements and constraints of the application. In this design, a manual calculation approach has been employed.

The following document is organized into six sections, each addressing specific aspects of an 2nd stage opf 2 stage Amplifier design project. In Section 2, the Amplifier Specifications are thoroughly discussed, outlining the desired performance requirements and design constraints of the amplifier. Section 3 focuses on Hand Calculation, providing a step-by-step analysis and calculation of key parameters such as gain, bandwidth, and power consumption. Moving on to Section 4, Cadence Simulation, a detailed simulation using the Cadence software is performed to validate the hand calculations and evaluate the amplifier's performance under realistic conditions. Section 5 presents the Results obtained from both the hand calculations and the Cadence simulations, providing a comprehensive comparison and analysis of the data. Finally, in Section 6, the Conclusion summarizes the findings of the project, highlights any challenges encountered, and offers insights into potential improvements or further work that could be pursued.

2 Amplifier Specifications

The two stage amplifier specifications and the design parameters is as shown in table 1 and 2 respectively.

Table 1: OTA Design Specifications

Specification	**Value**
Gain	> 90 dB
ω_{3dB}	> 2 kHz
Slew Rate	> 70 V/μs
Phase Margin	$> 60^\circ$
Power Consumption	< 300 μW
Unity Gain Frequency	85MHz

Table 2: OTA Design Parameters

Parameter	**Value**
V_{DD}	1.2 V
C_L	2 pF

Also, we assume the ICMR for the design to be 0.6V

3 Hand Calculation

This section describes the Hand calculations for obtaining the intial values of W/L for all transistors. The amplifier configuration is as shown in figure 1. For the second stage we use a common source amplifier. C_c is the compensation capacitor. M1 and M2 are the differential pair. M9 and M10 acts as current mirrors.

3.1 Determination of Process Parameters

Before going to the hand calculation we have to find the process parameters of the transistor models. The values are found in Assignment 3 and is as shown in tab 3

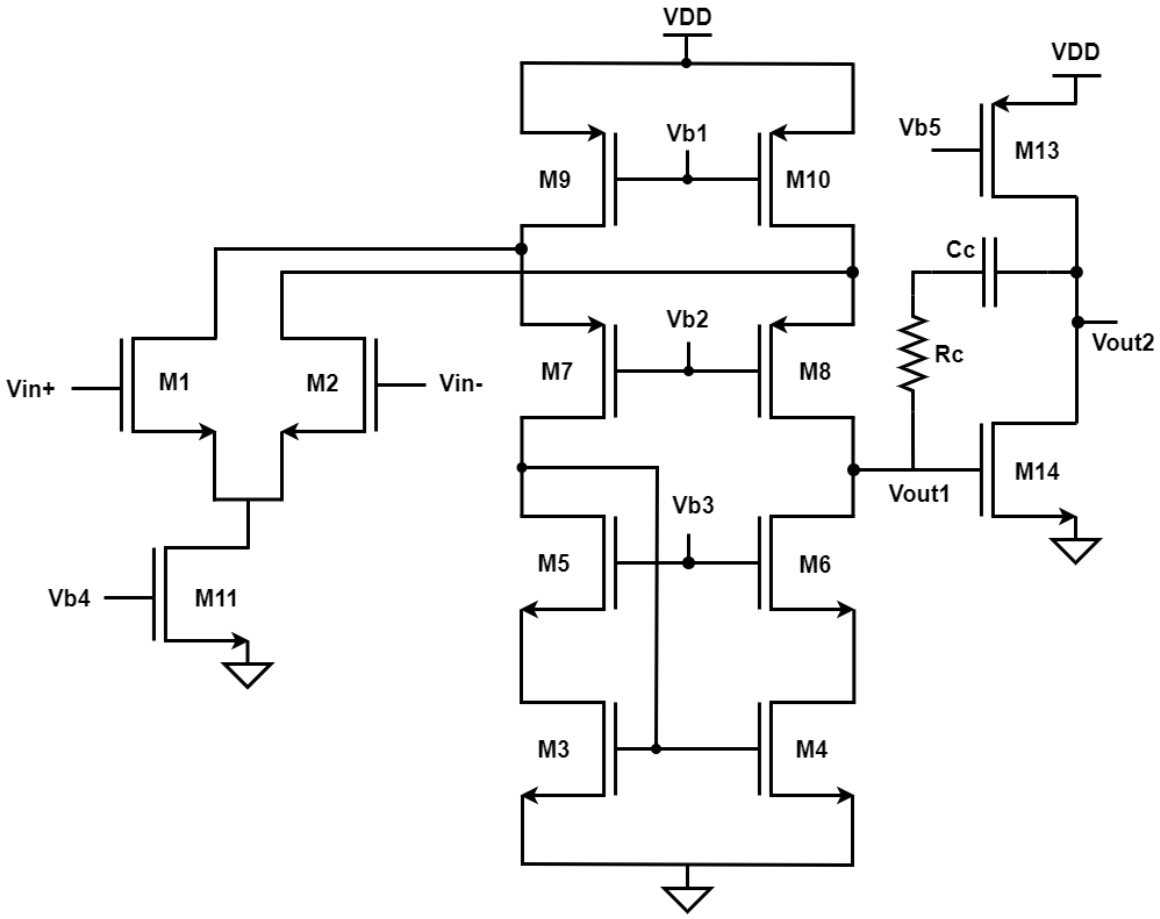

Figure 1: 2 Stage OTA Design

Table 3: Process parameters for NMOS and PMOS models

Parameter	**NMOS**	**PMOS**
V_{th}	0.322V	0.302V
μC_{ox}	$265\mu A/V$	126 $\mu A/V$

3.2 Equations

The equations, for this amplifier configuration, which can be used for the hand calculation is given in table 4

Table 4: Useful Equations

Parameter	**Equation**
Gain of stage 2, A_{v2}	$g_{m14} \times \frac{1}{g_{m13}}$
Slew Rate	$\frac{I_{D11}}{C_L}$ or $2\pi f_t V_{ov1}$
Unity gain frequency (f_t)	$\frac{g_{m1}}{2\pi C_C}$
Second Dominant Pole (f_{p2})	$\frac{g_{m14}}{2\pi C_L}$
Phase Margin	$90° - tan^{-1}\left(\frac{f_t}{f_{p2}}\right)$
Rc	$\frac{1}{g_{m14}}$

3.3 Second Stage Design

Before going towards hand calculation we need to find the values of g_{m1} for the previously designed OTA. This can be done using transient analysis and obtaining AC operating point of M1. The value of g_{m1} found is 739.6 μS. For the second stage we need a gain of 20dB (10 V/V). Therefore we get,

$$\begin{aligned} g_{m14} &> 10 g_{m13} \\ \implies V_{ov13} &> 10 V_{ov14} \end{aligned} \tag{1}$$

Also, Since we know the value of $V_{ov1} = 0.01\,V$ from previous part, writing equation for slew rate we get,

$$\begin{aligned} SR = 70\,V/\mu s &< 2\pi f_t V_{ov1} \\ \implies f_t &> 113.6\,MHz \end{aligned} \tag{2}$$

Now using the equation for the PM we get,

$$PM = 60° < 90° - tan^{-1}\left(\frac{f_t}{f_{p2}}\right)$$

$$\implies f_{p2} < 196\,MHz = \frac{g_{m14}}{2\pi C_L} \tag{3}$$

$$\implies g_{m14} > 2.5\,mS \tag{4}$$

Choosing g_{m14} as 3 mS and $V_{ov14} = 0.03\,V$ we get,

$$g_{m14} = \frac{2 \times I_{D14}}{V_{ov14}}$$

$$\implies I_{D14} = I_{D13} = 45\,\mu A \text{ and } V_{ov13} = 0.3\,V \tag{5}$$

Therefore, using equation of W/L we can easily calculate the value of $(W/L)_{13}$ and $(W/L)_{14}$. Which is found to be 8 and 377 respectively. Now using the equation of f_t and R_c we can find the value of C_c and R_c, which is found to be approximately 1 pF and 330 Ω respectively. The calculated values are summarized in table 5

Table 5: Calculated Values

Parameter	**Value**
$(W/L)_{13}$	8
$(W/L)_{14}$	377
C_c	1 pF
R_c	330 Ω

4 Cadence Simulation

The circuit shown in 1 is drawn in Cadence along with the load capacitance and ideal voltage sources for biasing the transistors and is as shown in figure 2. Taking all length as $1\mu m$, the circuit is first simulated with the initial values of W/L given in table 5. Note that the output obtained using this initial values will be really different from what we expect. This is because the software uses more sophisticated (BSIM4) transistor models whereas the hand calculation uses simple transistor models.

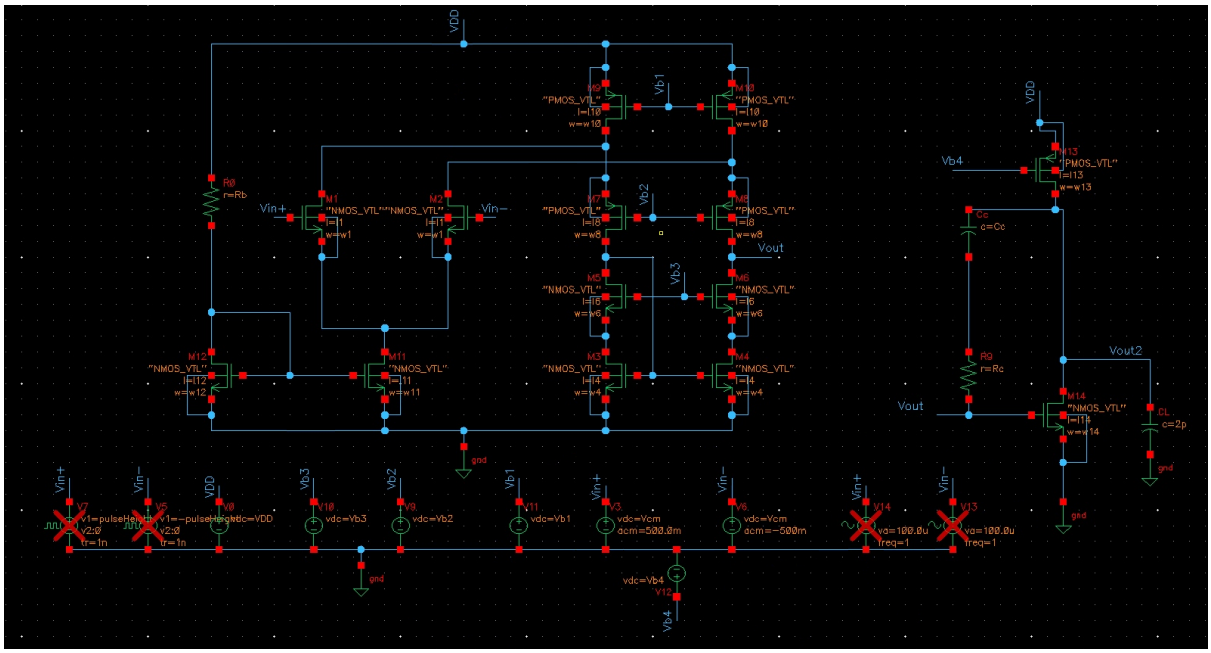

Figure 2: 2 Stage Amplifier Schematic in Cadence

Now we do AC simulation to obtain the gain, bandwidth. We try changing the width and the value of C_c of the second stage transistor till we get the required specifications. Some of the points to keep in mind while changing the width is as below,

- Rather than increasing the compensation capacitor C_C, the value of the series resistor R_C can be increased to improve the phase margin PM: For a given CC, increasing R above places the transmission zero at a negative real-axis location , where the phase it introduces adds to the phase margin. Thus, PM can be improved without affecting f_t.
- Increasing the PM is desirable because it reduces the overshoot in the step response of the op amp.

- Gain of the second stage can be increased by changing the width of M13.

Section 5 goes through the final results obtained. The final values of (W/L) obtained through iteration is as shown in table 6. We note that these values are reasonably close to those predicted by hand analysis.

Table 6: Final Parameters

Transistor	Value
M14	45
M13	8
C_c	500 fF
R_c	330 Ω

5 Results

This section shows the simulation results for the final W/L ratios given in table **??**. The ADEL window for simulation is as shown in figure 3. In the output section the ADEL window we are plotting the bode plot, calculating the bandwidth (row 2), gain (row 3), phase margin (row 4), Unity gain frequency (row 5) and power (row 7).

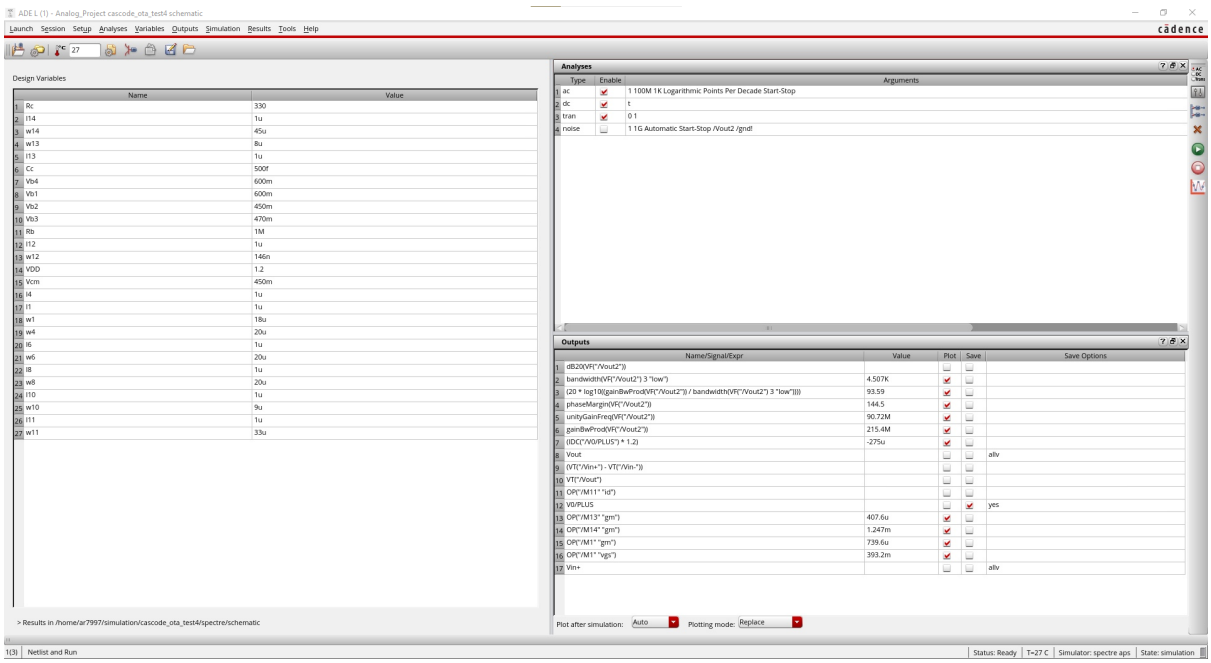

Figure 3: ADEL window after AC simulation

5.1 AC Simulations

The bode plot is as shown in figure 4.

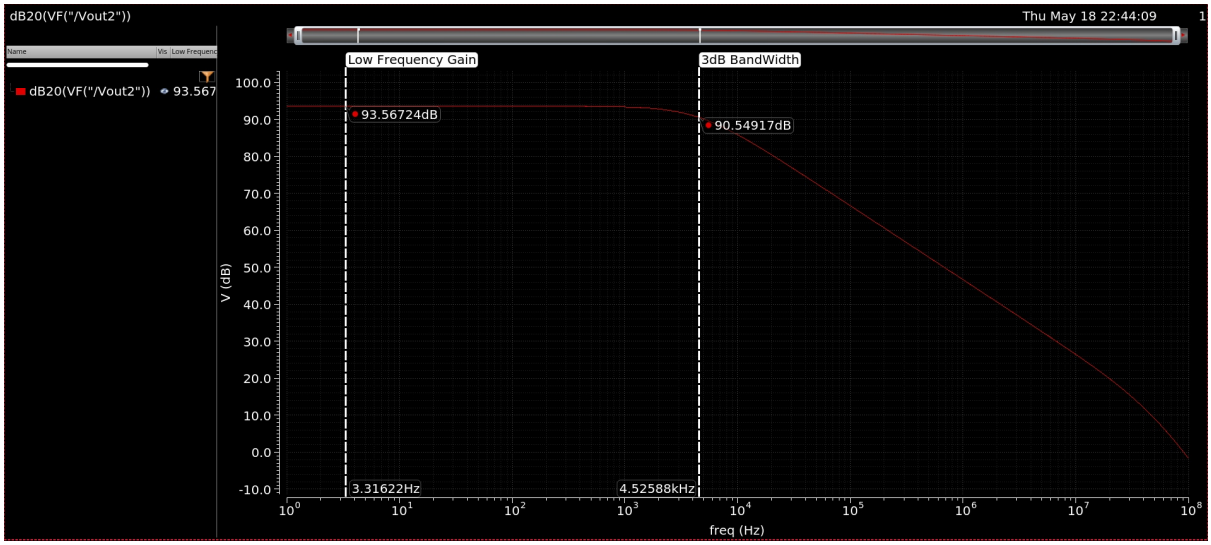

Figure 4: Bode plot showing low frequency gain of 93.5dB and 3dB bandwidth of 4.5kHz

5.1.1 Amplifier Gain

It is clear from figure 3 that we obtained a gain of 93.59dB, which is greater than required gain of 90dB

5.1.2 3dB Bandwidth

The bandwidth is calculated using the function 'bandwidth'provided by the cadence calculator. It is clear from figure 3 that we obtained a 3dB bandwidth of 4.5kHz.

5.1.3 Phase Margin

The bandwidth is calculated using the function 'phaseMargin'provided by the cadence calculator. It is clear from figure 3 that we obtained a phase margin of 144.5^o.

5.2 Slew Rate

To calculate the slew rate we connect the negative input terminal to the output of the OTA and apply a pulse signal of 1V. We do transient simulation for the output and measure the slope when the output starts rising. The slope measurement is as shown in figure 5. It is clear that we obtained a slew rate of $62.57\,V\mu s$

5.3 Power Consumption

To measure the power consumed by the Amplifier we perform DC simulation. The power is given by the current drawn from VDD multiplied by VDD.The power output is as shown in figure 3. The power consumed is nearly equal to $275.4\,\mu W$ which is less than the required value.

5.4 Noise Analysis

The input noise spectrum of the OTA is obtained using cadence and is as shown in figure 6 and noise summary obtained is as shown in figure 7. It is seen that the input differential pair contributes the most amount of the noise nearly 24.07%, which is as expected.

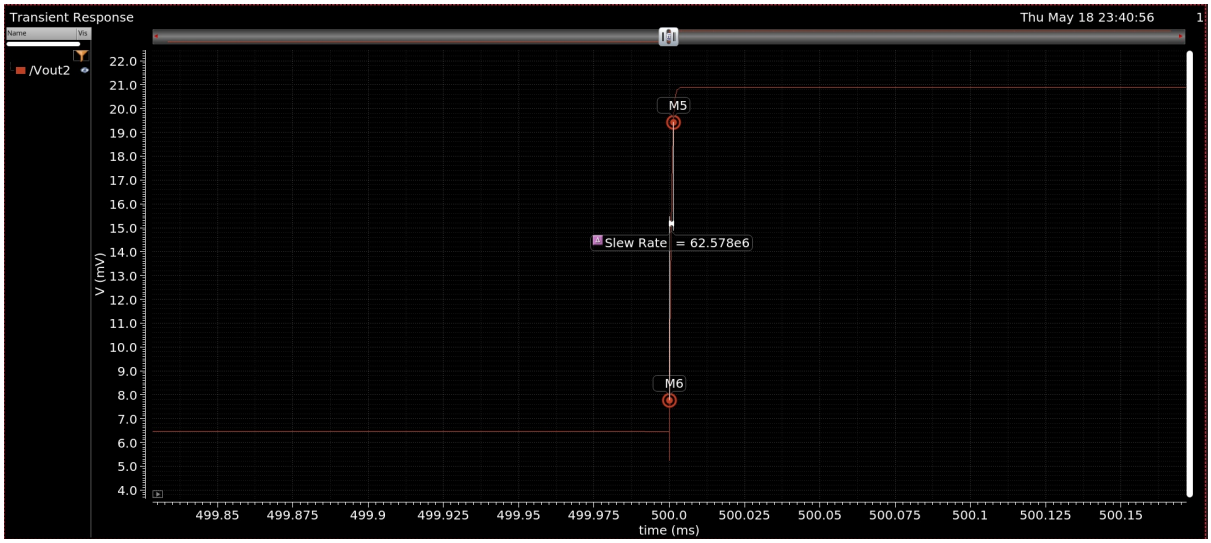

Figure 5: Slew rate calculation, slew rate is given by the slope of the rising edge.

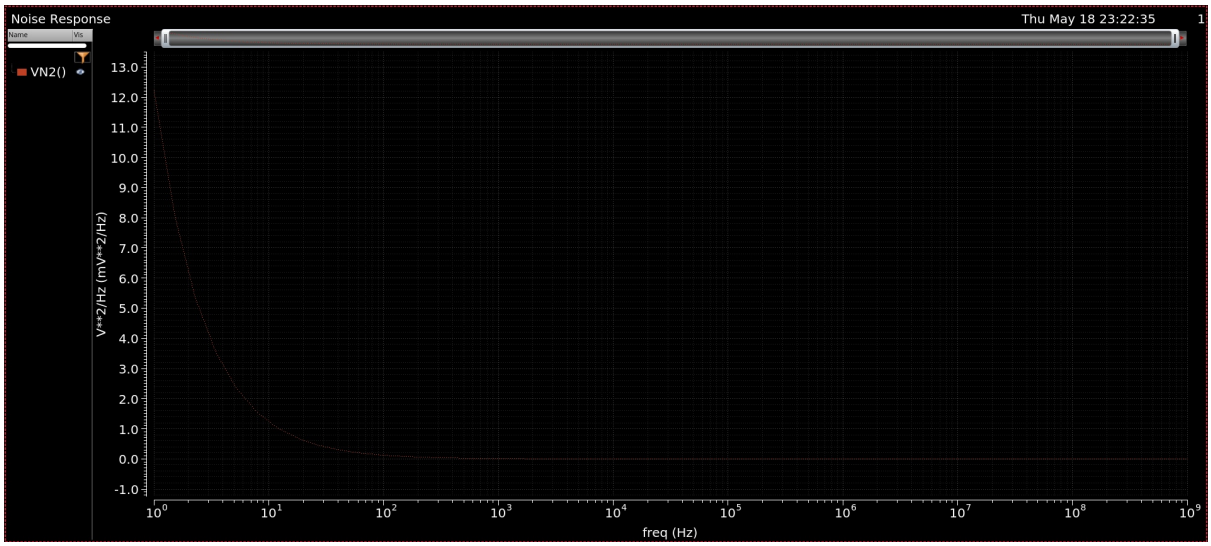

Figure 6: Input Noise Spectrum of the Designed OTA

Device	Param	Noise Contribution	% Of Total
/M2	fn	0.0260593	24.07
/M1	fn	0.0260184	24.03
/M10	fn	0.0189506	17.50
/M9	fn	0.0188859	17.44
/M4	fn	0.00843934	7.79
/M3	fn	0.00841086	7.77

Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Summarized Noise = 0.108276
Total Input Referred Noise = 0.000437283
The above noise summary info is for noise data

Figure 7: Noise Summary of the designed OTA

5.5 Transient Simulation

Transient simulation is performed using 'vsin' from analogLib as the voltage source. The output is as shown in figure 8. Let us see if this matches with the gain we obtained through AC analysis,

$$Gain = \frac{V_{p-p,out}/2}{V_{in+}} = \frac{1.15}{0.05} = 23000 \text{ or } 87.23dB \text{ at 1kHz Frequency}$$

Which is as expected.

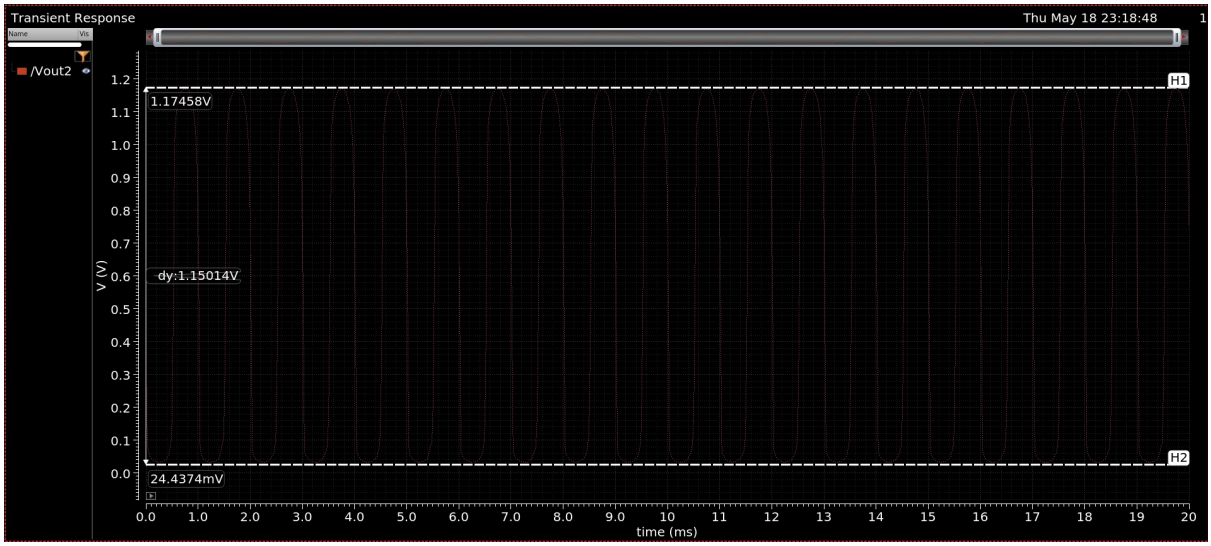

Figure 8: Output obtained for transient simulation with sin wave of frequency 1kHz

6 Conclusion

An overview of a general approach to design a 2 stage amplifier has been described in this report. The procedure presented follows a pencil-and- paper method wherein the general equations obtained from behavioral characteristics of CMOS transistors are used to determine various design parameters of the transistor, to meet the prescribed system constraints. Necessary simulations and schematic diagrams implemented in Cadence have been added to the report. As for the future scope of the project optimized designs for lower power dissipation and higher gain bandwidth product can be obtained with fine tuning of the trade-offs involved in the design. The obtained specifications and given specifications are shown in table 7. It is clear that the designed Amplifier meets all the specifications (except Slew rate).

Specification	**Given Value**	**Obtained Value**
Gain	$> 90dB$ dB	93.59dB
ω_{3dB}	$>$ 2 kHz	4.5kHz
Slew Rate	$>$ 70 V/μs	$\approx 62.5V/\mu s$
Phase Margin	$> 60°$	144.5°
Power Consumption	$<$ 300 μW	$275\mu W$
Unity gain frequency	$> 85MHz$	$90.72MHz$

Table 7: Comparison b/w required and obtained value.