Indian Institute of Technology Palakkad
भारतीय प्रौद्योगिकी संस्थान पालक्काड
Under Ministry of Human Resource Development, Govt. of India
मानव संसाधन विकास मंत्रालय के अधीन, भारत सरकार

BTP Phase 1 Project Progress

Electrical Engineering

IIT Palakkad

January 19, 2022

Developing a Radar Signal Processor for the Detection of Drones

Mentors: Dr. Swaroop Sahoo & Dr. Subrahmanyam Mula

Name	: Aswin Raj K
Roll Number	: 121801008
Department	: Electrical Engineering

Developing a Radar Signal Processor for the Detection of Drones

Objectives Overview

Project Objectives Overview

1. **Simulating the radar using Matlab.**
   - Before implementing the radar onto an actual FPGA, we need to find the right parameters to ensure it is working as expected.
   - A matlab simulation of the radar model is done to finalize the required parameters which meets our need.
2. **Implementing the transmitter on the FPGA.**
   - Chirp signal generator is to be implemented on the FPGA in digital domain.
   - This generated digital signal needs to be sent to the SDR for transmitting it through the antenna.
3. **Ensuring that the chirp pulses transmitted from the FPGA is as expected.**
   - This can be done using another receiver and observing the transmitted signal transmitted from the FPGA.
4. **Implementing the receiver on the FPGA.**
   - Storing the echo data received by the SDR onto the memory block of FPGA.
   - Processing the digitized data on the FPGA itself.
   - Blocks for Hamming window, 3 pulse canceler, Matched filtering, Threshold detection, and FFT is to be designed for processing the data.
5. **Exporting the processed data for visualization.**
   - Export the final processed data from the FPGA to matlab for easy visualization.
   - Plotting the result in matlab to ensure that the radar is working as expected.

Completed and Incompleted Objectives

Completed	Incompleted
Matlab simulation of pulse doppler radar.	Blocks for 3 pulse canceler and matched filtering.
FFT Implementation.	Chirp signal generation in the digital domain.
Hamming Window implementation.	SDR configuration.
Integration of the Data matrix, Hamming window and FFT block.	PRF staggering and detection using CFAR.