



Indian Institute of Technology Palakkad

भारतीय प्रौद्योगिकी संस्थान पालक्काड

Under Ministry of Human Resource Development, Govt. of India
मानव संसाधन विकास मंत्रालय के अधीन, भारत सरकार

BTP Mid Term Report

Electrical Engineering

IIT Palakkad

October 11, 2021

Developing a Radar Signal Processor for the Detection of Drones

Mentors: Dr. Swaroop Sahoo & Dr. Subrahmanyam Mula

Name : Aswin Raj K
Roll Number : 121801008
Department : Electrical Engineering

Developing a Radar Signal Processor for the Detection of Drones

Abstract

In this report, the work done as a part of developing the radar signal processor for the detection of drones is discussed. The signal processing part is designed to be implemented on an FPGA (ZC702^[2]) board. It is designed to produce pulses with monotonous frequency as well as chirp^[1]. The required RF pulse is generated at baseband that will be upconverted to X-band on the SDR^[3] and is transmitted out. The signal transmitted is scattered and received by the radar. The FPGA is also programmed to store the sampled data coming from the SDR in the form of a data matrix. The data stored in the data matrix is used to extract the doppler^[1] and range information. Before its implementation onto an actual FPGA board the radar is simulated using Matlab to find the best parameters required for the radar to operate. The Matlab implementation of the radar is clearly explained in the report.

1 Introduction

Radars are an important component of any aerospace surveillance system. The working of radar is essentially based on the electromagnetic principle of backscattering at radio frequencies, which occurs when an object is illuminated by the radar beam. This approach works very well when dealing with large drones made of metal pieces, carbon fiber, and composite material. The main difficulty arises when the size of the drones to be detected is small, where the probability of detection is reduced because of the smaller radar cross-section of drone made of plastic or styrofoam. The detection of such drones is possible only if the signal processing system is sensitive enough to smaller changes produced by such targets. Thus, designing sensitive signal processors and post-processing algorithms is very important for the detection of such drones. These processors and algorithms should not give a false alarm for birds and clutter. Considering these the signal processors and algorithms have to be designed for detecting the changes due to the micro-Doppler effect.

The first step in designing the radar system is determining the pulse width and pulse repetition frequency (PRF) of the pulse to be transmitted. The next step is that pulse width determines the resolution of the radar while pulse repetition frequency determines the range of detection. The resolution of radar is its ability to distinguish between targets that are in very close proximity. It is given by the equation

$$\rho = \frac{cT}{2} \quad (1)$$

where c is the speed of light and T is the pulse width.

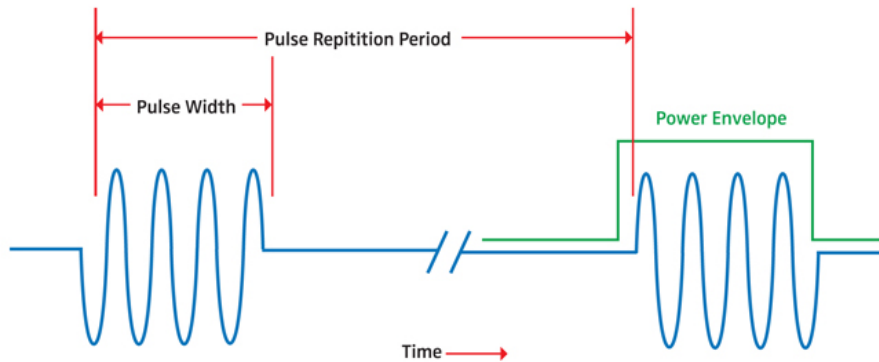


Figure 1: Normal pulse

The radar sends RF pulses at regular intervals and these pulses get reflected by the target. After transmitting the pulse, the radar switches to a listening mode where it listens for the reflected signal

from the target. The radar will down-convert the received signal to baseband, sample it and store the IQ data in the form of a data matrix. Each row in the data matrix corresponds to radar returns from each pulse and each column corresponds to the sampled data (or Range Bin). A 4×10 Data Matrix is as shown in figure 2.

In figure 2 the orange and green bin refers to two different targets. From figure 2 it is clear that the orange target lies in the same range bin for each pulse interval whereas the green target is changing the range bin which indicates that the later is moving whereas the former one is stationary. Each range bin corresponds to a particular distance from the radar which depends on the sampling frequency of the received pulses. If the magnitude of the sampled data goes above a particular threshold we can conclude that the target is located at that range from the radar which corresponds to that particular range bin. Thus we can easily calculate the range information of the target from the data matrix and now to get the velocity of the target we calculate the doppler shift using fast fourier transform. We take FFT along the slow time samples so that we can get the frequencies corresponding to every range bin. The newly created matrix after taking FFT is as shown below in figure 3.

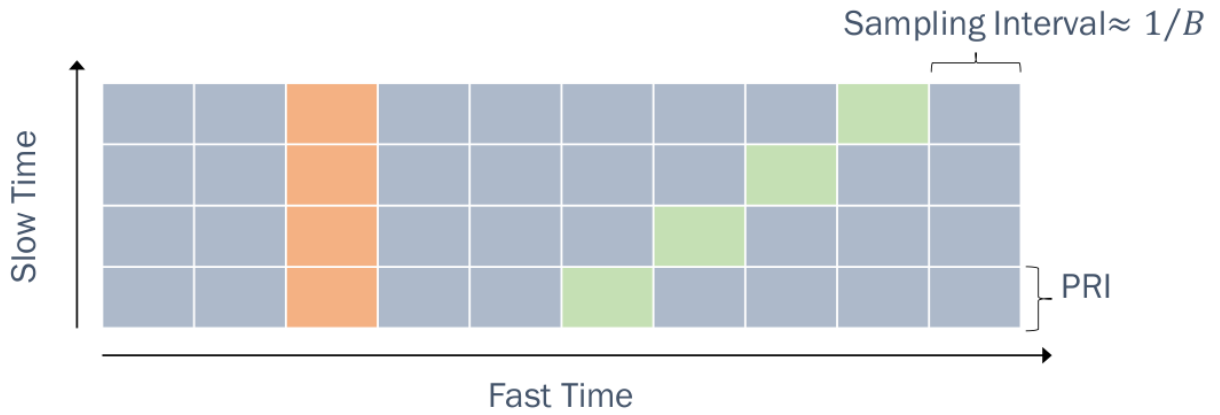


Figure 2: Data matrix with fast time samples along the row and slow time samples along the columns.

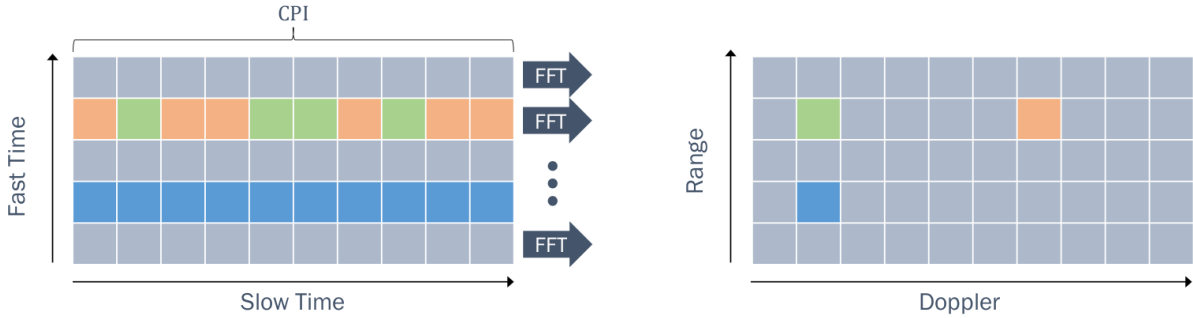


Figure 3: Taking FFT along Slow Time samples to produce another matrix which has both Range and Doppler Information

Project Objectives

- ① **Simulating the radar using Matlab.**
 - Before implementing the radar onto an actual FPGA, we need to find the right parameters to ensure it is working as expected.
 - A matlab simulation of the radar model is done to finalize the required parameters which meets our need.
- ② **Implementing the transmitter on the FPGA.**
 - Chirp signal generator is to be implemented on the FPGA in digital domain.
 - This generated digital signal needs to be sent to the SDR for transmitting it through the antenna.
- ③ **Ensuring that the chirp pulses transmitted from the FPGA is as expected.**
 - This can be done using another receiver and observing the transmitted signal transmitted from the FPGA.
- ④ **Implementing the receiver on the FPGA.**
 - Storing the echo data received by the SDR onto the memory block of FPGA.
 - Processing the digitized data on the FPGA itself.
 - Blocks for Hamming window, 3 pulse canceler, Matched filtering, Threshold detection, and FFT is to be designed for processing the data.
- ⑤ **Exporting the processed data for visualization.**
 - Export the final processed data from the FPGA to matlab for easy visualization.
 - Plotting the result in matlab to ensure that the radar is working as expected.

Objective 1 is completed in this till now and some part of Objective 2 & 3 is also completed as the part of OELP the previous semester. Slight changes need to be made to the work done during the OELP. Section 2 describes how the radar is simulated in Matlab to ensure its feasibility before implementing onto an actual FPGA board.

2 Matlab Simulation

The entire radar is first simulated using matlab. Matlab simulation can be split into mainly two parts which are,

- Creating the received echo signal with some targets positioned at a particular range and velocity relative to the radar.
- Extraction of the target range and velocity from this unprocessed (echo) data.

2.1 Creating the test data

Sample data is created using matlab. Chirp signal is used as the pulse. The equation for generating a chirp signal is given below,

$$S(t) = e^{j\pi\omega \left(nT_s - \frac{Tf_s - 1}{2f_s} \right)} \quad (2)$$

where T is the pulse width, f_s is the sampling frequency.

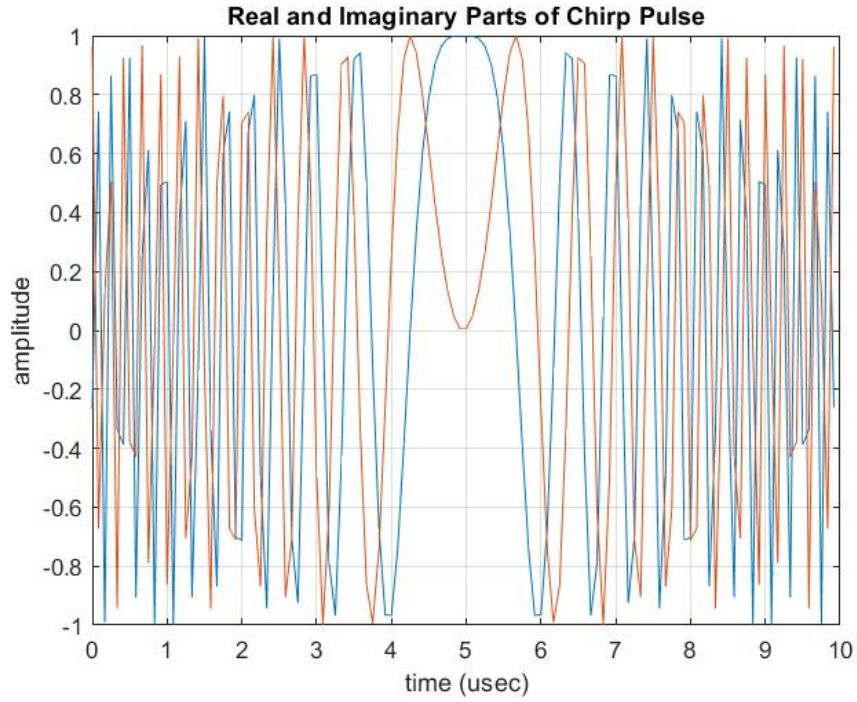


Figure 4: Chirp signal to be used

The pulse parameters used is as follows,

- $T = 10\mu s$ (Pulse Width)
- $PRF = 25 \text{ kHz}$
- $PRI = 40\mu s$
- R.F Frequency = 10 GHz
- $R_{min} = 1.8\text{km}$ & $R_{max} = 5.7\text{km}$
- Unambiguous Range = 3.9 km
- Unambiguous Velocity = 375 m/s

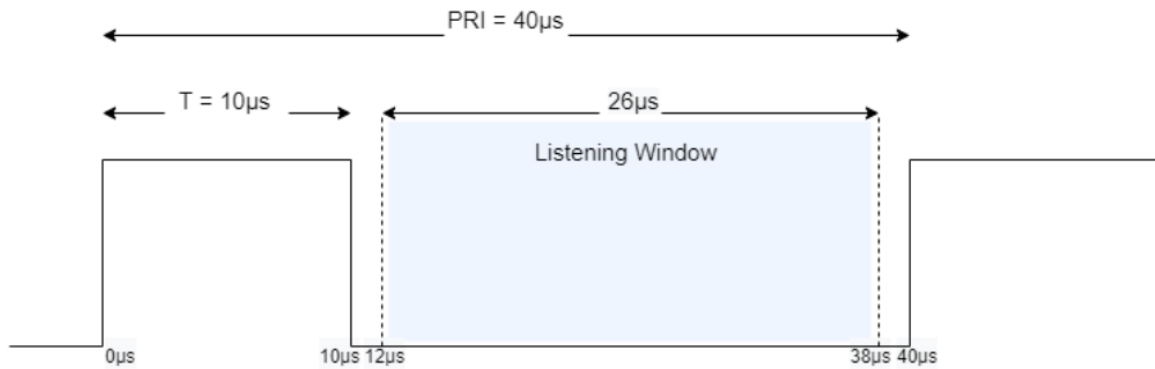


Figure 5: Pulse used for simulation

Also 4 targets were specified with position and velocity as given in the table 1. The echo signal is calculated depending on the position and velocity of the target.

| Target No | Range (km) | SNR (dB) | Velocity (m/s) |
|-----------|------------|----------|----------------|
| 1 | 2.3 | 10 | -112.5 |
| 2 | 2.7 | 20 | -56.5 |
| 3 | 3.1 | 10 | 37.5 |
| 4 | 3.1 | 20 | 93.75 |

Table 1: Targets Specified

After adding the target information onto the echo signal Gaussian noise and clutter is added to the signal. The signal is then sampled at the desired sampling frequency of 12MHz. A total of 40 pulses and its received echo is simulated. The received echo for a period of $26\mu\text{s}$ has a total of 313 samples. Since 40 pulses are used we will have a total of 313×40 samples. These samples can be represented in the form of a data matrix of size 40×313 with slow time samples along the columns and fast time samples along the rows.

2.2 Processing the test data

The test data is now processed to extract the position and velocity of the target. The signal at each stage is plotted for clarity.

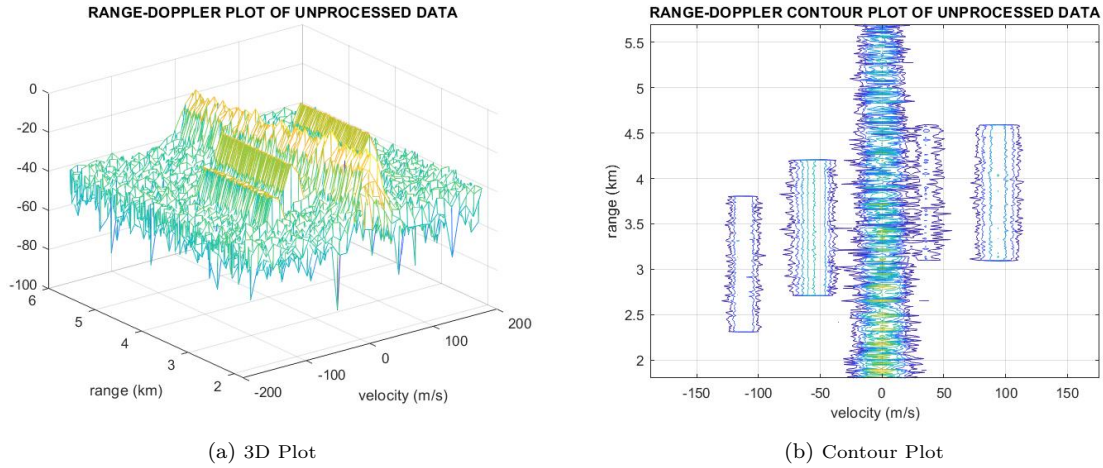


Figure 6: Range and contour plot of unprocessed data

It is clear from figure 6 that there is clutter^[4] (with velocity = 0) and noise present in the echoes. Several signal processing techniques are employed to get rid of the clutter^[4] and noise to extract the target information.

Looking at the figure 7 it is clear that the clutter^[4] is successfully removed but it adds up high frequency noise. Now to remove the noise, matched filtering^[1] in range is employed. Matched filtering^[1] can significantly improve the SNR ratio. The figure 8 shows the data after matched filtering. Looking at figure 8b it is seen that the noise is significantly reduced and the peaks are clearly seen which represents the target. There is a total of 4 peaks which represents the 4 target. The velocity and position of the target is obtained from the data and is tabulated in the table 2 below,

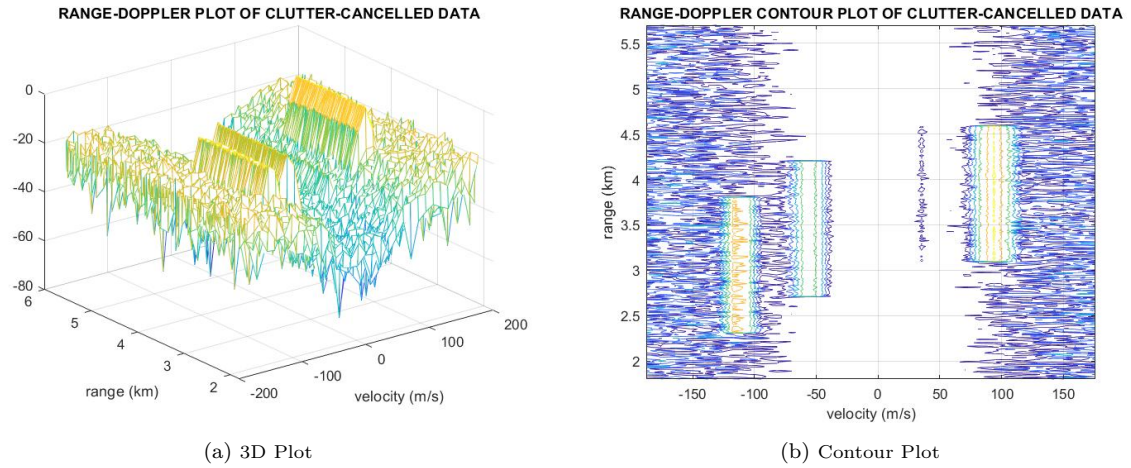


Figure 7: Range and contour plot after clutter cancellation

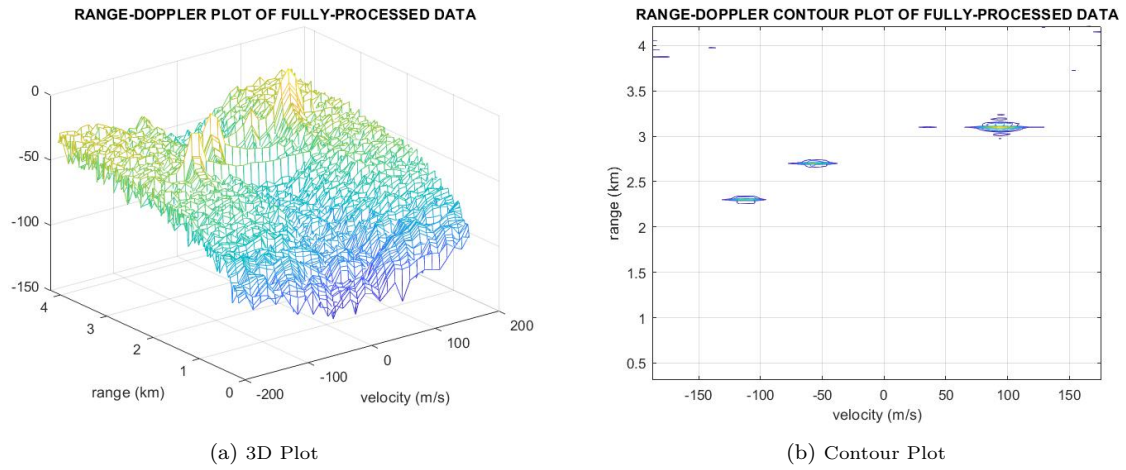


Figure 8: Range and contour plot after clutter cancellation and matched filtering

| Target Number | Rel Amp (dB) | Range (km) | Velocity (m/s) |
|---------------|--------------|------------|----------------|
| 1 | -11 | 2.3 | -113.3 |
| 2 | -0.482 | 2.7 | -57 |
| 3 | 0 | 3.1 | 93.76 |

Table 2: Estimated Target Parameters

3 Hardware Implementation

The matlab simulation is successfully completed and we can use the parameters used in the simulation for our actual design. The entire signal processor is to be implemented onto an FPGA board with an SDR attached to it. Chirp Signal Generator, Matched filter^[1], Clutter Canceler^[4], 32-point FFT^[4] and Hamming Window are to be designed using Vivado and later implemented onto actual hardware. The entire process is summarised in the figure 9 below,

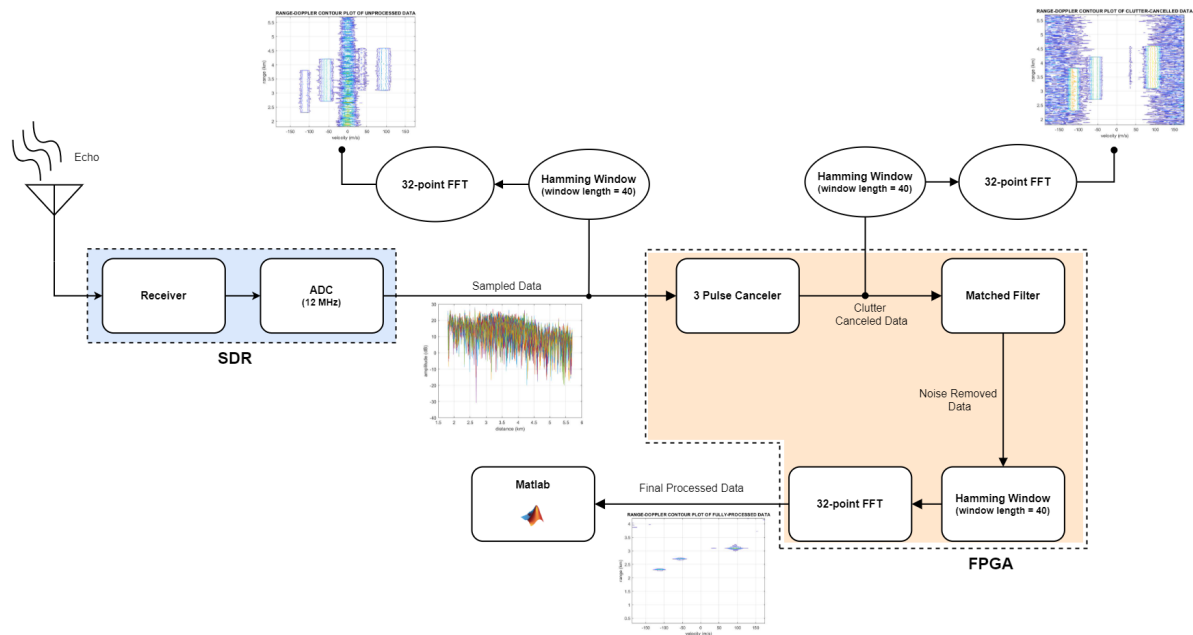


Figure 9: Block Diagram

4 Conclusion and Future Work

Matlab simulation of the radar model is successfully completed. The target parameters were successfully extracted and it matches with the actual target parameters. Now with the radar parameters used to simulate the radar we can start designing each of the individual modules which is later implemented onto FPGA.

5 References

- [1] Merrill I. Skolnik, (2001). Introduction To Radar Systems (3rd ed.). Tata McGraw-Hill Edition 2001.
- [2] Xilinx User Guide for ZC702 Evaluation Board for the Zynq-7000 XC7Z020 SoC.
- [3] Analog Devices AD-FMCOMMS3-EBZ User Guide.
- [4] Fundamentals of Radar Signal Processing, Mark A Richards.