CHAPTER 1

COMPARISON REPORT

Using DA Algorithm:

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	69	960	7%
Number of Slice Flip Flops	24	1920	1%
Number of 4 input LUTs	130	1920	6%
Number of bonded IOBs	18	66	27%
Number of GCLKs	1	24	4%

Table 1.1: DEVICE UTILIZATION OF DA BASED METHOD

Using Multiplier approach:

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	287	960	29%
Number of Slice Flip Flops	33	1920	1%
Number of 4 input LUTs	541	1920	28%
Number of bonded IOBs	27	66	40%
Number of GCLKs	1	24	4%

Table 1.2: DEVICE UTILIZATION OF MULTIPLIER APPROACH

	Normal Operation	DA Algorithm
Maximum Frequency	47.1 MHz	94.26MHz
Cell Usage	1034	176
Maximum Path Delay	31.338nsec	15.293nsec

Table 1.3: THE COMPARISON TABLE OF BOTH APPROACHES

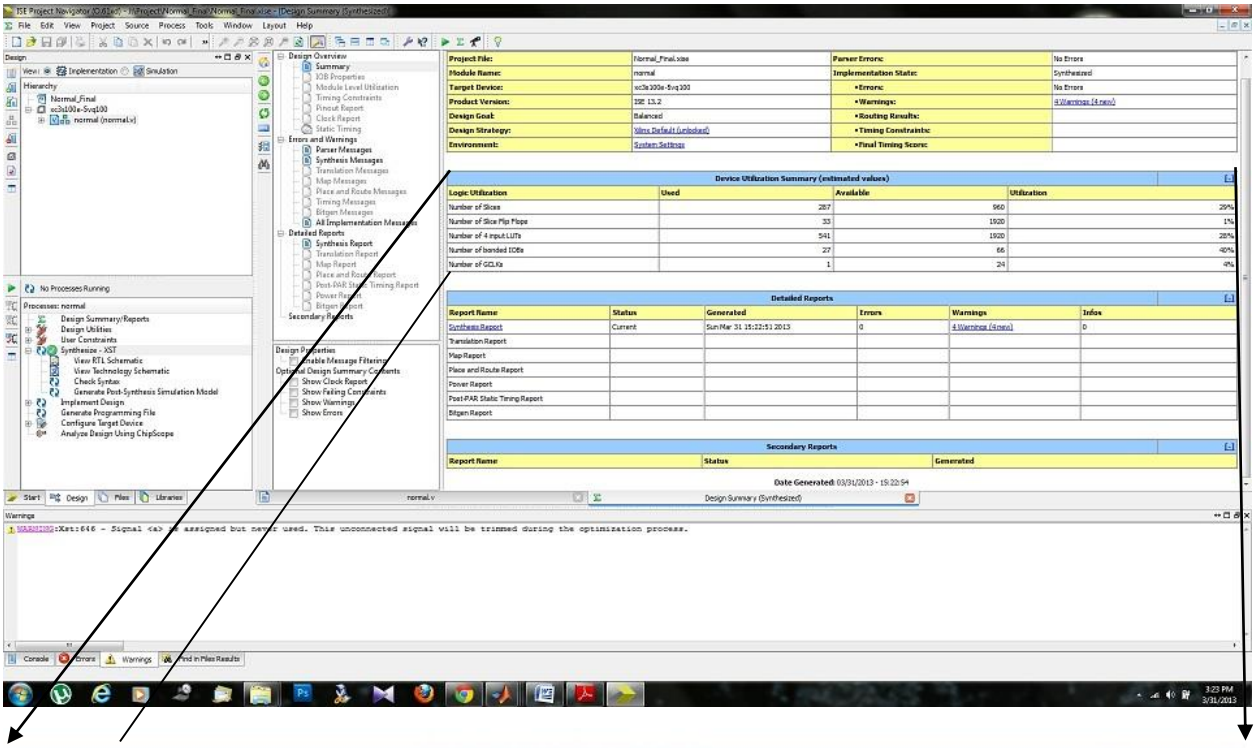
From the above table we can analyze that in the normal operation i.e., the method using multipliers the maximum frequency is 47.1 MHz whereas in the DA based algorithm the maximum frequency is 94.26Mhz, which means that by using the DA based algorithm we almost get twice the maximum frequency .This further implies that by using the DA based algorithm we can make the system twice the rate faster. The normal multiplier method uses large number of logic devices and this leads to more amount of cell usage. Now instead when we use the DA algorithm we see that cell usage is reduced to almost half the amount that was used in the normal operation. The delay time consumed in the normal operation is more and from the table 5 also we can infer that the maximum path delay is 31.338 n sec which is very high when compared to the DA algorithm. Thus over all the power consumed by the system using DA is also reduced by 50%.

CHAPTER 2

SIMULATION AND ANALYSIS

The simulation of the project we have implemented is shown below.

1. The existing model is implemented. The simulation report of which is given below:



Device Utilization Summary (estimated values)			
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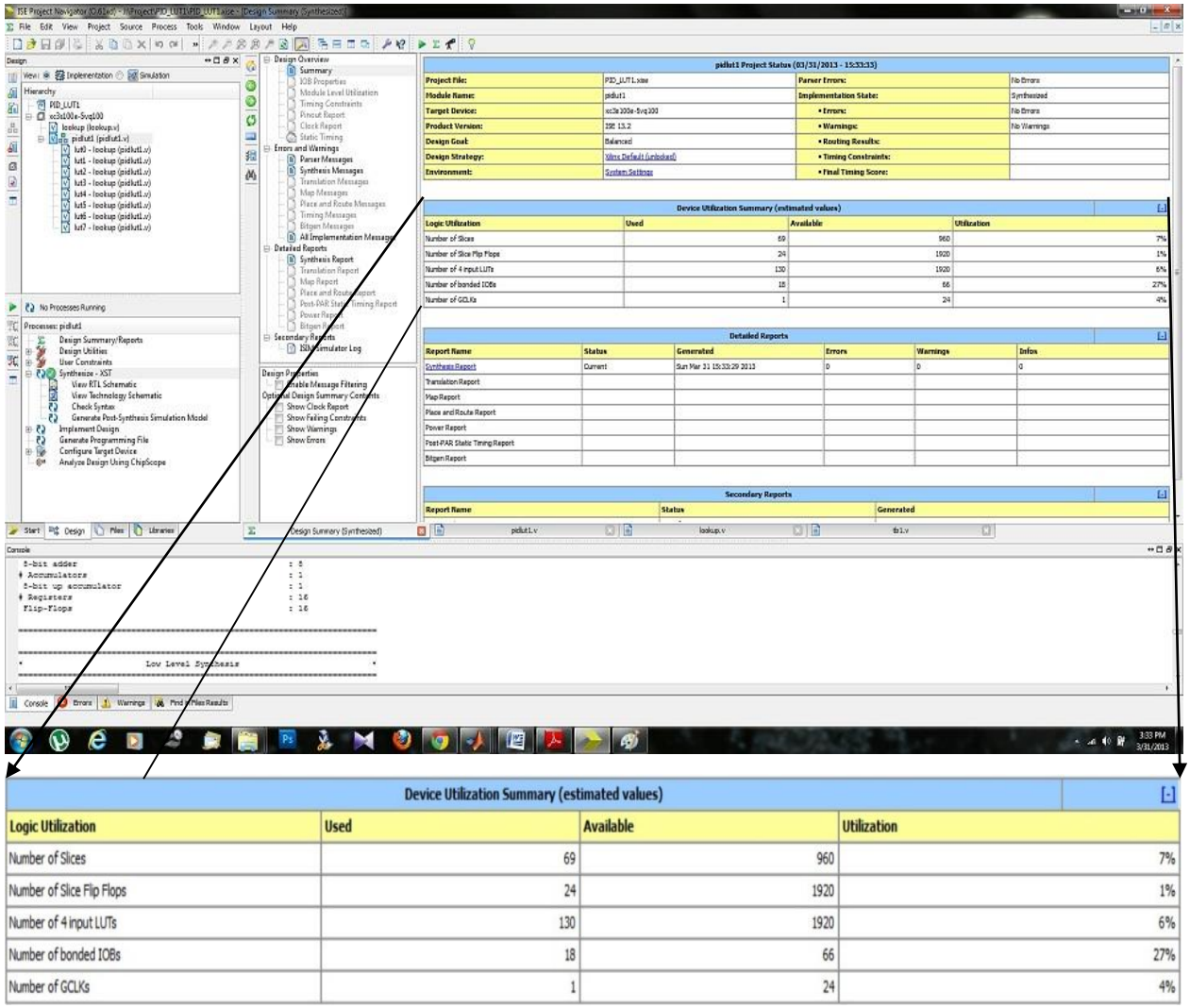
Number of GCLKs	1	24	4%

Fig 2.1: Summary of the existing model

2. The proposed model is implemented and the simulation model is given below:



Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	69	960	7%
Number of Slice Flip Flops	24	1920	1%
Number of 4 input LUTs	130	1920	6%
Number of bonded IOBs	18	66	27%
Number of GCLKs	1	24	4%

Fig 2.2 : Summary of the proposed model

3.The Xilinx and MATLAB is linked with each other and the matlab block is given below using System Generator Block.

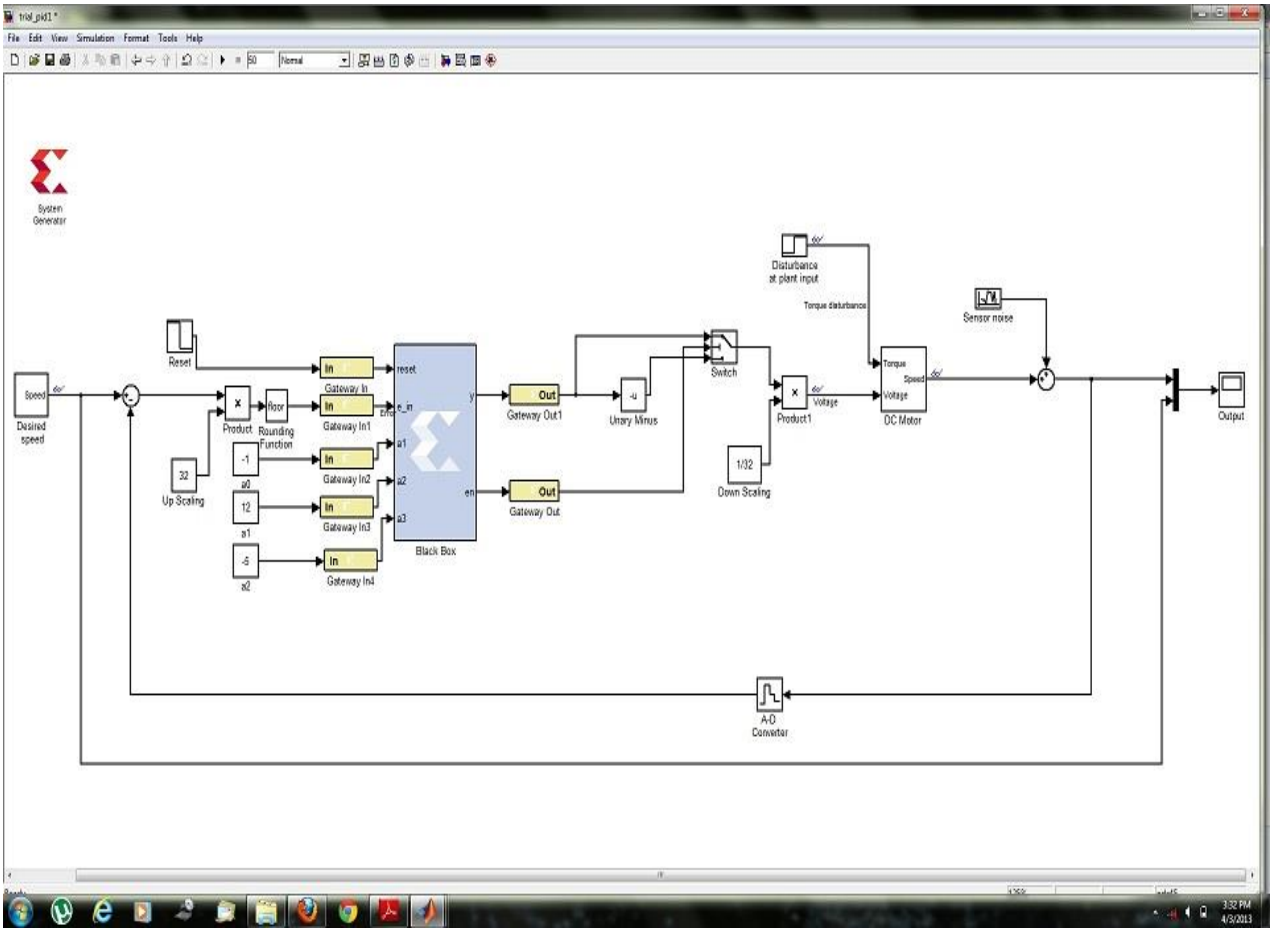


Fig 2.3: MATLAB implementation block

This block contains the black box in which we linked it to the .v (verilog) file i.e., the Xilinx file and then we get our required output .

4. The output of the proposed PID model

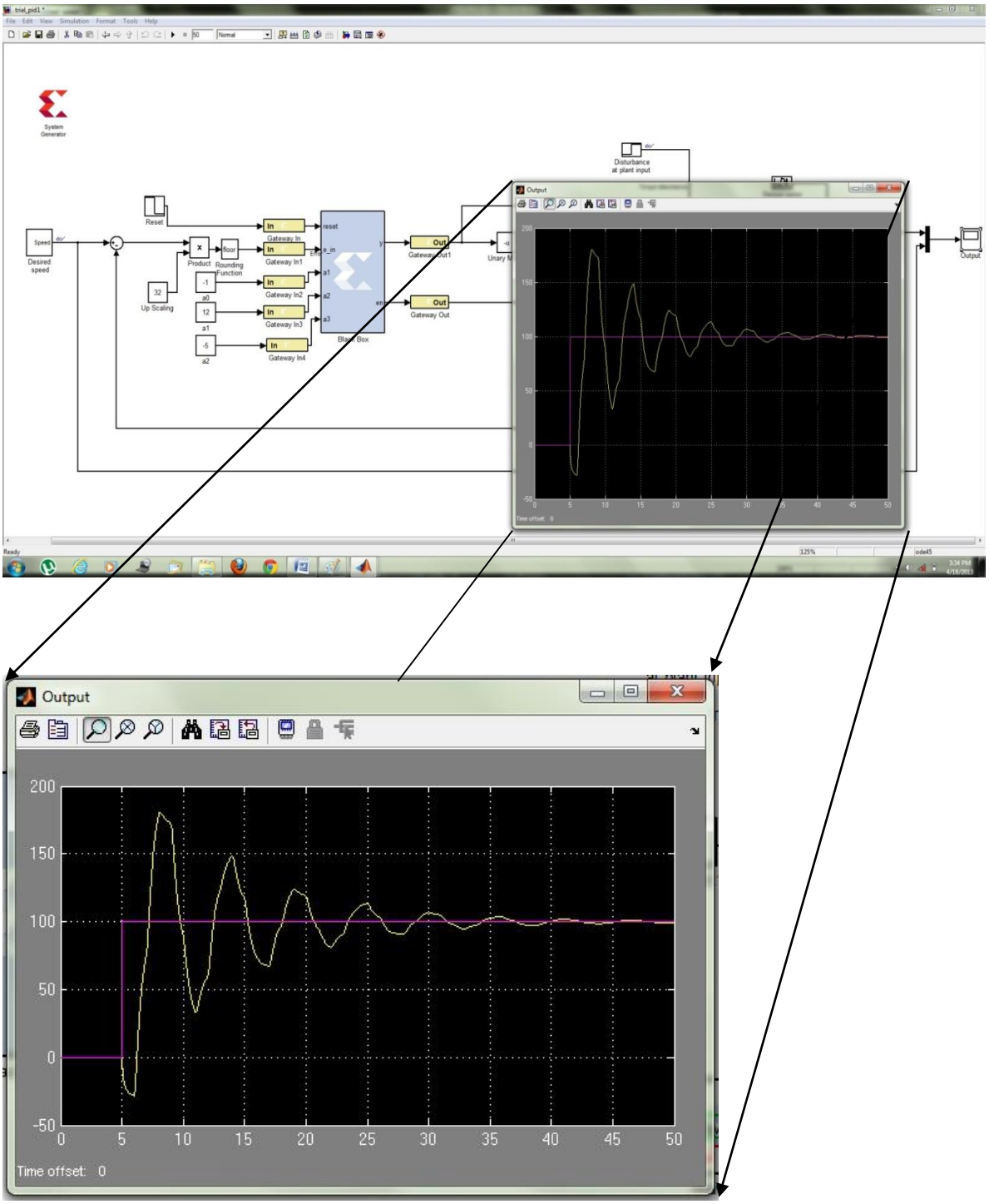


Fig 2.4: The output of the proposed model

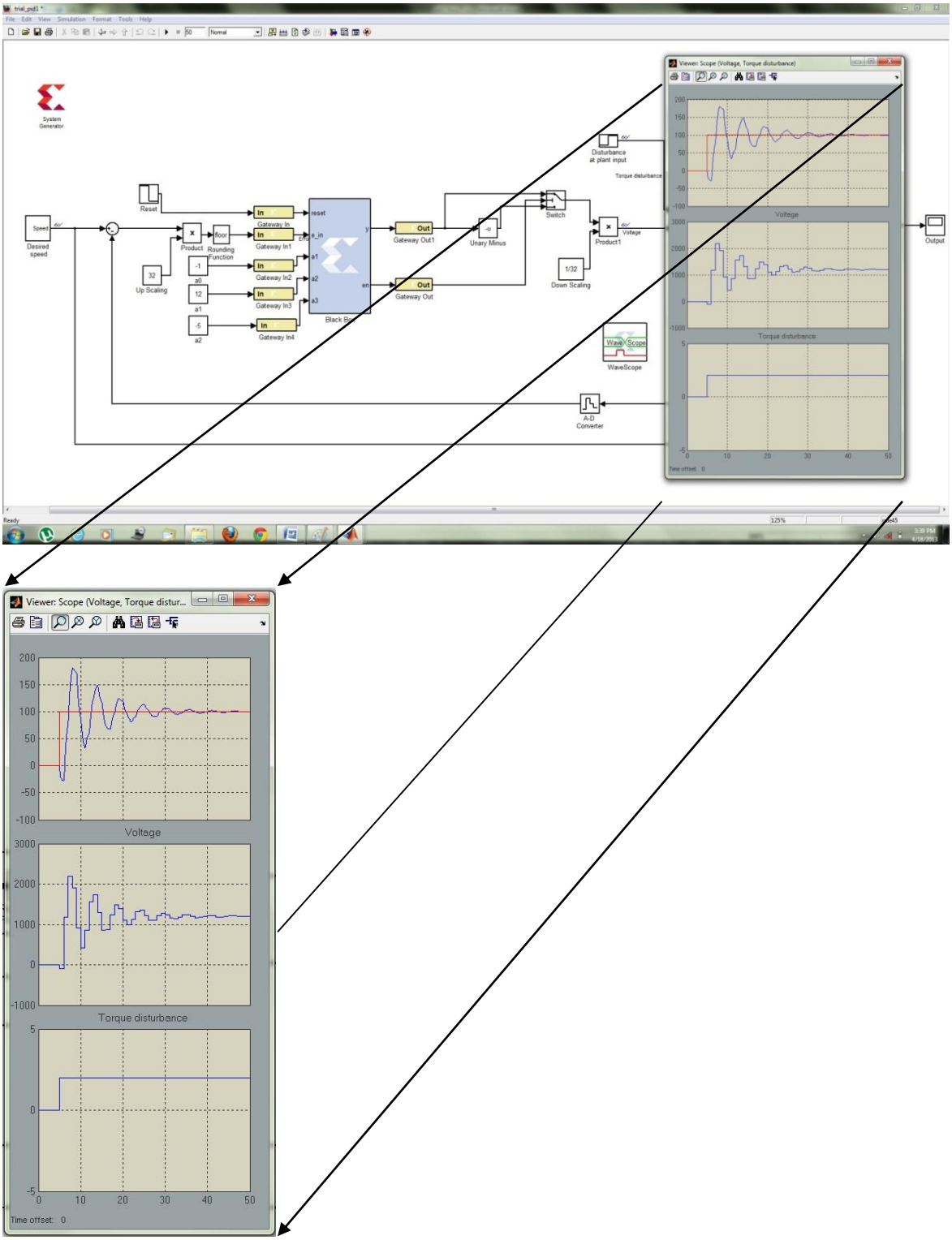


Fig 2.5: The detailed output showing voltage and torque disturbance

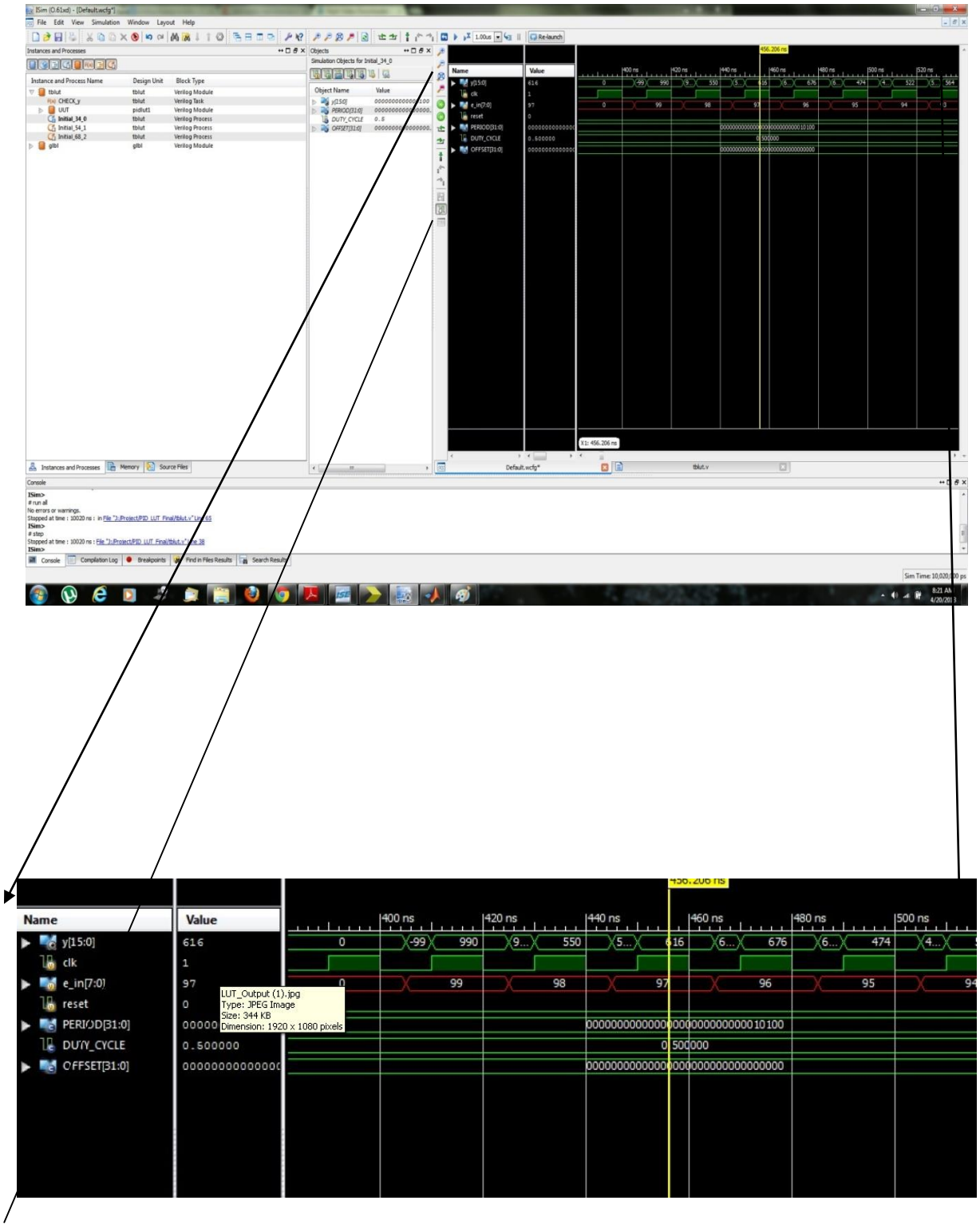


Fig 2.6: The output waveform obtained in Xilinx

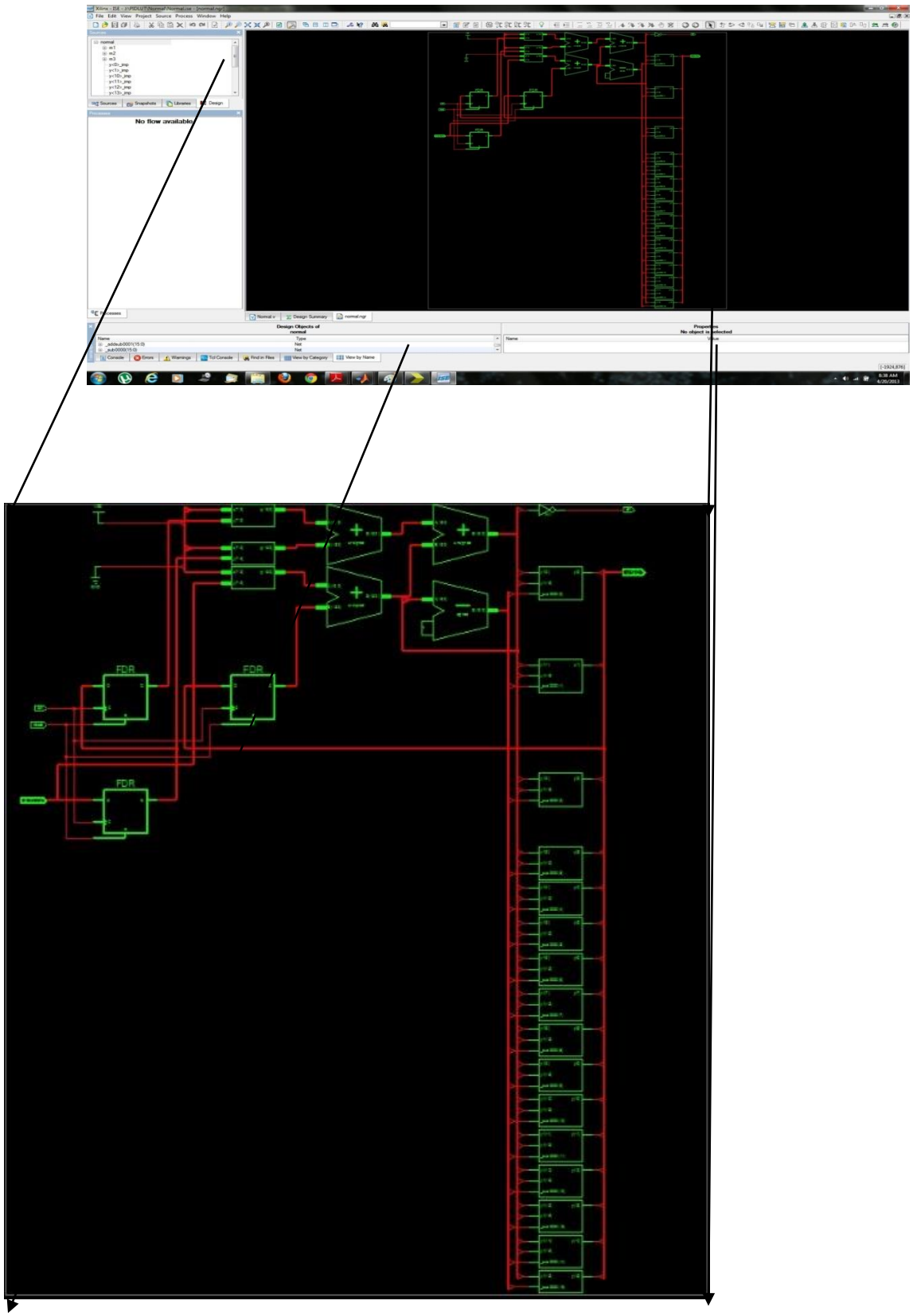


Fig 2.7: RTL schematic of the normal multiplier implementation

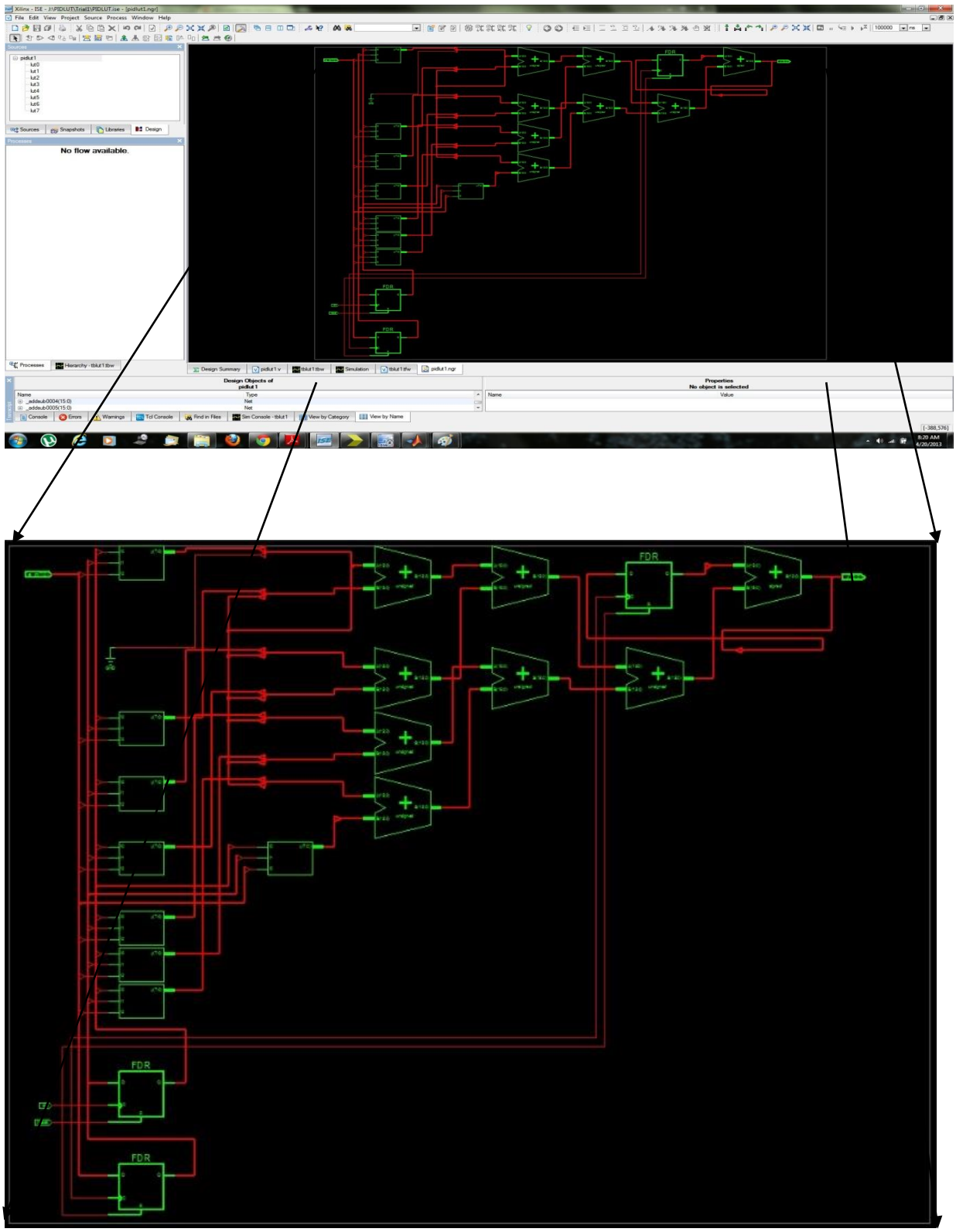


Fig 2.8: RTL schematic of LUT based implementation