

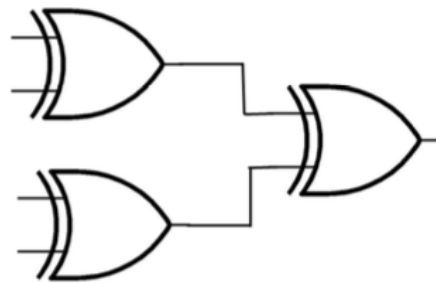
ESE 555 | CAD ASSIGNMENT 2

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OBJECTIVE:

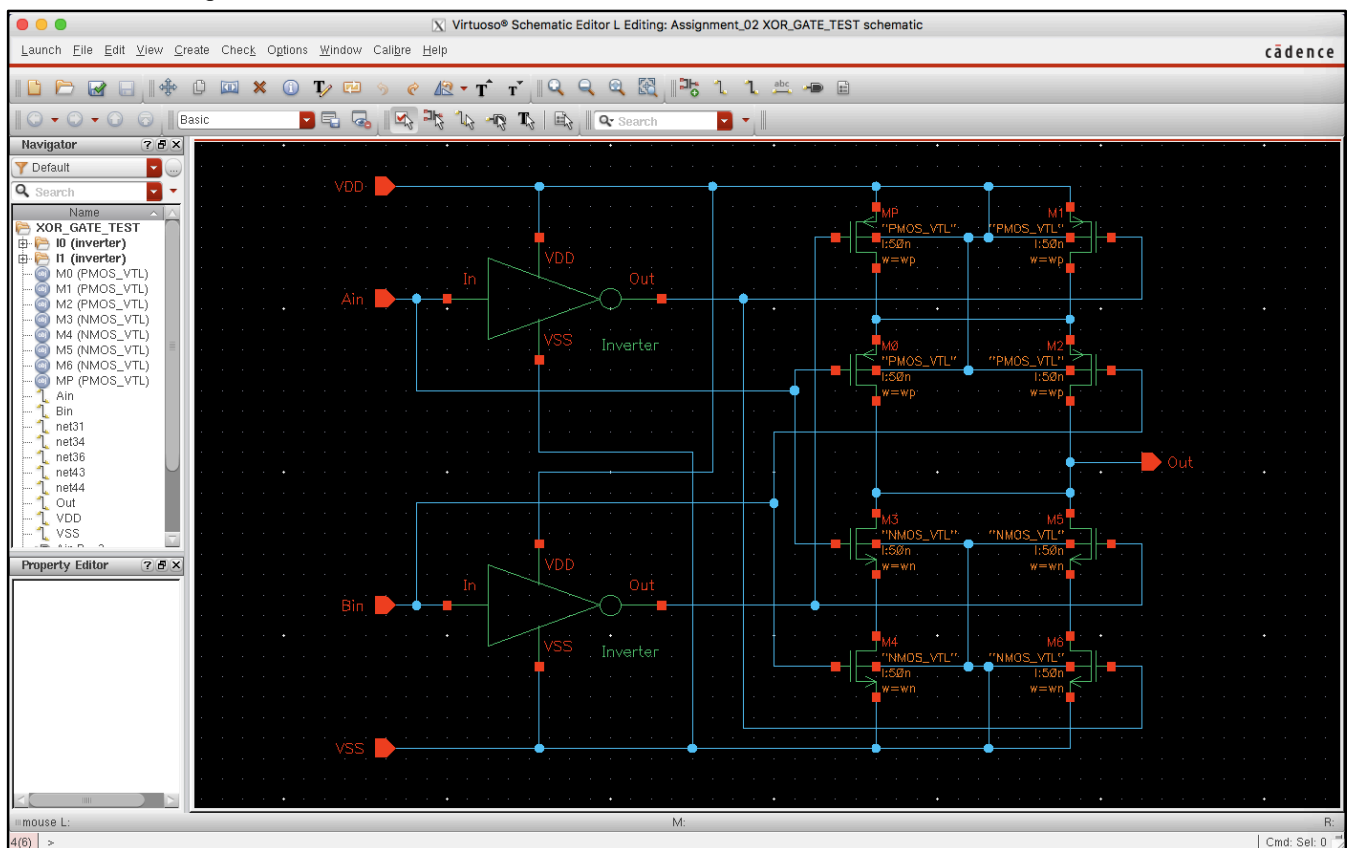
Design and verify a four-input parity generator consisting of three XOR Gates in the 45 nm CMOS technology.



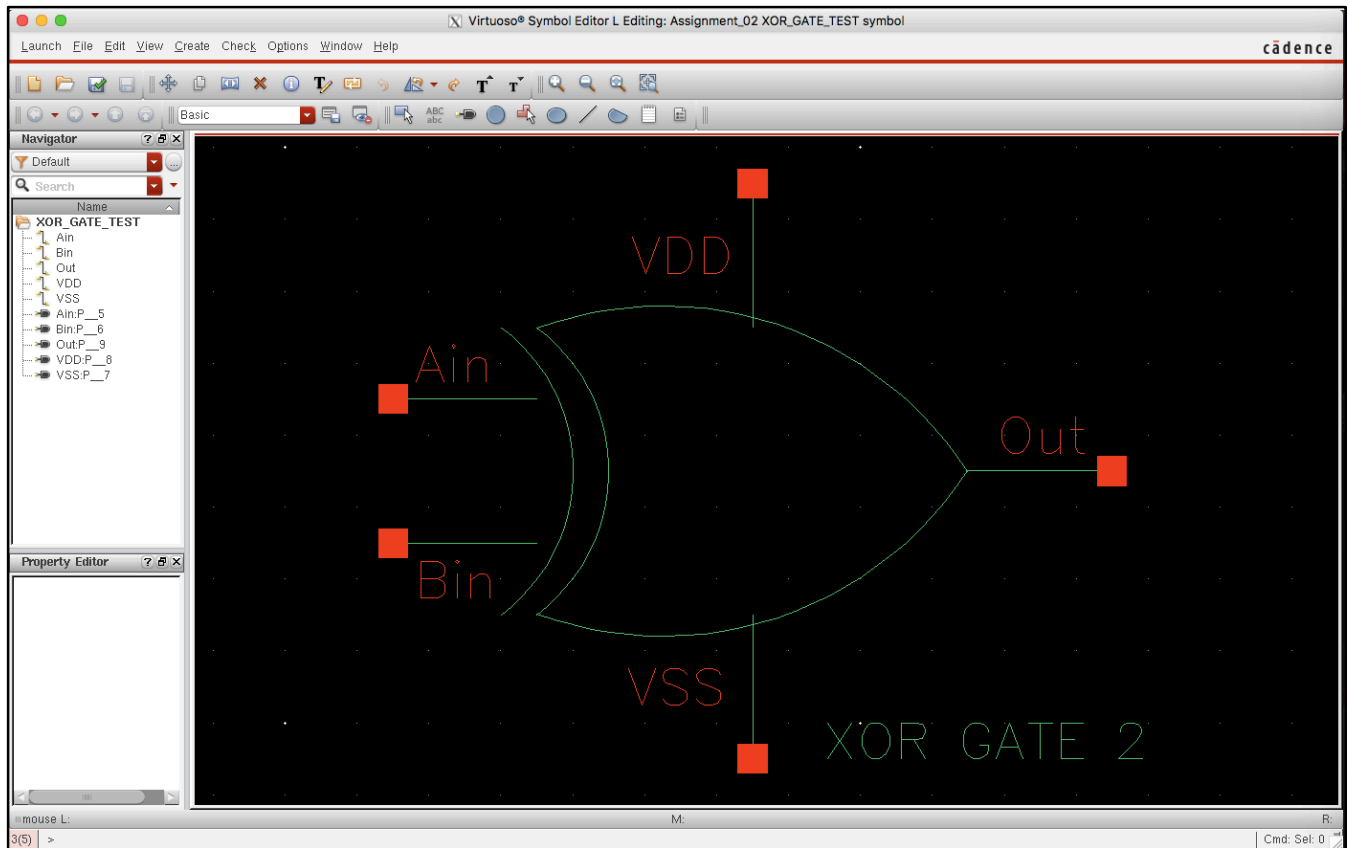
DESIGN SPECIFICATIONS:

- Logic Circuit Style : Static CMOS
- Nominal Supply Voltage : 1.1 V
- External Load : 12 fF
- Rise/Fall Time : 100ps

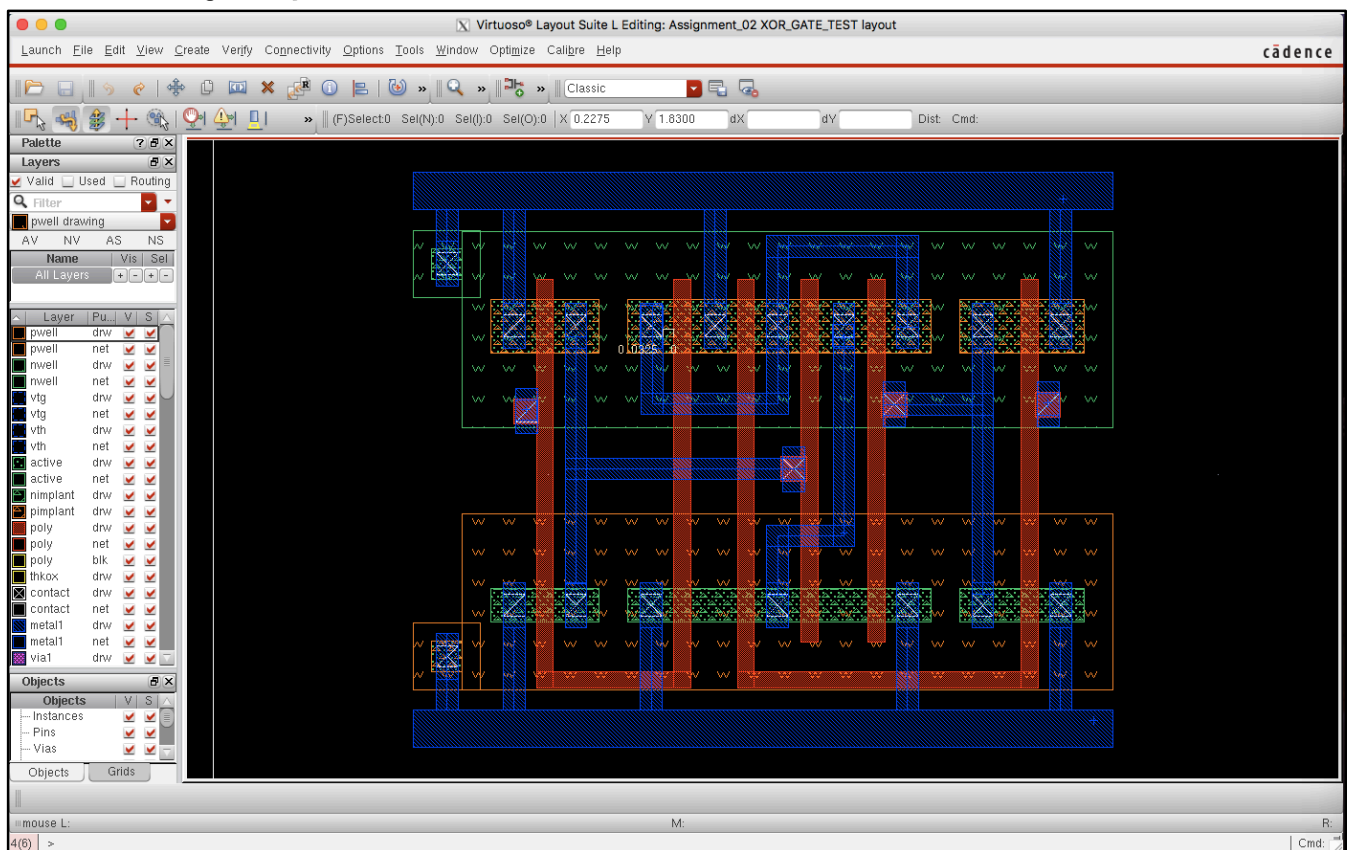
1. XOR Gate Design [Circuit Schematic]



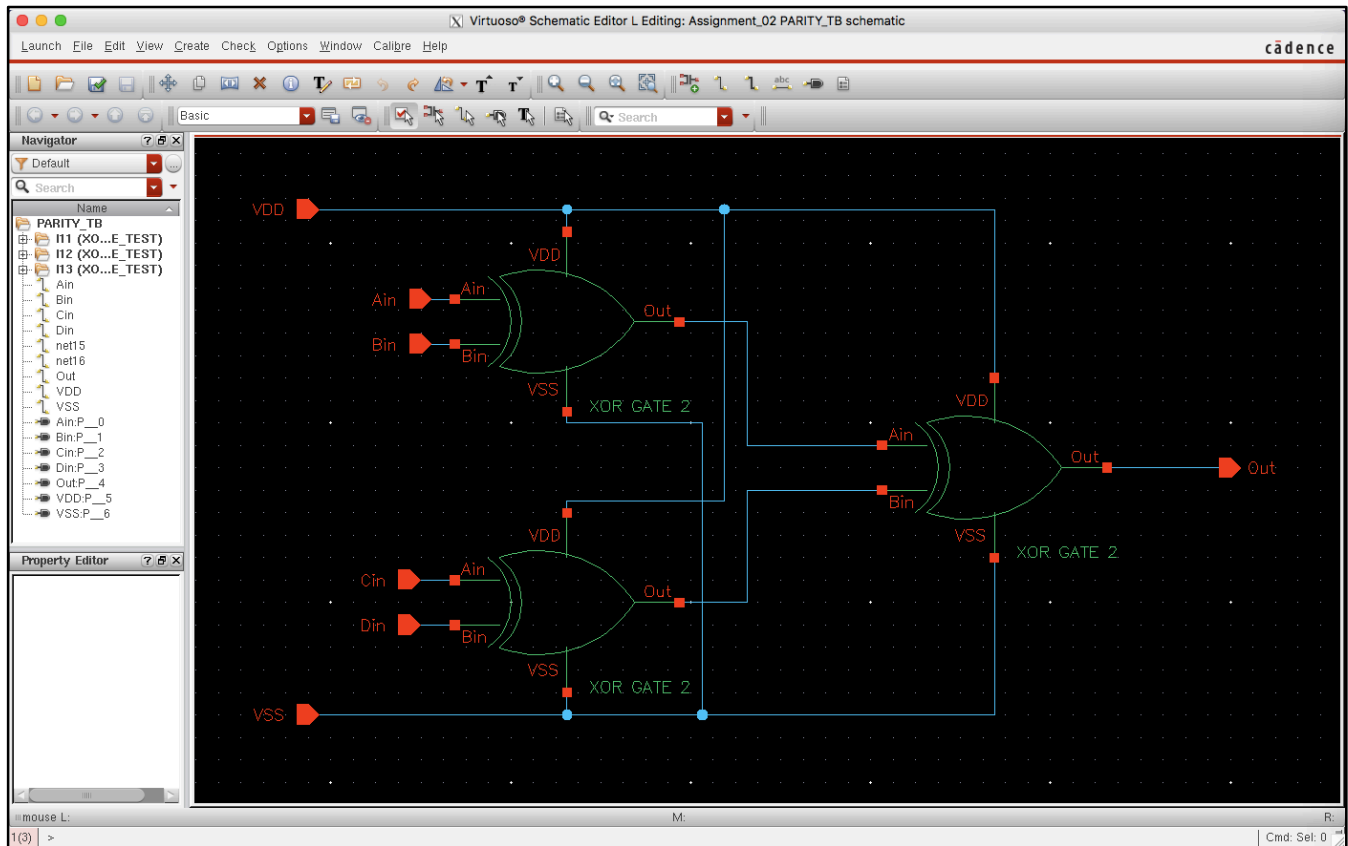
2. XOR Gate Design [Symbol]



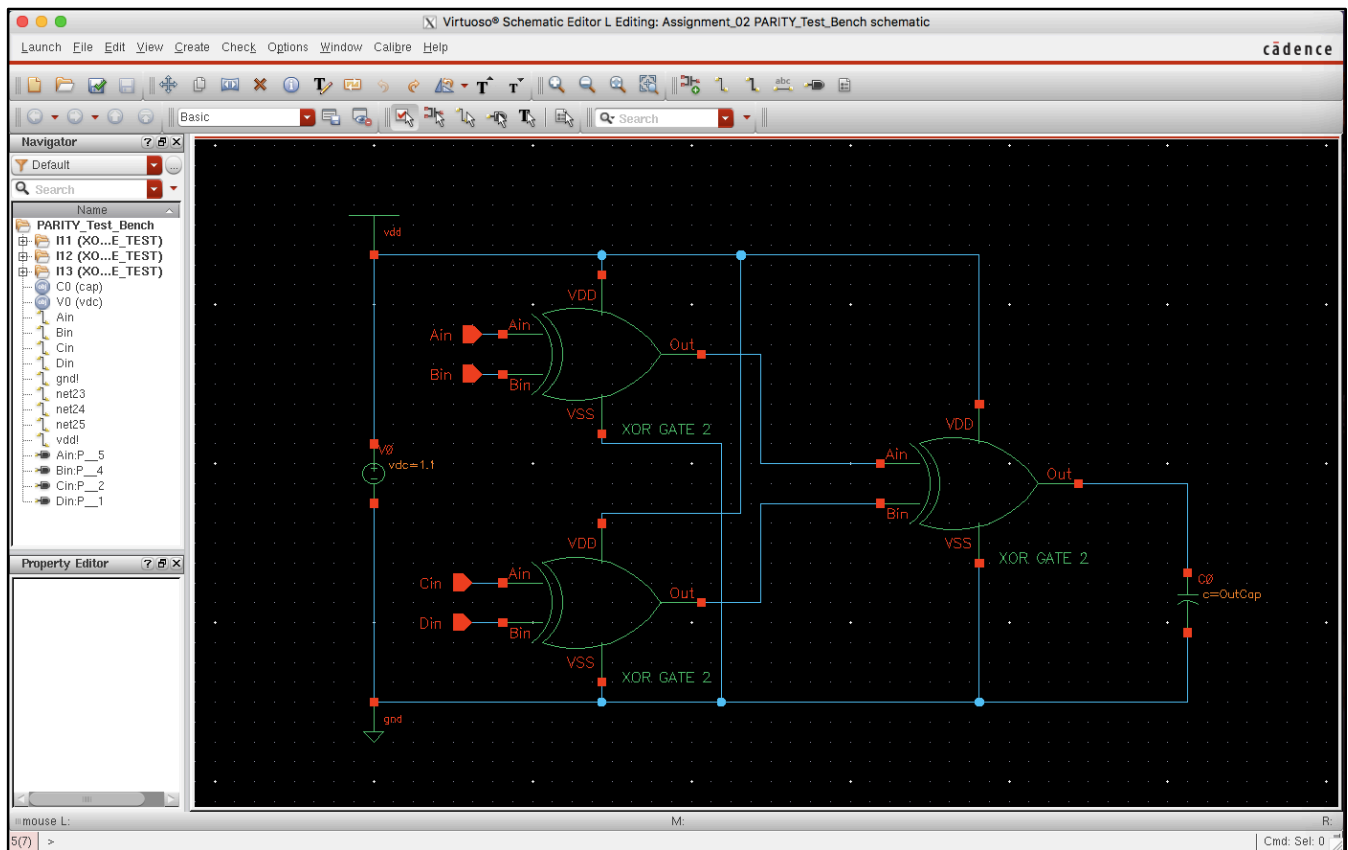
3. XOR Gate Design [Layout]



4. Parity Generator Design [Circuit Schematic]



5. Parity Generator Test-Bench [Circuit Schematic]

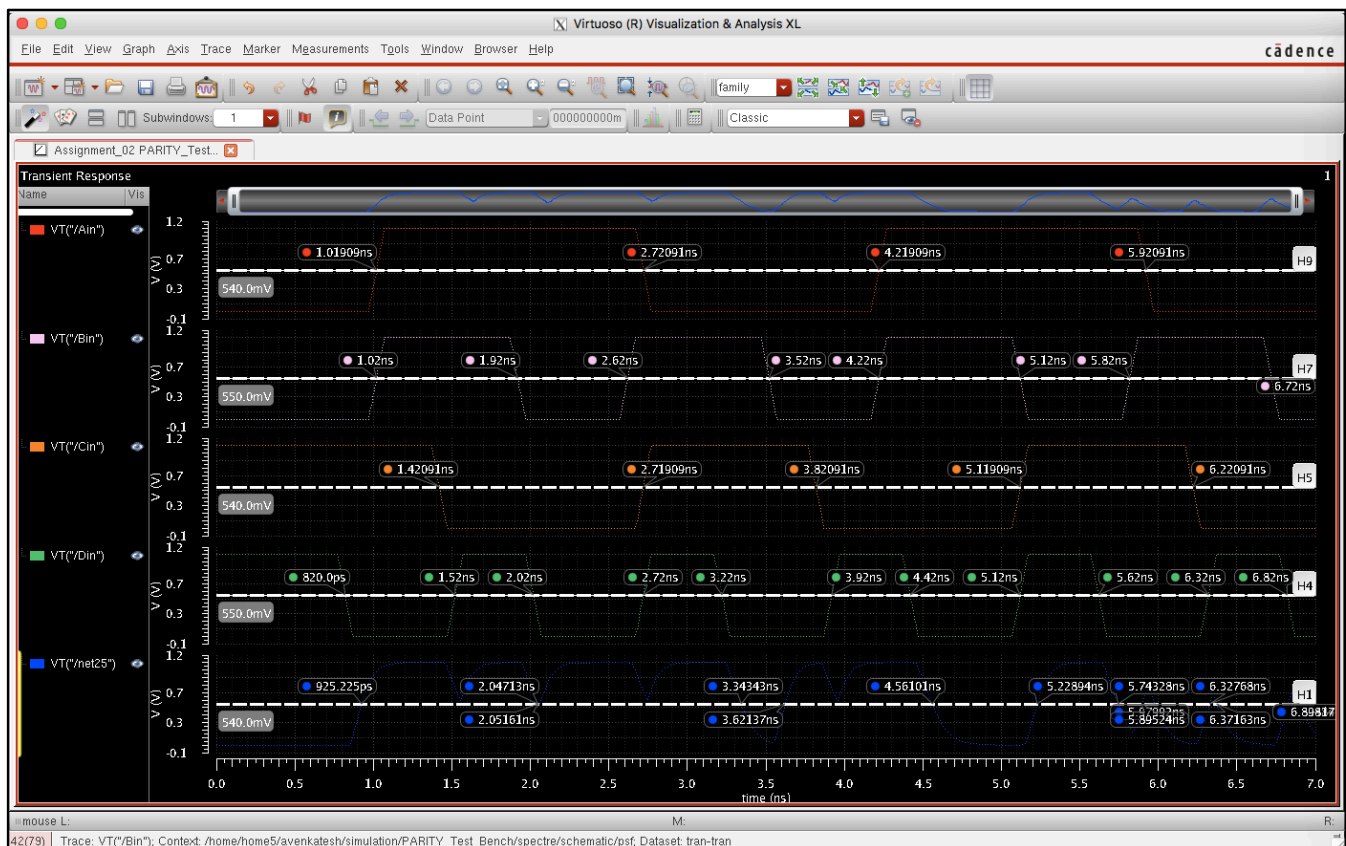


6. Estimating Wn & Wp Ratio for Least Power Delay Product

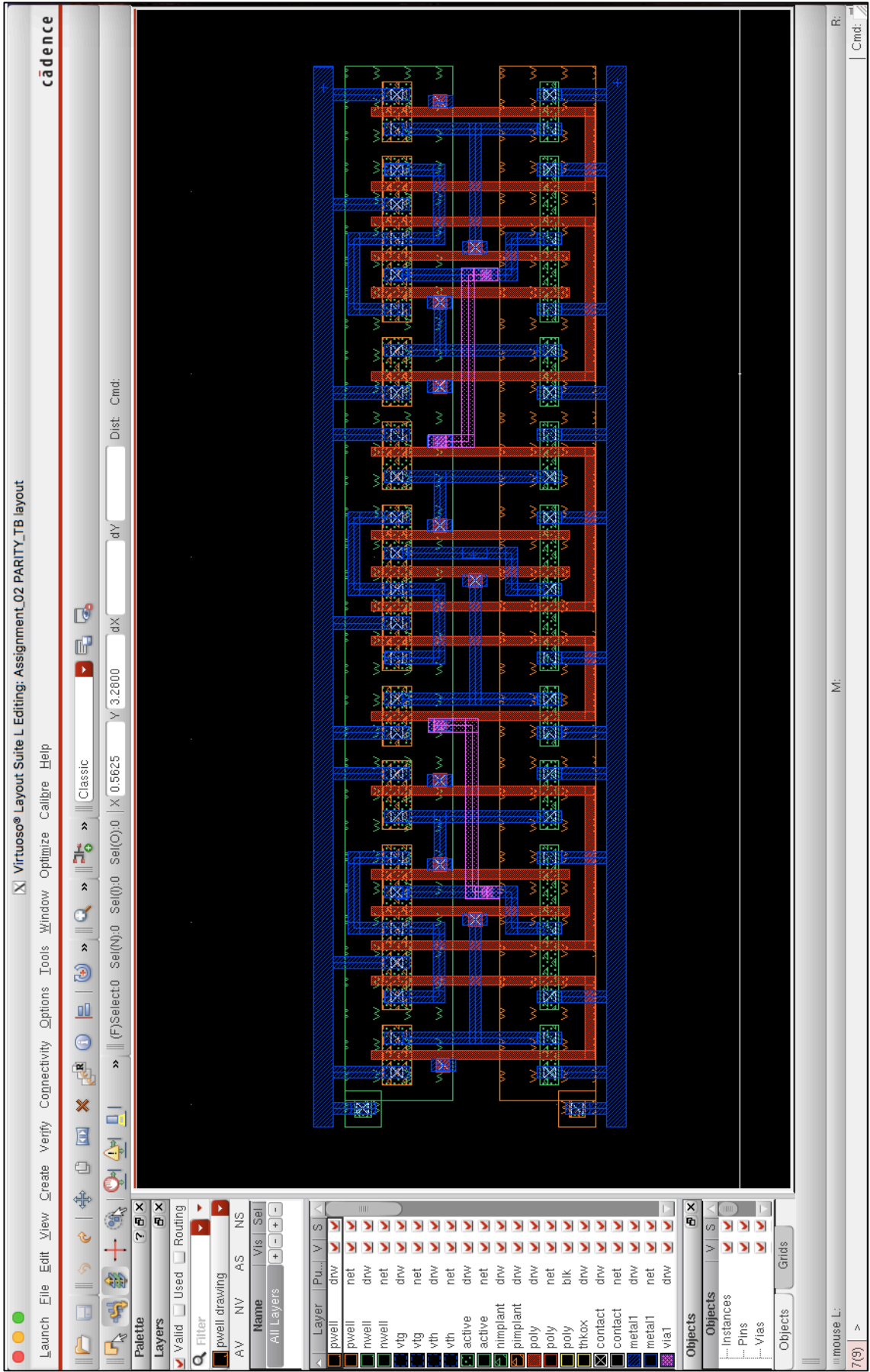
Pmos Width (nM)	Nmos Width (nM)	Average Current (uA)	Voltage (V)	Power (uW)	Average Propagation Delay (t _{phl} & t _{plh}) (pS)	Power Delay Product (WS)
160	100	25.93	1.1	28.52	133.79	3816.05
180	100	27.00	1.1	29.70	128.54	3817.67
140	100	24.80	1.1	27.28	141.70	3865.55
140	90	23.86	1.1	26.25	148.46	3896.47
100	90	22.69	1.1	24.96	159.49	3980.72
120	100	23.58	1.1	25.94	154.58	4009.56
120	90	22.69	1.1	24.96	161.18	4022.85
100	100	22.23	1.1	24.45	168.95	4131.44

Final W/L values for Pmos and Nmos are 160nM and 100nM respectively. This is obtained by iterating multiple W/L ratios and 1.6x yields the lowest power delay product.

7. Transient Analysis – Input & Output Waveform



8. Parity Generator Final Layout [Minimized Area Design]



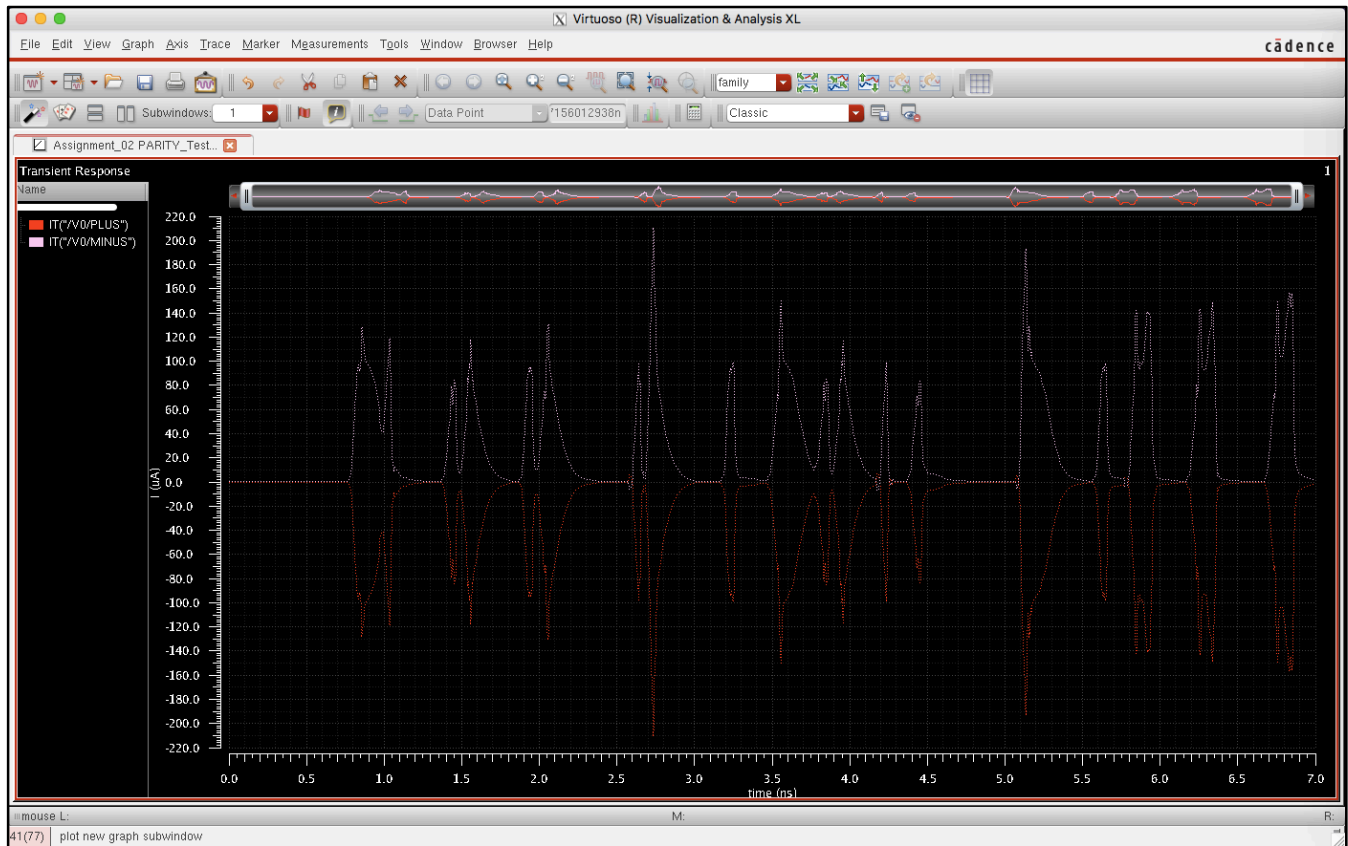
Pmos Dimensions

- Length: 50 n M
- Width: 160n M

Nmos Dimensions

- Length: 50 n M
- Width: 100n M

9. Transient Analysis – Current Waveform



10. Parity Generator Design – DRC Successful Result

The screenshot displays the Calibre - RVE v2014.4_28.20 : PARITY_TB.drc.results window. The window shows a list of DRC checks and their results, all of which are successful (0 violations). The checks include:

Check / Cell	Results
Check Well.1	0
Check Well.2	0
Check Well.4	0
Check Poly.1	0
Check Poly.2	0
Check Poly.3	0
Check Poly.4	0
Check Poly.5	0
Check Poly.6	0
Check Active.1	0
Check Active.2	0
Check Active.3	0
Check Active.4	0
Check Implant.1	0
Check Implant.2	0
Check Implant.3	0
Check Implant.4	0
Check Implant.6	0
Check Contact.1	0
Check Contact.2	0

The bottom of the window shows the Rule File Pathname: `/home/home5/svenkatesh/aswinesse555/_calibreDRC.rul_` and the message: `nvell and pwell must not overlap`.

11. Parity Generator Design – LVS Successful Result

The screenshot displays the Calibre RVE v2014.4.28.20 interface. The left pane shows the 'Results' section with 'Comparison Results' selected. The main pane shows the 'Cell PARITY_TB Summary (Clean)' and 'INITIAL NUMBERS OF OBJECTS' table.

Ports:	Layout	Source	Component Type
	7	7	
Nets:	24	24	
Instances:	18	18	NN (4 pins)
	18	18	MP (4 pins)
Total Inst:	36	36	

The right pane shows the 'LVS Report File - PARITY_TB.lvs.report' with the following content:

```

#####
**          CALIBRE SYSTEM          **
**          LVS REPORT              **
#####

REPORT FILE NAME:  PARITY_TB.lvs.report
LAYOUT NAME:      /home/home5/averkatesh/aswinese555/Parity_TB.sp ('PAR')
SOURCE NAME:      /home/home5/averkatesh/aswinese555/Parity_TB.src.net
RULE FILE:        /home/home5/averkatesh/aswinese555/_calibreLVS.rul_
RULE FILE TITLE:  LVS Rule File for FreePDK45
CREATION TIME:    Fri Oct 13 01:35:29 2017
CURRENT DIRECTORY: /home/home5/averkatesh/aswinese555
USER NAME:        averkatesh
CALIBRE VERSION:  v2014.4.28.20      Thu Dec 4 12:46:29 PST 2014

OVERALL COMPARISON RESULTS

#####
**          CORRECT              **
#####

***** CELL SUMMARY *****
Result      Layout      Source
CORRECT     PARITY_TB     PARITY_TB

***** LVS PARAMETERS *****

o LVS Setup:
LVS COMPONENT TYPE PROPERTY  element
LVS COMPONENT SUBTYPE PROPERTY  model
// LVS PIN NAME PROPERTY
LVS POWER NAME                'VDD'
// LVS POWER NAME

```

12. Parity Generator Design – PEX Successful Result – Parasitic Capacitances

The screenshot displays the Calibre RVE v2014.4.28.20 interface. The left pane shows the 'Results' section with 'Parasitics' selected. The main pane shows the 'PEX Report File - PARITY_TB.pex.report' and a table of parasitic capacitances.

No.	Layout Net	Source Net	R Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	1	NET16	26	2.60326E-16	3.75318E-16	6.35644E-16
2	2	NET15	26	2.71449E-16	4.07433E-16	6.78882E-16
3	3	AIN	12	1.85381E-16	1.29867E-16	3.15248E-16
4	4	XI12/NET92	13	1.01099E-16	3.30873E-16	4.31972E-16
5	5	5	12	4.85136E-17	2.29696E-16	2.78210E-16
6	6	XI12/NET52	13	1.02016E-16	1.50922E-16	2.52938E-16
7	7	BIN	12	1.93613E-16	1.59867E-16	3.53481E-16
8	8	XI13/NET92	13	9.42647E-17	2.40557E-16	3.34822E-16
9	9	OUT	7	3.56809E-17	1.17629E-16	1.53310E-16
10	10	10	12	4.78339E-17	2.28589E-16	2.76423E-16
11	11	XI13/NET52	13	1.05811E-16	1.34586E-16	2.40396E-16
12	12	DIN	12	1.93715E-16	1.60068E-16	3.53783E-16
13	13	XI11/NET52	13	1.02448E-16	1.51152E-16	2.53600E-16
14	14	14	12	4.85080E-17	2.29704E-16	2.78212E-16
15	15	XI11/NET92	13	1.01066E-16	3.43788E-16	4.44854E-16
16	16	CIN	12	1.85179E-16	1.30657E-16	3.15836E-16
17	17	VSS	63	4.36755E-16	3.35372E-16	7.70326E-16
18	18	VDD	48	4.24399E-16	4.71034E-16	8.95433E-16

The right pane shows the 'PEX Report File - PARITY_TB.pex.report' with the following content:

```

#####
**          Calibre xRC          **
**          Export Lumped Parameters          **
#####

LAYOUT NAME:  PARITY_TB
RULE FILE NAME:  rules
CREATION TIME:  Fri Oct 13 01:41:33 2017

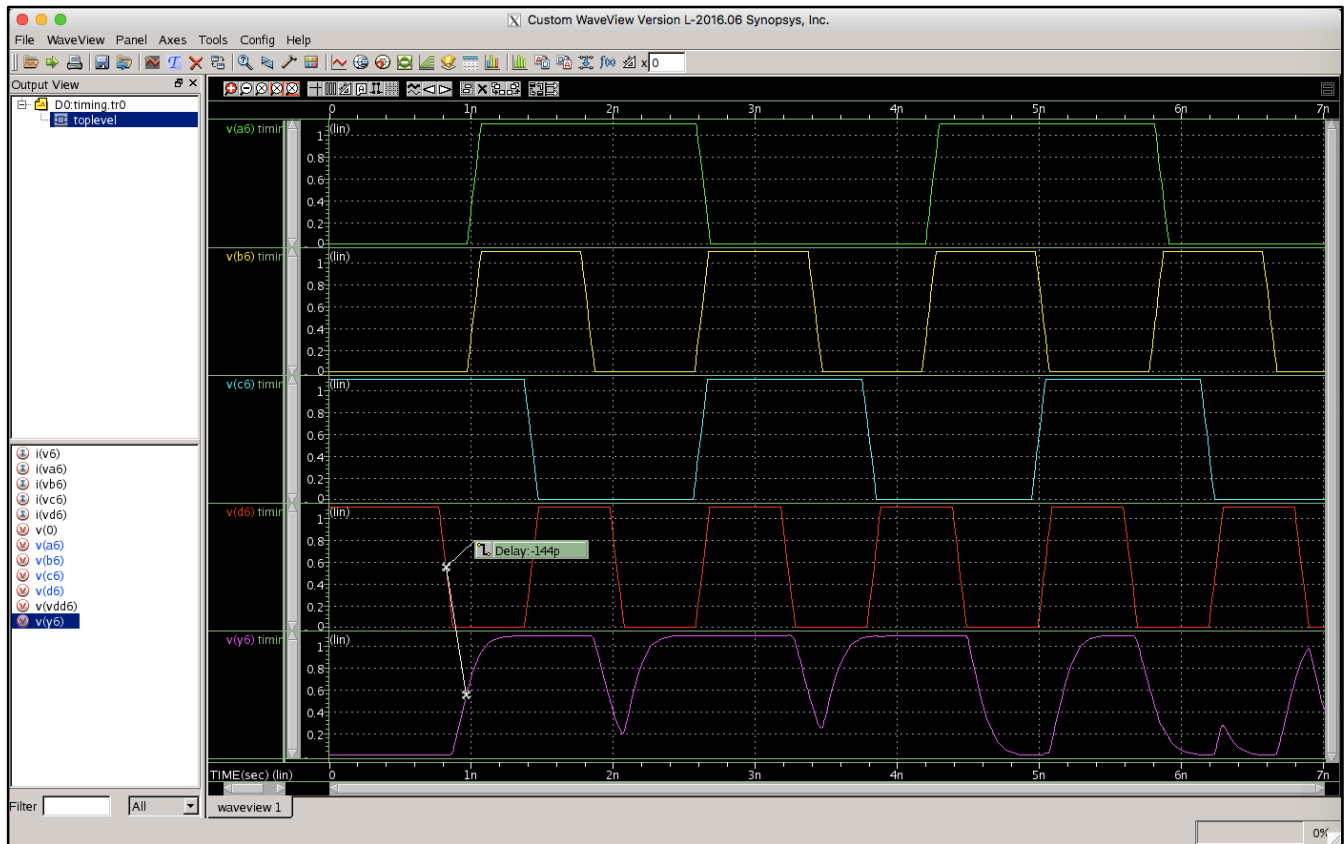
UNITS:
Resistance = ohm
Capacitance = farad
Time = ns

CELL NAME:  PARITY_TB

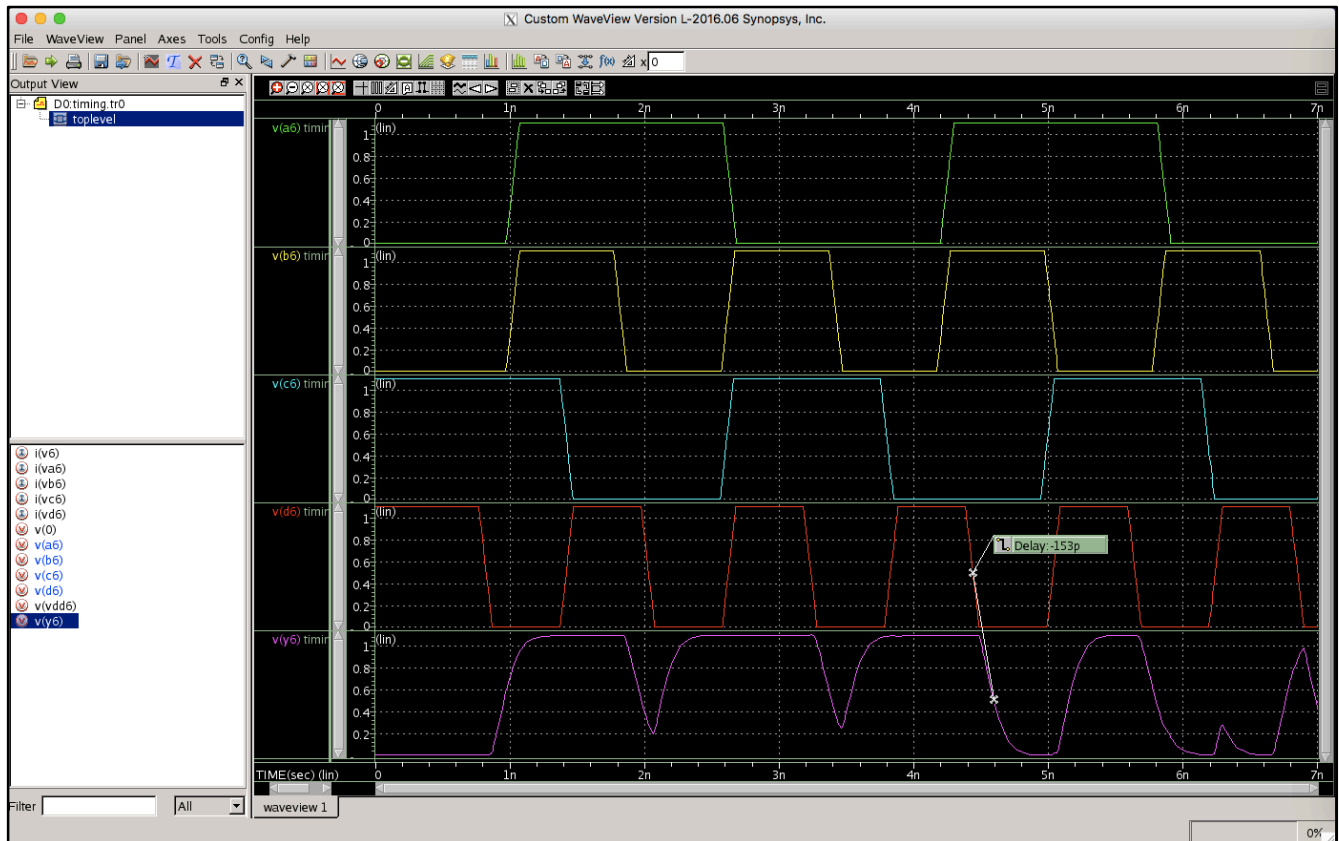
Netid      R(UpperBound)      Cvalue      %Coupled      RC(UpperBound)      Netname
-----
1          0.0      6.35644e-16      59.0453      0.0      NET16
- Coupled nets
  N_NET15_XI13/MM4_g_N_NET15_c_88_n_N_XI12/NET92_XI12/MM5_g_N_XI12/
- Intrinsic Capacitance
  2.60326e-16
- Coupled capacitance
  1.61213e-17      netid: N_NET15_XI13/MM4_g
  1.61213e-17      netid: N_NET15_c_88_n
  1.95609e-18      netid: N_XI12/NET92_XI12/MM5_g
  5.28015e-18      netid: N_XI12/NET92_XI12/MM5_g
  1.04998e-18      netid: N_XI12/NET92_XI12/MM5_g
  3.42327e-18      netid: N_XI12/NET92_XI12/MM5_g
  5.55443e-19      netid: N_XI12/NET92_XI12/MM5_g
  1.76736e-18      netid: N_XI12/NET92_XI12/XI10/MM0_d
  3.81323e-19      netid: N_XI12/NET92_XI12/XI10/MM0_d
  3.396e-19      netid: N_XI12/NET92_XI12/XI10/MM0_d
  6.08248e-19      netid: N_XI12/NET92_XI12/XI10/MM0_d
  3.19643e-18      netid: N_XI12/NET92_c_215_n
  6.19874e-18      netid: N_XI12/NET92_c_216_n
  2.6469e-18      netid: N_XI12/NET92_c_216_n
  1.0059e-16      netid: N_XI12/NET92_c_216_n
  2.40708e-18      netid: N_XI12/NET92_c_219_n
  1.04998e-18      netid: N_XI12/NET92_c_219_n
  7.53801e-18      netid: N_noxref_5_XI12/MM1_s
  8.50684e-18      netid: N_noxref_5_XI12/MM1_s
  1.28849e-17      netid: N_noxref_5_c_257_n
  3.35807e-19      netid: N_noxref_5_c_258_n
  4.93127e-18      netid: N_noxref_5_c_258_n
  5.95432e-19      netid: N_noxref_5_c_258_n
  1.48909e-18      netid: N_XI12/NET52_XI12/MM6_g
  9.21573e-19      netid: N_XI12/NET52_XI12/MM6_g
  3.36055e-18      netid: N_XI12/NET52_XI12/MM6_g
  1.48909e-18      netid: N_XI12/NET52_XI12/MM6_g
  1.00734e-18      netid: N_XI12/NET52_XI12/XI1/MM0_d
  4.40953e-18      netid: N_XI12/NET52_XI12/XI1/MM0_d

```

13. Post Layout Simulation – Low to High Propagation Delay Graph



14. Post Layout Simulation – High to Low Propagation Delay Graph



15.Design Summary

Simulation Results	Final Width of Pmos : 160 nM			Final Width of Nmos : 100 nM				
	Average Current (uA)	Voltage (V)	Power (uW)	Load Capacitance (fF)	Propagation Delay			Power Delay Product (WS)
					t _{phi}	t _{plh}	Avg	
Schematic	25.93	1.1	28.52	12	128.43	139.15	133.79	3816.05
Post layout	25.00	1.1	27.50	12	144.00	153.00	148.50	3817.67

-----END OF REPORT -----

APPENDIX

**** INCLUDE 45NM MODEL FILE

.PROT

.INC '/USR/LOCAL/CDS/FREEDK45/NCPU_BASEKIT/MODELS/HSPICE/HSPICE_NOM.INCLUDE'

.INC 'PARITY_TB.PEX.NETLIST'

.UNPR

**** SET NOMINAL SUPPLY VOLTAGE

.PARAM PVDD=1.1

**** SET TEMPERATURE AND GLOBAL GROUND

.PARAM PTEMP=25

.PARAM GND=0

**** SET TIMING PARAMETERS

.PARAM FREQA=0.31G

.PARAM FREQB=0.625G

.PARAM FREQC=0.42G

.PARAM FREQD=0.83G

.PARAM PERIA=1/FREQA

.PARAM PERIB=1/FREQB

.PARAM PERIC=1/FREQC

.PARAM PERID=1/FREQD

.PARAM LOAD=12FF

.PARAM RT=100P

.PARAM ONA=PERIA*0.5-RT

.PARAM ONB=PERIB*0.5-RT

.PARAM ONC=PERIC*0.5-RT

.PARAM OND=PERID*0.5-RT

.PARAM STOP=7N

**** SET PARITY INPUT AND OUTPUT

V6 VDD6 0 PVDD

C6 Y6 0 LOAD

VA6 A6 0 PULSE (0 PVDD 0.97N RT RT ONA PERIA)

VB6 B6 0 PULSE (0 PVDD 0.97N RT RT ONB PERIB)

VC6 C6 0 PULSE (PVDD 0 1.37N RT RT ONC PERIC)

VD6 D6 0 PULSE (PVDD 0 0.77N RT RT OND PERID)

**** INSTANTIATE INVERTER

XINVX1 A6 B6 Y6 D6 C6 0 VDD6 PARITY_TB

**** SET CONDITIONS AND OPTIONS

.IC V(XINVX1.Y6)=0

.TEMP PTEMP

.OPTION MACMOD=1 CAPTAB POST

**** MEASURE DELAYS, OUTPUT SLEWS, AND SWITCHING POWERS

** INVX1

.MEASURE TRAN IAVG6 AVG I(V6) FROM=0 TO=STOP

.MEASURE TRAN RISE6 TRIG V(Y6) VAL=PVDD*0.1 TD=2N RISE=1 TARG V(Y6) VAL=PVDD*0.9 TD=2N RISE=1

.MEASURE TRAN FALL6 TRIG V(Y6) VAL=PVDD*0.9 TD=2N FALL=1 TARG V(Y6) VAL=PVDD*0.1 TD=2N FALL=1

.MEASURE TRAN A6LH TRIG V(A6) VAL=PVDD*0.5 TD=2N FALL=4 TARG V(Y6) VAL=PVDD*0.5 TD=2N RISE=4

.MEASURE TRAN A6HL TRIG V(A6) VAL=PVDD*0.5 TD=2N RISE=4 TARG V(Y6) VAL=PVDD*0.5 TD=2N FALL=4

.MEASURE TRAN DELAY6 PARAM='(A6LH+A6HL)/2'

.MEASURE TRAN POWER6 PARAM=IAVG6*PVDD

.MEASURE TRAN SLEW6 PARAM=0.5*RISE6+0.5*FALL6

.TRAN 0.01N STOP

.END