ESE 555 CAD ASSIGNMENT 2 FALL 2015
Due October 13

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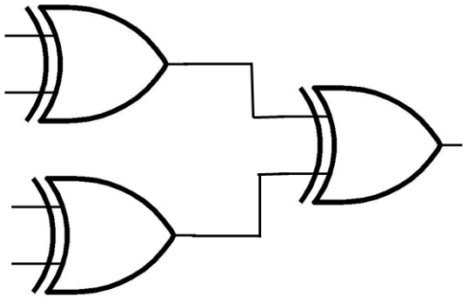
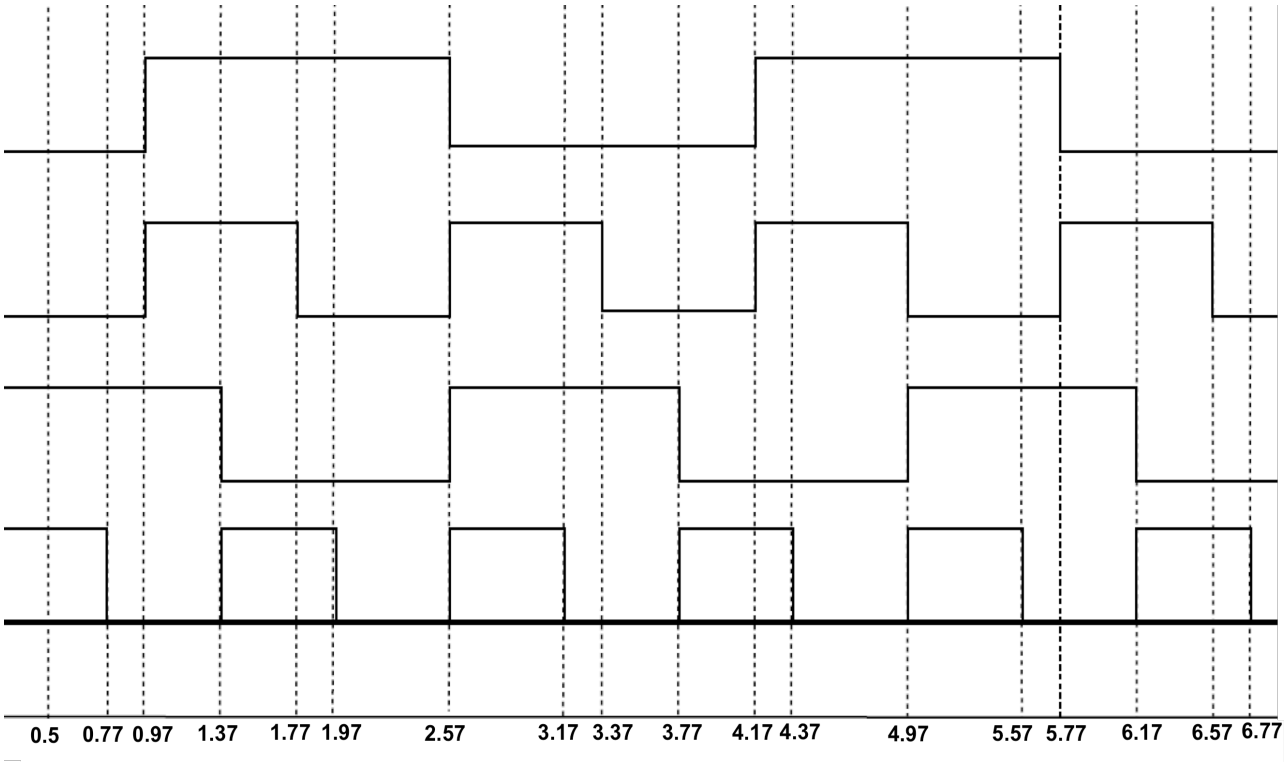
Objective: Design and verify a four-input parity generator consisting of three XOR gates in the 45 nm CMOS technology.



You can choose any logic circuit style (static CMOS, complementary pass logic or transmission gate based logic). The nominal supply voltage is set to 1.1 Volts. The circuit should drive an external load of 12 fF in addition to the internal parasitic capacitances that exist in the circuit. Assume 100 ps of rise/fall times for your input signals.

Design constraints: The primary design objective is to minimize the power-delay product of the circuit for the input pattern provided below. Delay should correspond to the worst case delay between input and output. Power should correspond to the average power consumption over 7 ns for the input pattern below. In the worst case, the circuit should have a propagation delay of no more than 200 ps.



To determine average power consumption, you should plot the overall transient current drawn from the power supply of 1.1 Volts. Then, you should calculate the average current using the calculator tool's ``average" function and multiply the result with 1.1 volts.

For your final schematic design, draw the layout. The secondary objective is to minimize the area of the layout. Pass DRC, LVS and simulate the extracted netlist. Determine power-delay product of the extracted netlist.

REPORT: In your report, explain how you how you decided the W/L ratios of the transistors in your circuit. If you iterated over multiple ratios, include the important iterations in your report as well as final values of the W/L ratios. For your final design, include screen snapshots showing your schematic design, input/output transient simulation results with the marked delay values (for the worst case delay), layout, successful DRC and LVS results, and post layout simulation data.