# ESE 555 | CAD ASSIGNMENT 1

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## 1. LOW-TO-HIGH & HIGH-TO-LOW PROPAGATION MANUAL CALCULATION

### ➢ GIVEN DATA:

[1] $(W/L)_{nmos}$ = 100nm/50nm
[2] $(W/L)_{pmos}$ = 200nm/50nm
[3] $(Vth)_n$ = 0.4106 Volts
[4] $(Vth)_p$ = -0.3842 Volts
[5] $\mu_n$=270cm2/(V-s)
[6] $\mu_p$ =70cm2 /(V-s)
[7] $\varepsilon_{ox}$ =3.97x$\varepsilon$0
[8] $\varepsilon_0$ = 8.85 x $10^{-12}$ (F/m)
[9] $T_{ox,\ nmos}$ = 1.14 X $10^{-9}$ (m)
[10] $T_{ox,\ pmos}$ = 1.26 X $10^{-9}$ (m)
[11] $C_L$ = 2 (fF)

### ➢ PART 1: HIGH TO LOW PROPAGATION DELAY

$$t_{PHL} = \frac{C_{load}}{K_n(V_{DD} - V_{T(n)})}\left[\frac{2\,V_{T(n)}}{V_{DD} - V_{T(n)}} + \ln\left(\frac{4\,(V_{DD} - V_{T(n)}}{V_{DD}} - 1\right)\right]$$

$$= \frac{2\times10^{-15}}{0.1664\times10^{-3}\times(1-0.4106)}\left[\frac{2\times0.4106}{(1-0.4106)} + \ln\left(\frac{4\,(1-0.4106)}{1} - 1\right)\right]$$

$$= 2.0389\times10^{-12}\times[1.3932 + 0.3057]$$

$$t_{PHL} = 3.4646\times10^{-12}\ ps$$

$$K_n = \mu_n \times \frac{\epsilon_{ox}}{t_{ox\,(nmos)}} \times \frac{W_{nmos}}{L_{nmos}}$$

$$= (270\times10^{-4}) \times \left[\frac{3.97\times8.85\times10^{-12}}{1.14\times10^{-9}}\right] \times \frac{100}{50}$$

$$K_n = 1.6642\times10^{-3}$$

### ➢ PART 2: LOW TO HIGH PROPAGATION DELAY

$$t_{PLH} = \frac{C_{load}}{K_p(V_{DD} - |V_{T(p)}|)}\left[\frac{2\,|V_{T(p)}|}{V_{DD} - |V_{T(p)}|} + \ln\left(\frac{4\,(V_{DD} - |V_{T(p)}|}{V_{DD}} - 1\right)\right]$$

$$= \frac{2\times10^{-15}}{7.807\times10^{-4}\times(1-|-0.3842|)}\left[\frac{2\times|-0.3842|}{(1-|-0.3842|)} + \ln\left(\frac{4\,(1-|-0.3842|)}{1} - 1\right)\right]$$

$$= 4.1597\times10^{-12}\times[1.2478 + 0.3806]$$

$$t_{PLH} = 6.7738\times10^{-12}\ ps$$

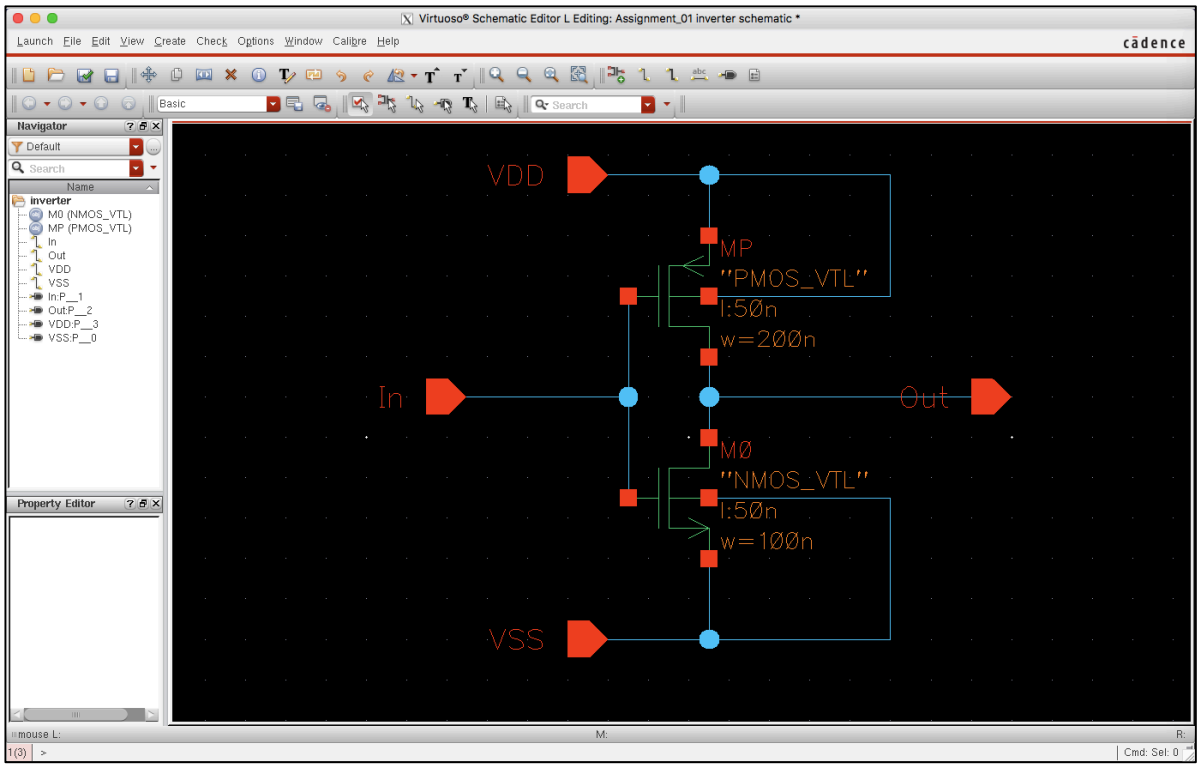
$$K_p = \mu_p \times \frac{\epsilon_{ox}}{t_{ox\,(pmos)}} \times \frac{W_{pmos}}{L_{pmos}}$$

$$= (70\times10^{-4}) \times \left[\frac{3.97\times8.85\times10^{-12}}{1.26\times10^{-9}}\right] \times \frac{200}{50}$$

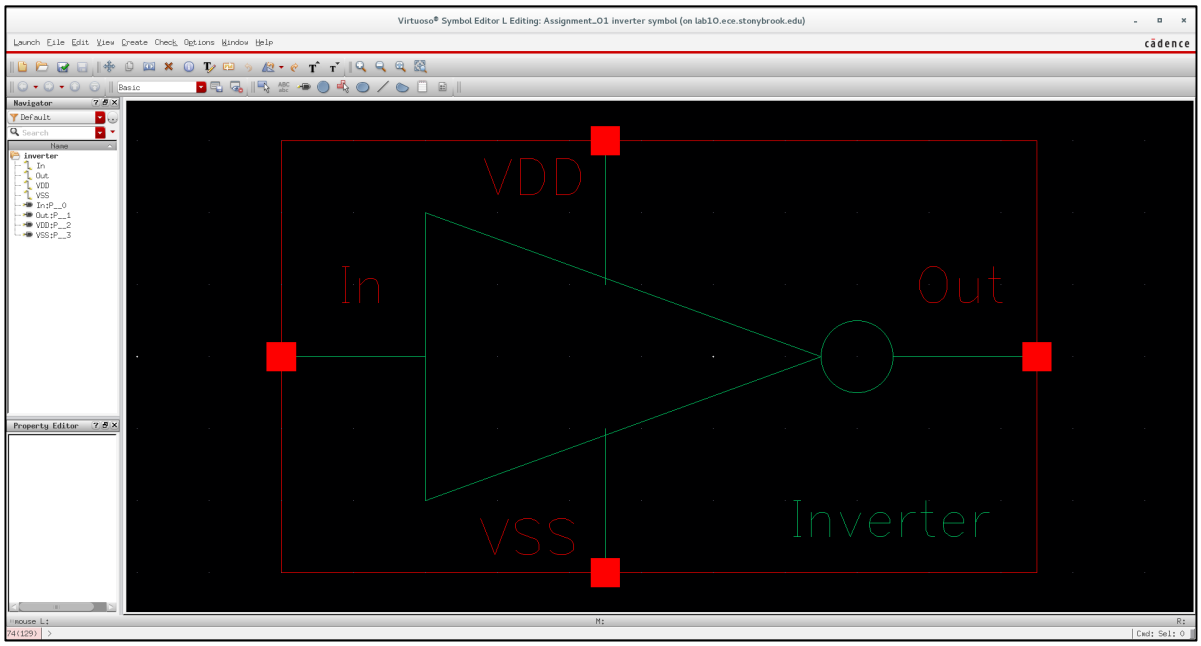
$$K_p = 7.80766\times10^{-4}$$

## 2. PART A – INVERTER DESIGN (Schematic + Symbol + Test Bench)

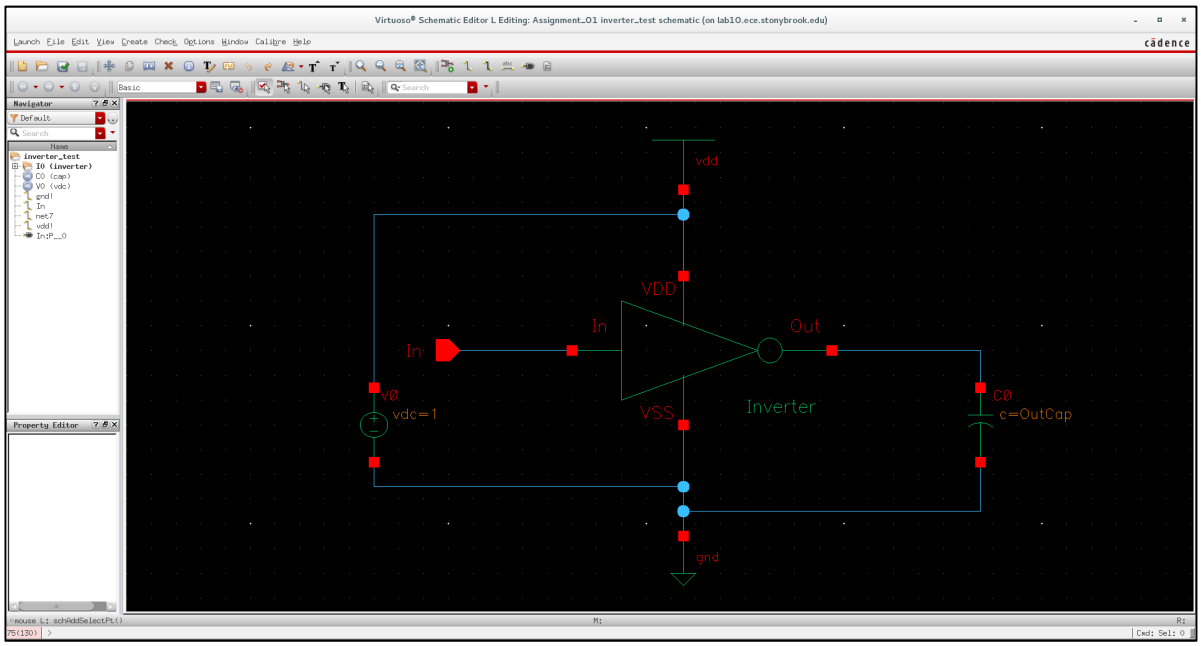
### a. Schematic View of Inverter




### b. Symbol of Inverter

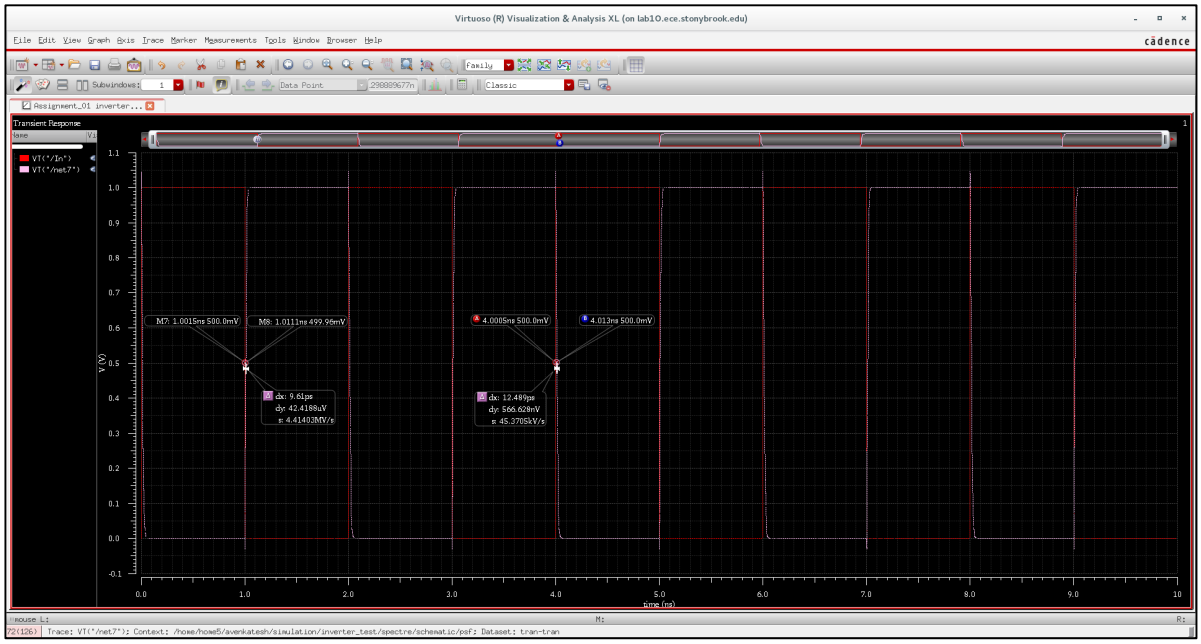


c. Test-Bench Design

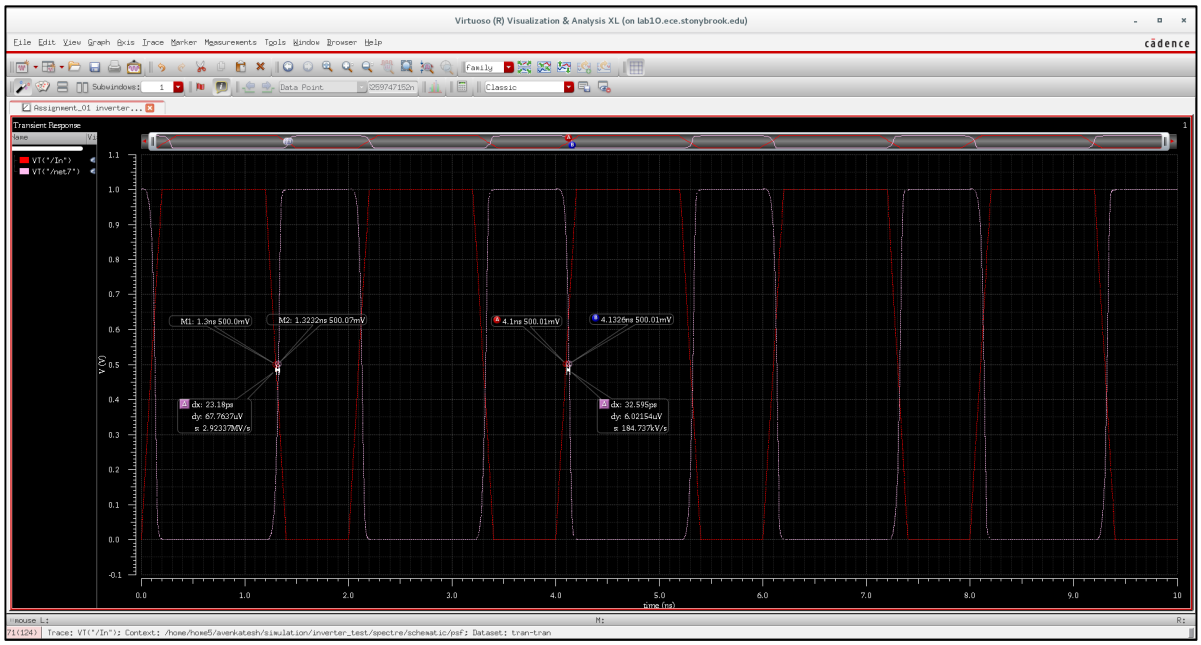



## 2. PART B – LOW-TO-HIGH & HIGH-TO-LOW PROPAGATION DELAY FROM TRANSIENT ANALYSIS

a. $t_{PLH}$ & $t_{PHL}$ | When Rise/Fall times of the input signal is 1ps



b. $t_{PLH}$ & $t_{PLH}$ | When Rise/Fall times of the input signal is 200ps

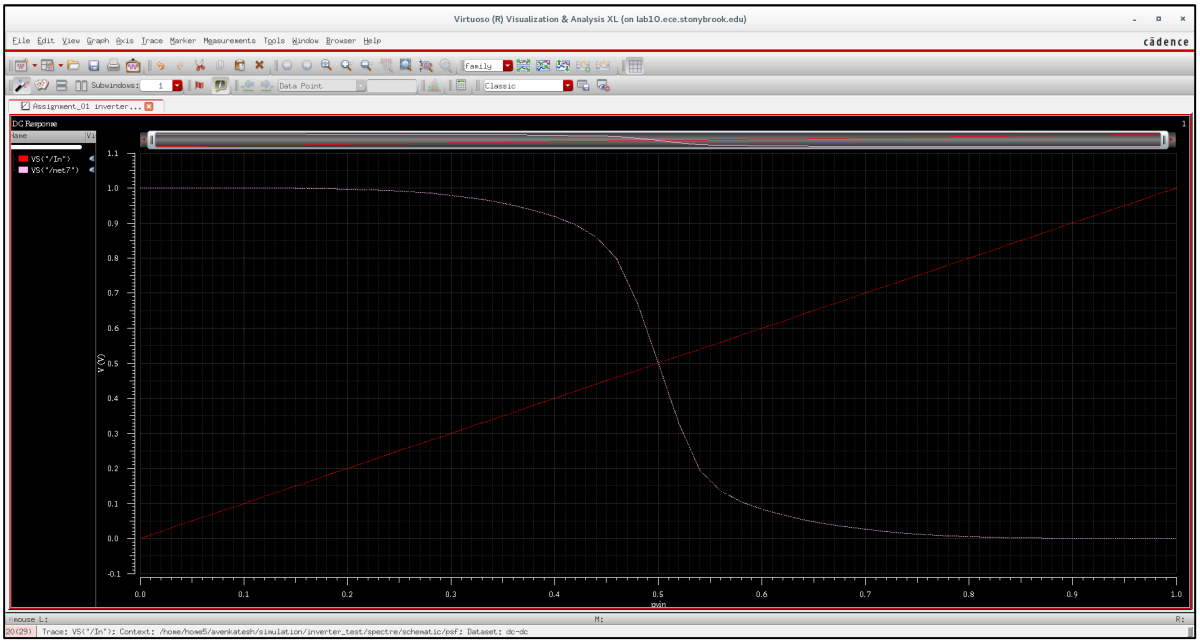



c. Comparison of simulation results with Step 1 manual calculation

> ➢ The average propagation delay computed manually is **3.50ps**, while the average propagation delay measured during simulation is **11.50ps** for **1ps** rise/fall time and **27.89ps** for **200ps** rise/fall time. This difference is delay values is accounted because the limitation and omission of second-order effects in delay model used in Step 1.

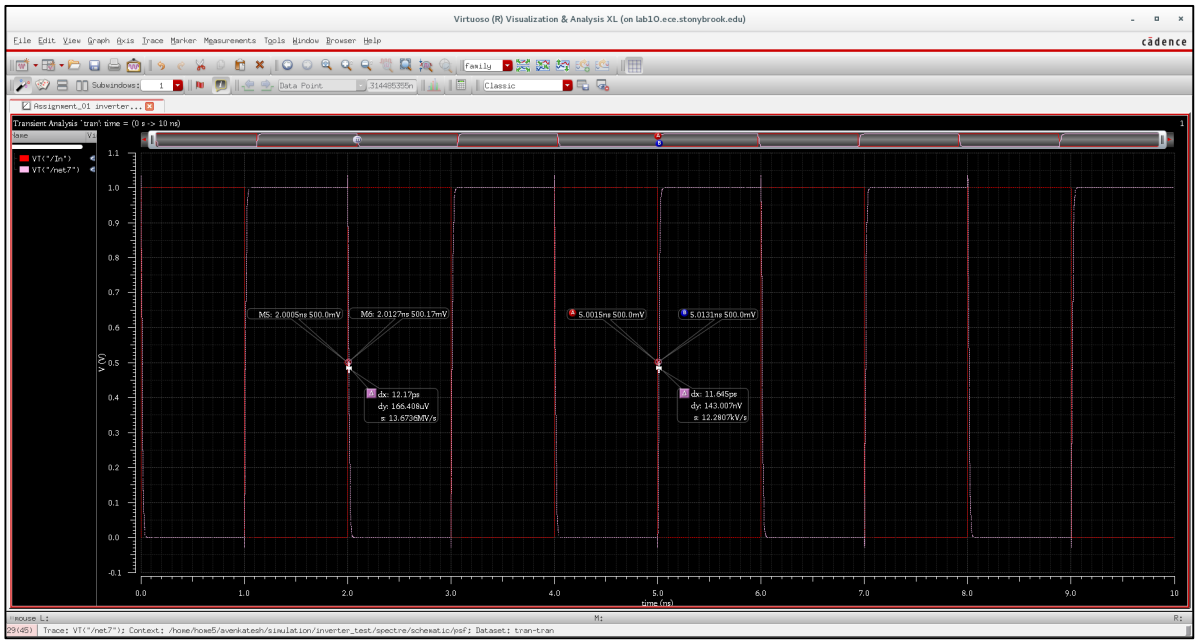
## 3. Symmetric Operation of Inverter

a. DC Transfer Characteristics

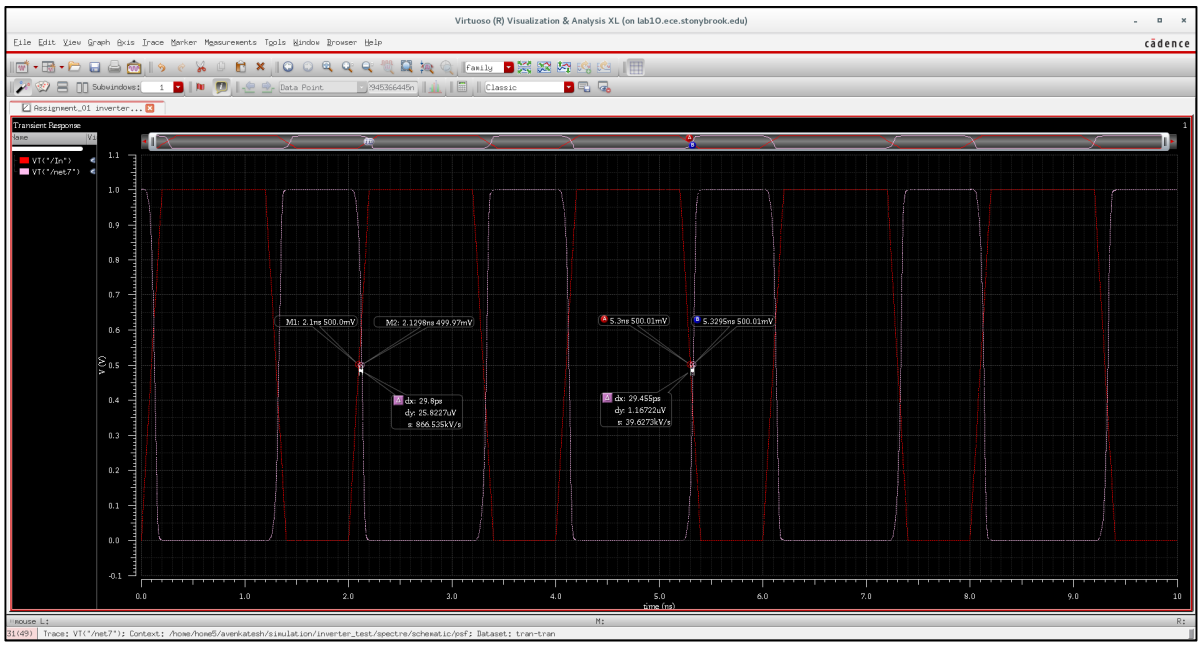


| New Transistor Dimensions for Symmetric Operation | |
|---|---|
| $(W/L)_{nmos}$ = 100nm/50nm | $(W/L)_{pmos}$ = 160nm/50nm |

b. New Transient Analysis - When Rise/Fall times of the input signal is 1ps

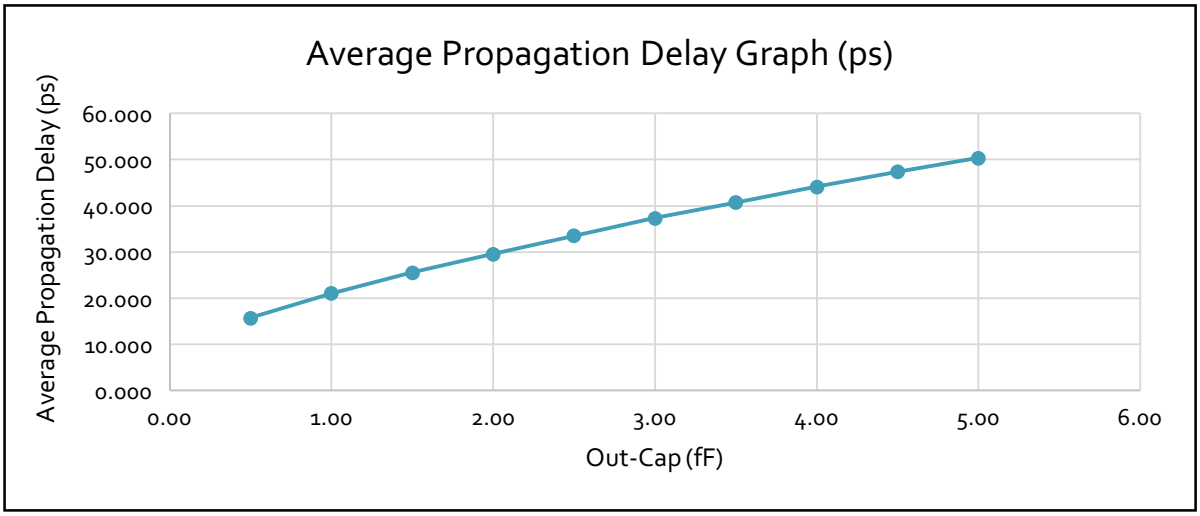



c. New Transient Analysis - When Rise/Fall times of the input signal is 200ps



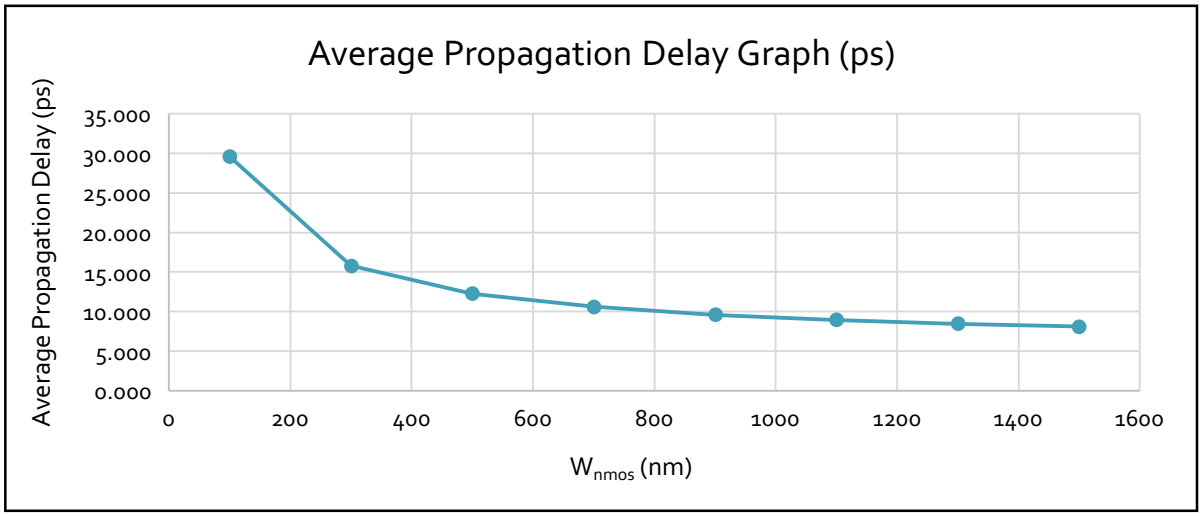
4. Transient Analysis – Sweeping Capacitance from 0.5 fF – 5.0 fF

| Out-Cap (fF) | Propagation delay (ps) | | |
|---|---|---|---|
| | Low to High | High to Low | Average Delay |
| **0.50** | 15.702 | 15.653 | 15.677 |
| **1.00** | 20.974 | 21.068 | 21.021 |
| **1.50** | 25.510 | 25.507 | 25.508 |
| **2.00** | 29.329 | 29.797 | 29.563 |
| **2.50** | 33.421 | 33.613 | 33.517 |
| **3.00** | 37.049 | 37.587 | 37.318 |
| **3.50** | 40.563 | 40.893 | 40.728 |
| **4.00** | 43.882 | 44.396 | 44.139 |
| **4.50** | 47.048 | 47.692 | 47.370 |
| **5.00** | 50.143 | 50.648 | 50.396 |



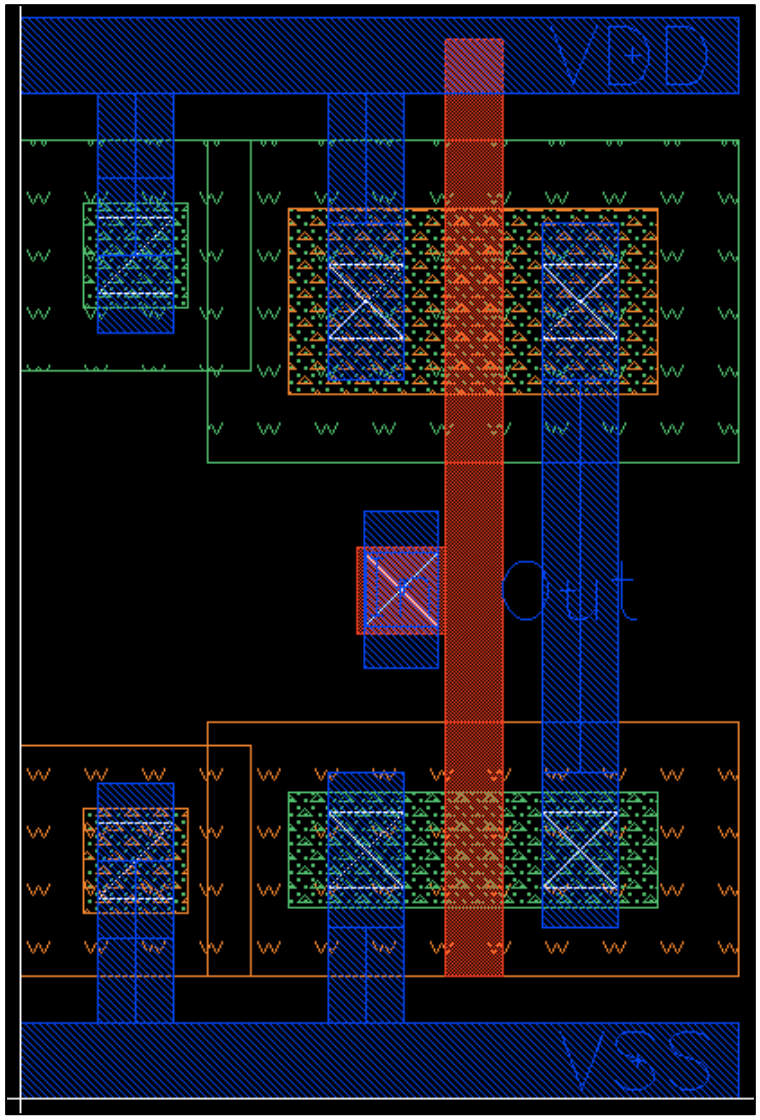

5. Transient Analysis – Sweeping $W_{nmos}$ Until $1.5\mu M$

| Wn (Nmos) | W Pmos | Out-Cap (fF) | Propagation Delay (ps) | | |
|---|---|---|---|---|---|
| | | | Low to High | High to Low | Average Delay |
| **100** | 160 | 2fF | 29.329 | 29.797 | 29.563 |
| **300** | 480 | 2fF | 16.157 | 15.415 | 15.786 |
| **500** | 800 | 2fF | 12.667 | 11.850 | 12.258 |
| **700** | 1120 | 2fF | 11.030 | 10.172 | 10.601 |
| **900** | 1440 | 2fF | 10.039 | 9.159 | 9.599 |
| **1100** | 1760 | 2fF | 9.393 | 8.513 | 8.953 |
| **1300** | 2080 | 2fF | 8.813 | 8.088 | 8.450 |
| **1500** | 2400 | 2fF | 8.488 | 7.735 | 8.112 |




## 6. Inverter Layout I DRC & LVS

a. Inverter Layout



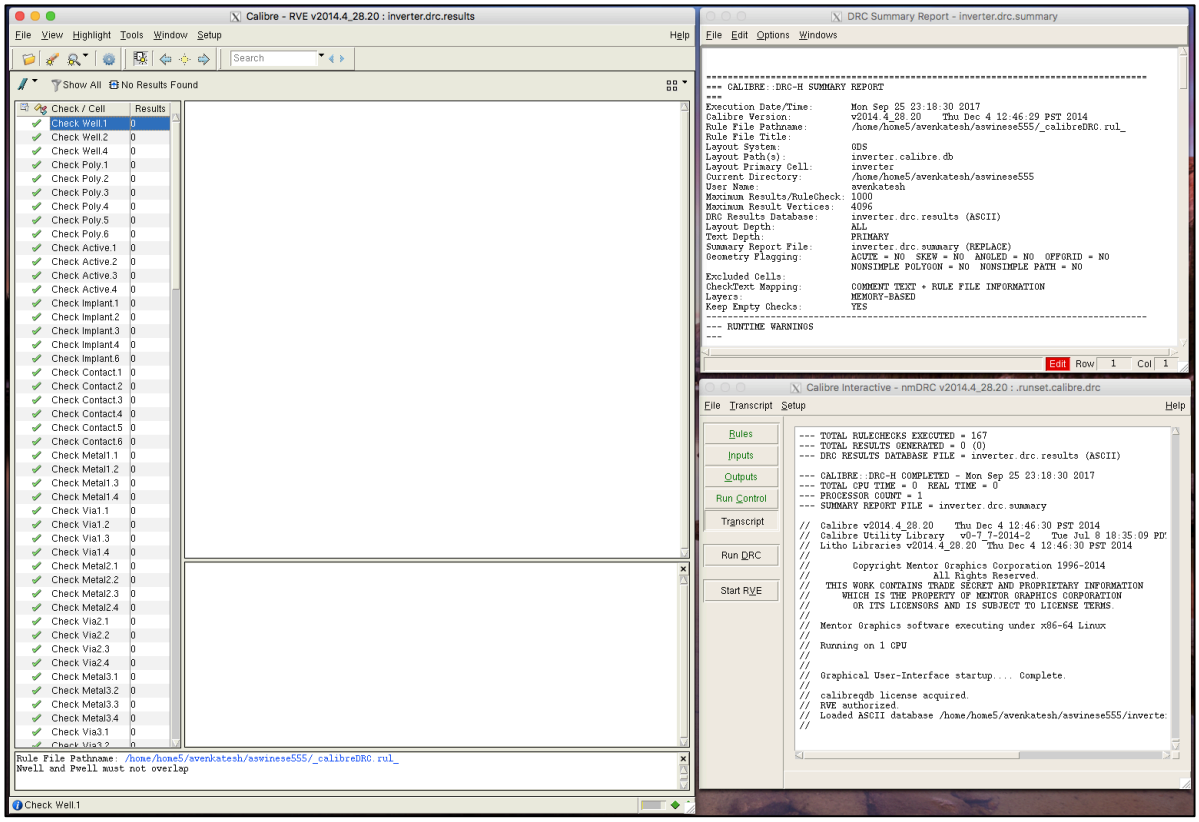

$P_{mos}$ Dimensions

Width : 160 n
Length : 50 n

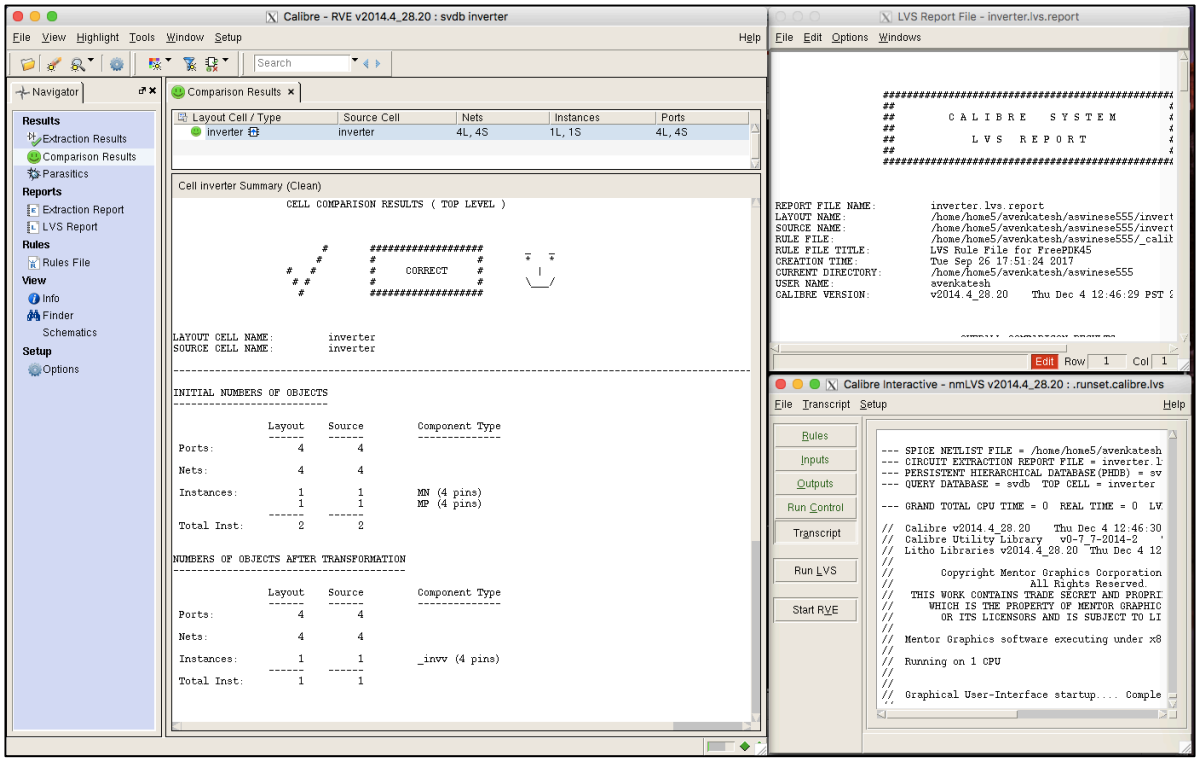
$N_{mos}$ Dimensions

Width : 100 n
Length : 50 n

## b. DRC – Successful

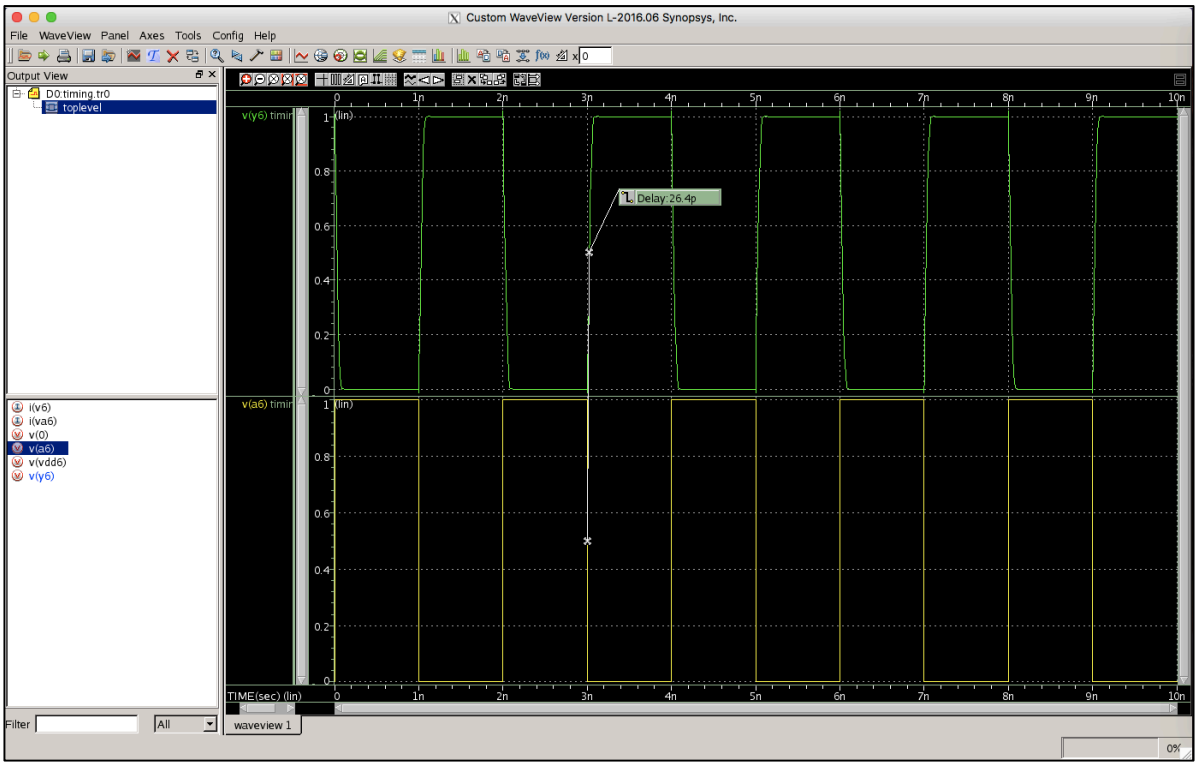



## c. LVS – Successful

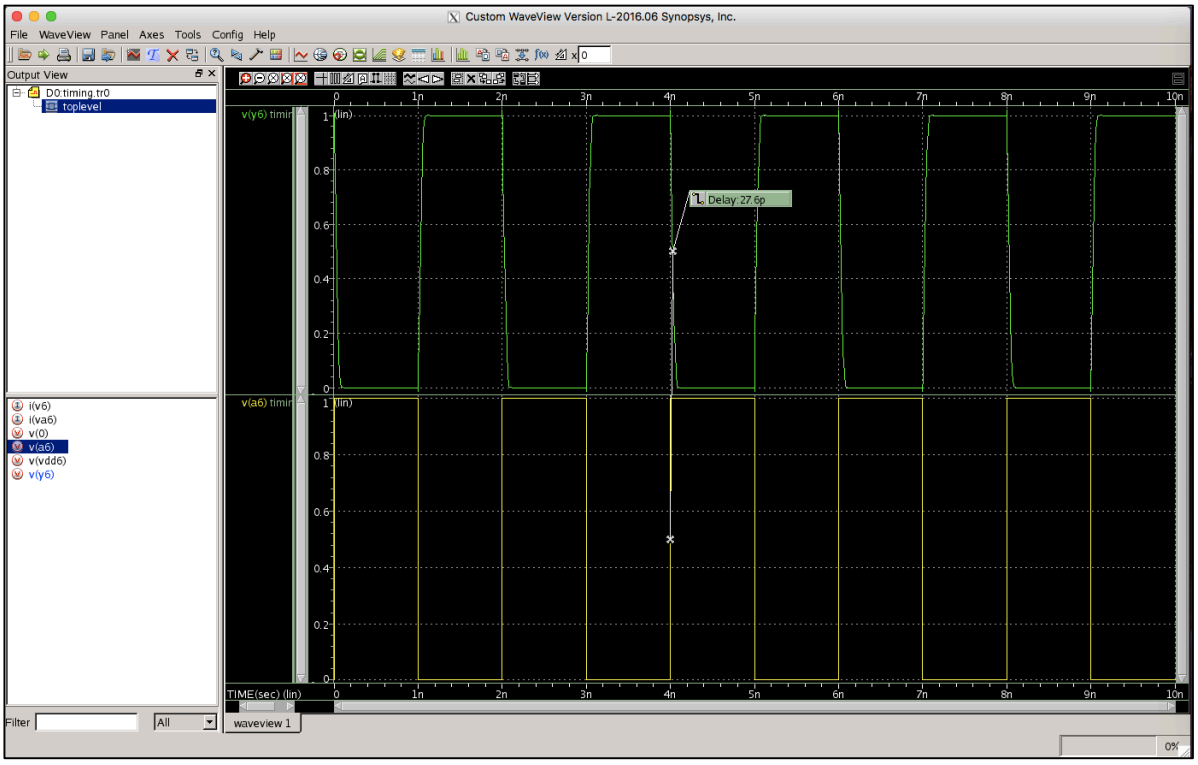


## 7. HSPICE SIMULATION

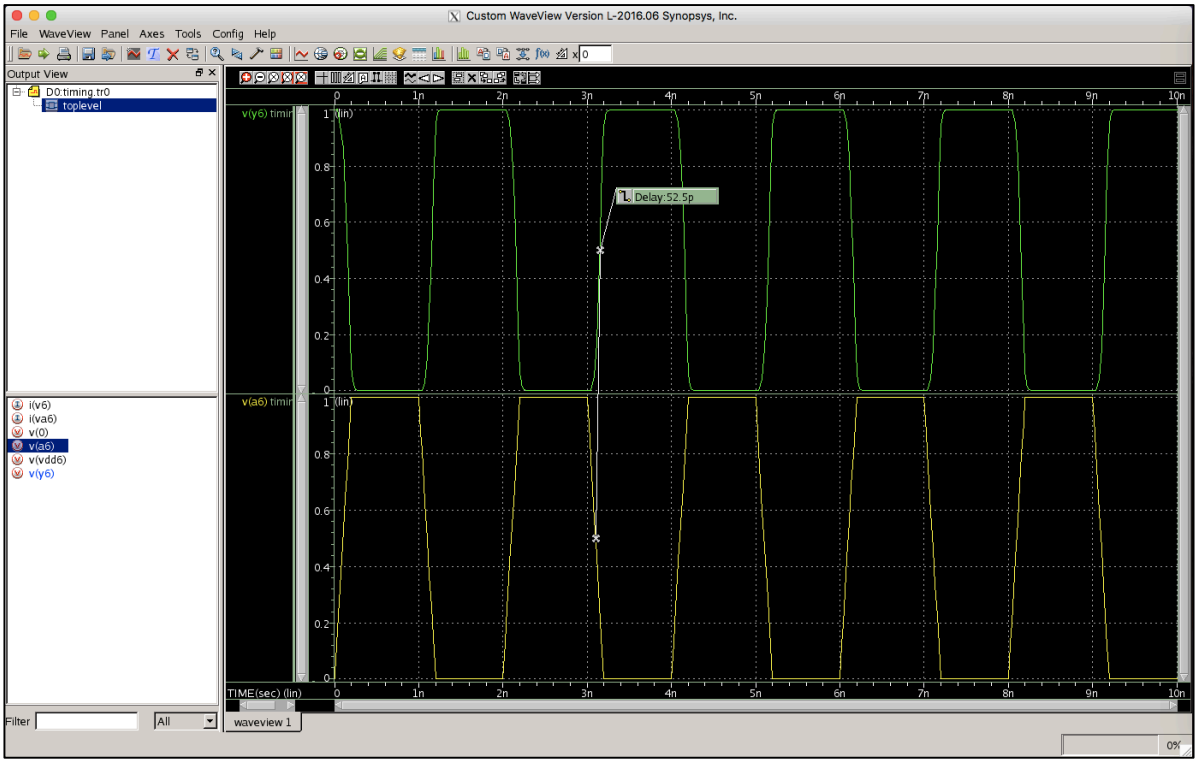
a. Transient Analysis | When Rise/Fall times of the input signal is 1ps | $\tau_{PLH}$



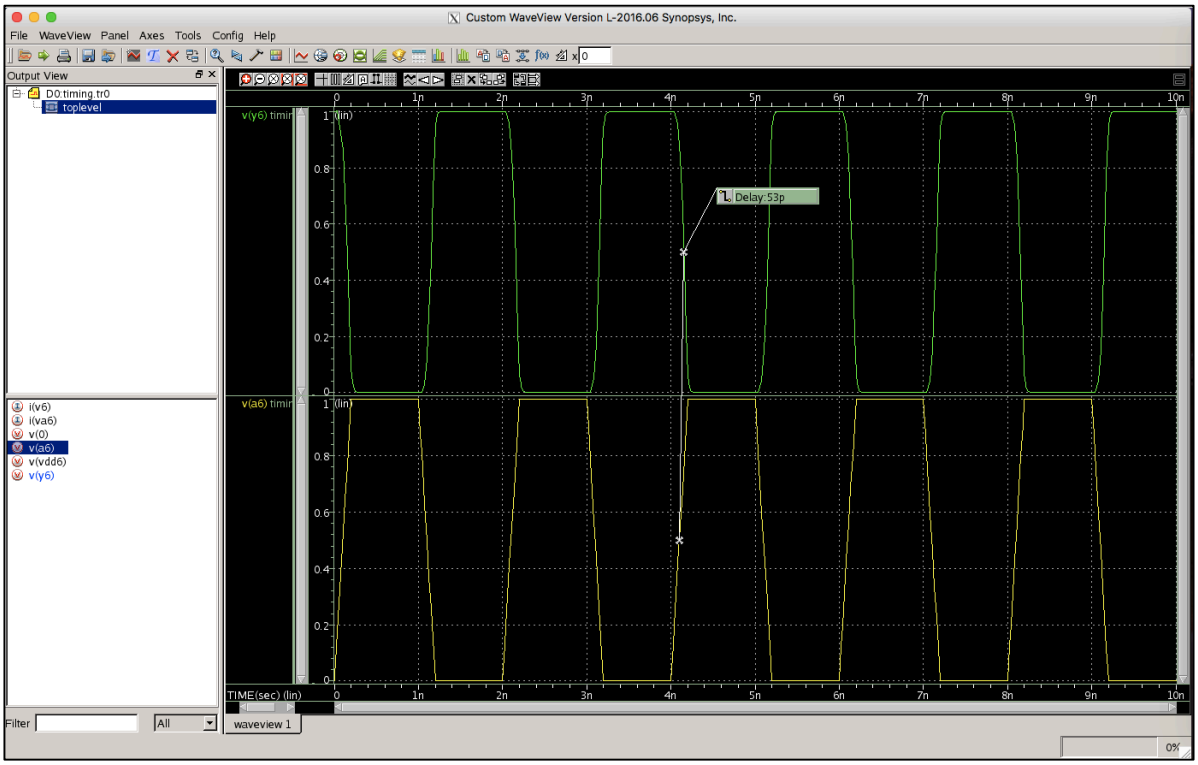

Transient Analysis | When Rise/Fall times of the input signal is 1ps | $\tau_{PHL}$



b. Transient Analysis | When Rise/Fall times of the input signal is 200ps | $\tau_{PLH}$




Transient Analysis | When Rise/Fall times of the input signal is 200ps | $\tau_{PHL}$



c. Summary of Transient Analysis

| Stages of Assignment | W Nmos | W Pmos | Out Cap (fF) | Propagation Delay (ps) | | |
|---|---|---|---|---|---|---|
| | | | | Low to High | High to Low | Average delay |
| Question 1 - Manual Calc. | 100 | 200 | 2.00 | 3.54 | 3.46 | 3.50 |
| Question 2 - Part A (1 ps) | 100 | 200 | 2.00 | 9.61 | 12.49 | 11.05 |
| Question 2 - Part B (200 ps) | 100 | 200 | 2.00 | 23.18 | 32.60 | 27.89 |
| Question 3 - Part A (1 ps) | 100 | 160 | 2.00 | 12.17 | 11.65 | 11.91 |
| Question 3 - Part B (200 ps) | 100 | 160 | 2.00 | 29.80 | 29.46 | 29.63 |
| HSPICE - Part A (1 ps) | 100 | 160 | 2.00 | 26.40 | 27.60 | 27.00 |
| HSPICE - Part B (200 ps) | 100 | 160 | 2.00 | 52.50 | 53.00 | 52.75 |

- The average propagation delay in Schematic netlist for the modified transistor size is **11.91ps** for **1ps** rise/fall time, while in HSPICE extracted netlist the average propagation delay is **52.75ps** for the same rise/fall time.
- The average propagation delay in Schematic netlist for the modified transistor size is **29.63ps** for **200ps** rise/fall time, while in HSPICE extracted netlist the average propagation delay is **27.00ps** for the same rise/fall time.

**-----END OF REPORT -----**

**APPENDIX:** HPSICE INPUT MODEL FILE

# APPENDIX

```
**** include 45nm model file
.prot
.inc '/usr/local/cds/freepdk45/ncsu_basekit/models/hspice/hspice_nom.include'
.inc 'inverter.pex.netlist'
.unpr

**** set nominal supply voltage
.param pvdd=1.0

**** set temperature and global ground
.param ptemp=25
.param gnd=0

**** set timing parameters
.param freq=0.5g
.param peri=1/freq
.param load=5ff
.param rt=200p
.param on=peri*0.5-rt
.param stop=5*peri
**** number of cycles
**** set inverter input and output
v6 vdd6 0 pvdd
c6 y6 0 load
va6 a6 0 pulse (0 pvdd 0 rt rt on peri)

**** instantiate inverter
xinvx1 a6 0 vdd6 y6 inverter
**** set conditions and options
.ic v(xinvx1.y6)=0

.temp ptemp
.option macmod=1 captab post

**** measure delays, output slews, and switching powers
** invx1
.measure tran iavg6 avg i(v6) from=0 to=stop
.measure tran rise6 trig v(y6) val=pvdd*0.1 td=2n rise=1 targ v(y6) val=pvdd*0.9 td=2n rise=1
.measure tran fall6 trig v(y6) val=pvdd*0.9 td=2n fall=1 targ v(y6) val=pvdd*0.1 td=2n fall=1
.measure tran a6lh trig v(a6) val=pvdd*0.5 td=2n fall=4 targ v(y6) val=pvdd*0.5 td=2n rise=4
.measure tran a6hl trig v(a6) val=pvdd*0.5 td=2n rise=4 targ v(y6) val=pvdd*0.5 td=2n fall=4
.measure tran delay6 param='(a6lh+a6hl)/2'
.measure tran power6 param=iavg6*pvdd
.measure tran slew6 param=0.5*rise6+0.5*fall6

.tran 0.01n stop
.end
```

# ESE 555 CAD ASSIGNMENT 1
# Due September 29

**Dr. Emre Salman**
**Electrical and Computer Engineering Department**
**Stony Brook University**

Assume a CMOS inverter designed in a 45 nm technology with the following transistor sizes.

a. (W/L)n = 100 nm / 50 nm
b. (W/L)p = 200 nm / 50 nm

1. Assuming that this inverter drives a capacitive load of 2 fF ($C_{load}$ = 2 fF), calculate the low-to-high and high-to-low propagation delays using the following parameters. Note that the nominal power supply voltage for this technology is 1 Volt. Assume that the input is a step function.

   a. $(V_{th})n$ = 0.4106 Volts
   b. $(V_{th})p$ = -0.3842 Volts
   c. $\mu_n$ = 270 $cm^2$ / (V-s)
   d. $\mu_p$ = 70 $cm^2$ / (V-s)
   e. $\varepsilon_{ox} = 3.97 \times \varepsilon_0$
   f. $\varepsilon_0 = 8.85 \times 10^{-12}$ (F/m)
   g. $T_{ox,\,nmos} = 1.14 \times 10^{-9}$ (m)
   h. $T_{ox,\,pmos} = 1.26 \times 10^{-9}$ (m)

2. Start Cadence and open a new schematic window named “inverter” under the main library. Design this inverter using Cadence schematic view. Generate a symbol. Next, start another schematic window named “inverter_test” under the same library to simulate (transient analysis) the inverter. Provide a pulse waveform as the input with a period of 2 nm and 50% duty cycle. Verify correct functionality. Next, simulate (perform transient analysis for 5 clock cycles, equal to 10 ns) the schematic netlist and determine both the low-to-high and high-to-low propagation delays for the following two cases:

   a. Rise/fall times of the input signal is 1 ps (practically step input)
   b. Rise/fall times of the input signal is 200 ps
   c. Compare the simulation results with the calculation results in Step 1 (Discuss the differences)

3. Obtain the DC transfer characteristic of the inverter by performing a DC analysis in Spectre. In DC analysis, a large signal at the input node will be swept from VSS to VDD and output will be analyzed for each input value. From the DC characteristics, determine if the inverter operation is symmetric. If not, resize the transistors to ensure that the DC transfer curve is symmetric (e.g., Vin=Vout line intersects the transfer function curve at half VDD). Re-perform the transient analysis to determine both low-to-high and high-to-low propagation delays again.

4. After adjusting the sizes in the previous step, sweep the load capacitance from 0.5 fF to 5 fF in steps of 0.5 fF. Perform transient analysis to determine low-to-high and high-to-low propagation delays. Plot average propagation delay ({low-to-high+high-to-low}/2) versus output load capacitance.

5. Keep the output load constant at 2 fF. Also keep the Wp/Wn ratio you found in Step 3 constant. Sweep Wn until 1.5 um (with step size of 200 nm) while keeping Wp/Wn ratio constant, so for each Wn, Wp also changes. Perform transient analysis to determine low-to-high and high-to-low propagation delays. Plot average propagation delay ({low-to-high+high-to-low}/2) versus Wn.

6. Change Wp and Wn back to the values determined in Step 3. Draw a physical layout of the final inverter using Cadence Virtuoso. Successfully pass DRC and LVS.

7. Extract the layout and simulate (perform transient analysis for 5 clock cycles) in HSPICE the extracted netlist to verify functionality. Also simulate both the low-to-high and high-to-low propagation delays for the following two cases:

    a. Rise/fall times of the input signal is 1 ps (practically step input)
    b. Rise/fall times of the input signal is 200 ps
    c. Compare the simulation results (transient analysis) of the extracted netlist with that of the schematic netlist

**REPORT: Your report should answer each question above. For each step except Step 1, you should include screen snapshots showing your schematic design, input/output transient simulation results with the marked delay values, DC transfer curve, layout, successful DRC and LVS results, and post layout simulation data.**

**Calculation required in Step 1 should be readable.**