ESE 555 | CAD ASSIGNMENT 2

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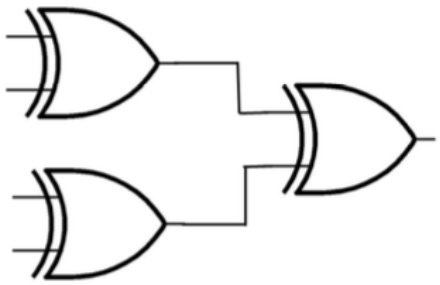
OBJECTIVE:

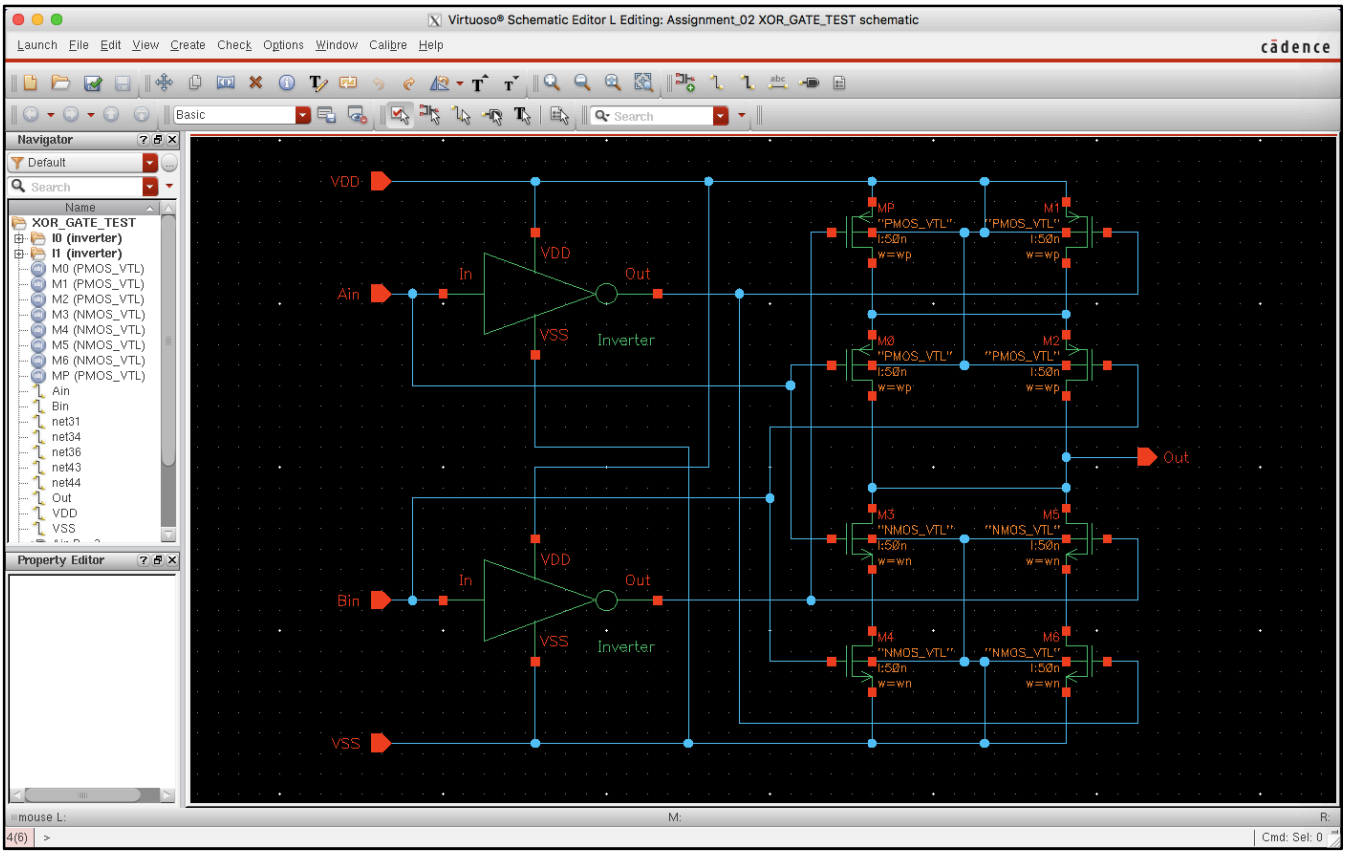
Design and verify a four-input parity generator consisting of three XOR Gates in the 45 nm CMOS technology.



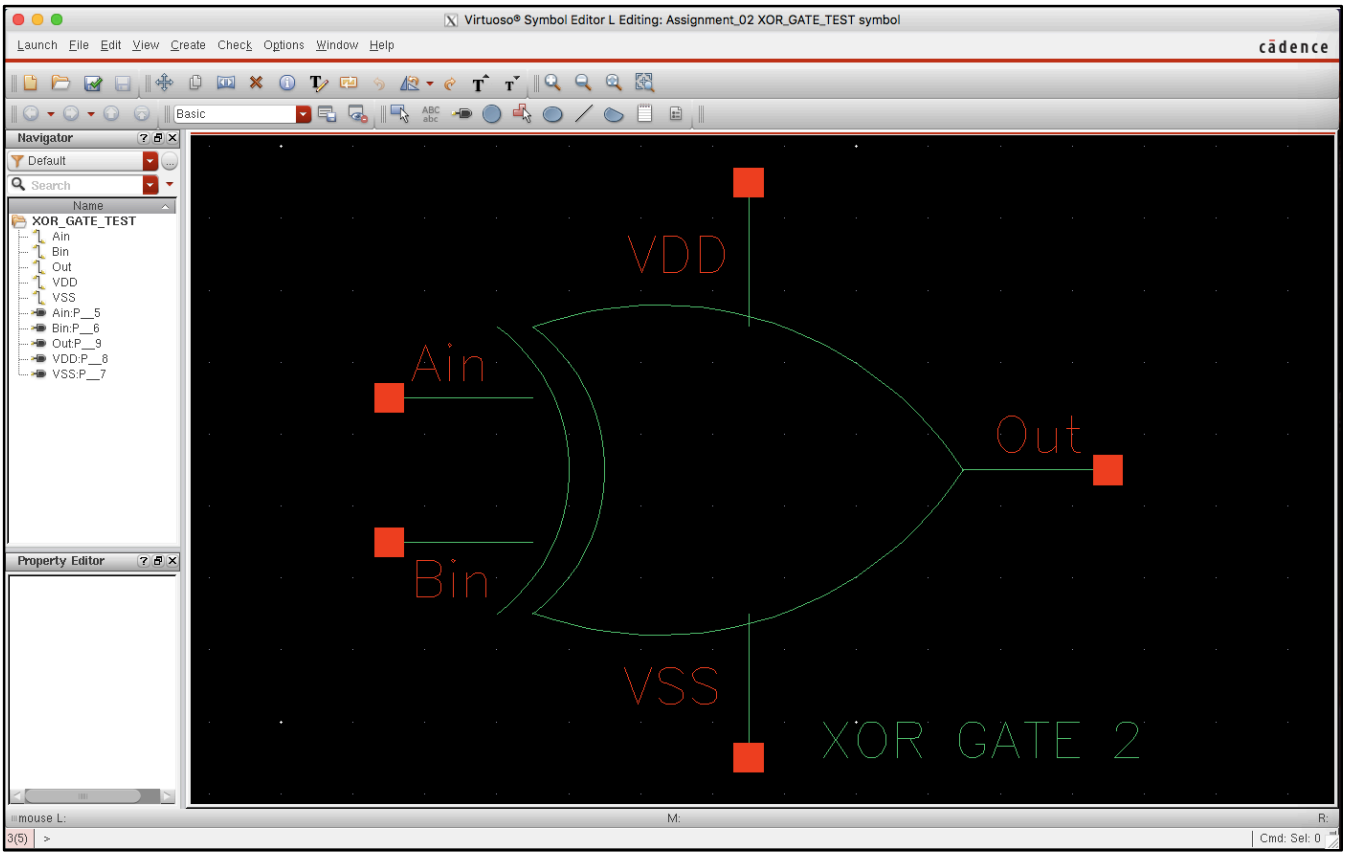
DESIGN SPECIFICATIONS:

- Logic Circuit Style : Static CMOS
- Nominal Supply Voltage : 1.1 V
- External Load : 12 fF
- Rise/Fall Time : 100ps

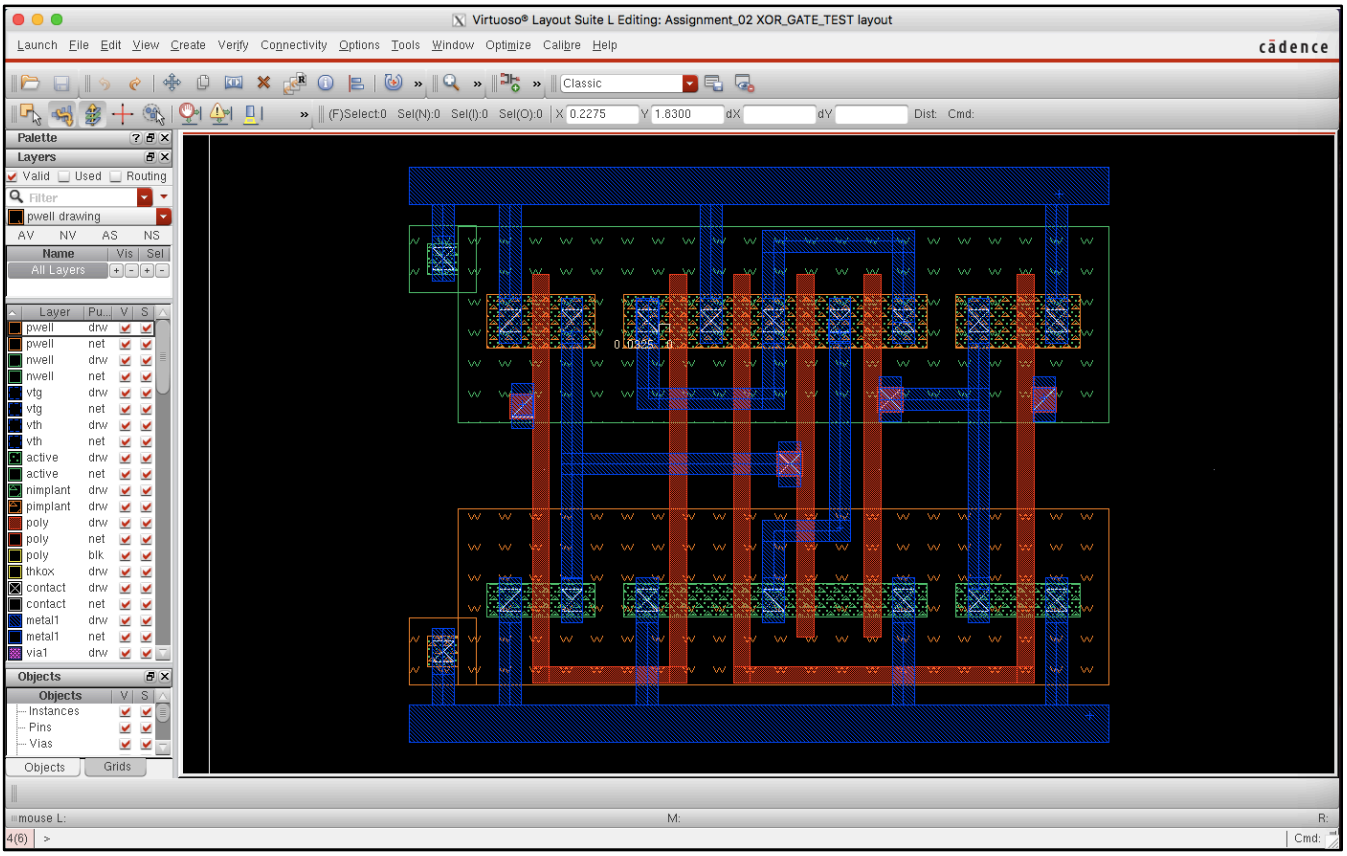
1. XOR Gate Design [Circuit Schematic]



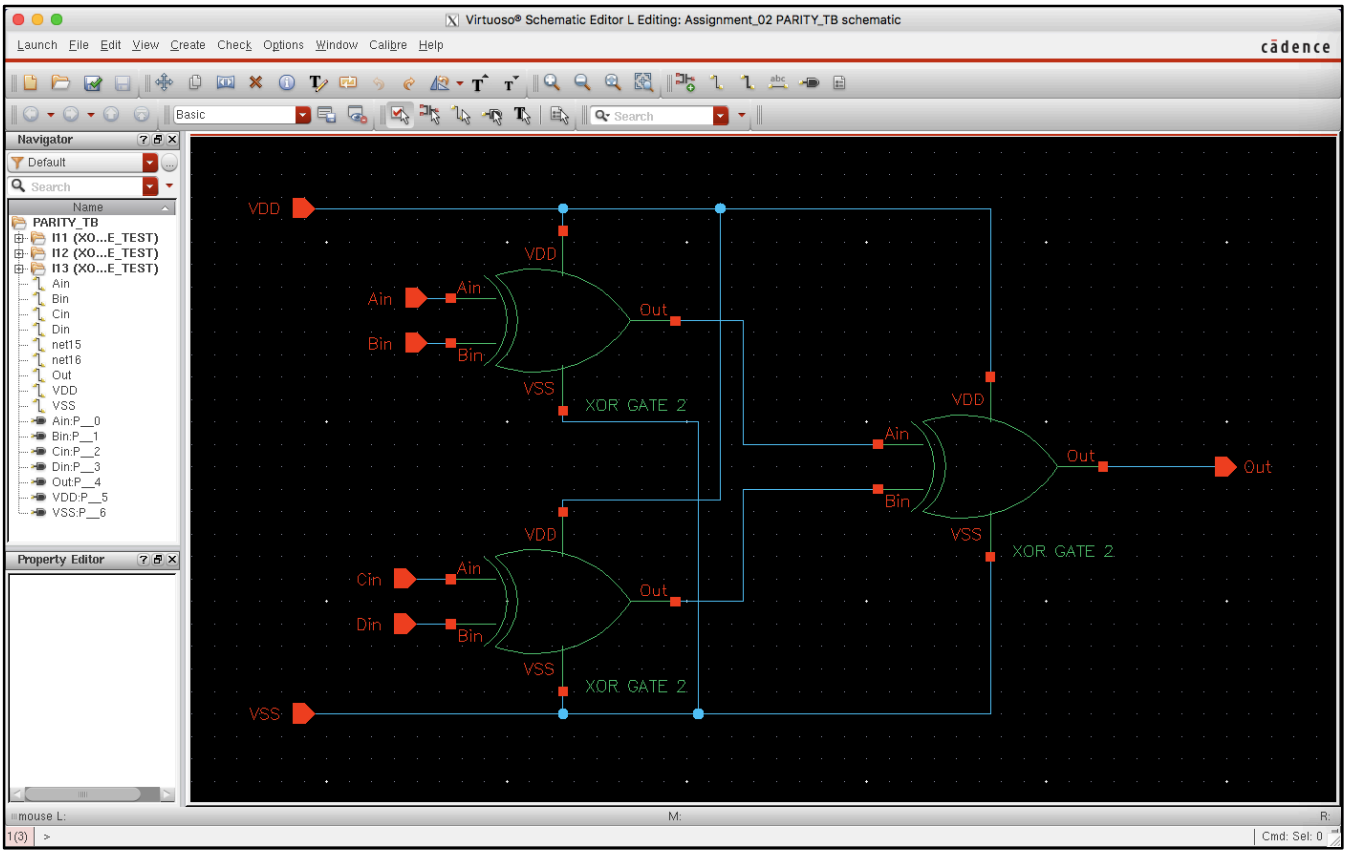
2. XOR Gate Design [Symbol]



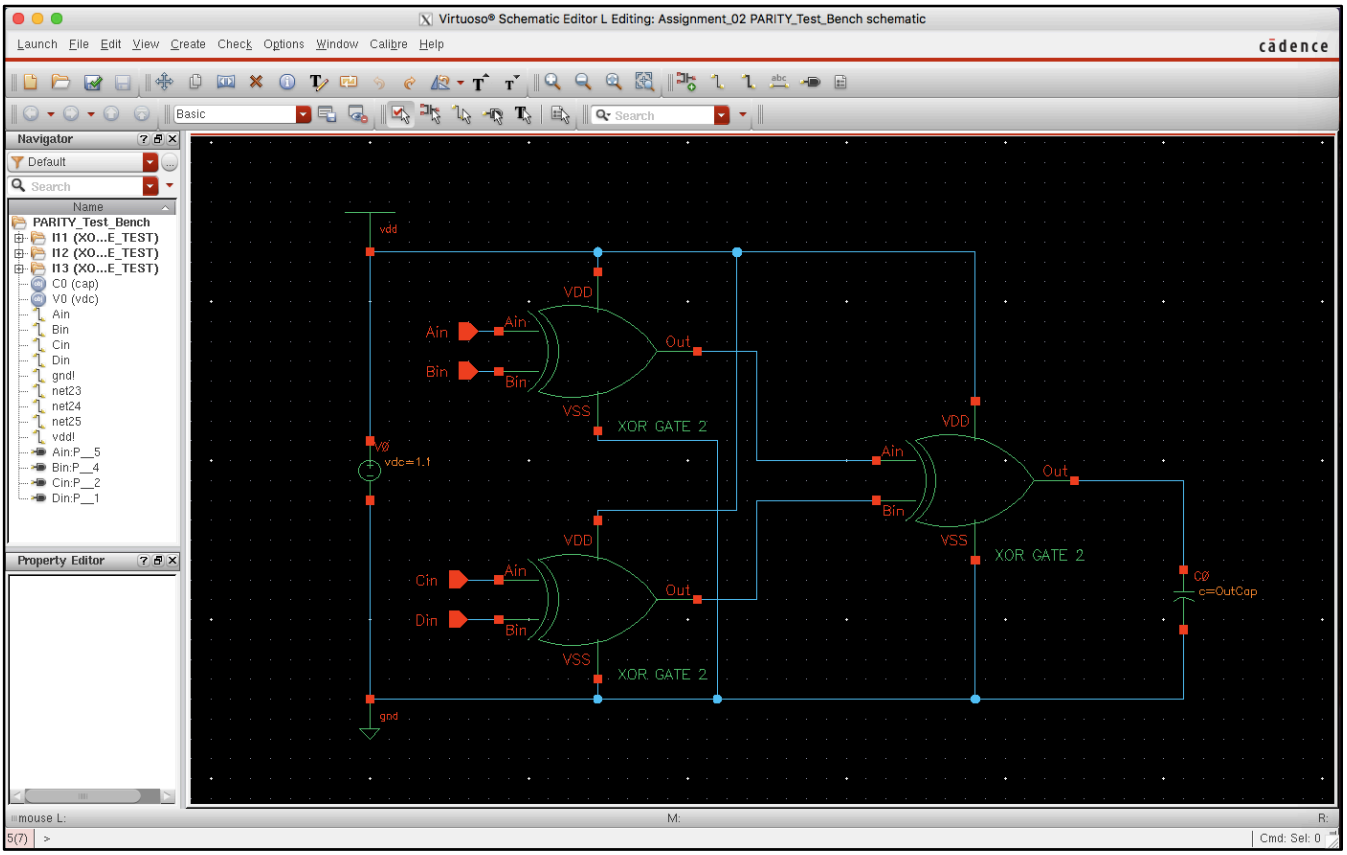
3. XOR Gate Design [Layout]



4. Parity Generator Design [Circuit Schematic]



5. Parity Generator Test-Bench [Circuit Schematic]

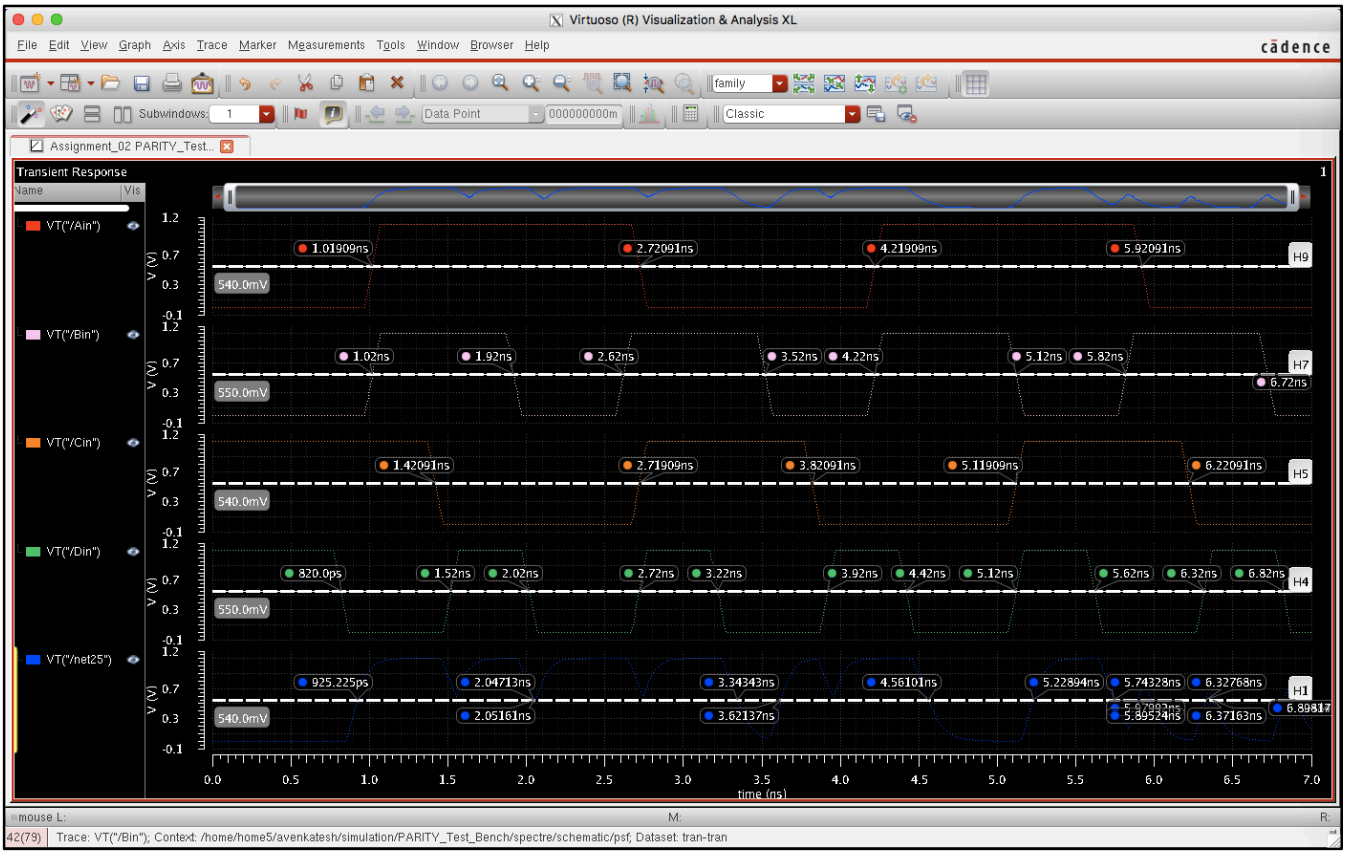


6. Estimating Wn & Wp Ratio for Least Power Delay Product

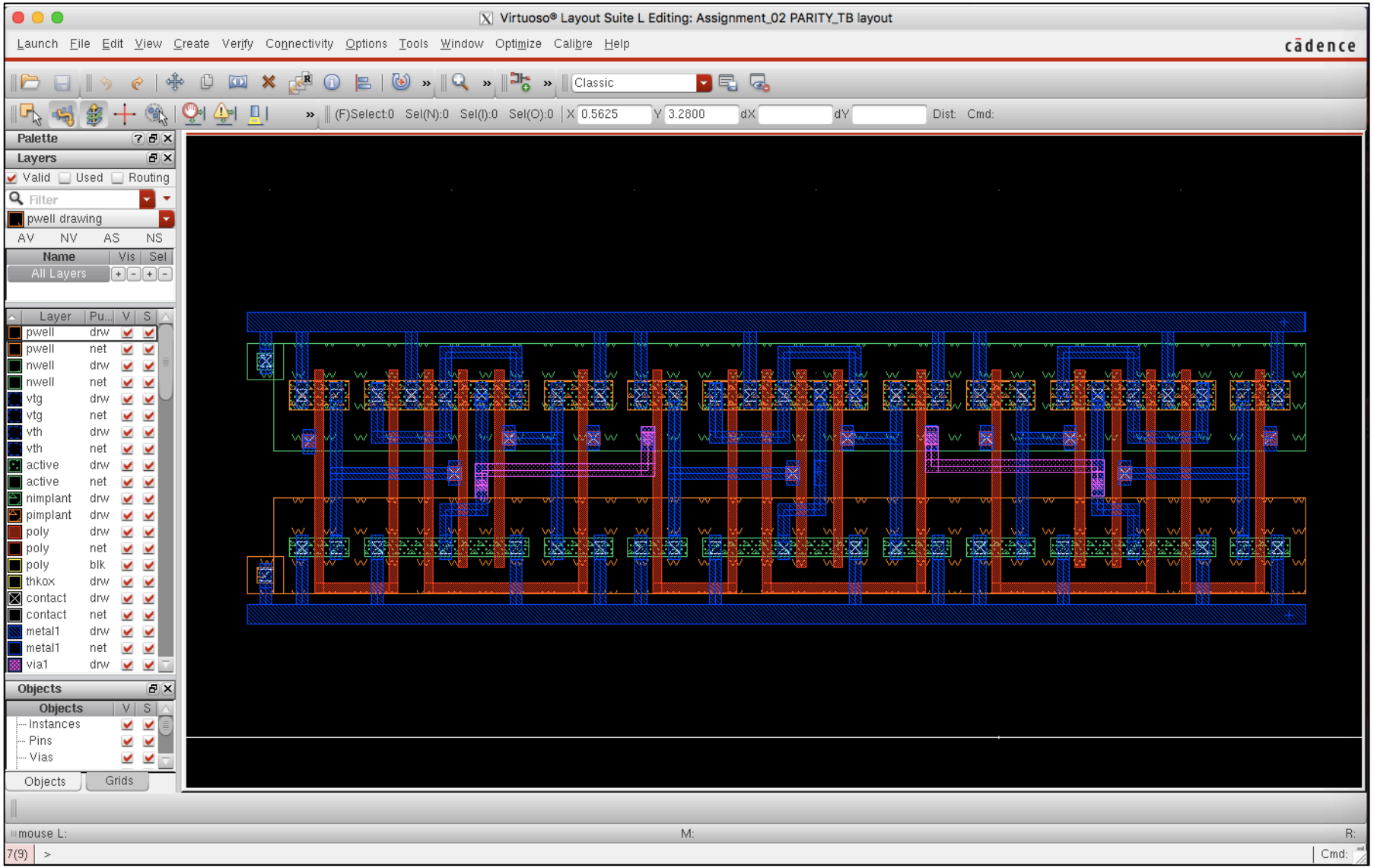
Pmos Width (nM)	Nmos Width (nM)	Average Current (uA)	Voltage (V)	Power (uW)	Average Propagation Delay (t_{phl} & t_{plh}) (pS)	Power Delay Product (WS)
160	100	25.93	1.1	28.52	133.79	3816.05
180	100	27.00	1.1	29.70	128.54	3817.67
140	100	24.80	1.1	27.28	141.70	3865.55
140	90	23.86	1.1	26.25	148.46	3896.47
100	90	22.69	1.1	24.96	159.49	3980.72
120	100	23.58	1.1	25.94	154.58	4009.56
120	90	22.69	1.1	24.96	161.18	4022.85
100	100	22.23	1.1	24.45	168.95	4131.44

Final W/L values for Pmos and Nmos are 160nM and 100nM respectively. This is obtained by iterating multiple W/L ratios and 1.6x yields the lowest power delay product.

7. Transient Analysis – Input & Output Waveform



8. Parity Generator Final Layout [Minimized Area Design]



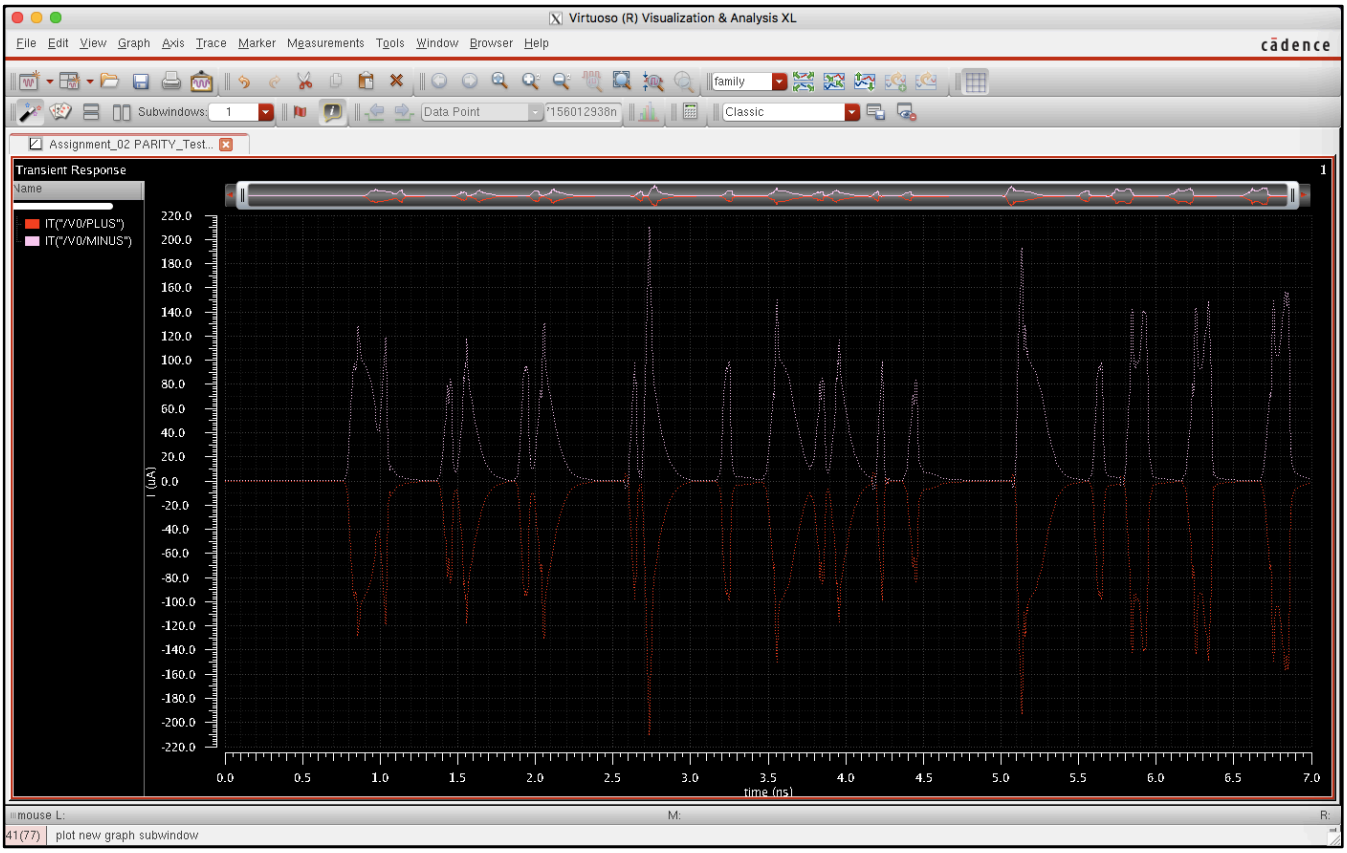
Pmos Dimensions

- Length: 50 n M
- Width: 160n M

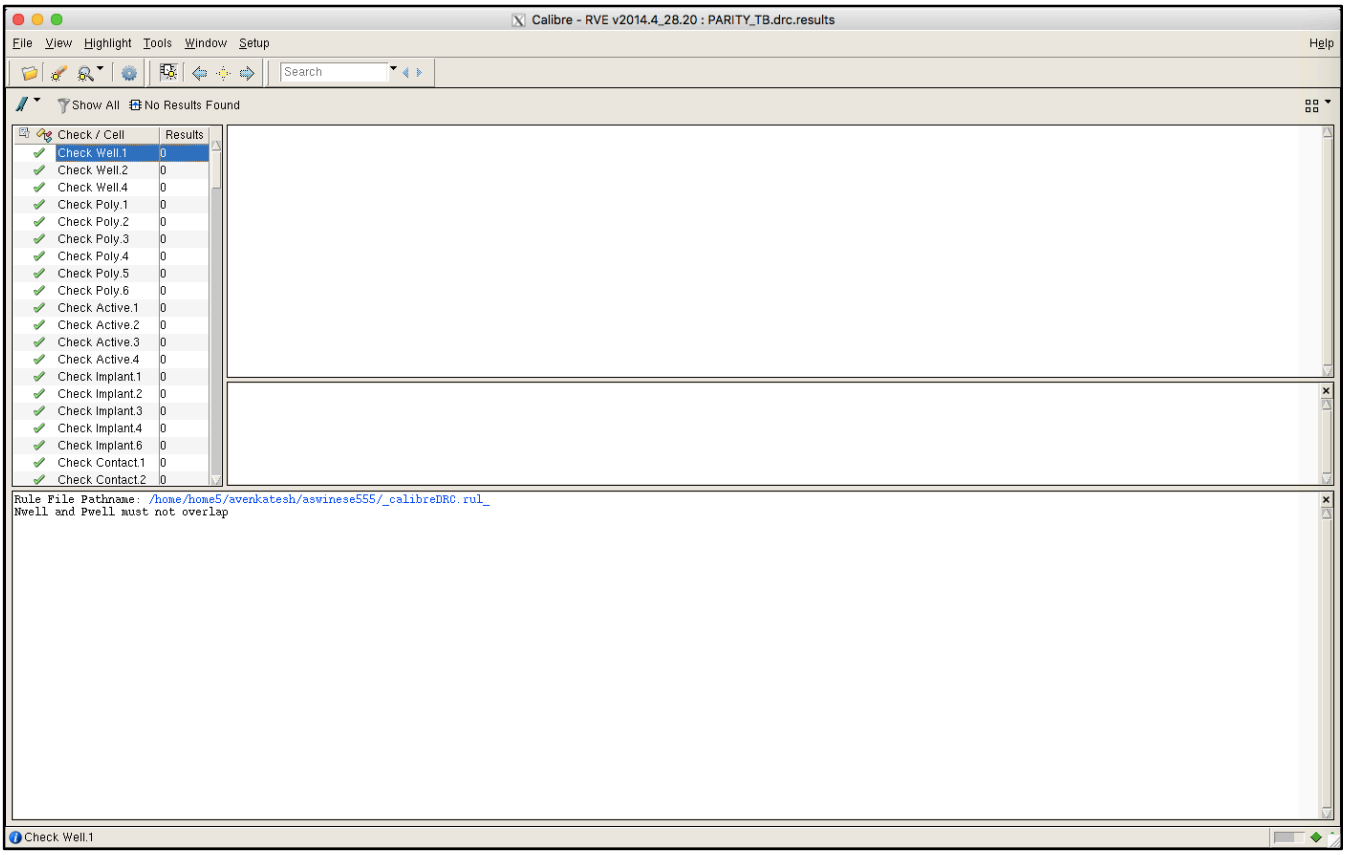
Nmos Dimensions

- Length: 50 n M
- Width: 100n M

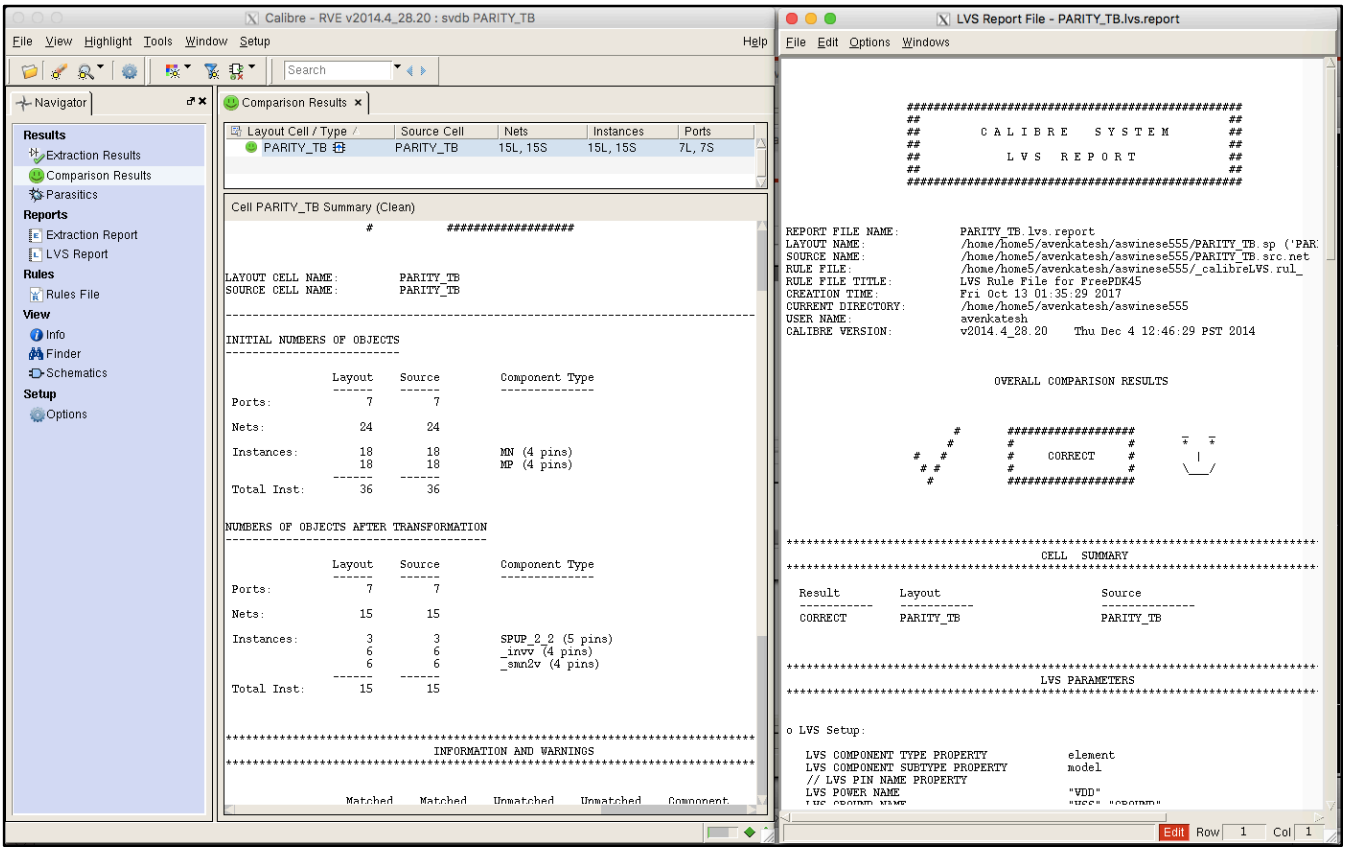
9. Transient Analysis – Current Waveform



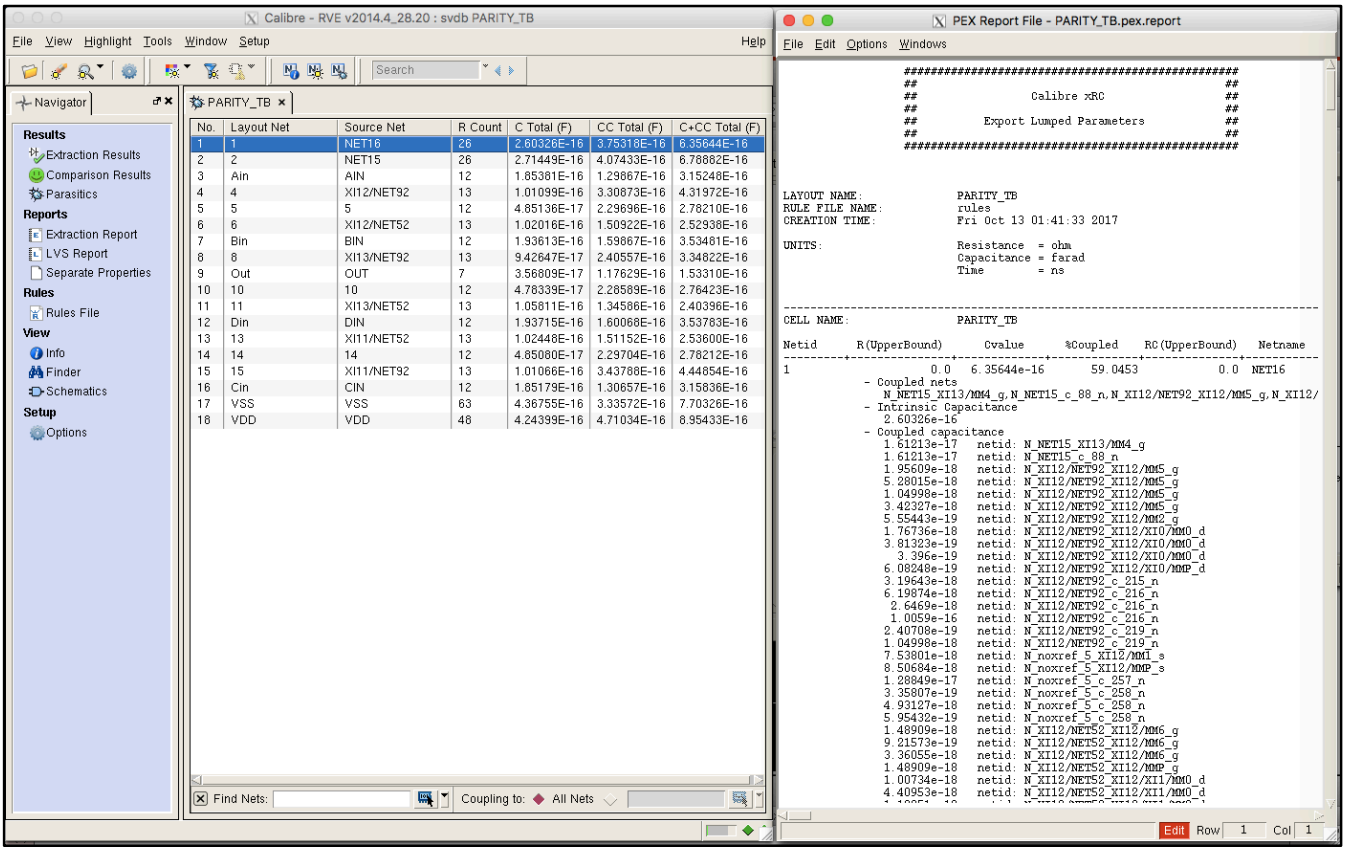
10. Parity Generator Design – DRC Successful Result



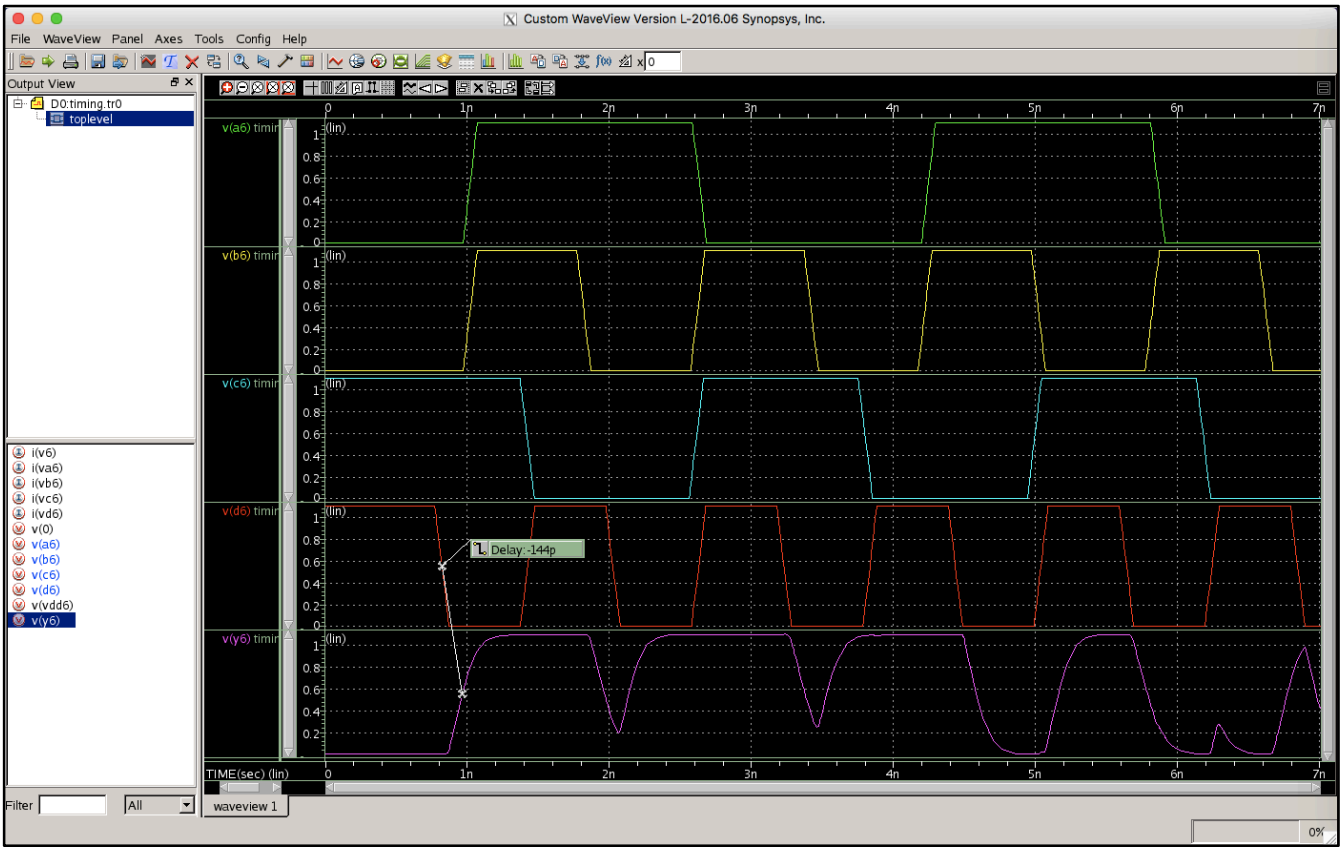
11. Parity Generator Design – LVS Successful Result



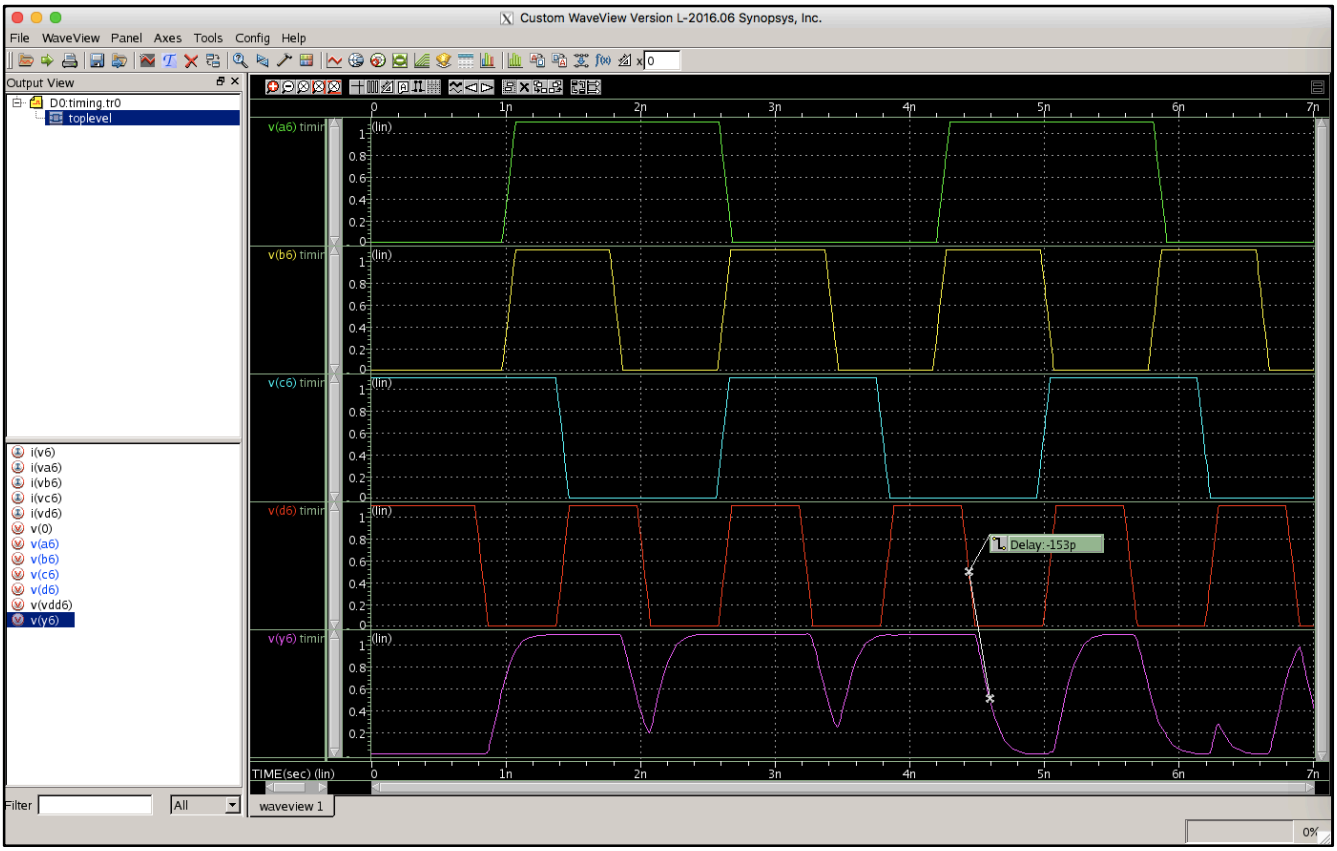
12. Parity Generator Design – PEX Successful Result – Parasitic Capacitances



13. Post Layout Simulation – Low to High Propagation Delay Graph



14. Post Layout Simulation – High to Low Propagation Delay Graph



15. Design Summary

Simulation Results	Final Width of Pmos : 160 nM			Final Width of Nmos : 100 nM				
	Average Current (uA)	Voltage (V)	Power (uW)	Load Capacitance (fF)	Propagation Delay			Power Delay Product (WS)
					t_{phl}	t_{plh}	Avg	
Schematic	25.93	1.1	28.52	12	128.43	139.15	133.79	3816.05
Post layout	25.00	1.1	27.50	12	144.00	153.00	148.50	3817.67

-----END OF REPORT -----

APPENDIX: HPSICE INPUT MODEL FILE

APPENDIX

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************************************************
**** INCLUDE 45NM MODEL FILE
.PROT
.INC '/USR/LOCAL/CDS/FREEPDK45/NCSU_BASEKIT/MODELS/HSPICE/HSPICE_NOM.INCLUDE'
.INC 'PARITY_TB.PEX.NETLIST'
.UNPR

**** SET NOMINAL SUPPLY VOLTAGE
.PARAM PVDD=1.1

**** SET TEMPERATURE AND GLOBAL GROUND
.PARAM PTEMP=25
.PARAM GND=0

**** SET TIMING PARAMETERS
.PARAM FREQA=0.31G
.PARAM FREQB=0.625G
.PARAM FREQC=0.42G
.PARAM FREQD=0.83G
.PARAM PERIA=1/FREQA
.PARAM PERIB=1/FREQB
.PARAM PERIC=1/FREQC
.PARAM PERID=1/FREQD
.PARAM LOAD=12FF
.PARAM RT=100P
.PARAM ONA=PERIA*0.5-RT
.PARAM ONB=PERIB*0.5-RT
.PARAM ONC=PERIC*0.5-RT
.PARAM OND=PERID*0.5-RT
.PARAM STOP=7N

**** SET PARITY INPUT AND OUTPUT
V6 VDD6 0 PVDD
C6 Y6 0 LOAD
VA6 A6 0 PULSE (0 PVDD 0.97N RT RT ONA PERIA)
VB6 B6 0 PULSE (0 PVDD 0.97N RT RT ONB PERIB)
VC6 C6 0 PULSE (PVDD 0  1.37N RT RT ONC PERIC)
VD6 D6 0 PULSE (PVDD 0  0.77N RT RT OND PERID)

**** INSTANTIATE INVERTER
XINVX1 A6 B6 Y6 D6 C6 0 VDD6 PARITY_TB

**** SET CONDITIONS AND OPTIONS
.IC V(XINVX1.Y6)=0

.TEMP PTEMP
.OPTION MACMOD=1 CAPTAB POST

**** MEASURE DELAYS, OUTPUT SLEWS, AND SWITCHING POWERS
** INVX1
.MEASURE TRAN IAVG6 AVG I(V6) FROM=0 TO=STOP
.MEASURE TRAN RISE6 TRIG V(Y6) VAL=PVDD*0.1 TD=2N RISE=1 TARG V(Y6) VAL=PVDD*0.9 TD=2N RISE=1
.MEASURE TRAN FALL6 TRIG V(Y6) VAL=PVDD*0.9 TD=2N FALL=1 TARG V(Y6) VAL=PVDD*0.1 TD=2N FALL=1
.MEASURE TRAN A6LH TRIG V(A6) VAL=PVDD*0.5 TD=2N FALL=4 TARG V(Y6) VAL=PVDD*0.5 TD=2N RISE=4
.MEASURE TRAN A6HL TRIG V(A6) VAL=PVDD*0.5 TD=2N RISE=4 TARG V(Y6) VAL=PVDD*0.5 TD=2N FALL=4
.MEASURE TRAN DELAY6 PARAM='(A6LH+A6HL)/2'
.MEASURE TRAN POWER6 PARAM=IAVG6*PVDD
.MEASURE TRAN SLEW6 PARAM=0.5*RISE6+0.5*FALL6

.TRAN 0.01N STOP
.END
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