ESE 555 | CAD ASSIGNMENT 3

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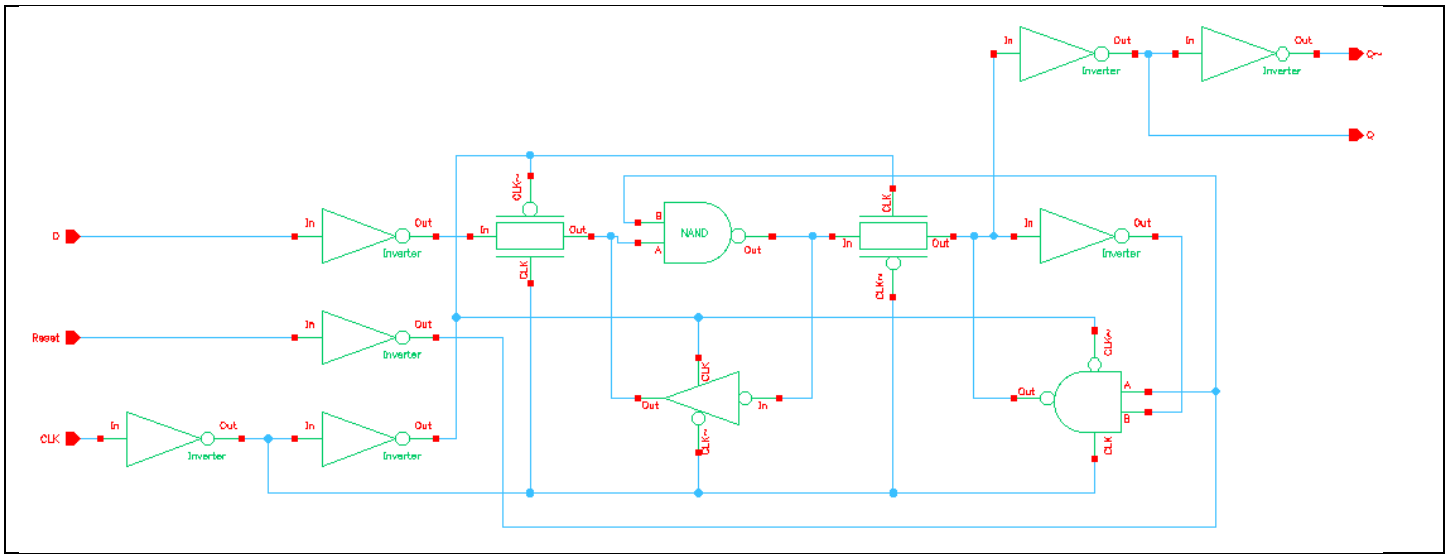
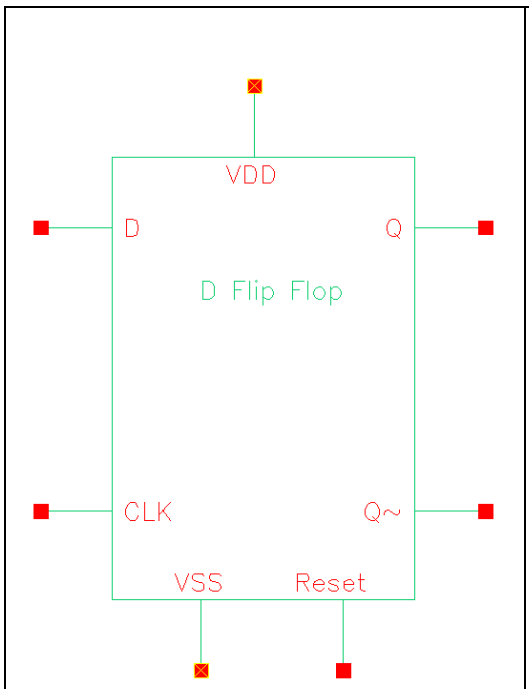
OBJECTIVE:

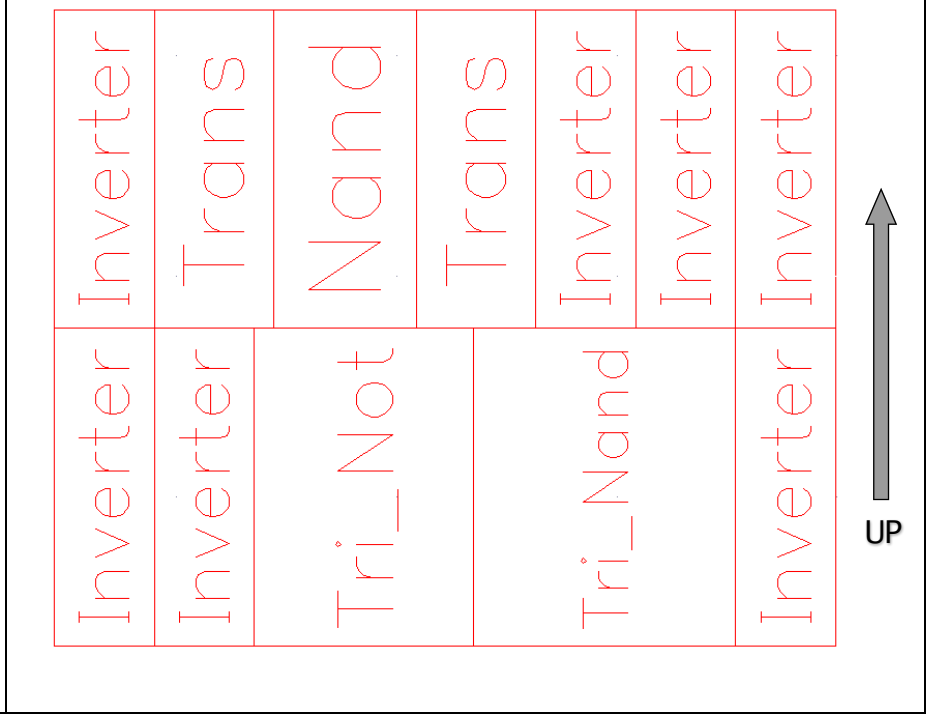
Design and verify a CMOS positive (rising) edge triggered master-slave D type flip-flop with an asynchronous reset (active at logic high) using 45 nm static CMOS technology.

1. **Master-Slave D-Type Flip Flop with Asynchronous Reset** [Circuit Schematic]

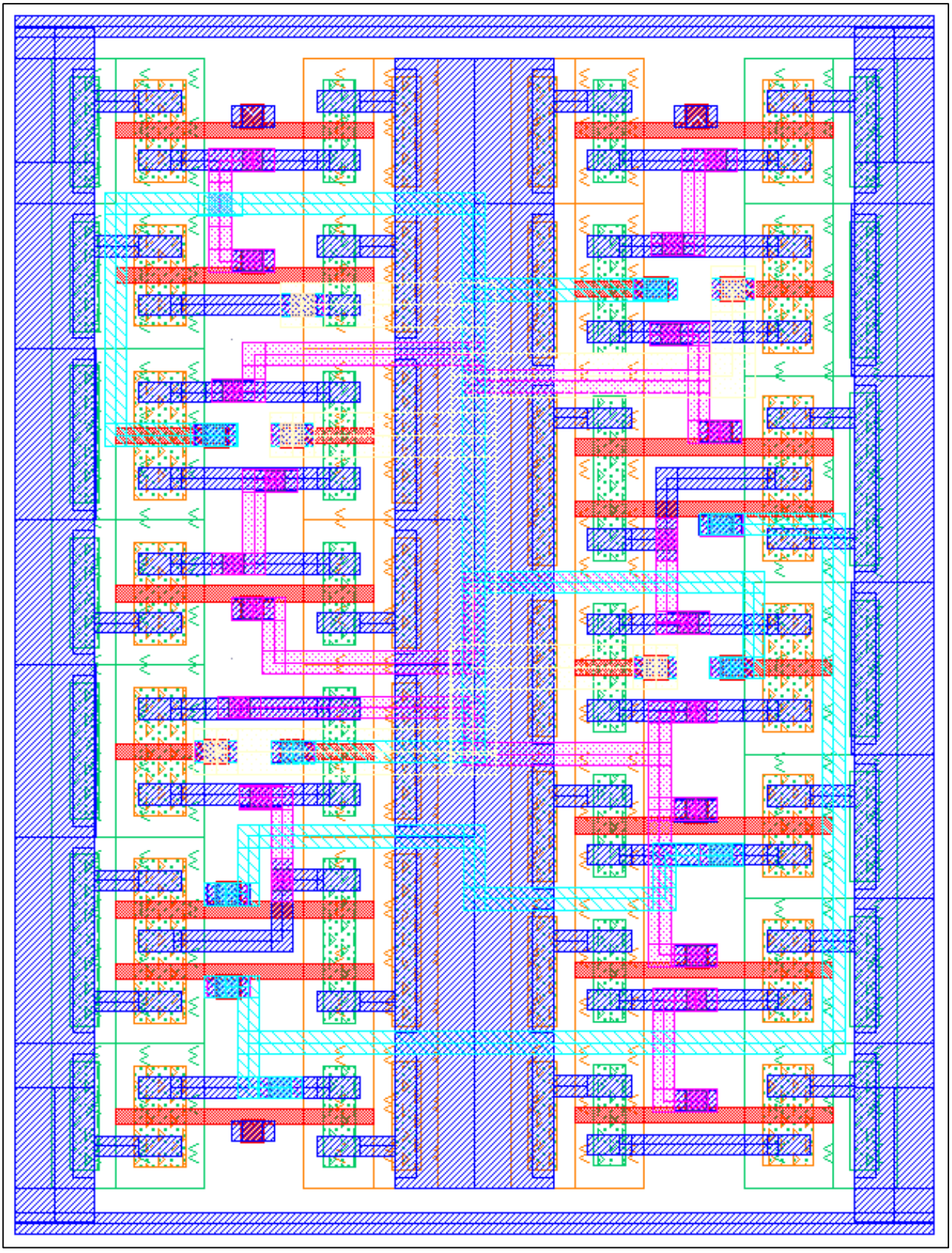


2. **Master-Slave D-Type Flip Flop with Asynchronous Reset** [Symbol & Layout- Instances Floor Plan]





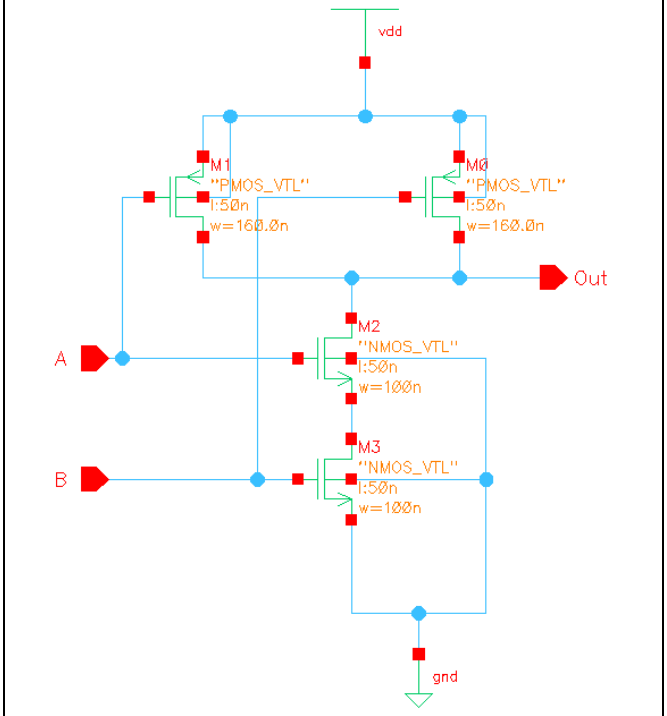
3. Master-Slave D-Type Flip Flop with Asynchronous Reset [Layout]

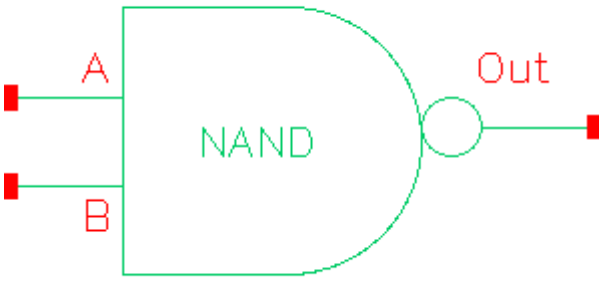


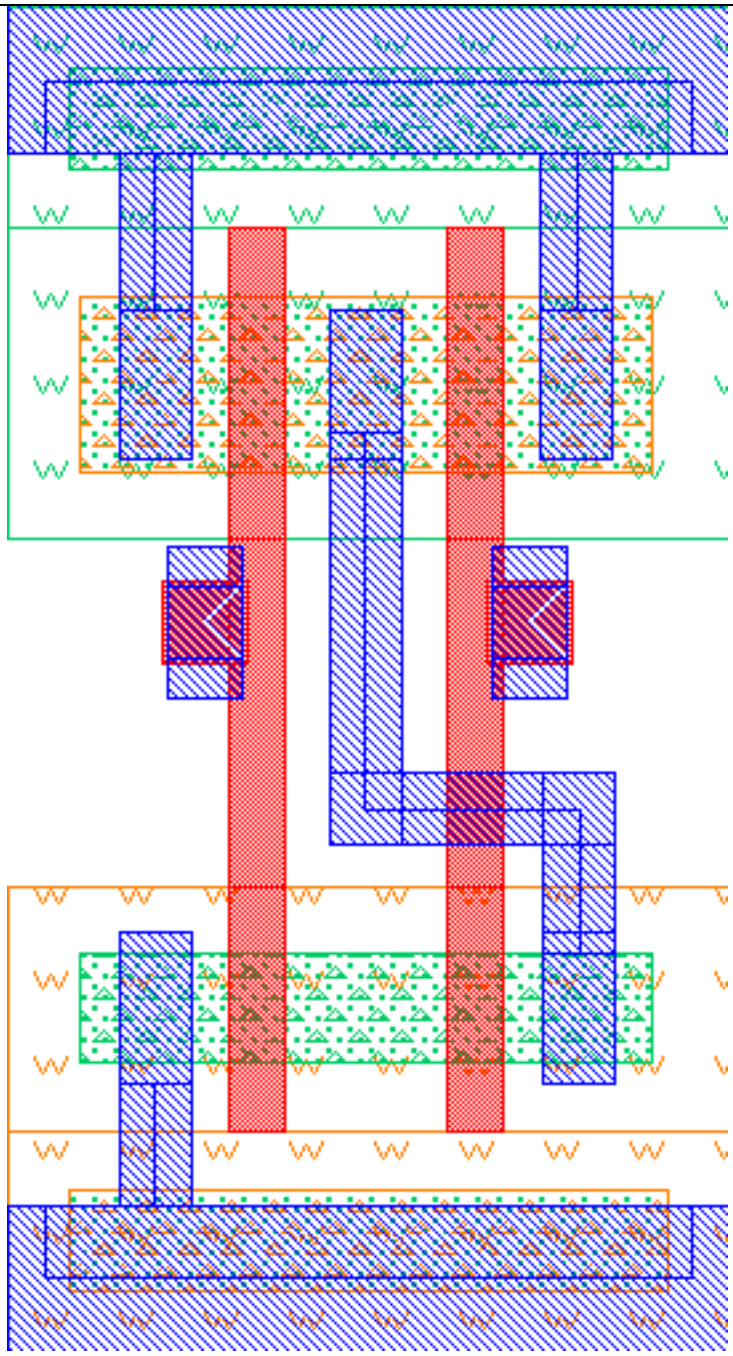
UP

The NAND Gate, Transmission Gate, Tri-State NAND Gate and Tri-State NOT Gate were designed for the included in the final design of D Flip Flop. The Schematic Diagrams and Layouts are shown below.

4. NAND Gate Instance - Descend View [Schematic + Symbol + Layout]

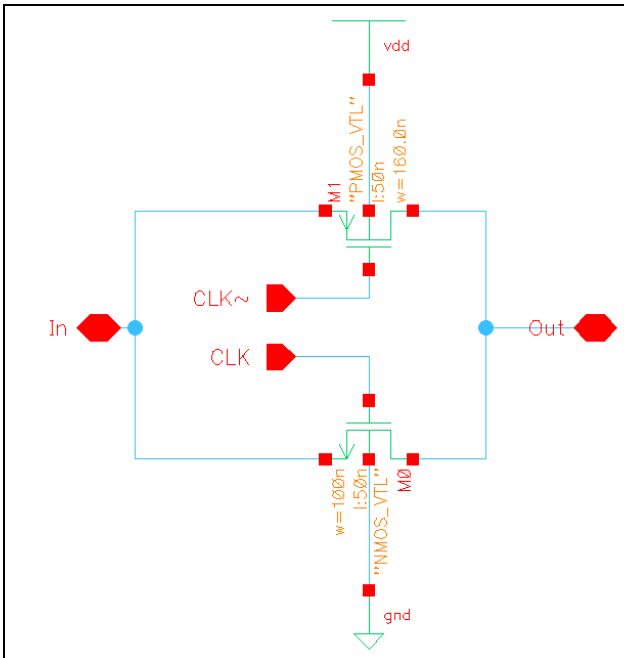


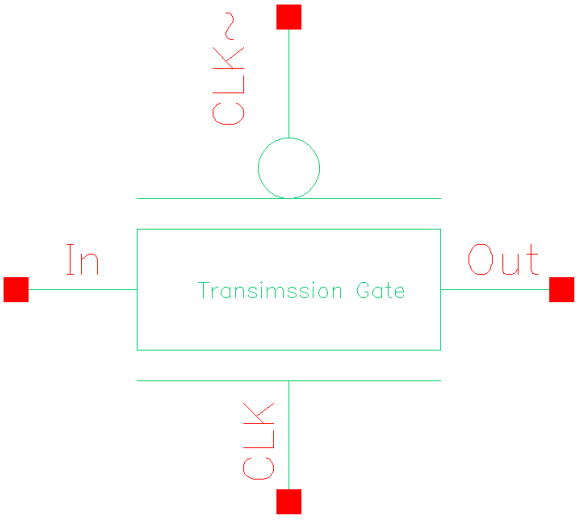


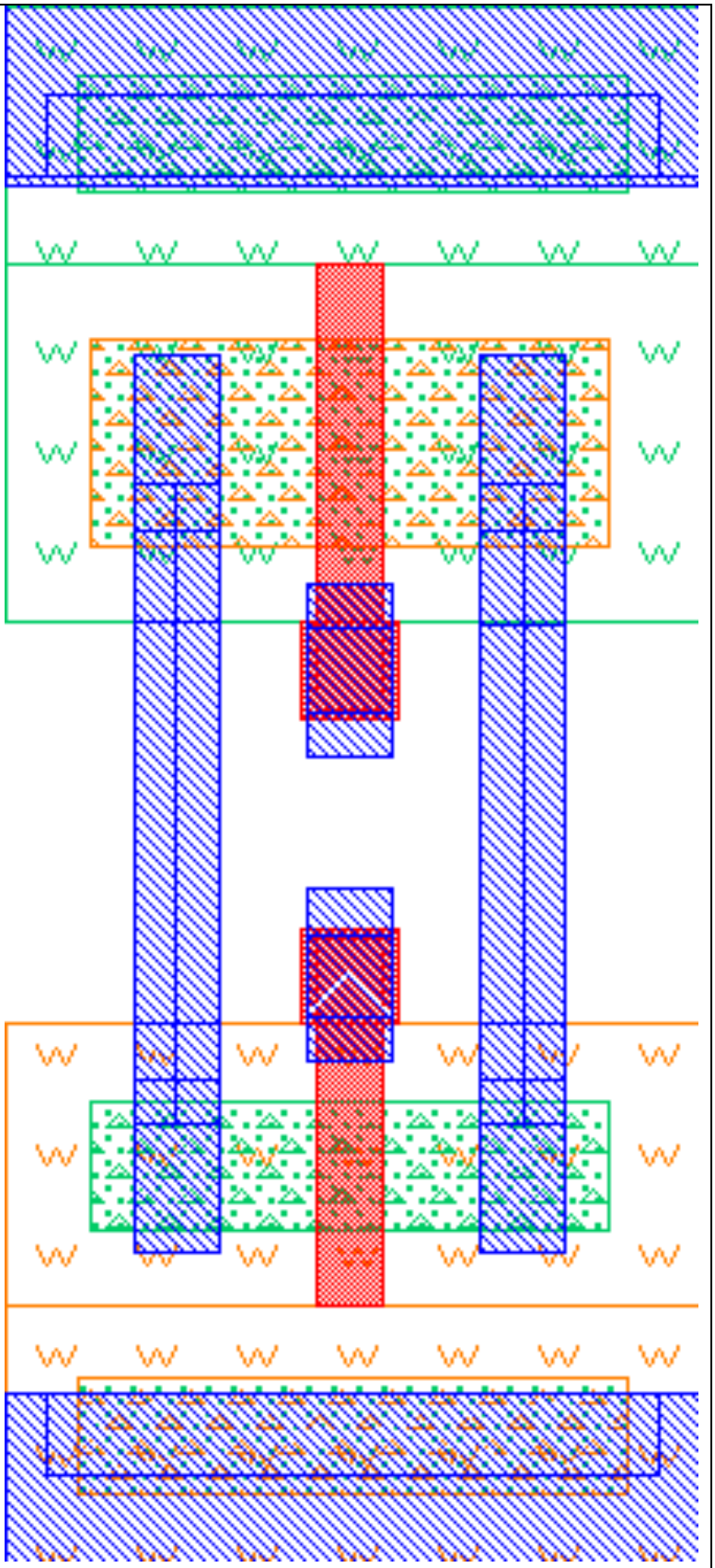


*VDD & GND in symbol are Connected Internally

5. Transmission Gate Instance - Descend View [Schematic + Symbol + Layout]

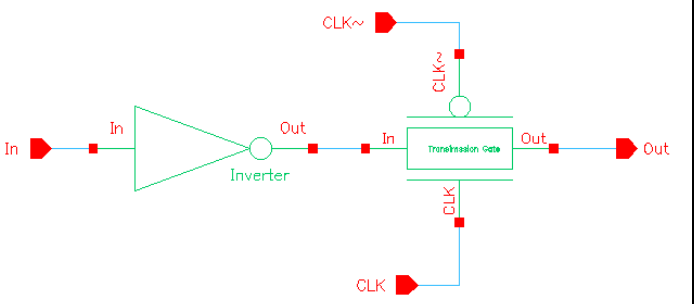


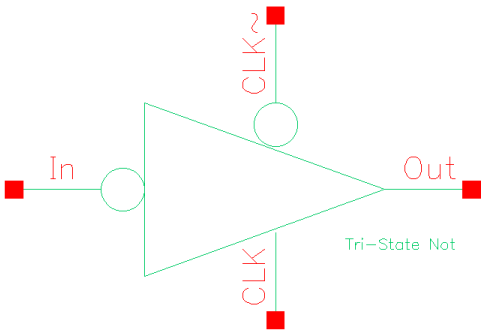


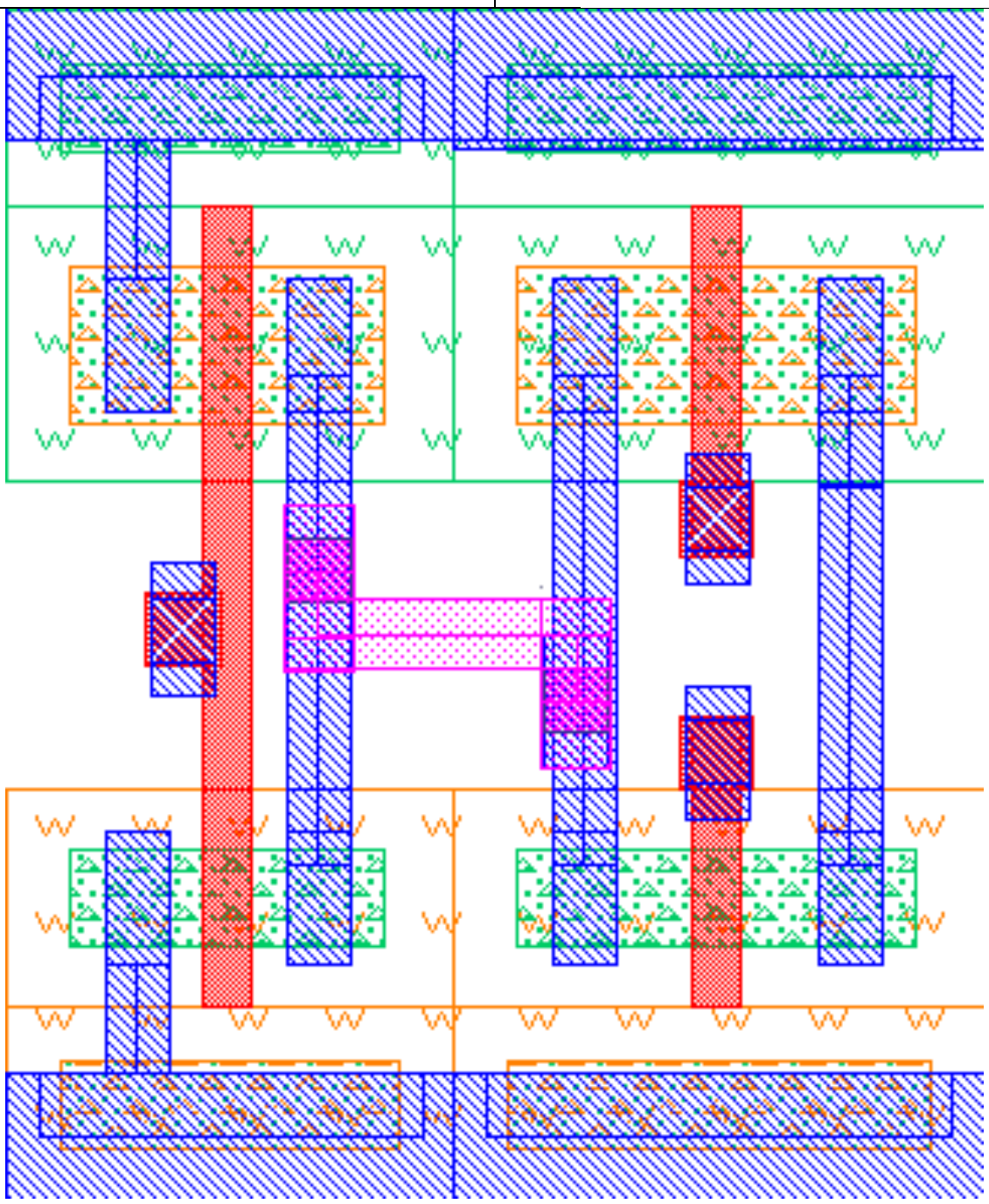


*VDD & GND in symbol as they are Connected Internally

6. Tri–State Not Gate Instance – Descend View [Schematic + Symbol + Layout]

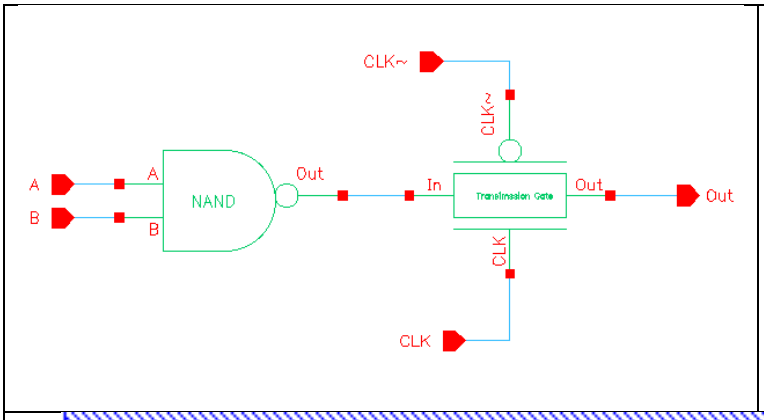


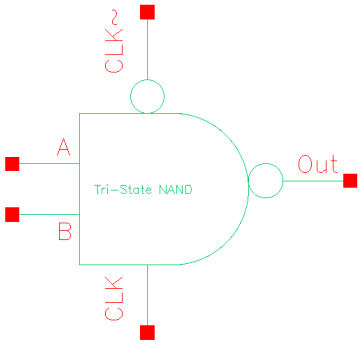


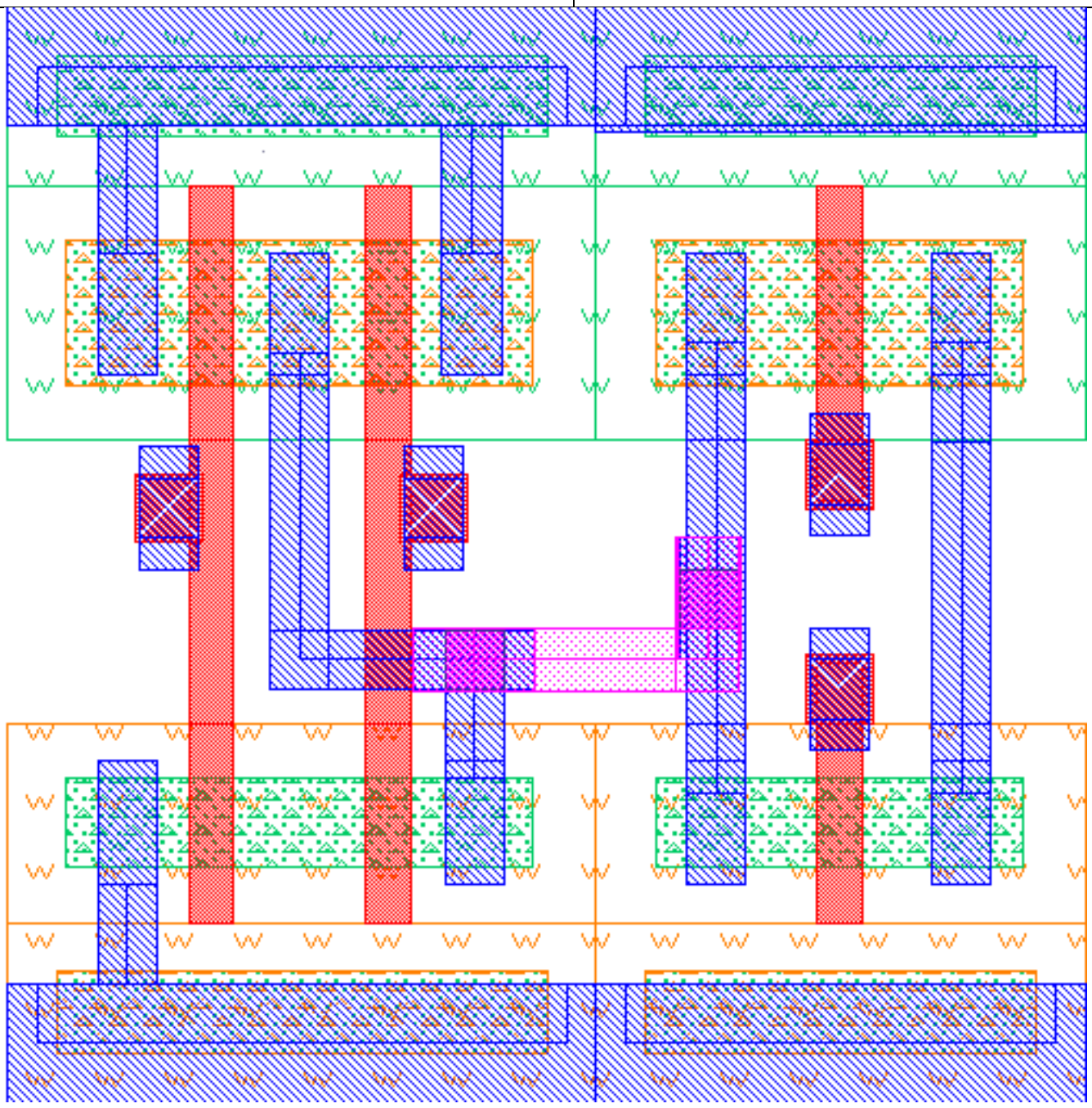


*VDD & GND in symbol as they are Connected Internally

7. Tri–State NAND Gate Instance [Schematic + Symbol + Layout]

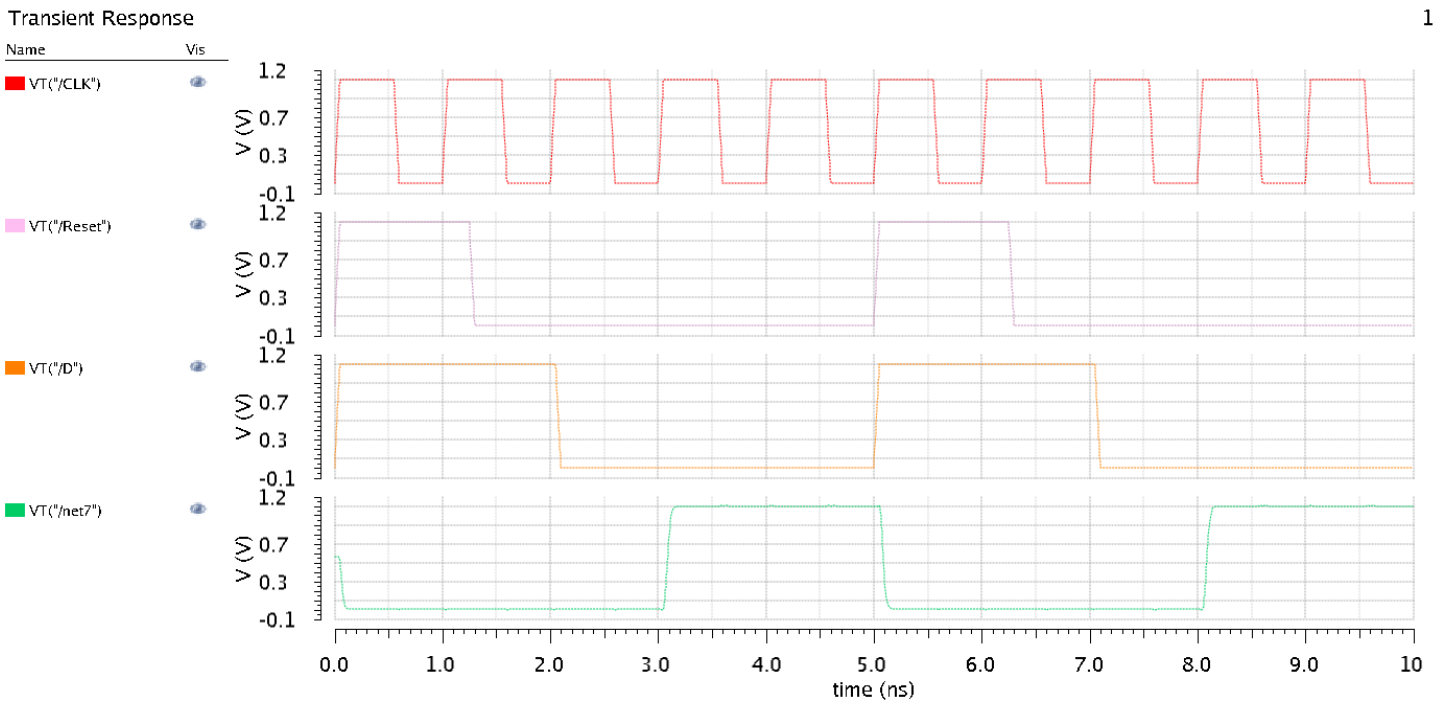


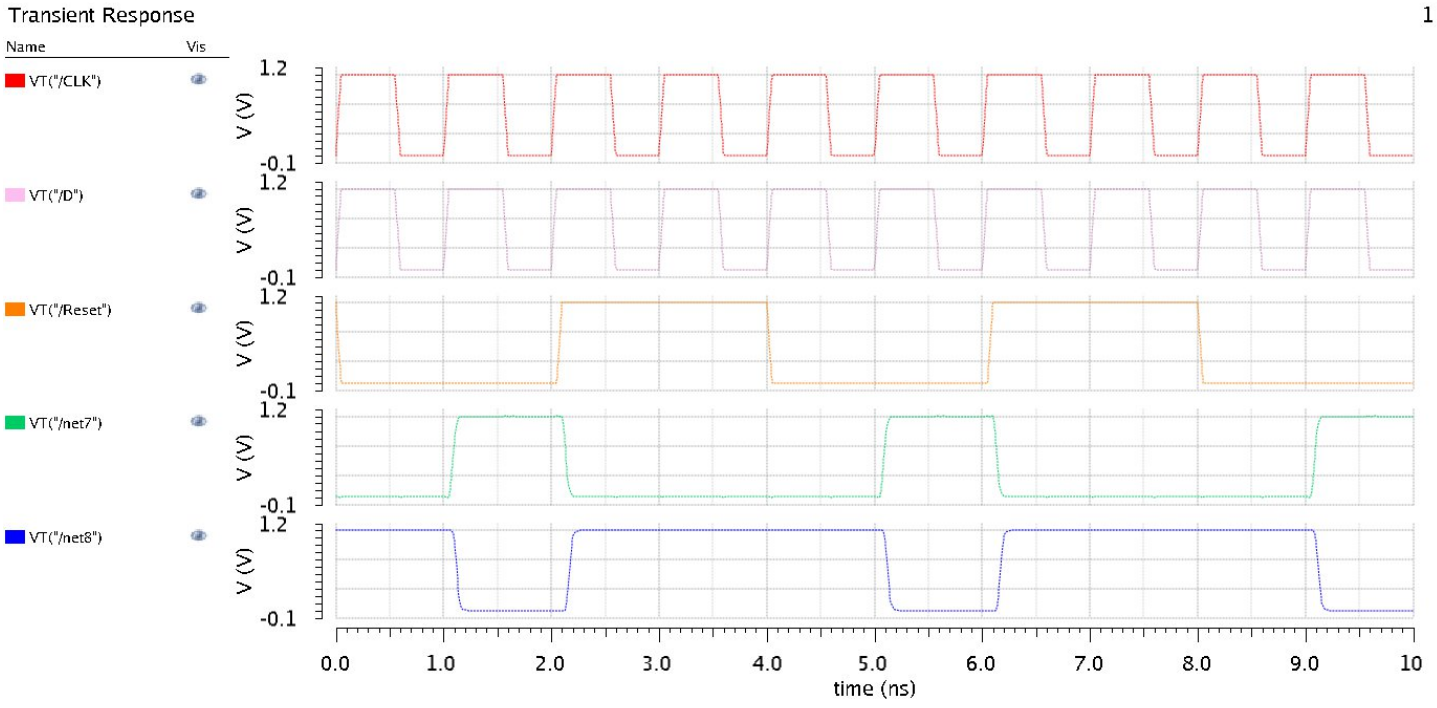




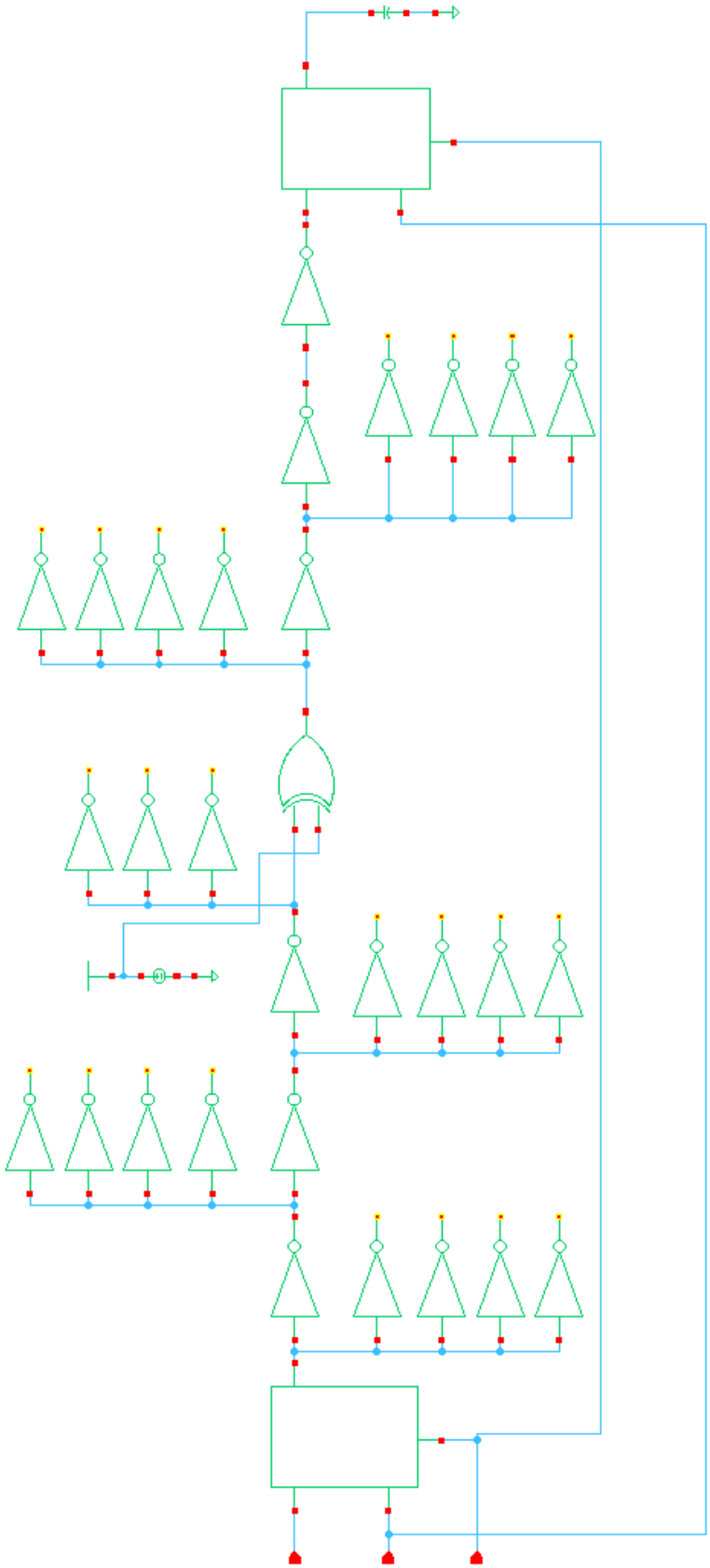
*VDD & GND in symbol as they are Connected Internally

8. Schematic Simulation of D FlipFlop using a basic Test-bench driving a 5f F Capacitive load





9. D FlipFlop Testing Circuit Schematic [Datapath Schematic]

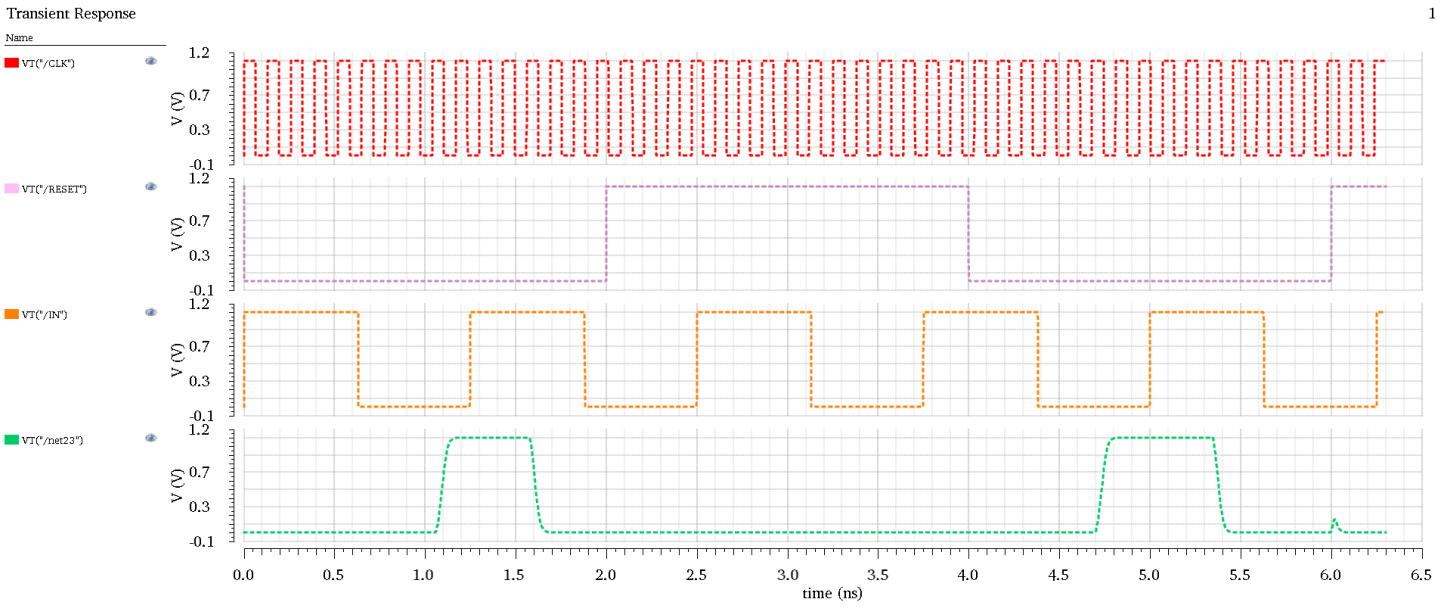


10. Testing of D Flip Flop using the Datapath Schematic [Observations]

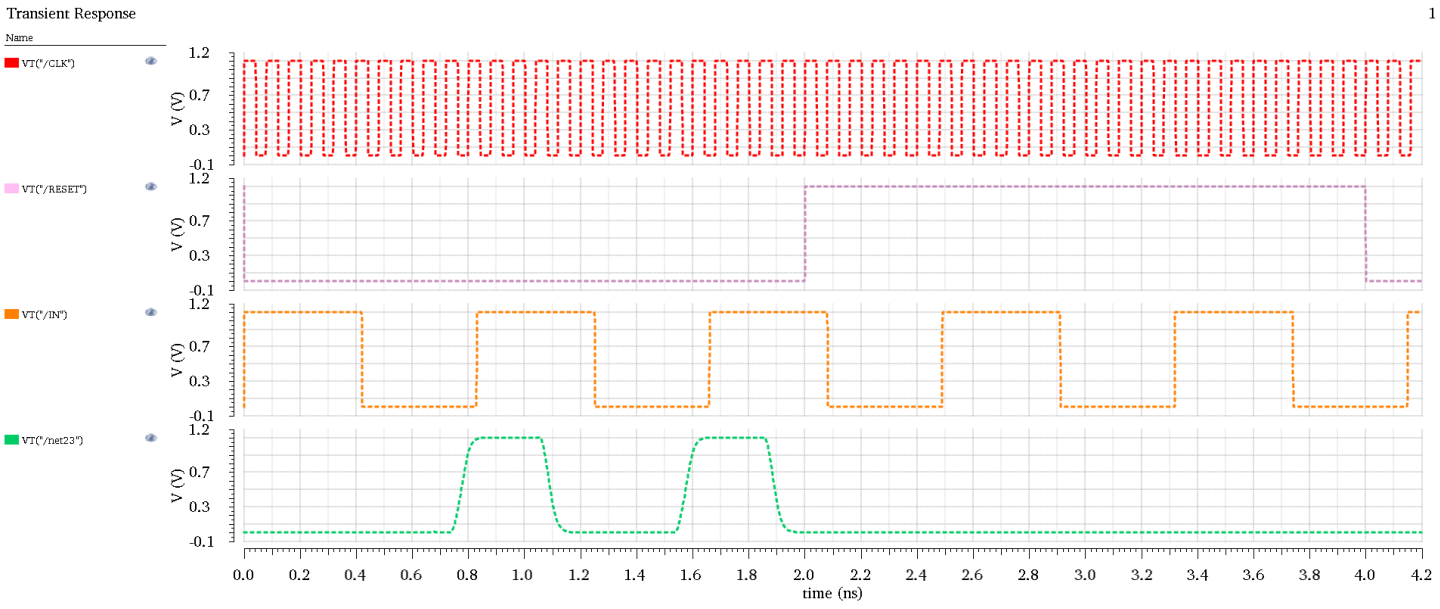
Table 1: Shows Input Clock and Data Signal Pulse Frequencies

CLK (GHZ)	*DATA (MHZ)*	*CLK Period (ns)*	*50% Duty Cycle (ns)*	*Data Period (ns)*	*Duty Cycle (ns)*
2	0.2	0.5	0.250	5.00	2.5
4	0.4	0.25	0.125	0.25	
8	0.8	0.13	0.063	1.25	0.63
12	1.2	0.08	0.042	0.83	0.42
16	1.6	0.06	0.031	0.63	0.31
20	2	0.05	0.025	0.50	0.25

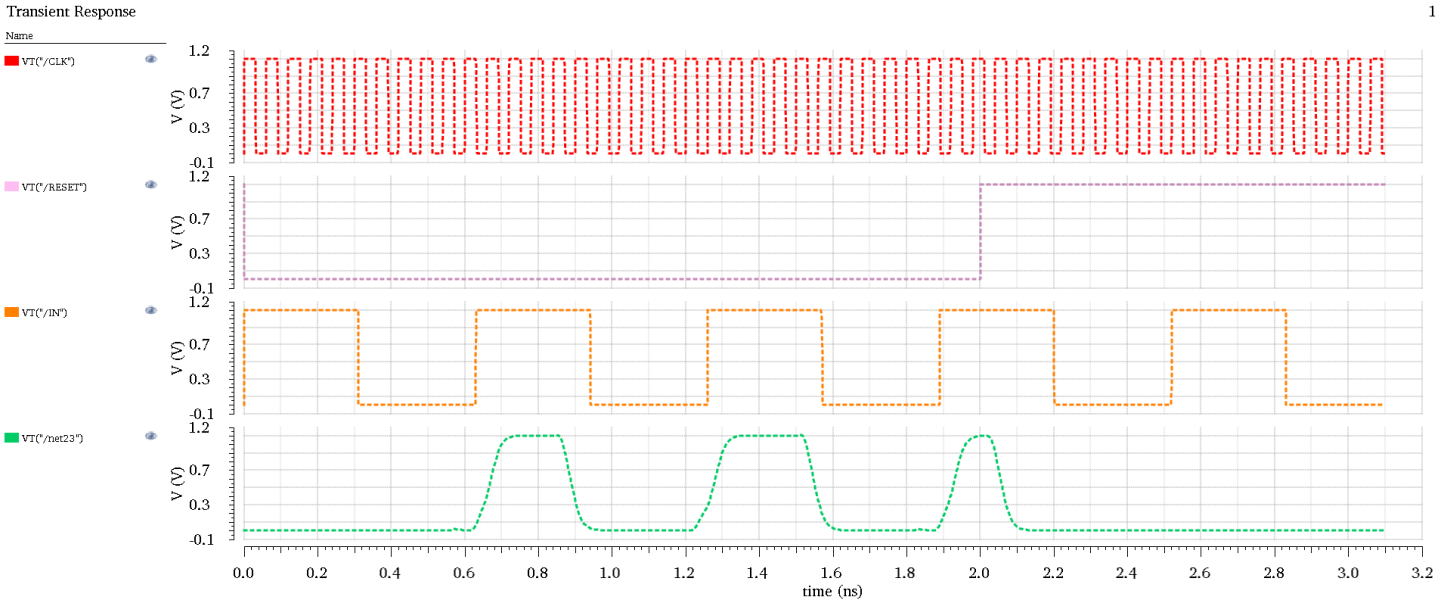
Graph 1: Transient Analysis for 8 GHZ CLK – Slack Met



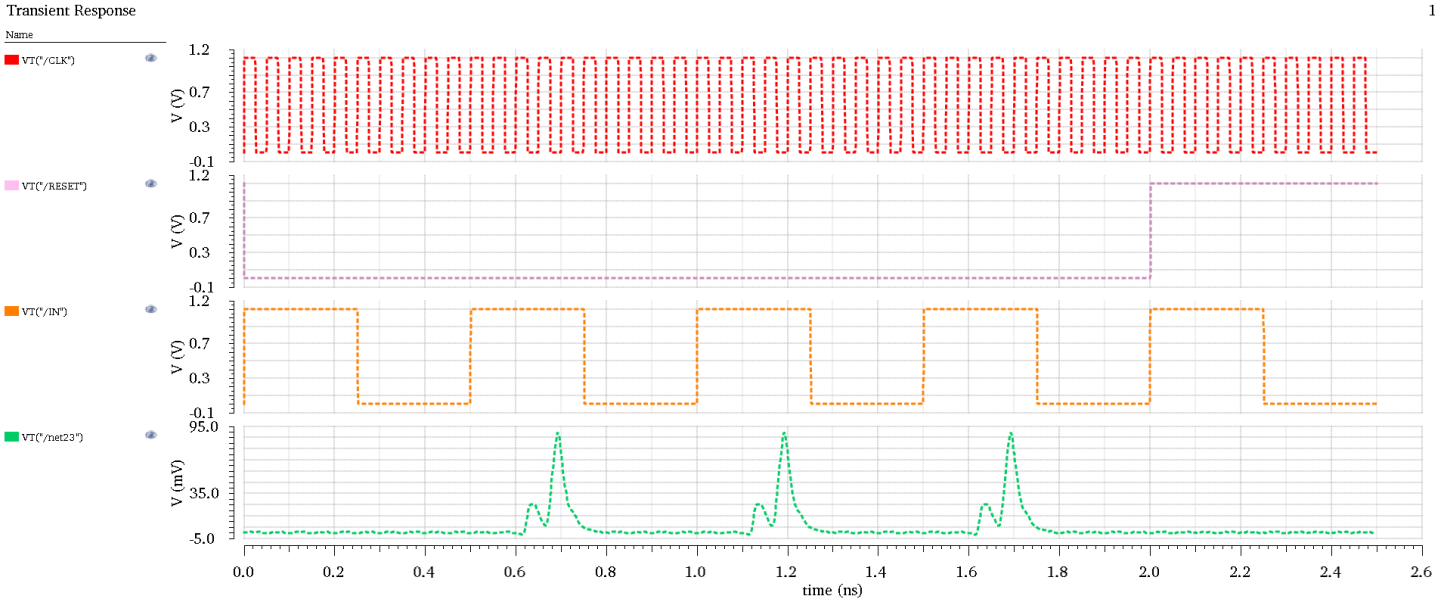
Graph 2: Transient Analysis for 12 GHZ CLK – Slack Met



Graph 3: Transient Analysis for 16 GHZ CLK – Slack Met



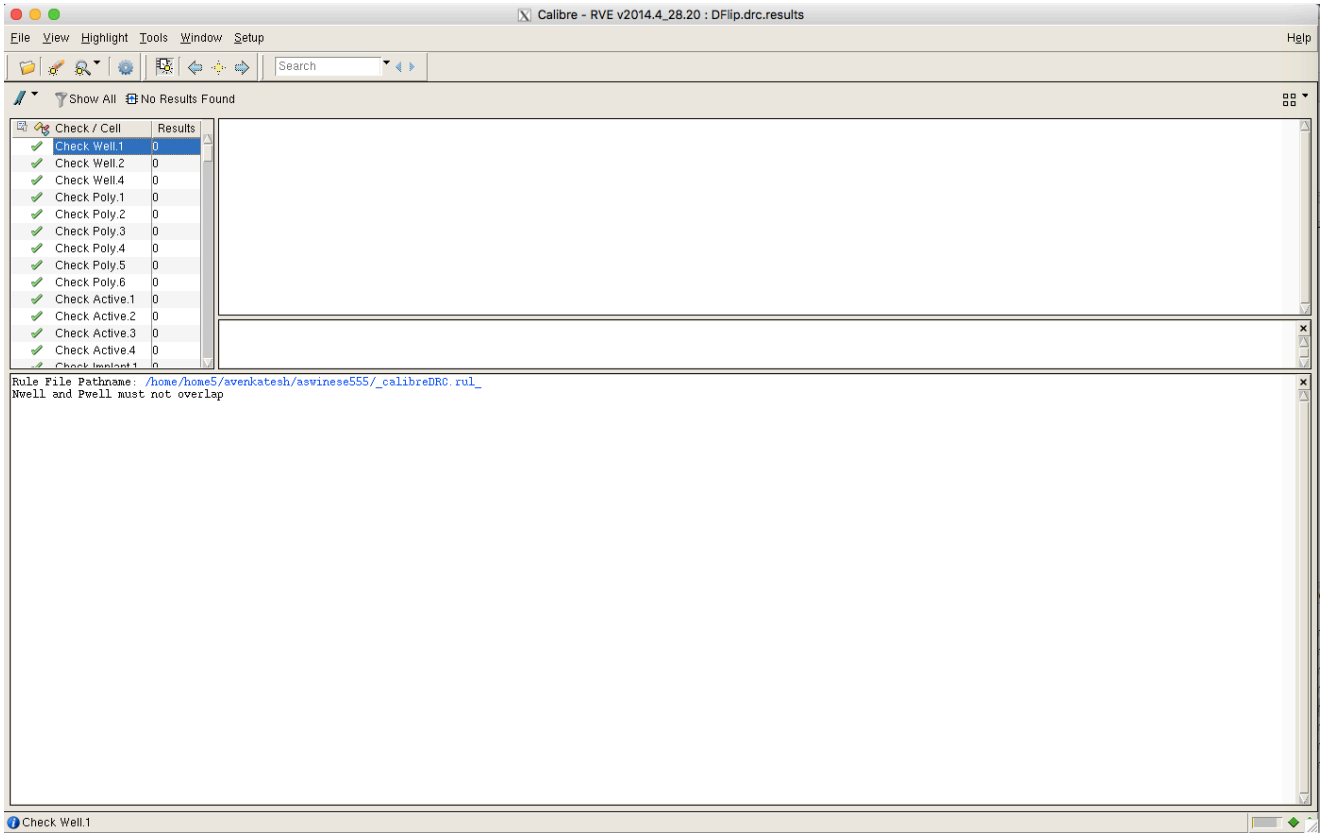
Graph 4: Transient Analysis for 20 GHZ CLK – Slack Violated



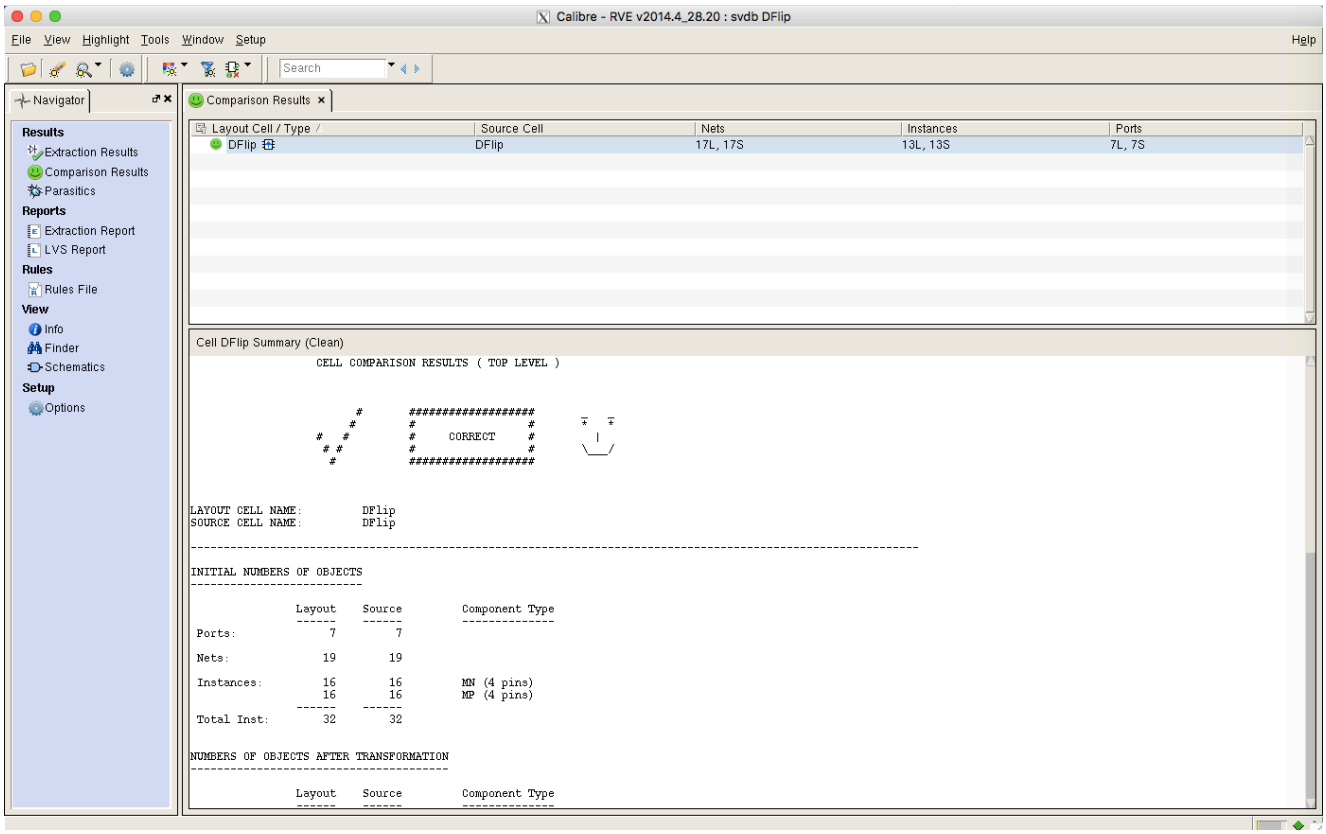
Observations from Graph 1-4

1) The designed D Flip Flop functions correctly as per the design requirement, that is at 2 GHz minimum clock period. It is able to perform the same at a maximum frequency of 16 GHz, after which the behaviour is abnormal. Graphs for 5 Data Cycles are plotted in the above graphs
2) The Graph 3 show the maximum frequency of operation (16 GHz) and Graph 4 shows the violated waveform for 20GHz.

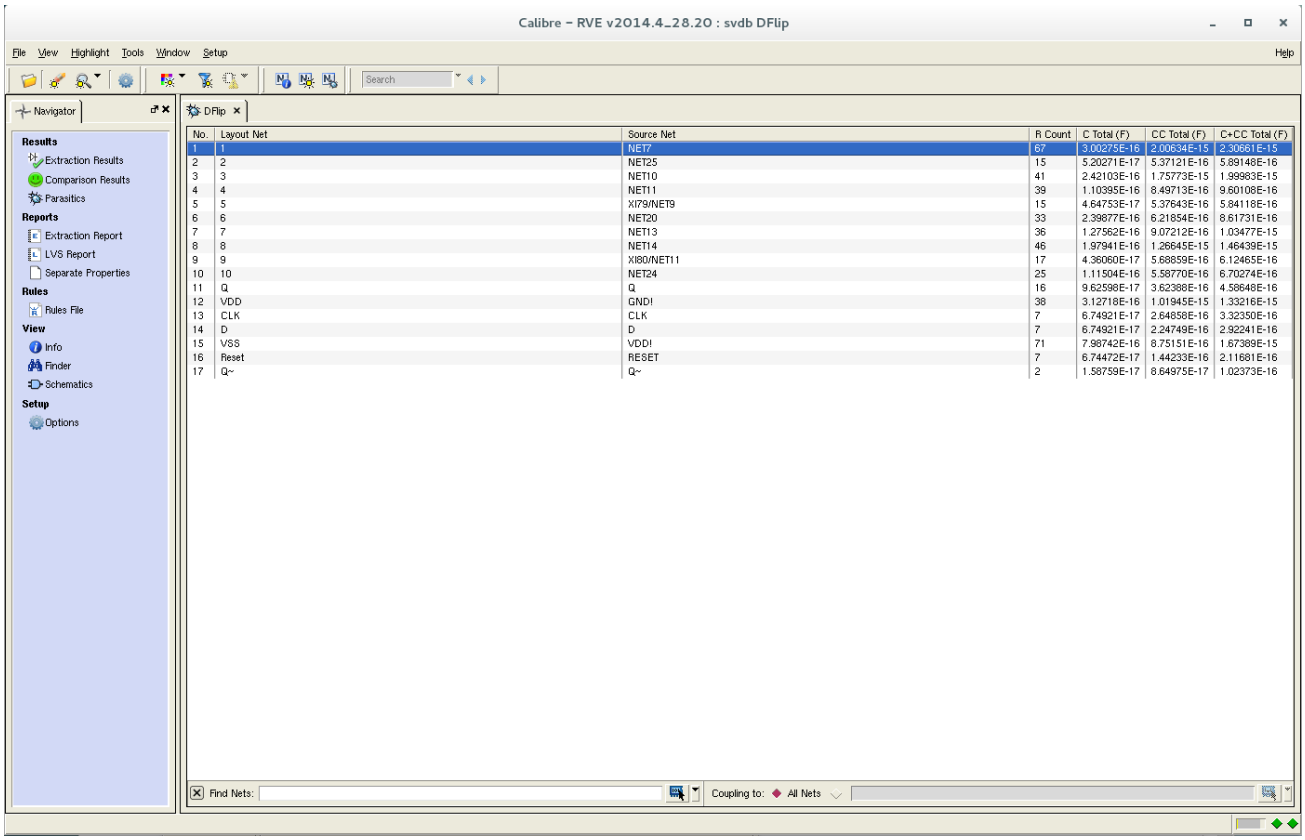
11. Layout DRC REPORT – Successful



12. Layout LVS REPORT – Successful

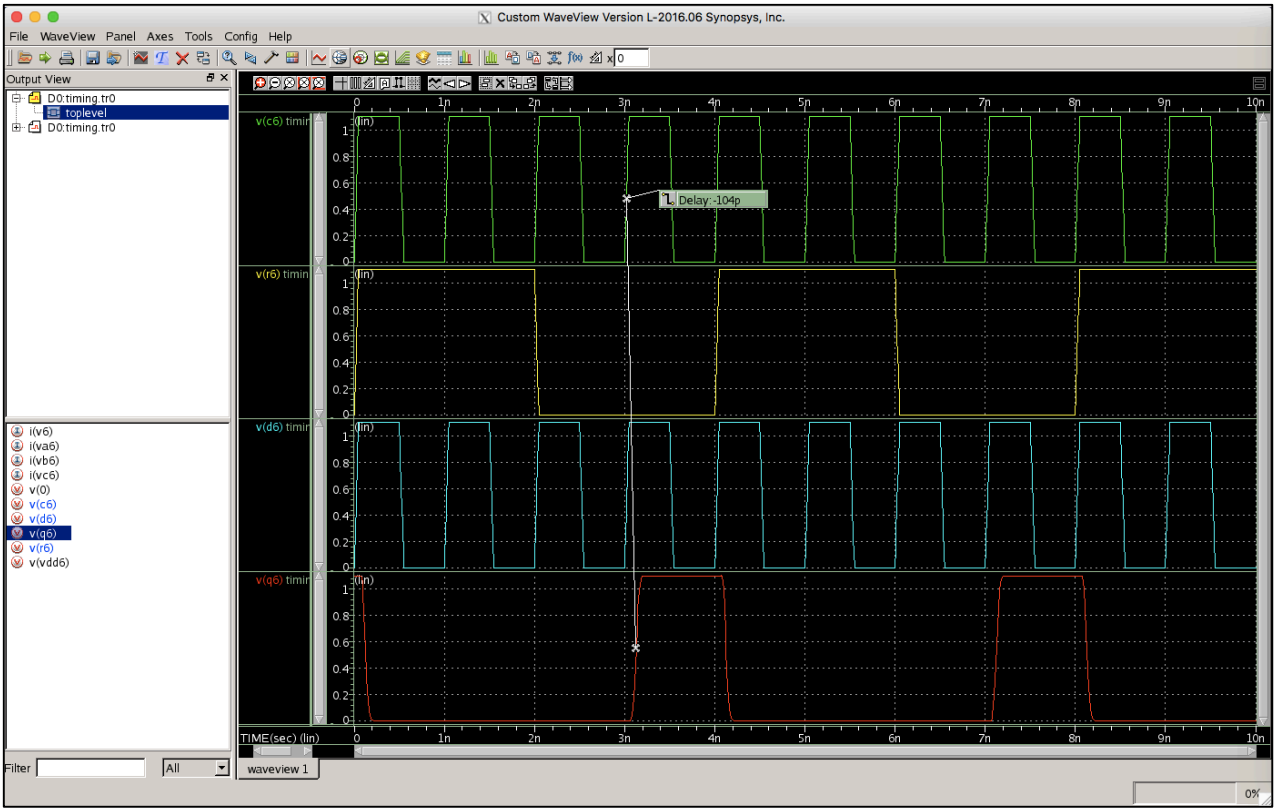


13. Layout PEX REPORT – Successful



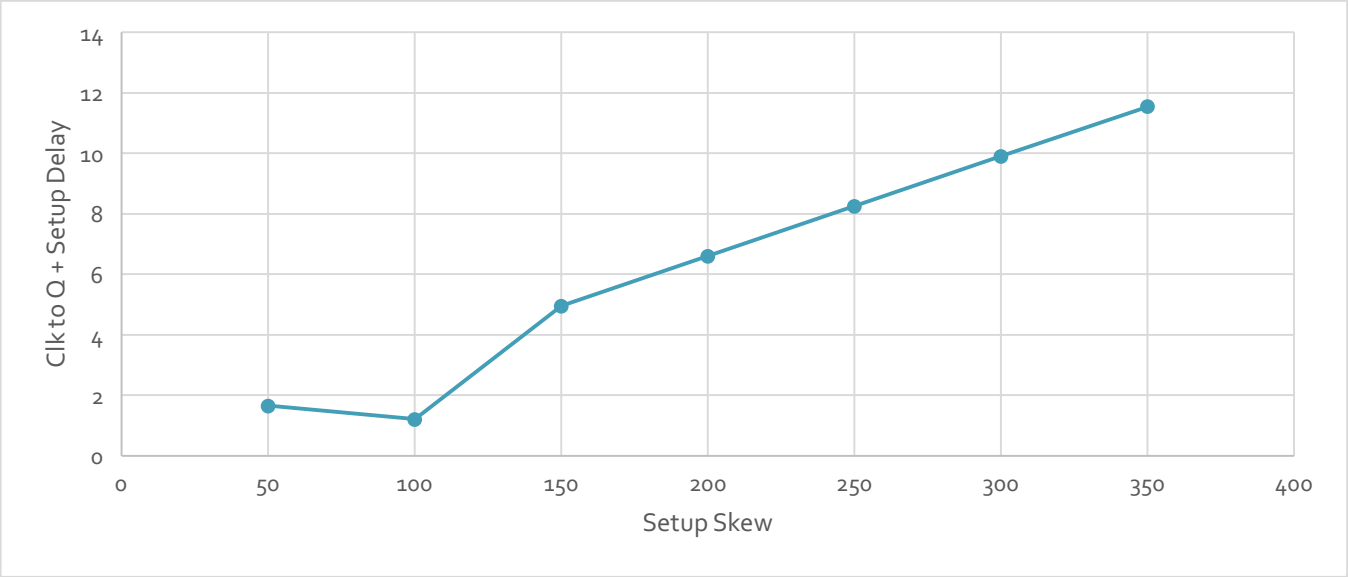
No.	Layout Net	Source Net	R Count	C Total (F)	CC Total (F)	C+CC Total (F)
1	1	NET7	67	3.00275E-16	2.00634E-15	2.30661E-15
2	2	NET25	15	5.20271E-17	5.37121E-16	5.89148E-16
3	3	NET10	41	2.42103E-16	1.75773E-15	1.99983E-15
4	4	NET11	39	1.10395E-16	8.49713E-16	9.60108E-16
5	5	XI79/NET9	15	4.64753E-17	5.37643E-16	5.84118E-16
6	6	NET20	33	2.39877E-16	6.21854E-16	8.61731E-16
7	7	NET13	36	1.27562E-16	9.07212E-16	1.03477E-15
8	8	NET14	46	1.97941E-16	1.26645E-15	1.46439E-15
9	9	XI80/NET11	17	4.36060E-17	5.68859E-16	6.12465E-16
10	10	NET24	25	1.11504E-16	5.58770E-16	6.70274E-16
11	Q	Q	16	9.62598E-17	3.62388E-16	4.58648E-16
12	VDD	GND!	38	3.12718E-16	1.01945E-15	1.33216E-15
13	CLK	CLK	7	6.74921E-17	2.64858E-16	3.32350E-16
14	D	D	7	6.74921E-17	2.24749E-16	2.92241E-16
15	VSS	VDD!	71	7.98742E-16	8.75151E-16	1.67389E-15
16	Reset	RESET	7	6.74472E-17	1.44233E-16	2.11681E-16
17	Q~	Q~	2	1.58759E-17	8.64975E-17	1.02373E-16

14. Clock to Q Time – Hspice Post Layout Simulation Data



Setup Time Tabulation & Graph

Set up Skew (ps)	Clock to Q Delay	Total Delay Setup + Clock to Delay
50	1.6	1.65
100	3.2	1.2
150	4.8	4.95
200	6.4	6.6
250	8	8.25
300	9.6	9.9
350	11.2	11.55



END OF REPORT

Appendix: HSpice Timing.sp File

```
**************************************************
**** include 45nm model file
.prot
.inc '/usr/local/cds/FreePDK45/ncsu_basekit/models/hspice/hspice_nom.include'
.inc 'DFlip.pex.netlist'
.unpr
**** set nominal supply voltage
.param pvdd=1.1
**** set temperature and global ground
.param ptemp=25
.param gnd=0
**** set timing parameters
.param freqd=0.1g
.param freqc=1g
.param freqr=0.15g
.param perid=1/freqd
.param peric=1/freqc
.param perir=1/freqr
.param load=5fF
.param rt=50p
.param ond=perid*0.5-rt
.param onc=peric*0.5-rt
.param onr=perir*0.5-rt
.param stop=10n
**** set dff input and output
v6 vdd6 0 pvdd
c6 q6 0 load
vd6 d6 0 pulse (0 pvdd 0 rt rt ond perid)
vc6 c6 0 pulse (0 pvdd 0 rt rt onc peric)
vr6 r6 0 pulse (pvdd 0 0 rt rt onr perir)
**** instantiate inverter
xinvx1 q6 0 c6 d6 r6 q6 vdd6 DFlip
**** set conditions and options
.ic v(xinvx1.q6)=0

.temp ptemp
.option macmod=1 captab post

**** measure delays, output slews, and switching powers
** INVX1
.measure tran iavg6 avg i(v6) from=0 to=stop
.measure tran rise6 trig v(y6) val=pvdd*0.1 td=2n rise=1 targ v(y6) val=pvdd*0.9 td=2n rise=1
.measure tran fall6 trig v(y6) val=pvdd*0.9 td=2n fall=1 targ v(y6) val=pvdd*0.1 td=2n fall=1
.measure tran a6lh trig v(a6) val=pvdd*0.5 td=2n fall=4 targ v(y6) val=pvdd*0.5 td=2n rise=4
.measure tran a6hl trig v(a6) val=pvdd*0.5 td=2n rise=4 targ v(y6) val=pvdd*0.5 td=2n fall=4
.measure tran delay6 param='(a6lh+a6hl)/2'
.measure tran power6 param=iavg6*pvdd
.measure tran slew6 param=0.5*rise6+0.5*fall6

.tran 0.01n stop
.end
```