Friday, October 20, 2017

ESE 555 | HOMEWORK 3

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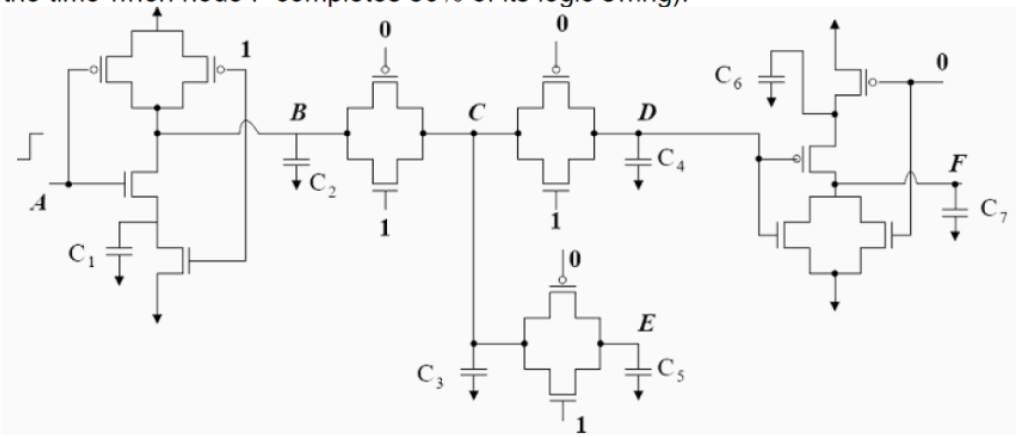
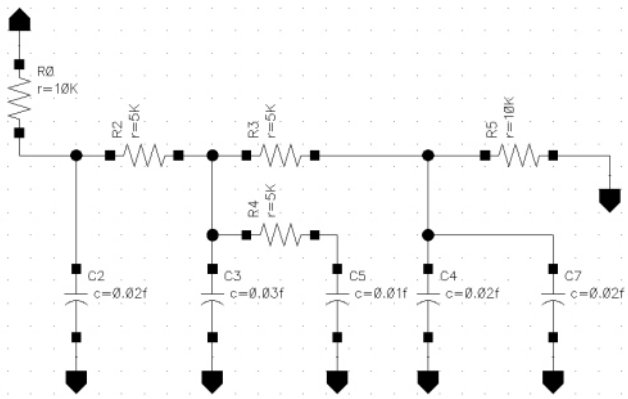
QUESTION:

Consider the circuit given below. Assume that the NOR gate is triggered when the node D completes 90% of its logic swing. Input A changes from 0 to 1 as a step input and the other inputs are stable with values as shown. The net capacitances at each node including gate, diffusion and interconnect capacitances are as follows: C1=0.01pF, C2=0.02pF, C3=0.03pF, C4=0.02pF, C5=0.01pF, C6=0.01pF and C7=0.02pF. All transistors have an effective ON resistance 10kΩ and OFF resistance infinity. Estimate the propagation delay from node A to node F (i.e. the delay from the time the step input is applied to node A to the time when node F completes 50% of its logic swing).



SOLUTION:

RC Tree:



Elmore Delay Calculation – A – D (0-90 %)

$$T_{DI} = \sum_{K} R_{KI} C_K$$

$T_{D1} = [R_0C_2 + (R_0+R_2)C_3 + (R_1+R_2)C_5 + (R_1+R_2+R_3)C_4] \times 2.2$

$= [10 \times 0.02 + (10+5)0.03 + (10+5)0.01 + (10+5+5)0.02] \times 2.2$

$= [10 \times 0.02 + (10+5)0.03 + (10+5)0.01 + (10+5+5)0.02] \times 2.2$ $10^3 \times 10^{-12}$

$\boldsymbol{T_{D1} = 2.76 \times 10^{-9}\, S = 2.76\, nS}$

Total Delay

$\boldsymbol{T_{D1} + T_{D2} = (2.76 \times 10^{-9})\, S + (0.138 \times 10^{-9}) S}$

$\boldsymbol{T_{D1} + T_{D2} = 2.898 \times 10^{-9}\, S}$

$\boldsymbol{T_D = 2.898 \times 10^{-9}\, S = 2.898\, nS}$

Elmore Delay Calculation – D –F (0-50 %)

$T_D = [R_5C_7] \times 0.69$

$= [10 \times 0.02] \times 0.69 \times 10^3 \times 10^{-12}$

$\boldsymbol{T_{D2} = 0.138 \times 10^{-9}\, S = 0.14\, nS}$