Aswin Natesh Venkatesh

Digital Design Engineer at InvenSense · Embedded Systems & Digital Design Enthusiast

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Experience

TDK InvenSense Inc.

San Jose, CA

Digital Design Engineer - Sr | FPGA Design Engineer (earlier)

Jan. 2019 - Present

- Member of the ASIC design group working on hardware design for motion sensor products.
- Responsible for micro-architecture and RTL implementation of InvenSense's 32-bit Microprocessor IP in Silicon. This involves the layout of a custom ISA with 80+ instructions, including specific motion algo. instructions to target performance and code density. Have worked on tool-chains, performance modelling, system-level integration, SW support and firmware debug.
- Other responsibilities include RTL implementation of Serial Interface IP (SPI, I2C, I3C) and provide maintenance support for satellite blocks.
- Explore hardware accelerator architectures for ML applications specific to decision trees, neural networks and complex arithmetic operations.
- Define timing constraints, analyze lint, synthesis, power, CDC reports, develop scripts for project management using GIT and Jenkins CI.
- Perform extensive bench testing and debug using oscilloscopes and protocol analyzers (SPI/I2C/I3C) to support new hardware bring-up.
- Assist in performing metal ECOs when required and formality checks during ASIC re-spins.
- Started early career as an FPGA designer responsible for integration and delivery of digital+analog chip-top models on Xilinx FPGAs platform for design emulation. This work involved defining the FPGA architecture, timing constraints and generate FPGA binaries. Worked on developing validation test cases for FPGA pre-release validation and sanity testing.

TDK InvenSense Inc.

San Jose, CA

Hardware Engineering Intern (ADC-FPGA protoyping)

May. 2018 - Aug. 2018

- Designed and Implemented a 150 MSPS ADC-FPGA System (Cyclone V) for sampling Ultrasonic (PZT) Signals.
- Task involved selection of ADC, FPGA & design of front-end low-noise amplifiers, impedance matching circuits for signal conditioning.
- Member of Advanced Technology Group, working on next-gen sensors lead by Peter Hartwell, InvenSense Inc.

Solarillion Foundation

Chennai, India

Research Assistant | Undergraduate Research Assistant (earlier)

Aug. 2015 - May. 2017

- Lead authored 2 publications and led 2 projects on smart and assistive living.
- Lead the design and development of device test-bench & Custom Made Sensors.
- Mentored undergraduate students and peers in embedded systems and hands-on circuit debugging.

Skills

Bus Protocols	AMBA AHB & APB Bus • SPI 3W/4W • I2C
Programming	System Verilog, Python, Shell, Embedded C, Latex
Hardware Platforms	Altera Cyclone V • Xilinx Zynq • Atmel Family • ARM M0, M7 • RISC-V
EDA/Software Tools	Cadence & Synopsys simulation, synthesis, formality, linting tools • Xilinx Vivado • IAR Toolchain • Jenkins • GIT
Validation Tools	Logic/protocol analyzer • Meters • Oscilloscopes • Signal generators
Experimental	Sensor System Development • New Hardware bring-up • DIY hacking & prototyping

Education

Stony Brook University

Stony Brook, NY

Masters in Electrical Engineering - (GPA 3.50/4.00)

Aug. 2017 - Dec. 2018

Concentration: Computer Architecture, Digital logic design, System specification and modelling
Research: Worked under Prof. Shan Lin on areas of Cyber Physical Systems and Sensor Networks

Anna University

Chennai, India

Bachelors in Engineering, Electrical and Electronics Engineering

Aug. 2012 - Apr. 2016

Select Projects

Micro-Architecture of Synergistic Processing Unit of Sony Cell — *Stony Brook, NY*

Part of Graduate Coursework "Computer Architecture" — *Jan 2018 - May 2018*

- Designed a SONY Cell Processor Architecture (SPU) that includes the detection of structural, data and control hazards. Involves behavioral modeling at RTL level using System Verilog to simulate the instruction flow in the pipelined processor.

Logic simulation and ATPG using PODEM — *Stony Brook, NY*

Part of Graduate Coursework "Advanced VLSI System Testing" — *Jan 2018 - May 2018*

- Implemented an algorithm in C++ to generate correct output of a large digital circuit. The algorithm also makes use of PODEM for Automatic Test Pattern Generation (ATPG) to find test vectors which detects all single stuck at faults in the circuits.

Hardware Generation Tool for ASIC — *Stony Brook, NY*

Part of Graduate Coursework "Adv. Digital System Design and Generation" — *Aug 2017 - Dec 2017*

- Developed a C++ based accelerated hardware generator(System Verilog) for performing Matrix Vector Multiplication with configurable 3 layer neural network, and an algorithm that effectively optimizes the hardware for the required degree of parallelism.

Research Publications

Low-Cost Wireless Intelligent Two Hand Gesture Recognition System — *Montreal, Canada*

Published at 2017 Annual IEEE Systems Conference (SysCon), Canada (goo.gl/dMd8Uz) — *Apr. 2017*

- Led the design implementation of a two hand gesture recognition system to recognize static gestures across 8 globally used sign languages and aid the audio vocally impaired. - Architected the hardware software co-design for the system.

Low Cost Smart Glove for Universal Control of IR Devices — *Kerala, India*

Published at 2016 IEEE International Symposium on Technology and Society (ISTAS) (goo.gl/48lzLd) — *Nov. 2016*

- Developed a gesture recognition system that acts as an universal remote control for multiple consumer electronic appliances. A custom designed sensory glove is used as input to the system.

Intelligent Smart Helmets for Automatic Control of Headlamps — *Banglore, India*

Published at 2015 IEEE International Conference on Smart Sensors and Systems (goo.gl/FrgtcC) — *Oct. 2015*

- Developed a smart helmet that enhances road safety among motorcyclist by tracking the user gestures and providing better visual aid at night.

Volunteer Work

Backstage Volunteer, Production Team — *Palo Alto, CA*

At IEEE Hot Chips Symposium (HCS) (Archive) — *Aug. 2020, 2021*

Achievements

2018 **Top 10**: BitCamp Hack 2018 - Best use of MLH Hardware — *Maryland, MD*

2018 **1st/36**: Hack @ CEWIT 2018 - Best use of CISCO'S MERAKI AP — *Stony Brook, NY*

2016 **Finalist**: AU Titan Hackathon 2015 - Anna University — *Chennai, India*

Certifications

Object Oriented Programming using C++ — NIIT Limited, India | License:11CUZZZZZ9276

Advanced Programming in 'C' — NIIT Limited, India | License:10DJZZZZZ8932

Scientific Python — TDK InvenSense, San Jose