Summary of Eight Bit Calculator Design

Jason Mobarak
ECE 338
May 12th, 2005

Introduction

The deign described in this document is an eight bit calculator with 4 different operations. The hardware for the eight be calculator is not described in this document.

In this design, it is assumed that there is an external device that provides input to the calculator and pulses a signal to indicate that input is present.

Normally, implementation of this calculator with a higher level hardware description language like VHDL or Verilog. However, this design chooses to describe the underlying mechanics of each operation, implemented at the gate level.

Product Specifications

Input Bus

The input bus receives all data for the calculator, operands and operators are all input through this one bus. Input is directed to the bus and an input valid signal is pulsed, on a positive clock edge of this signal input from the bus is loaded into a register.

The order of input is important. The first input is the left operand of the operation, second is the operator and third is the right operand. Example, the VHDL translation of the operation $2\cdot 5$ would be:

$$\begin{array}{l}
INPUT_{VALID}='0';INPUT_{BUS}=00000010;wait\ for\ CLK_{PERIOD};\\
INPUT_{VALID}='1';wait\ for\ CLK_{PERIOD};\\
INPUT_{VALID}='0';INPUT_{BUS}=00000010;wait\ for\ CLK_{PERIOD};\\
INPUT_{VALID}='1';wait\ for\ CLK_{PERIOD};\\
INPUT_{VALID}='0';INPUT_{BUS}=00000101;wait\ for\ CLK_{PERIOD};\\
INPUT_{VALID}='1';wait\ for\ CLK_{PERIOD};\\
INPUT_{VALID}='0';wait;--wait\ for\ output
\end{array}$$

Output Bus

The output bus transmits the result of an operation, the output bus should only be read when the OUTPUT_VALID signal has a positive clock edge. When OUTPUT_VALID does not have a positive clock edge the calculator is still attempting to calculate the result of the operation requested.

Output Range

Output from the calculator is unsigned and can only be in the range $[0,255]$. Should the result of any operation be greater that 255 or less than 0 the result should be 255 or 0, respectively.

Operator Implementation

Operators for this calculator can only be implemented with primitive gate operations. These operations include: AND, OR, NOR, NAND, XOR, and XNOR. Operations should be implemented by hand and not by a synthesis tool, full control over operator implementation is desired.

Design

The main calculator was designed as a state machine with 6 states. See Illustration 1 for a basic diagram of the main finite state machine.

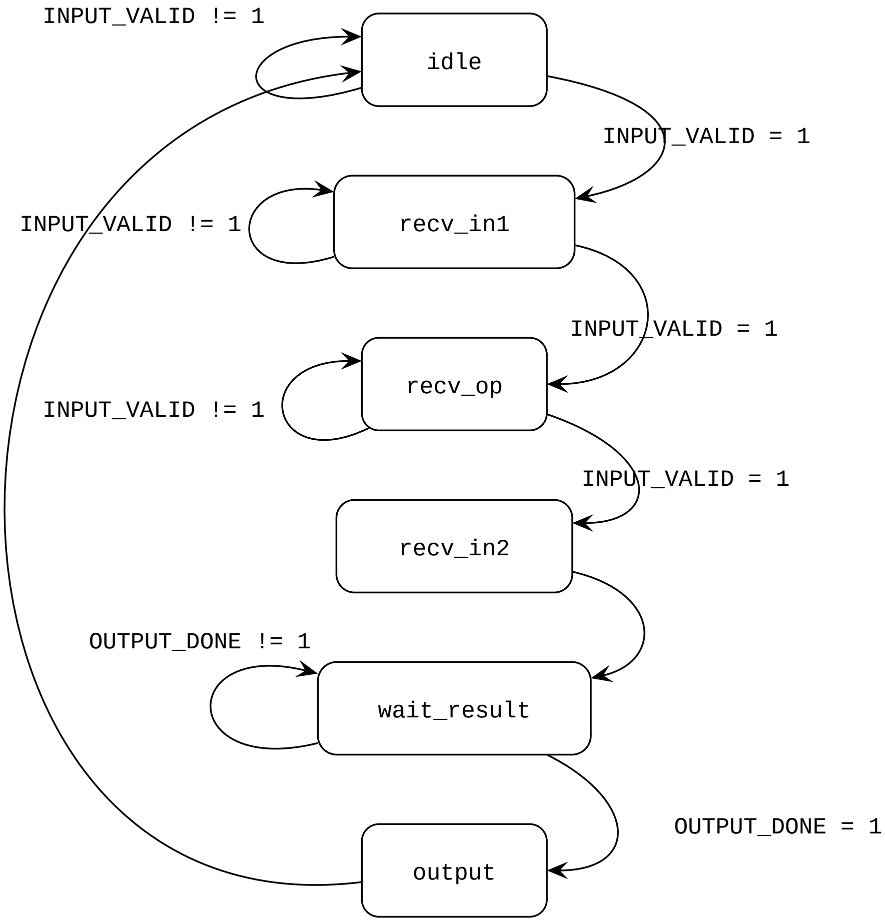

Illustration 1 - main calculator state machine