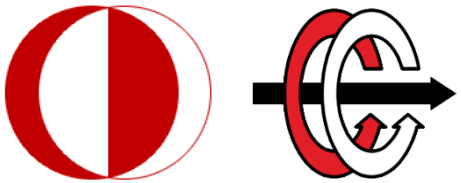
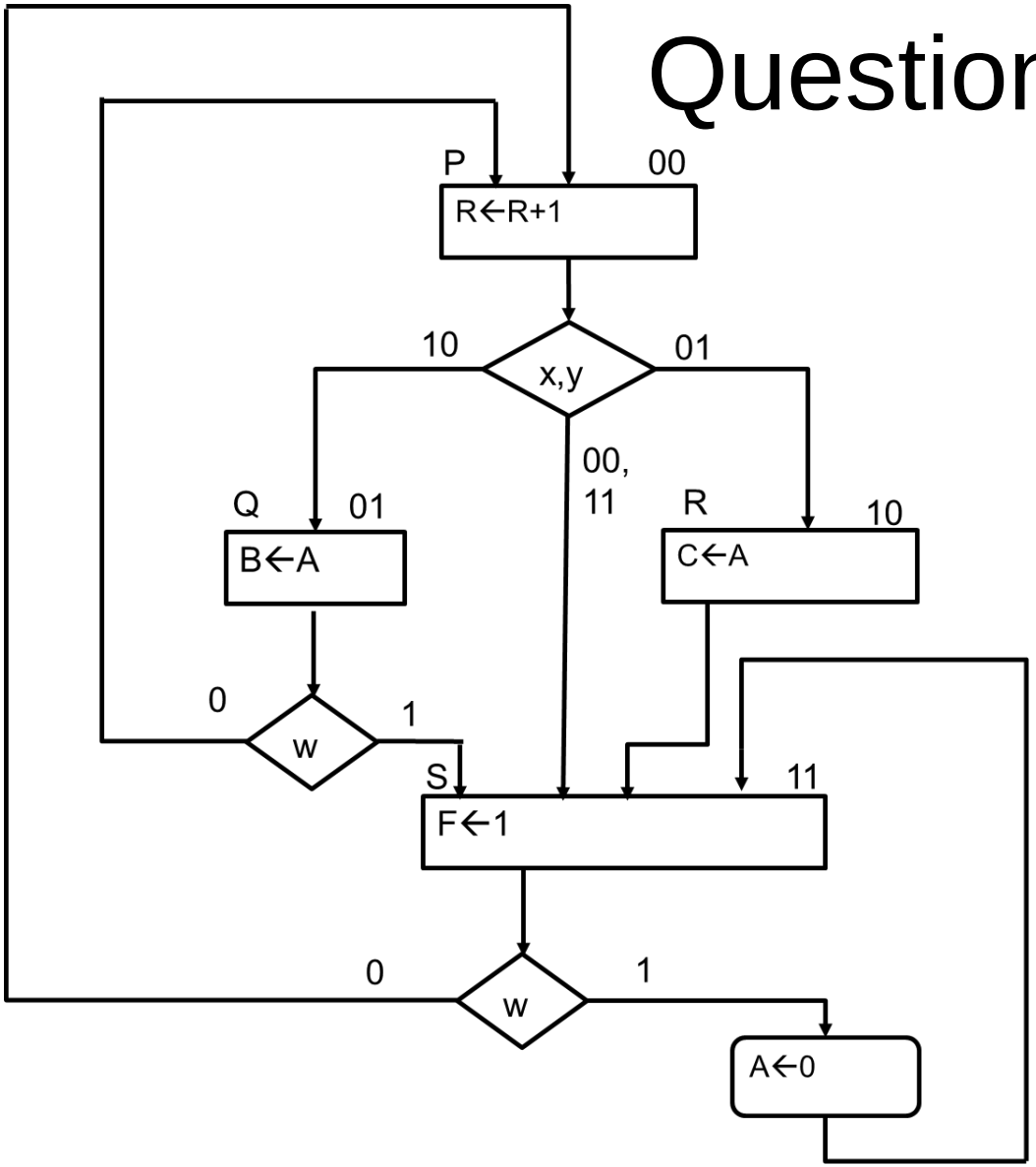


# Algorithmic State Machine

## Practice Questions

# Question 1

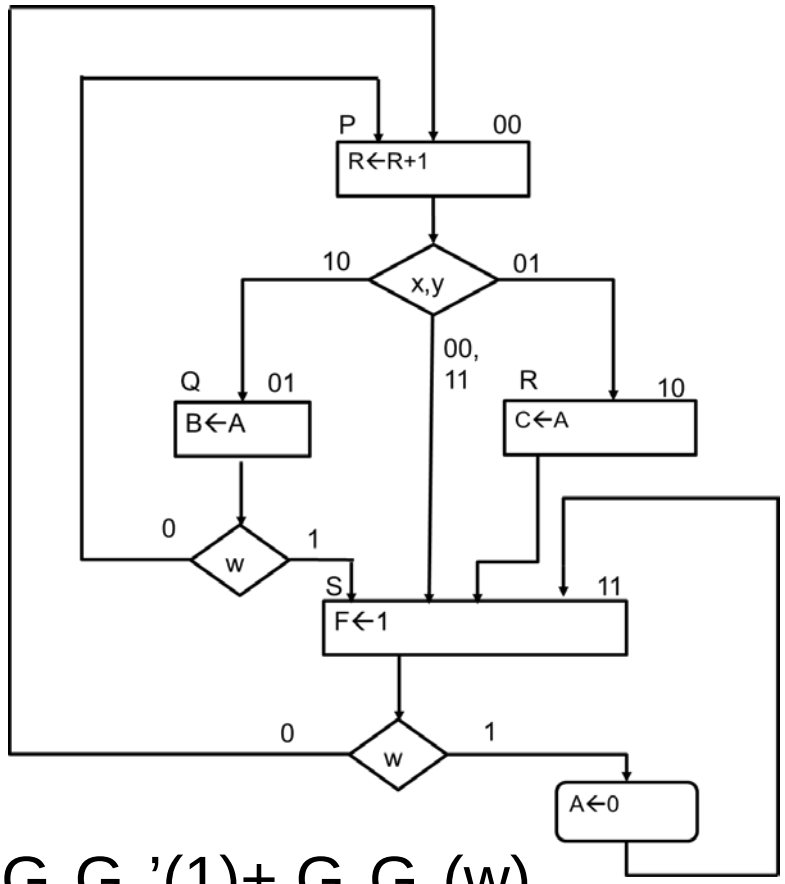



Design the control unit of the given ASM chart and give its circuit diagram using all methods. Use JK FFs for the classical sequential circuit design.

Design the Datapath with a counter R, Registers A, B, C and a D-FF F.

# Question 1 Solution with Multiplexer (modified D-FF)

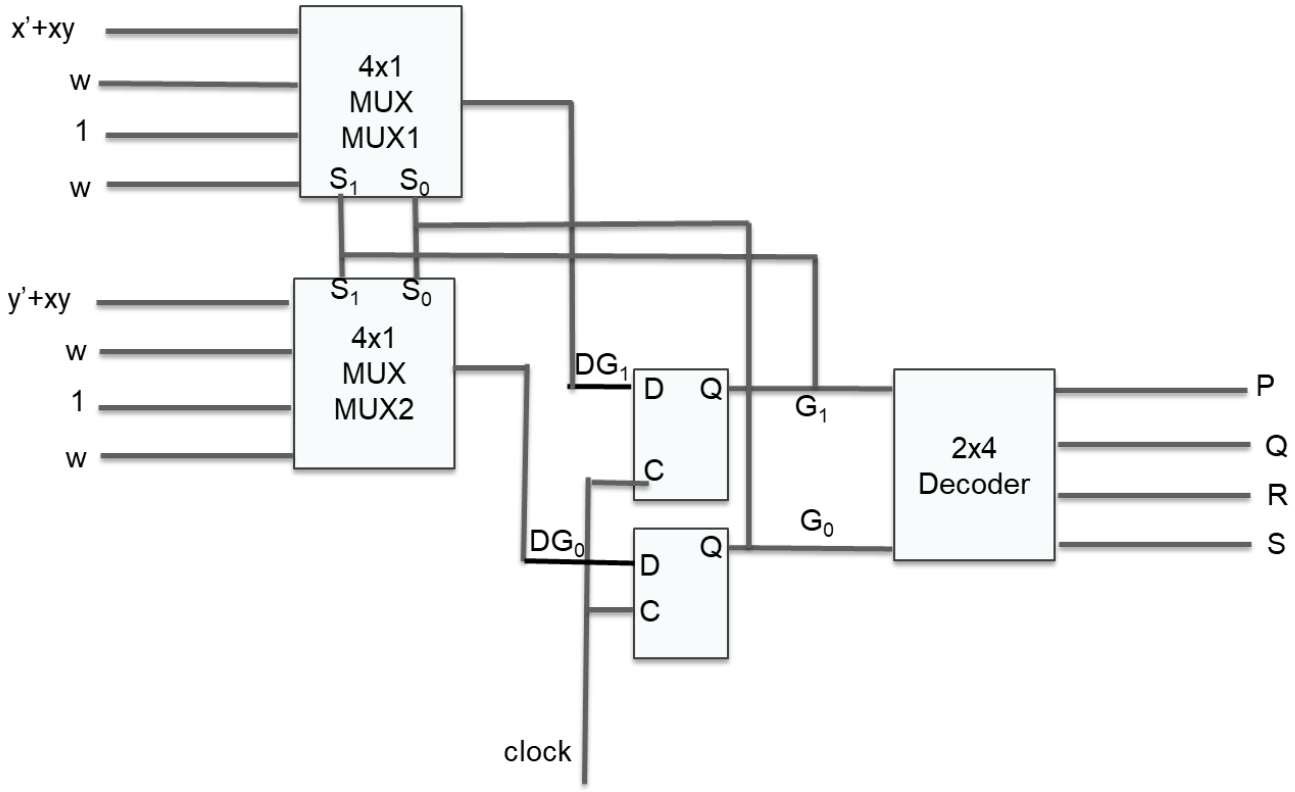
| Present State | | Next State | | Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Name | $G_1G_0$ | Name | $G_1G_0$ | x | y | w | P | Q | R | S |
| P | 00 | S | 11 | 0 | 0 | - | 1 | 0 | 0 | 0 |
| | 00 | S | 11 | 1 | 1 | - | 1 | 0 | 0 | 0 |
| | 00 | Q | 01 | 1 | 0 | - | 1 | 0 | 0 | 0 |
| | 00 | R | 10 | 0 | 1 | - | 1 | 0 | 0 | 0 |
| Q | 01 | P | 00 | - | - | 0 | 0 | 1 | 0 | 0 |
| | 01 | S | 11 | - | - | 1 | 0 | 1 | 0 | 0 |
| R | 10 | S | 11 | - | - | - | 0 | 0 | 1 | 0 |
| S | 11 | S | 11 | - | - | 1 | 0 | 0 | 0 | 1 |
| | 11 | P | 00 | - | - | 0 | 0 | 0 | 0 | 1 |




$$DG_1 = G_1'G_0'(x'y'+xy+x'y) + G_1'G_0(w) + G_1G_0'(1) + G_1G_0(w)$$

$$DG_0 = G_1'G_0'(x'y'+xy+xy') + G_1'G_0(w) + G_1G_0'(1) + G_1G_0(w)$$

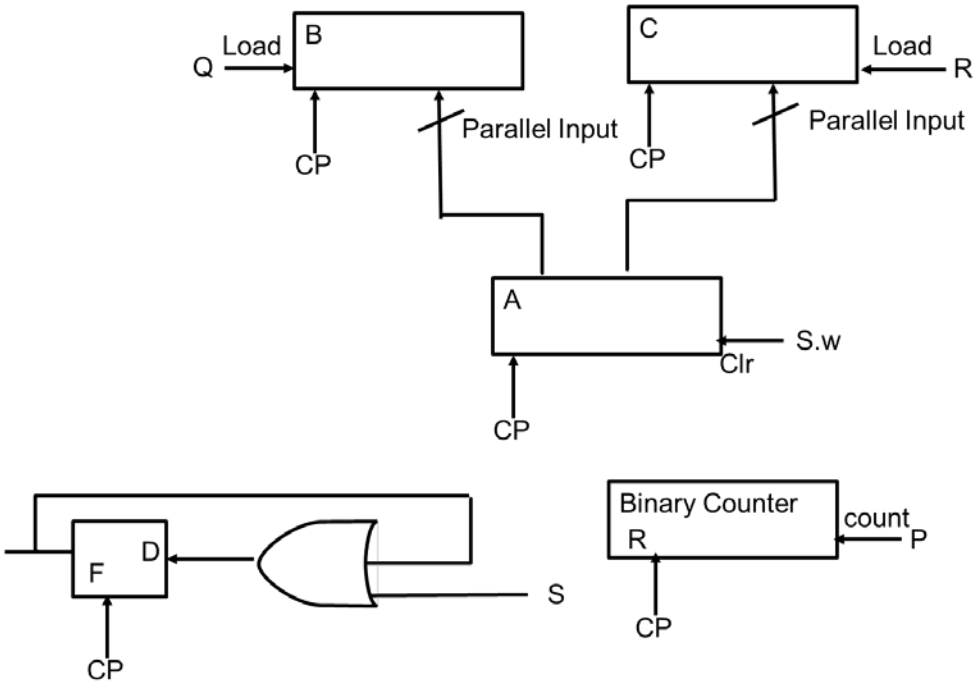
# Question 1 Solution

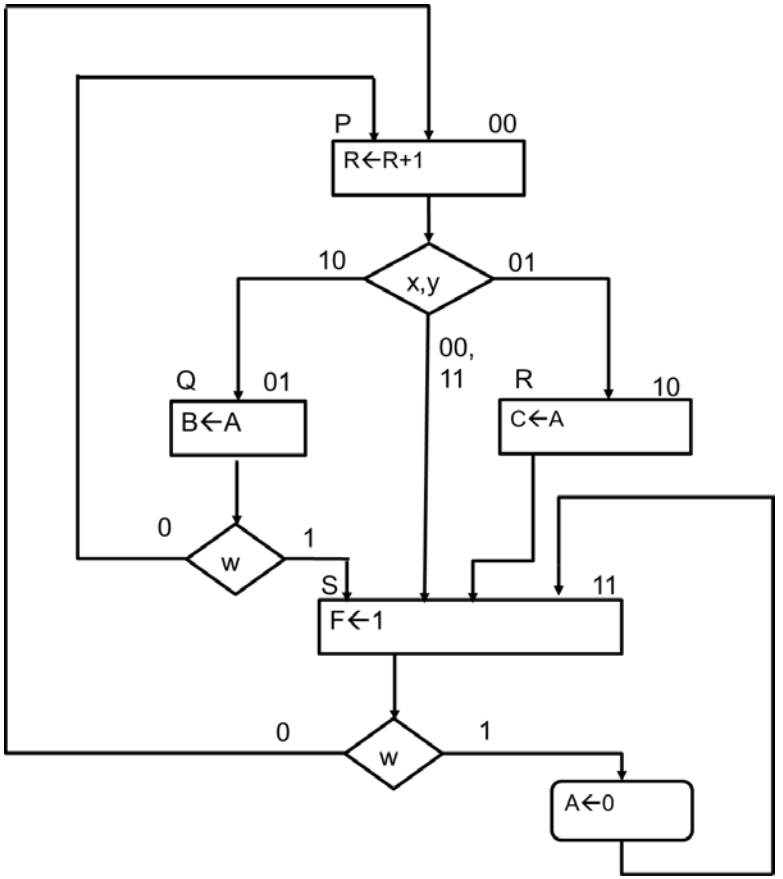



$DG_1=G_1'G_0'(x'y'+xy+x'y)+ G_1'G_0(w)+ G_1G_0'(1)+ G_1G_0(w)$

$DG_0=G_1'G_0'(x'y'+xy+xy')+ G_1'G_0(w)+ G_1G_0'(1)+ G_1G_0(w)$

# Question 1 Solution



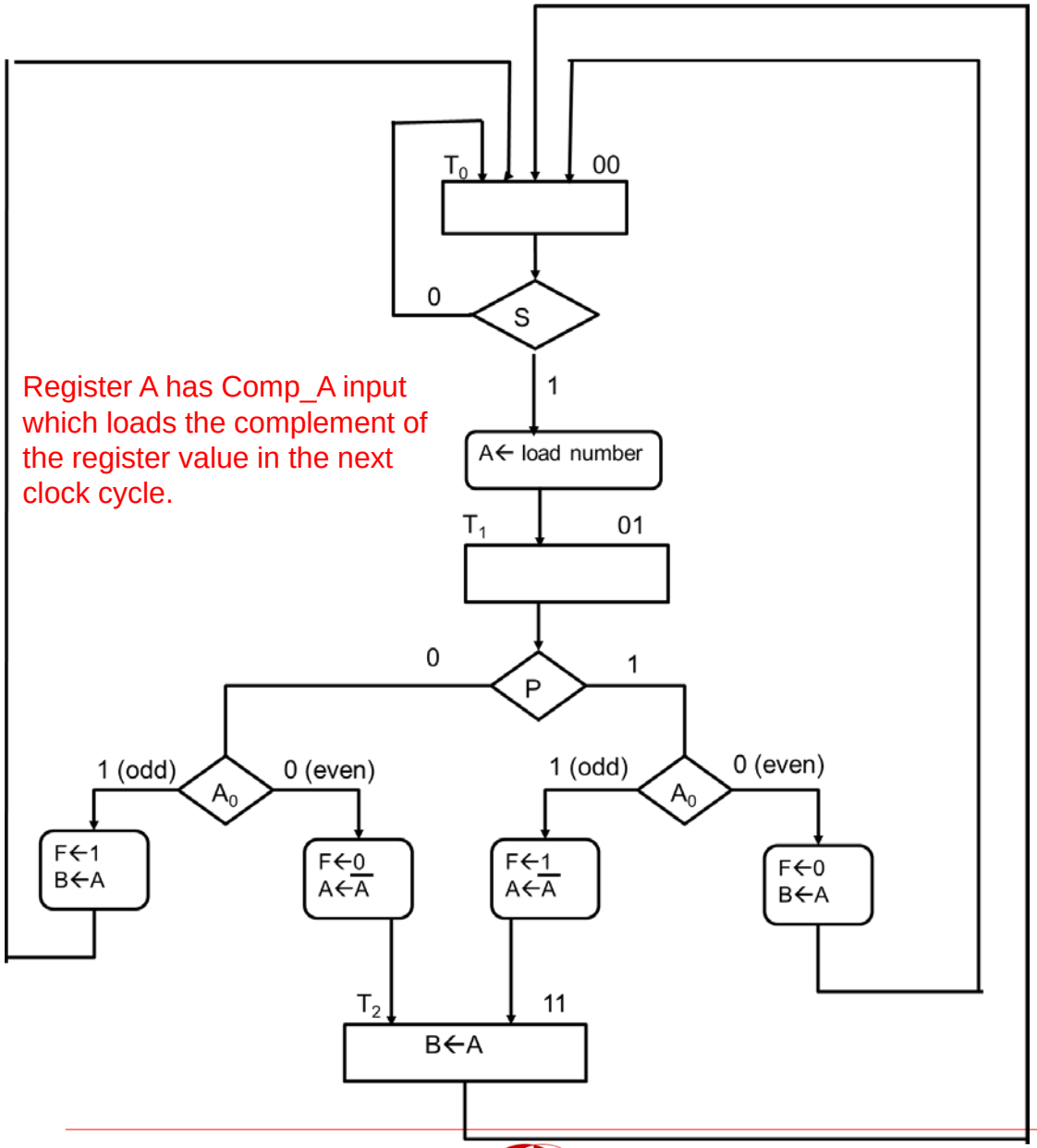
# Question 2

- Registers A and B and a JK FF that is called F will function as follows:
- A start signal S initiates the operation by loading an n-bit number to register A.
- Register A has Comp_A input which loads the complement of the register value in the next clock cycle
- Then an external signal P directs the operation as follows:
- If P=1:
  - If the content of A is an even number, F is cleared and the content of A is transferred to register B
  - If the content of A is an odd number, F is set and the complement of the content of A is transferred to register B
- If P=0:
  - If the content of A is an even number, F is cleared and the complement of the content of A is transferred to register B
  - If the content of A is an odd number, F is set and the content of A is transferred to register B

# Question 2

- Draw an ASM chart using a minimum number of state boxes.
- Draw the Data path circuit diagram
- Design the control unit using all methods. Use JK FFs for the classical sequential circuit design.

# Question 2 Solution

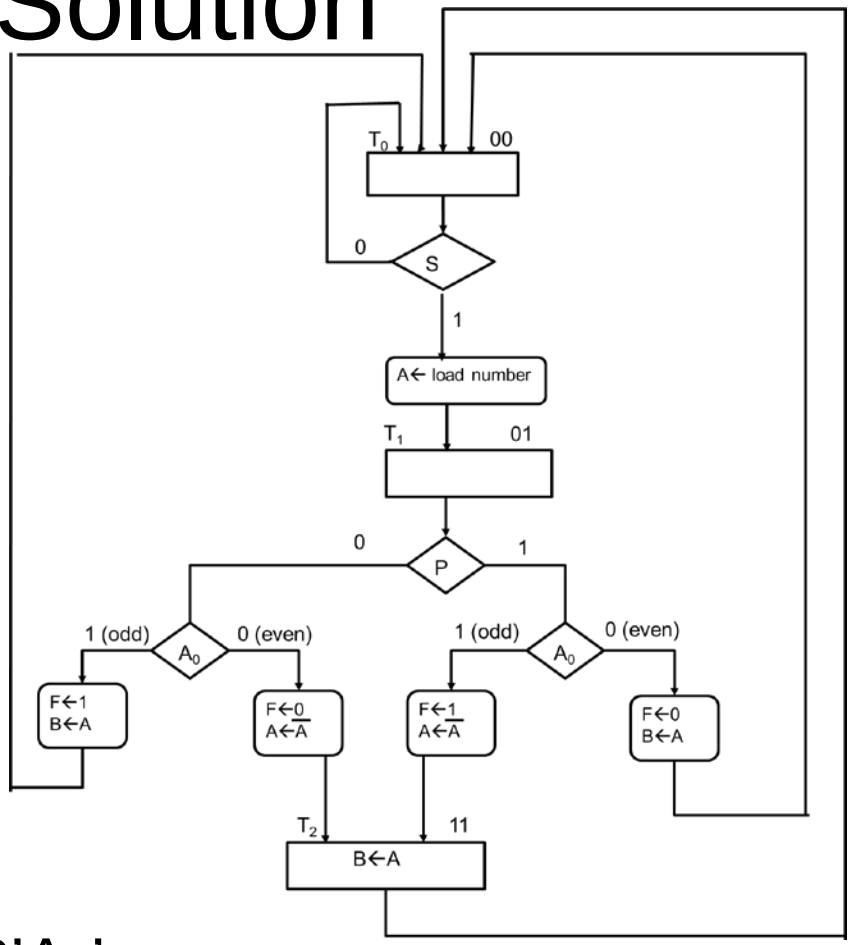



Register A has Comp_A input which loads the complement of the register value in the next clock cycle.

- A start signal S initiates the operation by loading an n-bit number to register A.
- Then
- If P=1:
  - If the content of A is an even number, F is cleared and the content of A is transferred to register B
  - If the content of A is an odd number, F is set and the complement of the content of A is transferred to register B
- If P=0:
  - If the content of A is an even number, F is cleared and the complement of the content of A is transferred to register B
  - If the content of A is an odd number, F is set and the content of A is transferred to register B

# Question 2 Solution

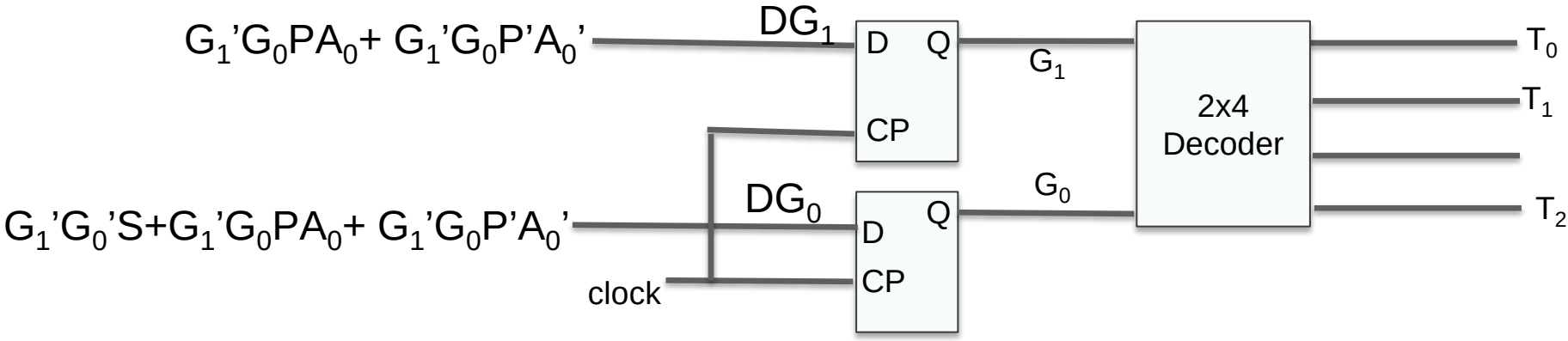
| Present State | | Next State | | Inputs | | | Outputs | | |
|---|---|---|---|---|---|---|---|---|---|
| Name | $G_1G_0$ | Name | $G_1G_0$ | S | P | $A_0$ | T0 | T1 | T2 |
| T0 | 00 | $T_0$ | 00 | 0 | - | - | 1 | 0 | 0 |
| | 00 | $T_1$ | 01 | 1 | - | - | 1 | 0 | 0 |
| T1 | 01 | $T_0$ | 00 | - | 1 | 0 | 0 | 1 | 0 |
| | 01 | $T_0$ | 00 | - | 0 | 1 | 0 | 1 | 0 |
| | 01 | $T_2$ | 11 | - | 1 | 1 | 0 | 1 | 0 |
| | 01 | $T_2$ | 11 | - | 0 | 0 | 0 | 1 | 0 |
| T2 | 11 | $T_0$ | 00 | - | - | - | 0 | 0 | 1 |




$DG_0=G_1'G_0'S+G_1'G_0PA_0+ G_1'G_0P'A_0'$

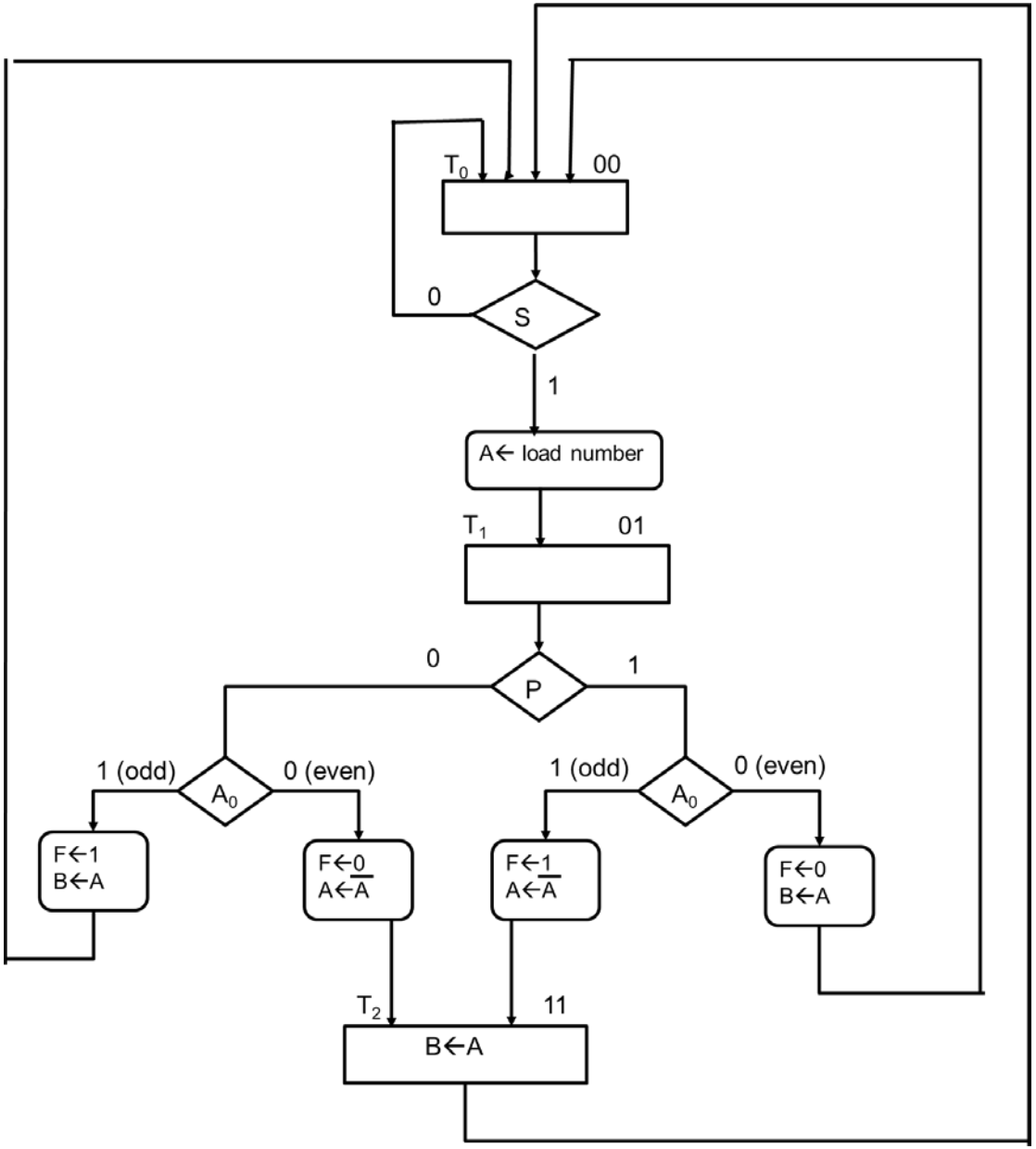
$DG_1=G_1'G_0PA_0+ G_1'G_0P'A_0'$

# Question 2 Solution




$DG_0=G_1'G_0'S+G_1'G_0PA_0+ G_1'G_0P'A_0'$

$DG_1=G_1'G_0PA_0+ G_1'G_0P'A_0'$



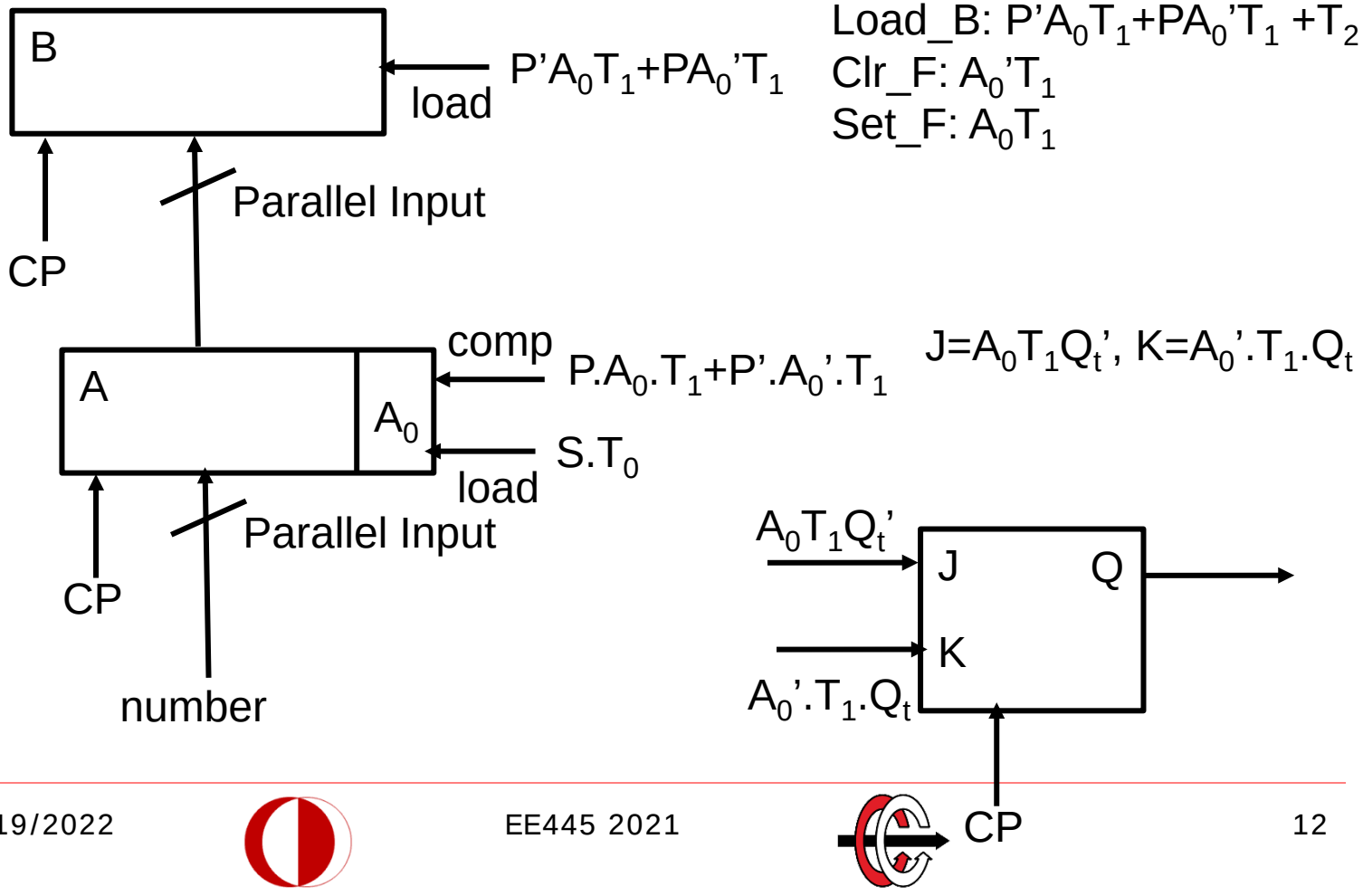

# Question 2 Solution

Load_A: $S.T_0$
Comp_A: $P.A_0.T_1+P'.A_0'.T_1$
Load_B: $P'A_0T_1+PA_0'T_1+T_2$
Clr_F: $A_0'T_1$
Set_F: $A_0T_1$

$J=A_0T_1Q_t'$, $K=A_0'.T_1.Q_t$

| $A_0$ | $T_1$ | $Q_t$ | $Q_{t+1}$ | J | K |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | x |
| 0 | 0 | 1 | 1 | x | 0 |
| 0 | 1 | 0 | 0 | 0 | x |
| 0 | 1 | 1 | 0 | x | 1 |
| 1 | 0 | 0 | 0 | 0 | x |
| 1 | 0 | 1 | 1 | x | 0 |
| 1 | 1 | 0 | 1 | 1 | x |
| 1 | 1 | 1 | 1 | x | 0 |

# Question 2 Solution



# Question 3

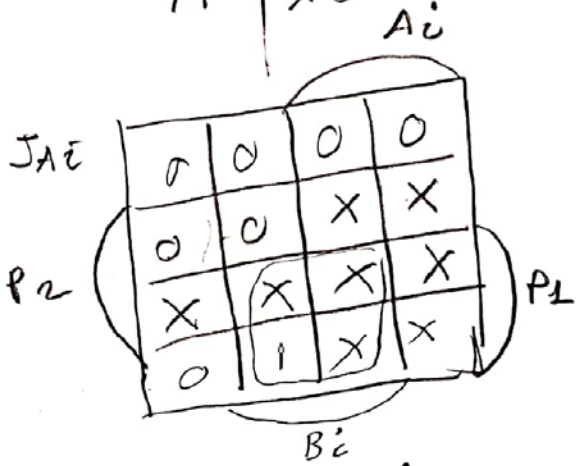
- Design and draw the typical cell Ai of register A as specified below using formal design method with a JK FF.
  - P1: A←B
  - P2: A←A.B
- The combinational circuit should be minimum.
- Show all steps of the design.
- Assume that P1.P2=0 is always satisfied.

# Question 3 Solution

| $P_1$ $P_2$ | $A_i$ $B_i$ | $\bar{A}_i$ | $J_{A_i}$ $K_{A_i}$ |
|---|---|---|---|
| 0 0 | X X | $A_i$ | 0 0 |
| 0 1 | 0 0 | 0 | 0 X |
| 0 1 | 0 1 | 0 | 0 X |
| 0 1 | 1 0 | 0 | X 1 |
| 0 1 | 1 1 | 1 | X 0 |
| 1 0 | 0 0 | 0 | 0 X |
| 1 0 | 0 1 | 1 | 1 X |
| 1 0 | 1 0 | 0 | X 1 |
| 1 0 | 1 1 | 1 | X 0 |
| 1 1 | X X | X | X X |

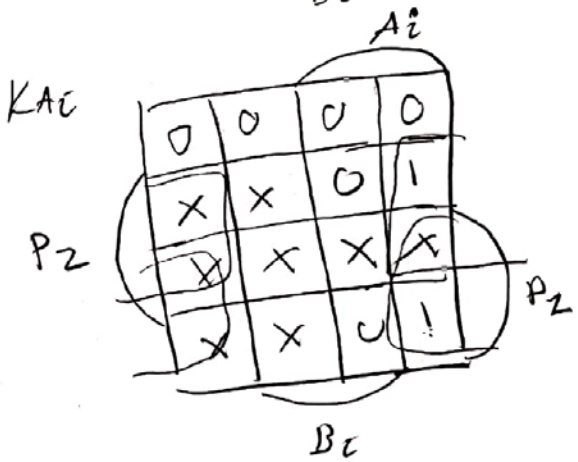
Excitation

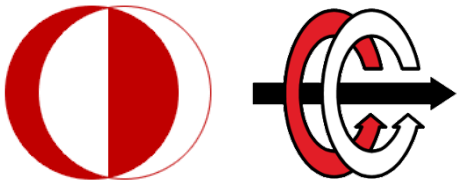
| $Q$ $\bar{Q}$ | J K |
|---|---|
| 0 0 | 0 X |
| 0 1 | 1 X |
| 1 0 | X 1 |
| 1 1 | X 0 |




$J_{A_i} = B_i P_1$

$K_{A_i} = B_i' P_2 + B_i P_1'$





# Algorithmic State Machine

## Practice Questions