Control Unit - Testing

Instruction 1 - 11001100011

LD R2, @A
1-**1001**-10-0011
*Q-**LD opcode**-R2-Address3*

Signals that will be controlled
IR Load Enable, PC Count Enable, opcode decoder(D9), Q, AR Load, R2 Load, DM Read, Bus Selection Controls, SC Clear

Instruction 2 – 01001000100

LD R0, #4
0-**1001**-00-0100
*Q-**LD opcode**-R0-Data=4*

Signals that will be controlled
IR Load Enable, PC Count Enable, opcode decoder(D9), Q, R0 Load, BUS Selection Controls, SC Clear

Instruction 3 – 00010011000

ADD R1, R2, R0
X-**0010**-01-10-00
*Q-**ADD opcode**-R1-R2-R0*

Signals that will be controlled
IR Load Enable, PC Count Enable, opcode decoder (D2), ALU OPR, BUS Selection Controls (Read from R0 and R2 and load R1), SC Clear

Instruction 4 – 01000010101

ST R1, @S
0-**1000**-01-0101
*Q-**ST opcode**-R1-Address5*

Signals that will be controlled
IR Load Enable, PC Count Enable, opcode decoder (D8), AR Load Enable, DM Write Enable, BUS Selection Controls(Read from R1), SC Clear

Instruction 5 – 01010000100

IO R1
0-**1010**-XX-01-XX
*Q-**IO opcode**-XX-R1-XX*

Signals that will be controlled
IR Load Enable, PC Count Enable, opcode decoder (D10), IR Load, BUS Selection Controls(Read from R1), SC Clear

Checklist for Control Unit

Clock

Sequence Counter

SC INR, CLR
How did you design SC?
When do you clear SC?

BUS control

Register selection
Memory selection
Loading from BUS
S_A, S_B, S_C, S_D selection signals

ALU Control

Operation
ALU Selection
Overflow

Register Control

PC, IR, AR, SP, Registers
Load / Clear / Inr / Dcr Signals
S_E for PC input selection
IN, Out selection

Memory Control

DM Read, DM Write, IM Read, SM Read, SM Write

Operations

Check flow and all control signals of LD, TSF, ST operations
Check flow and all control signals of CAL, RET, JMP, CJMP, JMR operations
Do you have ORG instruction?