# EE446 – LAB 5

## PRELIMINARY WORK

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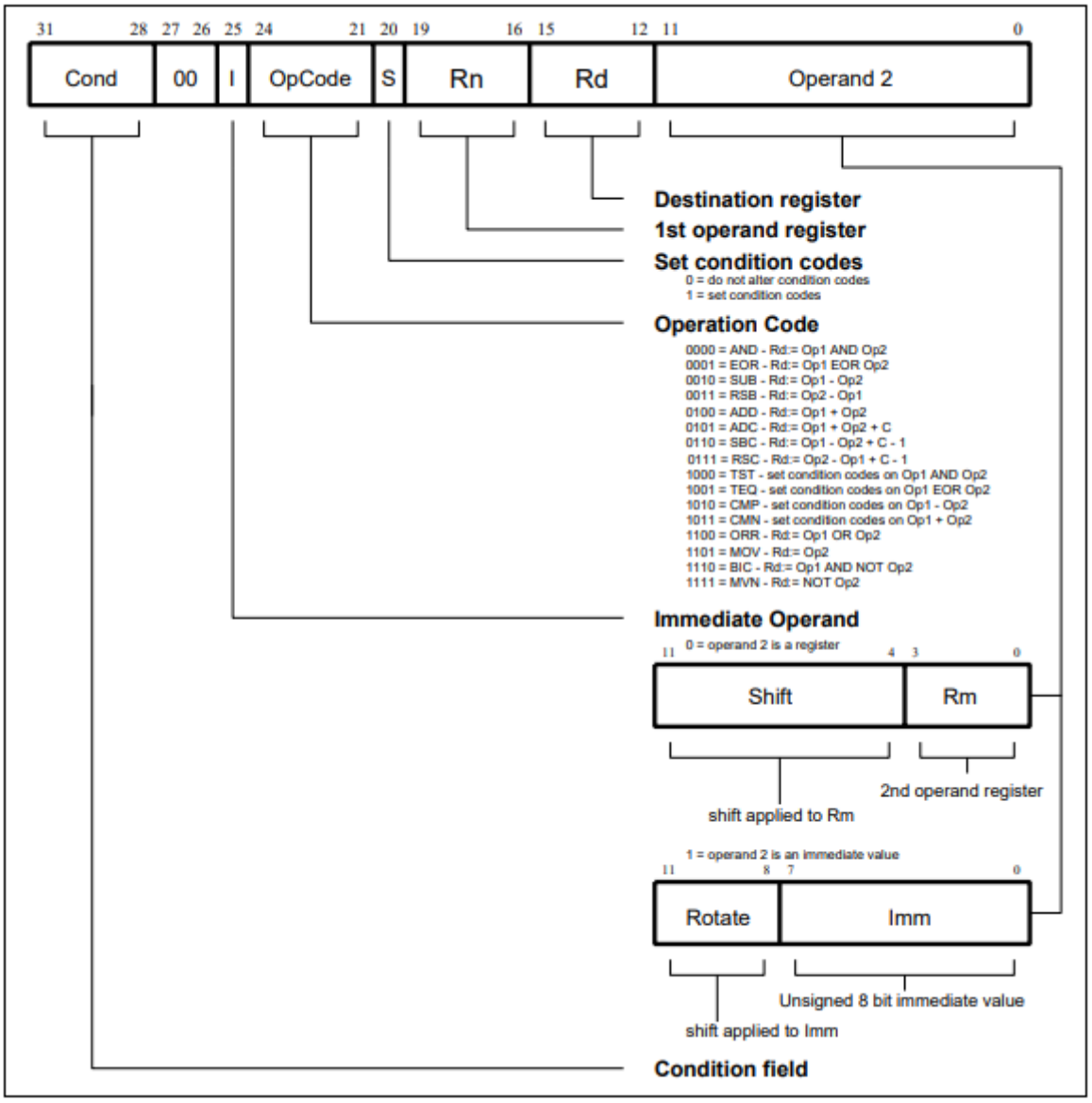
# 1. Controller Design

## 1.1. ISA

### 1.1.1. Data Processing

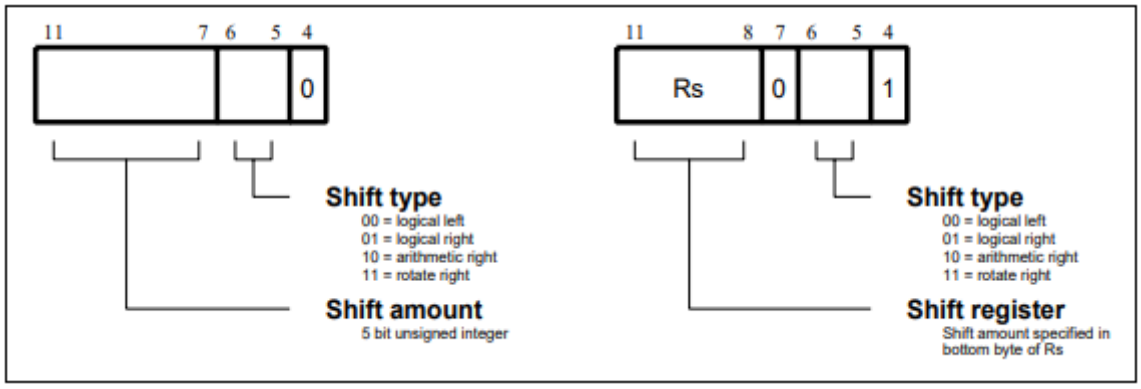


#### 1.1.1.1. ALU Function

| Assembler Mnemonic | OpCode | Action |
|---|---|---|
| AND | 0000 | operand1 AND operand2 |
| EOR | 0001 | operand1 EOR operand2 |
| SUB | 0010 | operand1 - operand2 |
| RSB | 0011 | operand2 - operand1 |
| ADD | 0100 | operand1 + operand2 |
| ADC | 0101 | operand1 + operand2 + carry |
| SBC | 0110 | operand1 - operand2 + carry - 1 |
| RSC | 0111 | operand2 - operand1 + carry - 1 |
| TST | 1000 | as AND, but result is not written |
| TEQ | 1001 | as EOR, but result is not written |
| CMP | 1010 | as SUB, but result is not written |
| CMN | 1011 | as ADD, but result is not written |
| ORR | 1100 | operand1 OR operand2 |
| MOV | 1101 | operand2(operand1 is ignored) |
| BIC | 1110 | operand1 AND NOT operand2(Bit clear) |
| MVN | 1111 | NOT operand2(operand1 is ignored) |

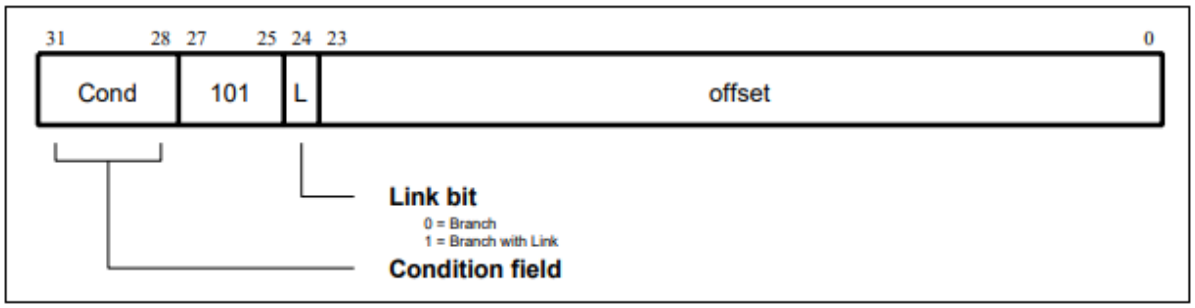
AND, ORR, EOR, BIC, ADD, SUB, CMP, MOV are implemented

#### 1.1.1.2. Shifter




Immediate shifter and register shifter is implemented. (LSL, LSR, ASR, ROR, ROL)

### 1.1.2. Branch

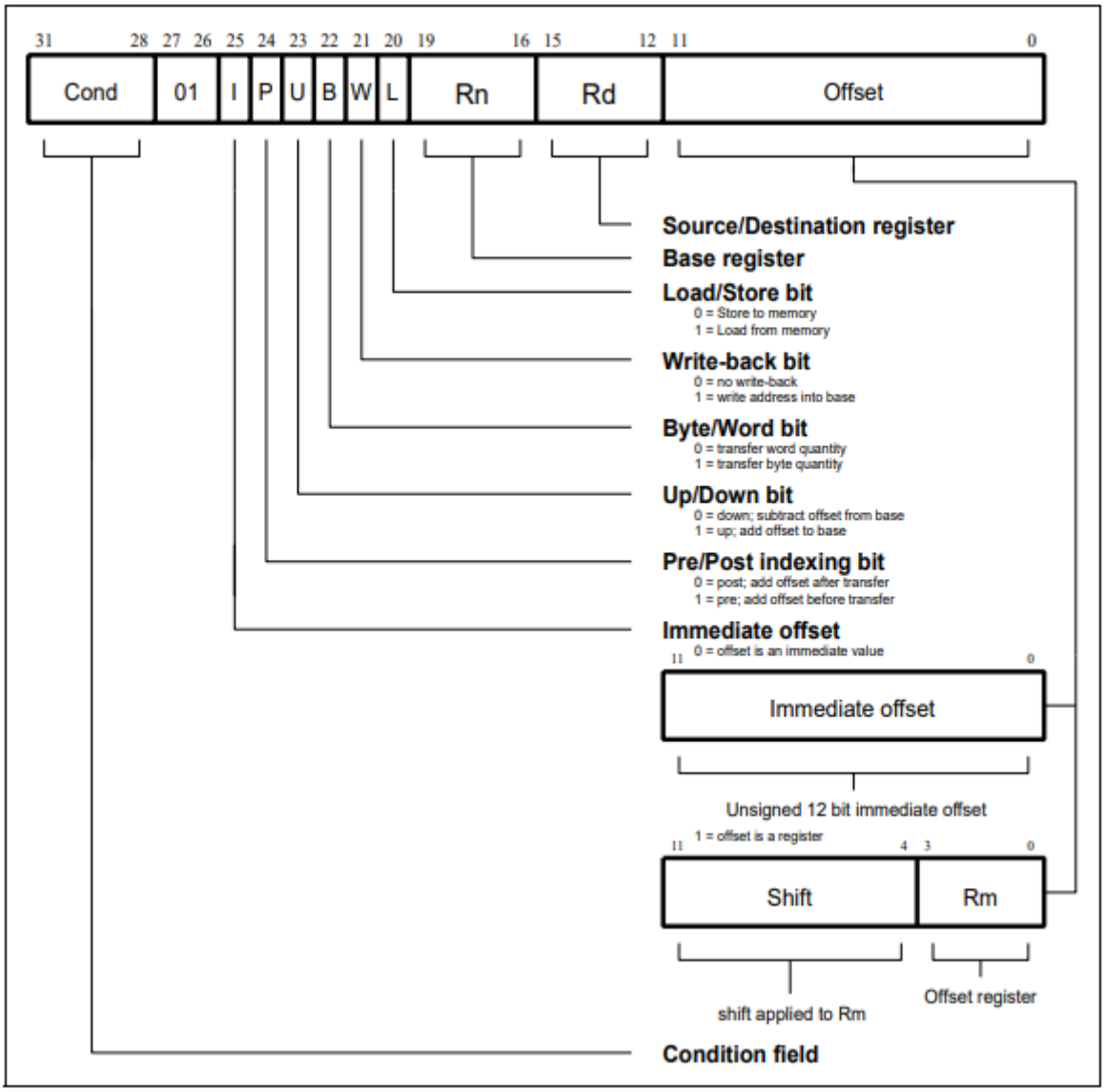



B and BL is implemented.

BX is implemented as:

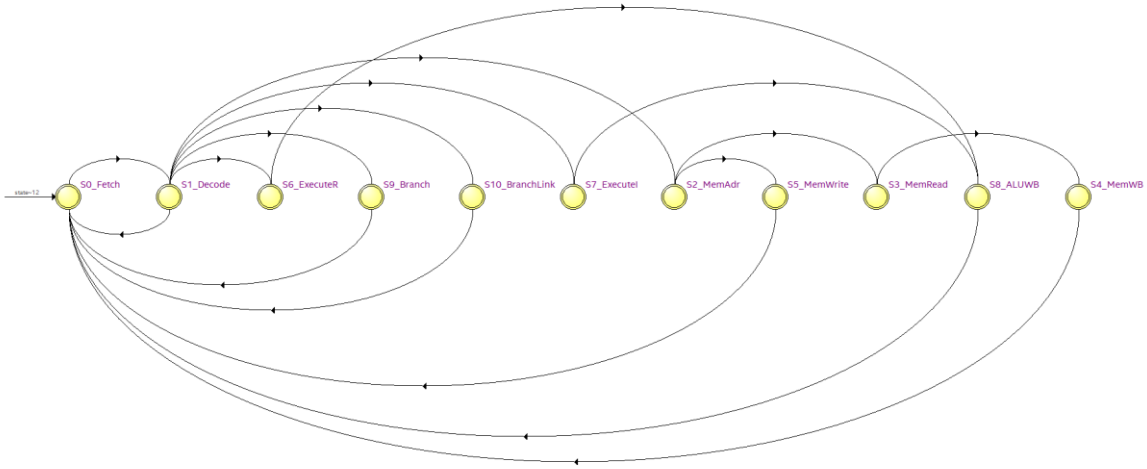
BX Rn -> MOV R15, Rn

### 1.1.3. LDR / STR



## 1.2. Controller Unit Design

### 1.2.1. FSM

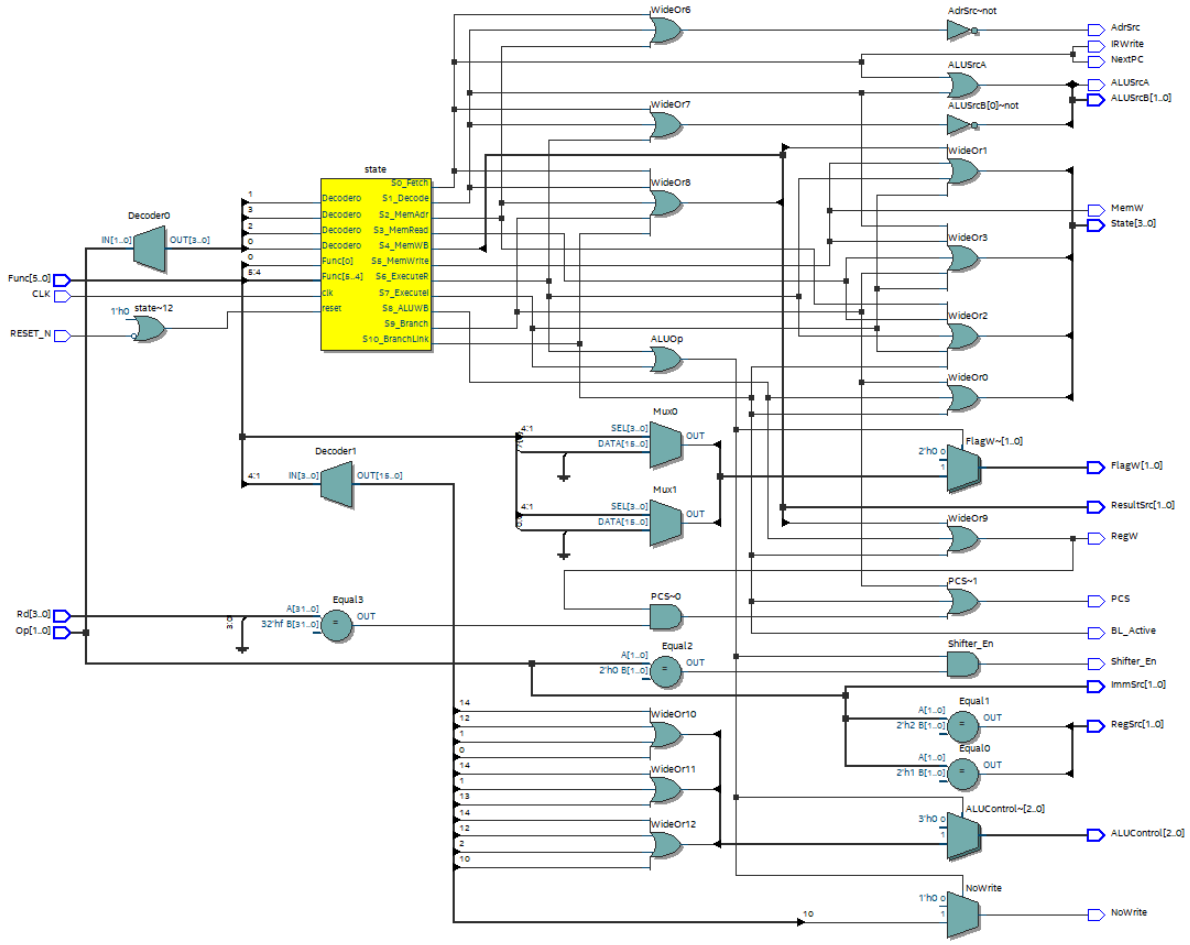



| From | To | Condition |
|---|---|---|
| S0_Fetch | S1_Decode | |
| S1_Decode | S10_BranchLink | (Func[4]).(Decoder0) |
| S1_Decode | S7_ExecuteI | (Func[5]).(Decoder0) |
| S1_Decode | S2_MemAdr | (Decoder0) |
| S1_Decode | S0_Fetch | (Decoder0) |
| S1_Decode | S6_ExecuteR | (!Func[5]).(Decoder0) |
| S1_Decode | S9_Branch | (!Func[4]).(Decoder0) |
| S2_MemAdr | S3_MemRead | (Func[0]) |
| S2_MemAdr | S5_MemWrite | (!Func[0]) |
| S3_MemRead | S4_MemWB | |
| S4_MemWB | S0_Fetch | |
| S5_MemWrite | S0_Fetch | |
| S6_ExecuteR | S8_ALUWB | |
| S7_ExecuteI | S8_ALUWB | |
| S8_ALUWB | S0_Fetch | |
| S9_Branch | S0_Fetch | |
| S10_BranchLink | S0_Fetch | |

Control Signals

| |
|---|
| PCWrite |
| RegWrite |
| MemWrite |
| IRWrite |
| AdrSrc |
| ResultSrc |
| ALUSrcA |
| ALUSrcB |
| ImmSrc |
| RegSrc |
| ALUControl |
| BL_Active |
| Shifter_En |
| State |

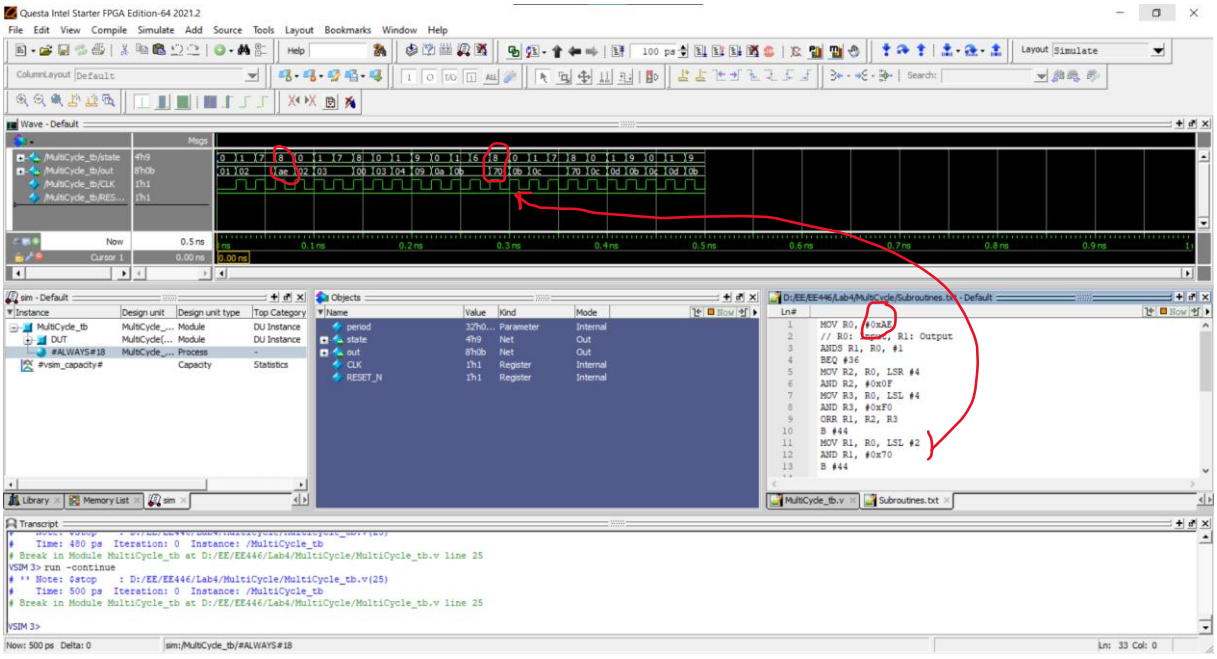
FSM Circuitry



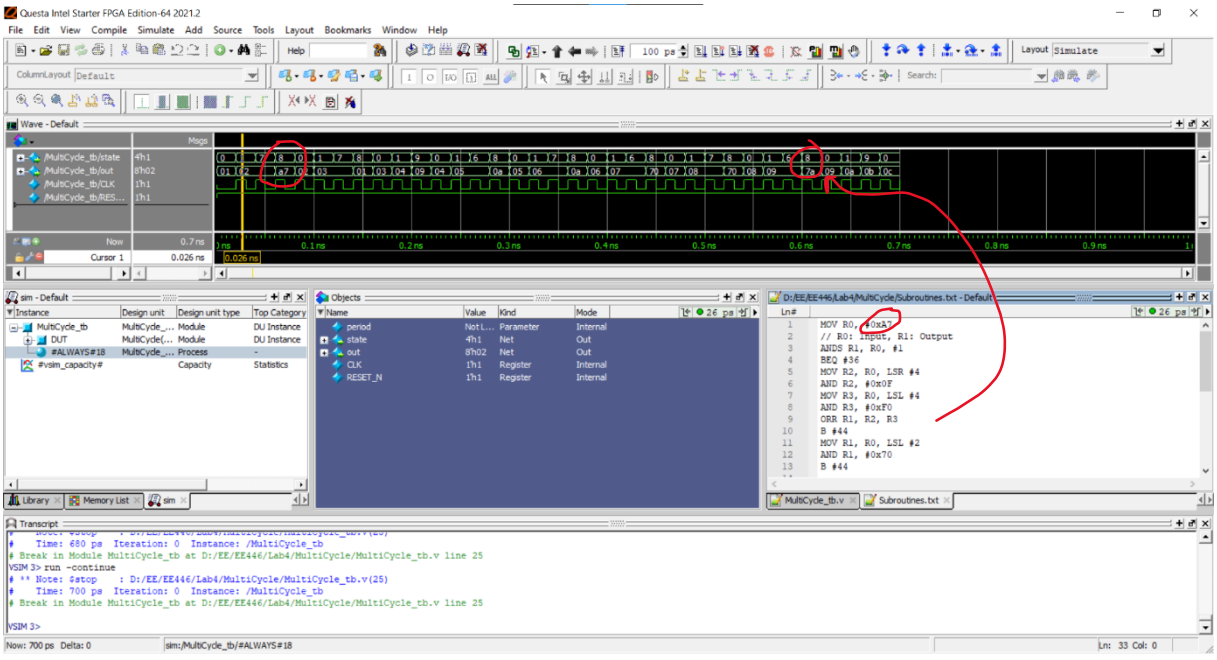
# 2. Validation

## 2.1. Even – Odd

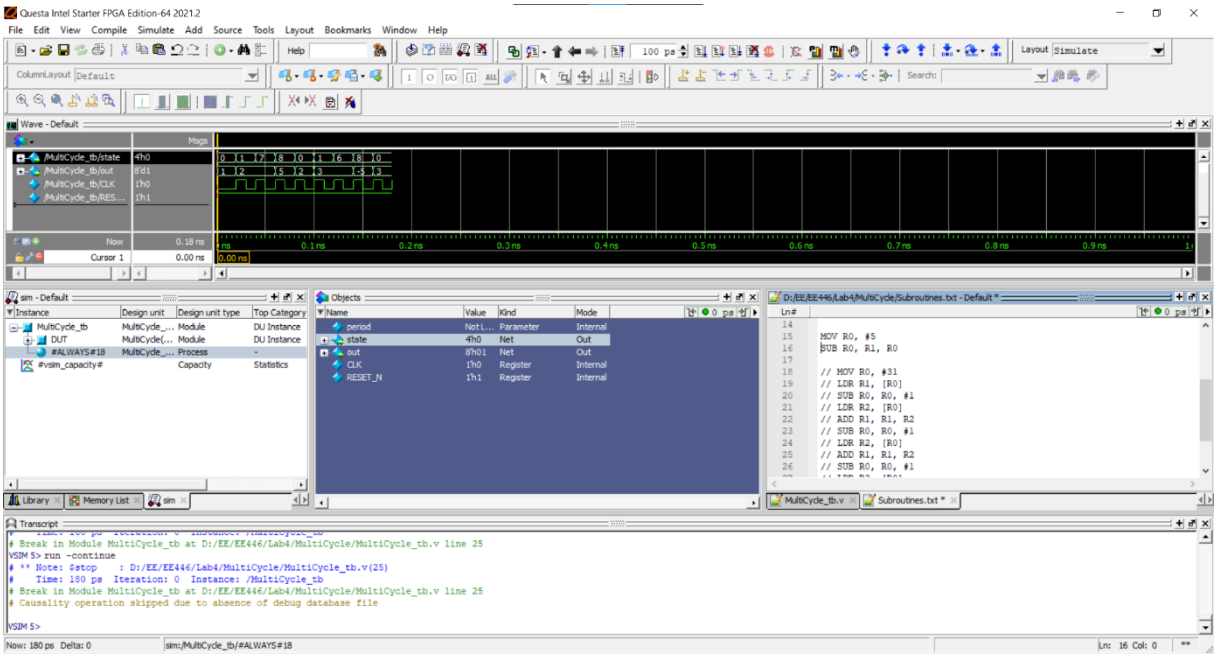
Even:




Odd:



## 2.2. 2's Compliment




## 2.3. Array Addition

Array: [5, 4, 3, 2, 1]