DE1-SoC FAQ

Q1

Can I set the I/O standard of DE1-SoC' s GPIO header to 2.5V? Does it support LVDS transmission?

A1 : The VCCIO of FPGA' s I/O bank connected to the GPIO pin has fixed voltage level to 3.3V, therefore it only allows 3.3V signal transmission. If you want to connect it to any 2.5V voltage level logic, you can design a voltage conversion circuit of your own.

On the other hand, the GPIO on DE1-SoC does not have LVDS routing so it cannot support LVDS signal transmission either.

Q2

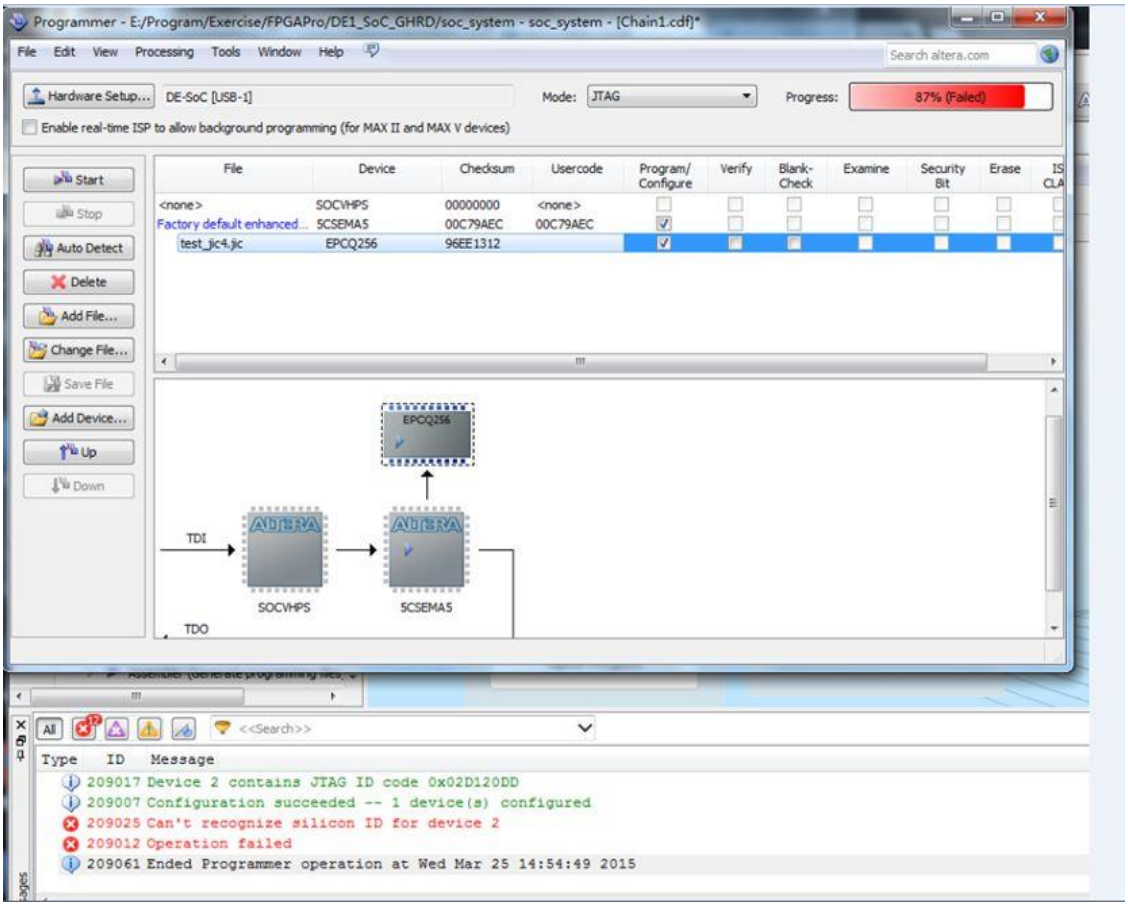
I built a Nios II project on DE1-SoC using a demo *(DE1_SoC_SDRAM_Nios_Test)* from the System CD. But the program execution of SDRAM was quite unstable. Do you have any related resources for timing analysis control for SDRAM on DE1-SoC?

A2 : Please download the project created by Terasic for its 2014 training session at:
http://download.terasic.com/downloads/cd-rom/de1-soc/FAQ/de1_soc_traning.zip

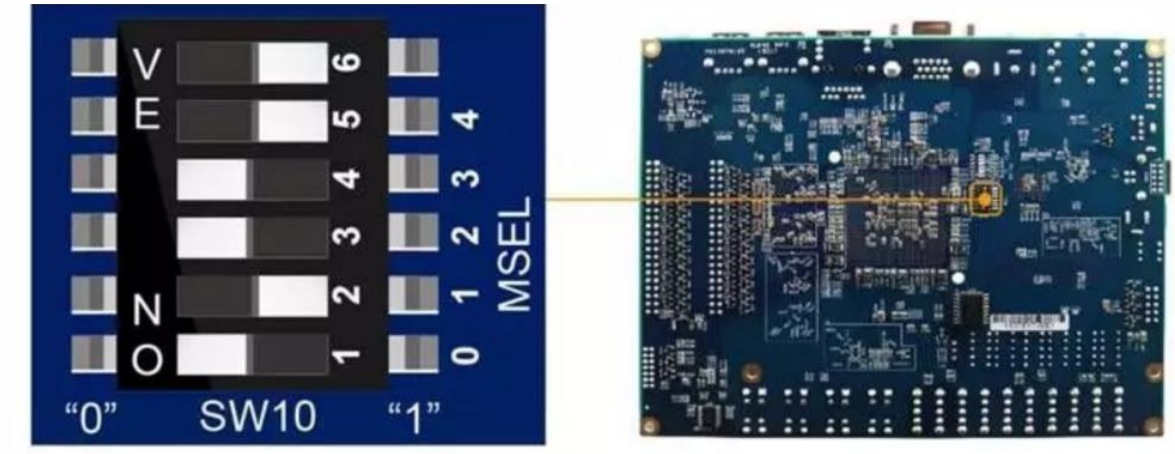
and see the timing from file route:
de1_soc_traning\de1_soc_traning\lab \Advanced_Demo\demo1_axi

Q3

After I programmed EPCQ256 device and have successfully generated *.jic* file, I tried to download the file, but a message *"209025 Can' t recognize silicon ID device 2"* showed up. What has gone wrong during the process?



A3 : The problem was caused by the MSEL setting error of your DE1-SoC. Please switch the MSEL to "10010" (AS mode) for FPGA configuration as illustrated in the picture below.



Q4

How do I properly shut down Linux and the DE1-SoC board after running the Linux desktop system?

A4 : DE1-SoC does not provide any physical power-down mechanism. You could simply power off the board after Linux is shut down and the screen goes black.

Q5

I tried to add signal DE1-SoC' s UART pin to the SignalTap tool in Quartus but was unable to find it. Nevertheless, the UART port is transmitting & receiving data without any problem. Why?

A5 : SignalTap is a tool which can run on the FPGA chip. On the other hand, HPS is a hard IP core and UART is a hardware that belongs to HPS. Therefore, you won' t be able to add UART signal in SignalTap.

Q6

I designed a project and downloaded it in the form of *.jic* to DE1-SoC. I tried to download again and clicked Auto Detect from the toolbar of the Programmer window, but a message popped up saying "Unable to scan device chain. Hardware is not connected". Why?

A6: It may be that the pin assignment in your design has illegal settings which causes the issue. The problem can be solved by overwriting the *.jic* to the board with the file from Terasic website (ex. .jic file from the factory example). Follow the steps below:

1. Switch the MSEL to “00000” mode.
2. Download *.sof* file from the default example (DE1_SoC_Default). Once the download is complete, set the MSEL to "10010" setting and download the *.jic* file of factory example to DE1-SoC.
3. If you plan to continue downloading *.jic* of your own project, we suggest you to modify the design first. To learn more about pin assignment, you could refer to the example provided in the System CD from Terasic website.

Q7

What are the differences between the Control Panel tool of DE1-SoC and other FPGA development boards?

A7 :

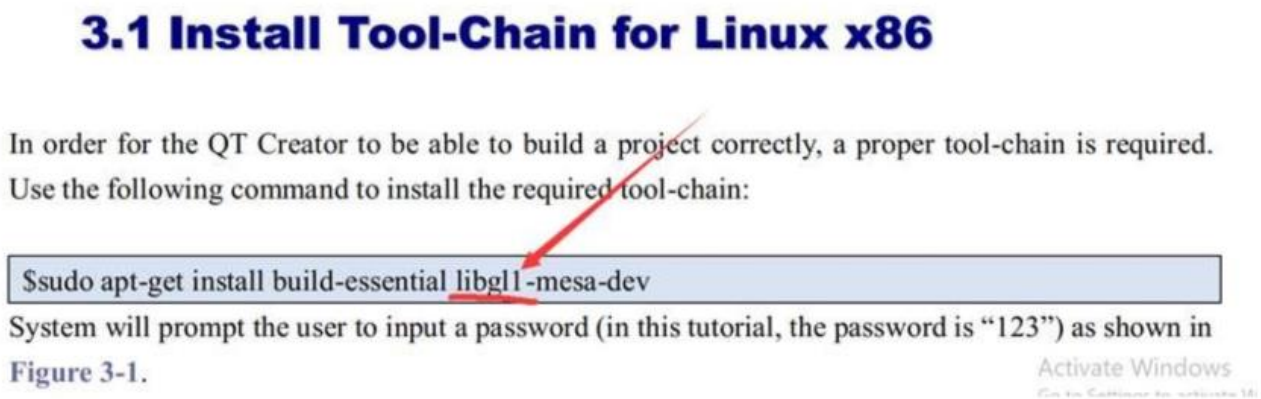
1. The Control Panel program of DE1-SoC was designed based on QT toolkit. The Control Panel of most non-SoC FPGA boards, on the other hand, is built with Borland C++ Builder.

2. The Control Panel of DE1-SoC runs Linux programs from its own HPS hardware and controls FPGA components through the on-chip AXI bus. By contrast, the Control Panel of non-SoC FPGA boards controls FPGA components from Windows program on Host PC through USB blaster circuit.

Q8

I followed the instruction from *DE1-SoC_Control_Panel.pdf* to install x86 GCC tool-chain, then inputted "udo apt-get install build-essential libgll-mesa-dev" and got a notification of "Command line option 'e' [from -mesa] is not understood in combination with the other options". Why?

A8 : There is a typo in your input command, it should be "libgl1" instead of "libglI", as shown in the picture.



3.1 Install Tool-Chain for Linux x86

In order for the QT Creator to be able to build a project correctly, a proper tool-chain is required. Use the following command to install the required tool-chain:

```
$sudo apt-get install build-essential libgl1-mesa-dev
```

System will prompt the user to input a password (in this tutorial, the password is "123") as shown in Figure 3-1.

Q9

How to connect and use D5M with DE1-SoC? Do you have any example?

A9 : For those who do not own a Quartus license, please refer to the following example for realizing FPGA image processing:
http://download.terasic.com/downloads/cd-rom/de1-soc/FAQ/DE1_SoC_D5M_GPIO1.zip

If you are searching for better image resolution and you have a Quartus license (or even VIP IP license), then you should take a look of the following:
http://download.terasic.com/downloads/cd-rom/de1-soc/FAQ/DE1_SoC_D5M_VIP.rar

Q10

Can the UART interface of DE1-SoC be used for controlling sending and receiving of signals via FPGA side?

A10: DE1-SoC' s UART is a hardware that belongs to the HPS fabric. Normally, we do not recommend user to control signals from the FPGA side since the implementation is likely to be quite complicated.

If you need a UART on the FPGA side, you can directly connect an external UART circuit onto the GPIO header, which is simpler to implement.