

CS224  
Lab No.6

Section No. 1

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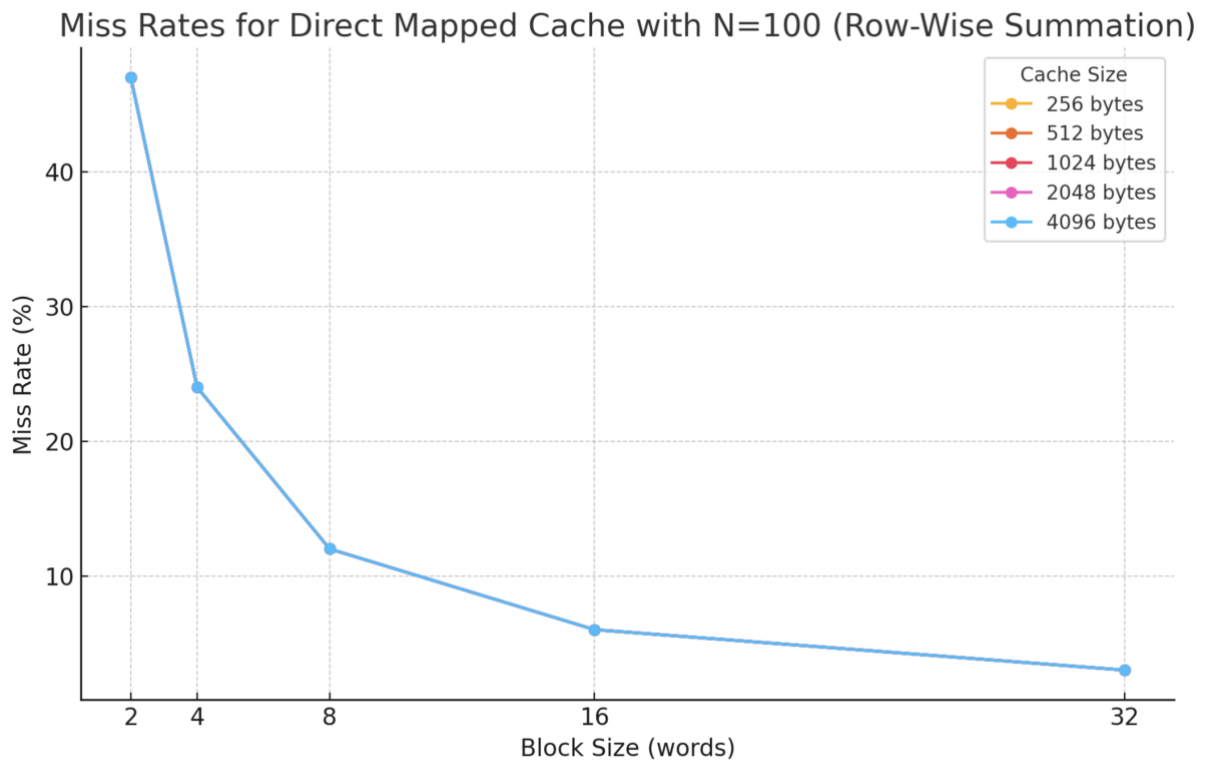
Date 11.12.2024

### Report ( Matrix with N=100)

Part A:

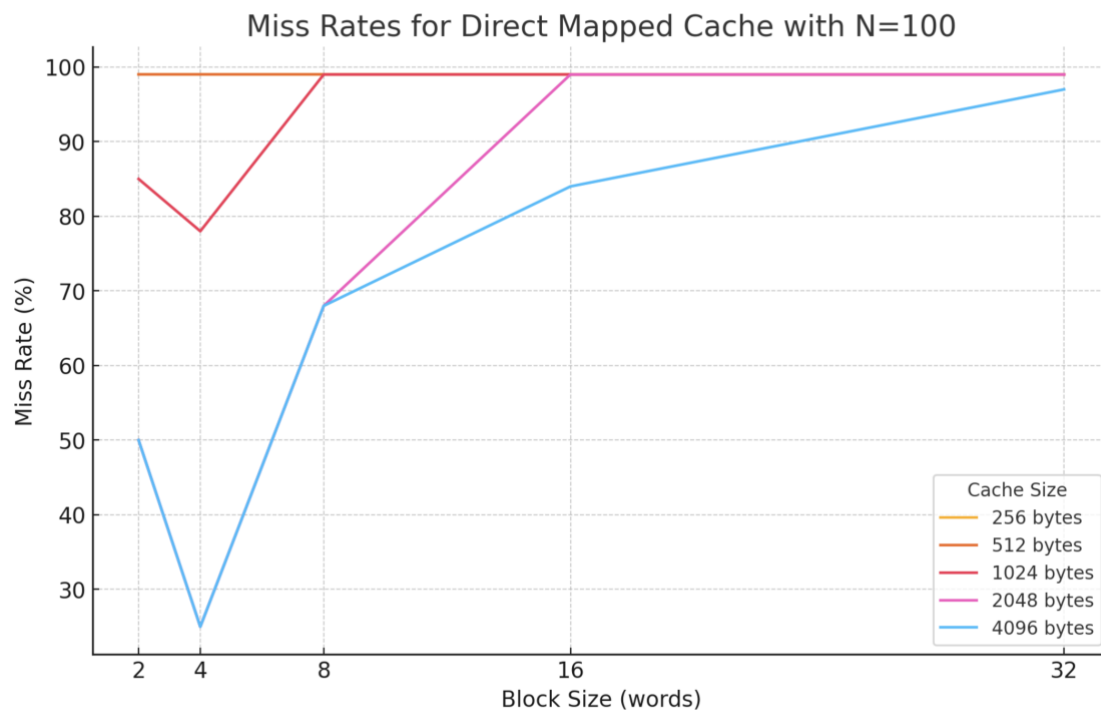
Block Size(words)  Cache Size (Bytes)	2	4	8	16	32
256	Miss rate: 47%  Hit rate: 53%  number of misses: 5016	Miss rate: 24%  Hit rate: 75%  number of misses: 2509	Miss rate: 12%  Hit rate: 88%  number of misses: 1255	Miss rate: 6%  Hit rate: 94%  number of misses: 628	Miss rate: 3%  Hit rate: 97%  number of misses: 315
512	Miss rate: 47%  Hit rate: 53%  number of misses: 5016	Miss rate: 24%  Hit rate: 75%  number of misses: 2509	Miss rate: 12%  Hit rate: 88%  number of misses: 1255	Miss rate: 6%  Hit rate: 94%  number of misses: 628	Miss rate: 3%  Hit rate: 97%  number of misses: 315
1024	Miss rate: 47%  Hit rate: 53%	Miss rate: 24%  Hit rate:	Miss rate: 12%  Hit rate:	Miss rate: 6%  Hit rate:	Miss rate: 3%  Hit rate:

	number of misses: 5016	75% number of misses: 2509	88% number of misses: 1255	94% number of misses: 628	97% number of misses: 315
2048	Miss rate: 47%  Hit rate: 53%  number of misses: 5016	Miss rate: 24%  Hit rate:  75%  number of misses: 2509	Miss rate: 12%  Hit rate:  88%  number of misses: 1255	Miss rate: 6%  Hit rate:  94%  number of misses: 628	Miss rate: 3%  Hit rate:  97%  number of misses: 315
4096	Miss rate: 47%  Hit rate: 53%  number of misses: 5016	Miss rate: 24%  Hit rate:  75%  number of misses: 2509	Miss rate: 12%  Hit rate:  88%  number of misses: 1255	Miss rate: 6%  Hit rate:  94%  number of misses: 628	Miss rate: 3%  Hit rate:  97%  number of misses: 315



Block Size(words)	2	4	8	16	32
Cache Size (Bytes)	2	4	8	16	32
256	Miss rate: 99% number of misses: 10017	Miss rate: 99% number of misses: 10017	Miss rate: 99% number of misses: 10010	Miss rate: 99% number of misses: 10006	Miss rate: 99% number of misses: 10003
512	Miss rate: 99%	Miss rate: 99%	Miss rate: 99%	Miss rate: 99%	Miss rate: 99%

	number of misses:  10017	Number of misses:  10010	number of misses:  11310	number of misses:  10016	number of misses:  10016
1024	Miss rate: 85%  number of misses: 8617	Miss rate: 78%  number of misses:  10052	Miss rate: 99%  number of misses:  10006	Miss rate: 99%  number of misses:  10004	Miss rate: 99%  number of misses:  10003
2048	Miss rate: 50%  number of misses:  5017	Miss rate: 25%  number of misses:  2510	Miss rate: 68%  number of misses:  7906	Miss rate: 99%  Number of misses:  10004	Miss rate: 99%  number of misses:  10003
4096	Miss rate: 50%  number of misses:  5020	Miss rate: 25%  number of misses:  2510	Miss rate: 68%  number of misses:  6934	Miss rate: 84%  number of misses:  8464	Miss rate: 97%  number of misses:  9917



- As block sizes increase, the miss rate tends to decrease due to improved spatial locality.
- In a cache of fixed size, the number of sets decreases with larger blocks, which can lead to more conflicts.
- The size of the cache itself remains unchanged in this scenario.
- With fully associative mapping, collisions are minimized because any memory block can be mapped to any cache block.

Part B ( n = 100)

	Good hit rate Cache size: 2048 Block size: 4	Medium hit rate Cache size: 1024 Block size: 4	Poor hit rate Cache size: 128 Block size: 2
Fully associative (LRU)	Miss Rate: 25% # of misses: 2524	Miss Rate: 86% # of misses: 17613	Miss Rate: 95% # of misses: 9988
Fully associative (Random)	Miss Rate: 32% # of misses: 7012	Miss Rate: 73% # of misses: 7586	Miss Rate: 97% Number of misses: 20010
Direct Mapped	Miss Rate: 24% # of misses: 5068	Miss Rate: 77% # of misses: 7921	Miss Rate: 98% # of misses: 10512

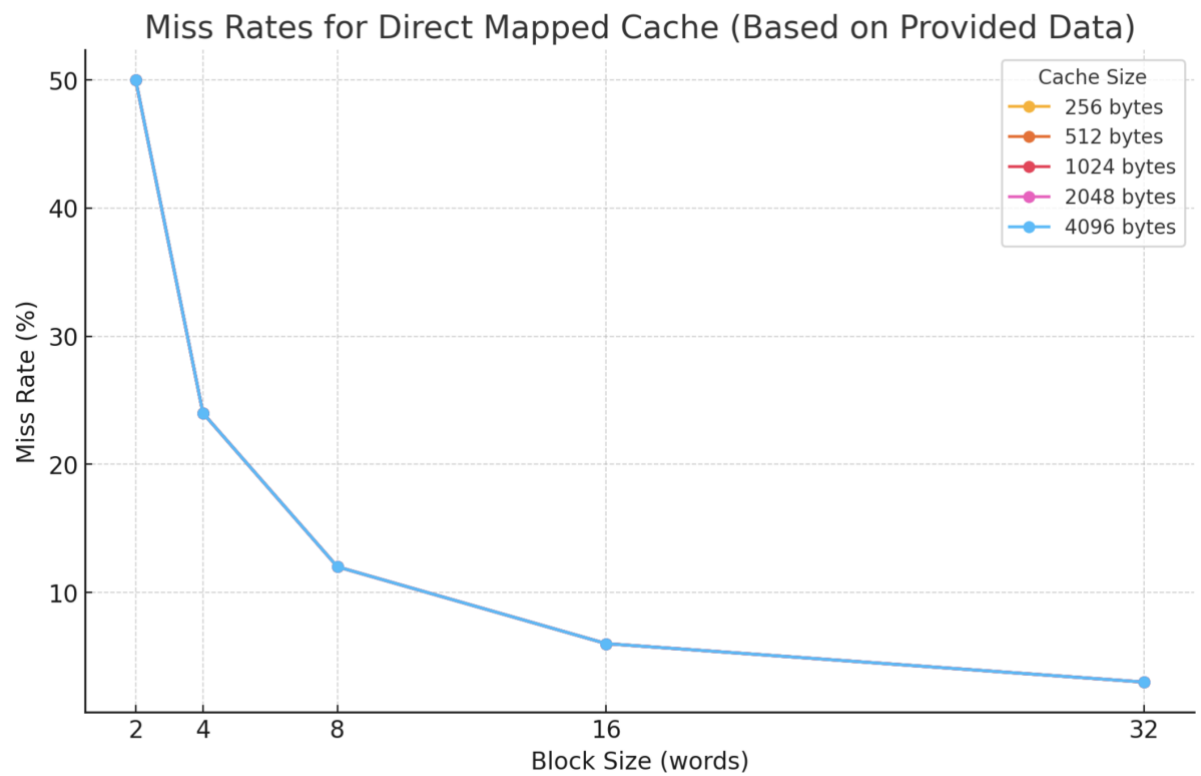
**Part C (n = 100)**

N-way Set Associative Cache Set Size	Good hit Cache: 2048 Block size: 4	Medium hit Cache: 1024 Block size: 4	Poor hit Cache: 128 Block size: 2
<b>2</b>	Miss Rate: 41% # of misses: 17158	Miss Rate: 95% # of misses: 10020	Miss Rate: 96% # of misses: 10004
<b>4</b>	Miss Rate: 24% # of misses: 2529	Miss Rate: 96% # of misses: 10024	Miss Rate: 98% # of misses: 10056
<b>8</b>	Miss Rate: 24% # of misses: 2529	Miss Rate: 97% # of misses: 10024	Miss Rate: 98% # of misses: 10098
<b>16</b>	Miss Rate: 22% # of misses: 2524	Miss Rate: 98% # of misses: 10154	Miss Rate: 96% # of misses: 10024

**Part A (n = 150)**

Block Size(words)					
Cache Size (Bytes)	2	4	8	16	32
256	Miss rate: 50%  number of misses: 11266	Miss rate: 24%  Hit rate: 75%  number of misses: 2509	Miss rate: 12%  Hit rate: 88%  number of misses: 1255	Miss rate: 6%  Hit rate: 94%  number of misses: 628	Miss rate: 3%  Hit rate: 97%  number of misses: 315
	Miss rate:	Miss rate:	Miss rate:	Miss rate:	Miss rate:

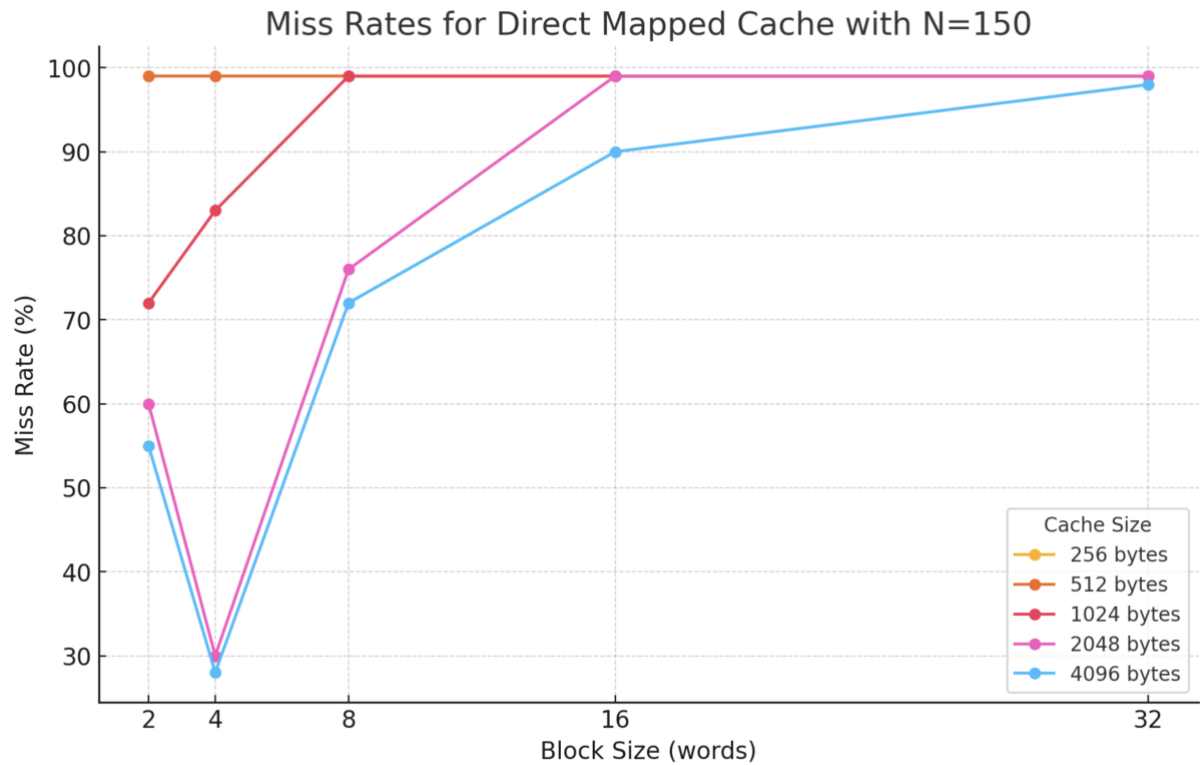
512	50%  number of misses: 11266	24%  Hit rate: 75%  number of misses: 5634	12%  Hit rate: 88%  number of misses: 2812	6%  Hit rate: 94%  number of misses: 1410	3%  Hit rate: 97%  number of misses: 706
1024	Miss rate: 50%  number of misses: 11266	Miss rate: 24%  Hit rate: 75%  number of misses: 5634	Miss rate: 12%  Hit rate: 88%  number of misses: 2812	Miss rate: 6%  Hit rate: 94%  number of misses: 1410	Miss rate: 3%  Hit rate: 97%  number of misses: 706
2048	Miss rate: 50%  number of misses: 11266	Miss rate: 24%  Hit rate: 75%  number of misses: 5634	Miss rate: 12%  Hit rate: 88%  number of misses: 2812	Miss rate: 6%  Hit rate: 94%  number of misses: 1410	Miss rate: 3%  Hit rate: 97%  number of misses: 706
4096	Miss rate: 50%  number of misses: 11266	Miss rate: 24%  Hit rate: 75%  number of misses: 5634	Miss rate: 12%  Hit rate: 88%  number of misses: 2812	Miss rate: 6%  Hit rate: 94%  number of misses: 1410	Miss rate: 3%  Hit rate: 97%  number of misses: 706



Block Size(words)					
Cache Size (Bytes)	2	4	8	16	32
256	Miss rate: 99%  number of misses: 22517	Miss rate: 99%  number of misses: 22510	Miss rate: 99%  number of misses: 22506	Miss rate: 99%  number of misses: 22504	Miss rate: 99%  number of misses: 22503
512	Miss rate: 99%  number of misses:	Miss rate: 99%	Miss rate: 99%	Miss rate: 99%	Miss rate: 99%



	22517	Number of misses: 22510	number of misses: 22506	number of misses: 22504	number of misses: 22503
1024	Miss rate: 64%  number of misses: 14567	Miss rate: 78%  number of misses: 22510	Miss rate: 99%  number of misses: 22506	Miss rate: 99%  number of misses: 22504	Miss rate: 99%  number of misses: 22503
2048	Miss rate: 50%  number of misses: 11267	Miss rate: 25%  number of misses: 222510	Miss rate: 68%  number of misses: 22506	Miss rate: 99%  Number of misses: 22504	Miss rate: 99%  number of misses: 22503
4096	Miss rate: 50%  number of misses: 11267	Miss rate: 25%  number of misses: 22510	Miss rate: 68%  number of misses: 22506	Miss rate: 84%  number of misses: 22504	Miss rate: 97%  number of misses: 22503



Expanding the cache size helps to decrease conflict and capacity misses. Similarly, increasing the block size can reduce compulsory misses by leveraging spatial locality, although it may lead to an increase in conflict misses.

Part B ( n = 150)

	Good hit Cache size: 2048 Block size: 4	Medium hit Cache size: 1024 Block size: 4	Poor hit Cache size: 128 Block size: 2
Fully associative (LRU)	Miss Rate: 68% # of misses: 22524	Miss Rate: 81% # of misses: 17613	Miss Rate: 95% # of misses: 22256
Fully associative (Random)	Miss Rate: 65% # of misses: 14704	Miss Rate: 73% # of misses: 14876	Miss Rate: 97% Number of misses: 22448
Direct Mapped	Miss Rate: 24% # of misses: 5634	Miss Rate: 77% # of misses: 15126	Miss Rate: 98% # of misses: 22512

**Part C (n = 150)**

N-way Set Associative Cache Set Size	Good hit Cache: 2048 Block size: 4	Medium hit Cache: 1024 Block size: 4	Poor hit Cache: 128 Block size: 2
<b>2</b>	Miss Rate: 59% # of misses: 17310	Miss Rate: 93% # of misses: 21409	Miss Rate: 99% # of misses: 22517
<b>4</b>	Miss Rate: 38% # of misses: 14110	Miss Rate: 92% # of misses: 22907	Miss Rate: 99% # of misses: 22517
<b>8</b>	Miss Rate: 24% # of misses: 11102	Miss Rate: 97% # of misses: 22741	Miss Rate: 99% # of misses: 22515
<b>16</b>	Miss Rate: 35% # of misses: 13782	Miss Rate: 98% # of misses: 22613	Miss Rate: 96% # of misses: 17815