

CS224

Lab No.:6

Section No.: 1

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Contents are in the below

QUESTION 1)

No.	Cache Size KB	N way cache	Word Size	Block size (no. of words)	No. of Sets	Tag Size in bits	Index Size (Set No.) in bits	Word Block Offset Size in bits	Byte Offset Size in bits	Block Replacement Policy Needed (Yes/No)
1	64	1	32 bits	4	2^{12}	16	12	2	2	NO
2	64	2	32 bits	4	2^{11}	17	11	2	2	YES
3	64	4	32 bits	8	2^9	18	9	3	2	YES
4	64	Full	32 bits	8	2^0	27	0	3	2	YES
9	128	1	16 bits	4	2^{14}	15	14	2	1	NO
10	128	2	16 bits	4	2^{13}	16	13	2	1	YES
11	128	4	16 bits	16	2^{10}	17	10	4	1	YES
12	128	Full	16 bits	16	2^0	27	0	4	1	YES

Question 2)

a)

Instruction	Iteration No.				
	1	2	3	4	5
lw \$t1, 0x4(\$0)	Compulsory	Hit	Hit	Hit	Hit
lw \$t2, 0xC(\$0)	Compulsory	Hit	Hit	Hit	Hit
lw \$t3, 0x8(\$0)	Hit	Hit	Hit	Hit	Hit

b)

V bit contains 1 bit.

Cache bit Capacity 8 words.

Block size is 2 words.

Tag bit contains 27 bits.

$$(1 + 27 + 32 + 32) * 4 = 368 \text{ bits.}$$

c)

1 AND is required for determining the hit signal.

1 COMPARATOR for determining whether tag is matching.

1 2:1 MUX for selecting the word.

Question 3)

a)

Instruction	Iteration No.				
	1	2	3	4	5
lw \$t1, 0x4(\$0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw \$t2, 0xC(\$0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw \$t3, 0x8(\$0)	Capacity	Capacity	Capacity	Capacity	Capacity

b)

Cache capacity is 2 words.

N is equal to 2.

Byte offset: 2

Data bits: 32

Set: 0

Block offset: 0

Tag = 30

1 for LRU

$$(1 + 30 + 32 + 1 + 32 + 30 + 1) = 127 \text{ bits}$$

c)

1 2:1 MUX determining the in the block

2 AND GATES for hit

1 OR GATE for hit

2 EQUALITY COMPARATOR for determining the tag match

QUESTION 4)

Tl1 = 1 clock cycle

Tl2 = 4 clock cycles

Main Memory = 40 clock cycles

AMAT = 2.2

Clock Rate 4GHZ = 0.25 ns

$10^3 * 2.2 * 0.25 = 550$ seconds