Bilkent University

EEE-202 Circuit Theory

Lab 5

Band-Pass Filter

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Section-3

Purpose:

The purpose of this lab is to design a band-pass filter with respect to the specifications in the Lab 5 document for 50 ohms resistor. The specifications can be seen in Figure 1.

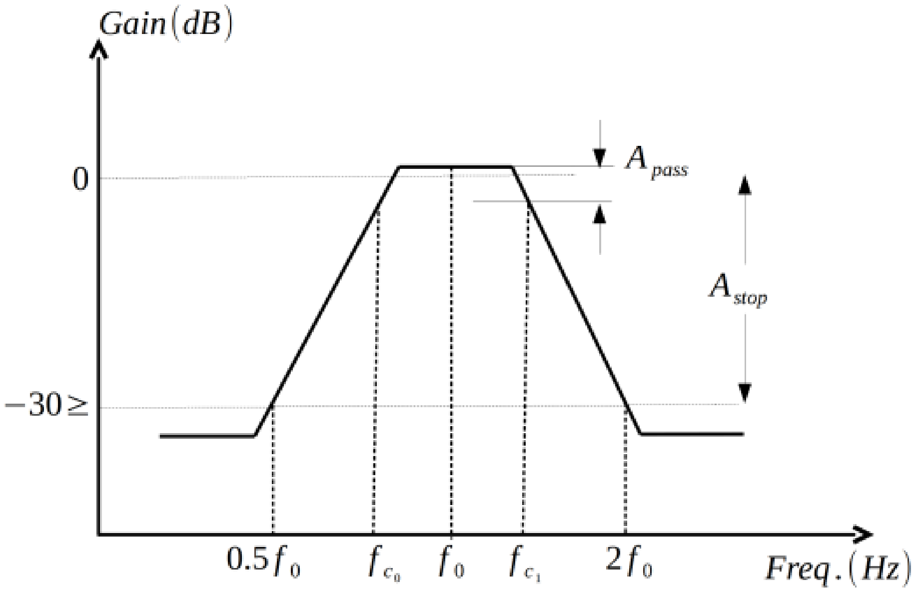

Figure 1: Frequency response of the filter

Central frequency: $2Mhz \leq f_0 \leq 5Mhz$
Passband width: $f_{c1} - f_{c0} = 0.05f_0$
Gain variation in the passband: $A_{pass} \leq 3dB$
Stopband attenuation: $A_{stop} \geq 30dB$

Figure 1: Band-Pass Filter Specifications

Let f_0 be 3MHz, then the passband width is $0.05 * f_0 = 150KHz$.

Let the input voltage be 2V peak value, 4V peak to peak.

Analysis:

In this part the reason of the selected circuit type, the components and the value of the components will be calculated and explained clearly. In order to complete the desired design, Butterworth filter is built. The minimum possible order of the butterworth filter is chosen to implement is easier in the hardware lab.

The minimum possible order is found with the below computations,

$$P_L = Load\ Power$$

$$P_A = Available\ Power$$

n = order of the circuit

$$\frac{P_L}{P_A} = \frac{1}{1 + \left(\frac{f_0}{\Delta f}\right)^{2n} * (\frac{f}{f_0} - \frac{f_0}{f})^{2n}}$$

Equation 1

By using Equation 1,

$$10\log\left(\frac{P_L}{P_A}\right) = 10log\left(\frac{1}{1+\left(\frac{f_0}{\Delta f}\right)^{2n} * \left(\frac{f}{f_0} - \frac{f_0}{f}\right)^{2n}}\right) \leq -30dB$$

Equation 2

When the values for the variables which are Since $\Delta f = fc1 - fc2 = 0.05\ f0\ and\ f_0$= 3MHz.

$$\log\left(\frac{1}{1+1+20^{2n}*(-\frac{3}{2})^{2n}}\right) = log\left(\frac{1}{1+(-30)^{2n}}\right) \leq -3dB$$

Equation 3

$$\log(1 + 30^{2n}) \geq 3dB\ then\ (1 + 30^{2n}) \geq 1000\ then\ 2n\ \geq 2.03$$

Equation 4

Since n ≥ 1.015, the minimum possible order of the desired circuit is second-order.

Figure 2 shows the general layout of a second-order Butterworth filter. Since the load resistance (R2) and source resistance (R1) in this instance are both 50Ω, the values of the inductor and capacitor must be ascertained.

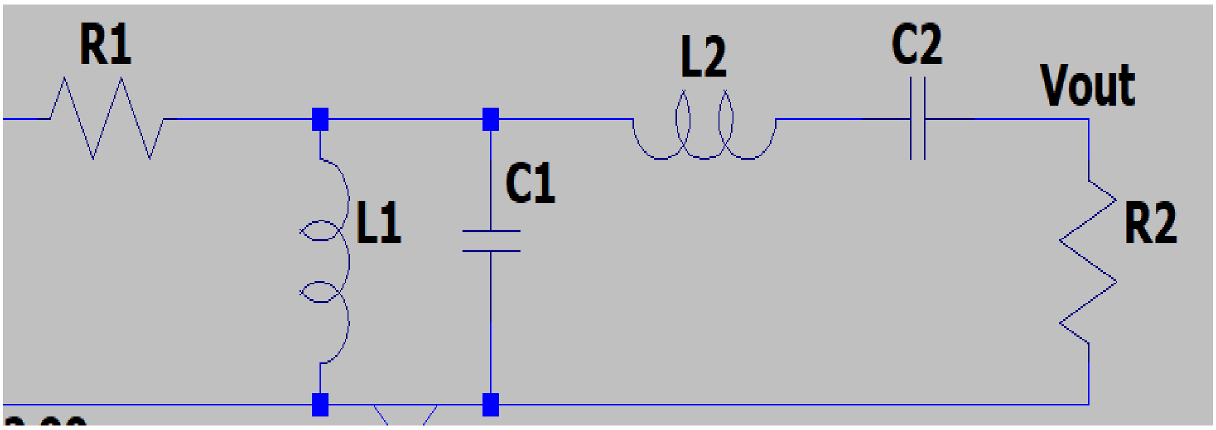

Figure 2: Overall Design of a Second-Order Butterworth filter

Let’s explain the process of designing a second-order Butterworth filter,

First Step: Create a second-order Butterworth low-pass filter with a cut-off frequency (-3dB) that is equivalent to the 150 kHz bandwidth of the BPF.

Second Step: f_0= 3MHz is the resonance frequency achieved by tuning the inductor with a series capacitor and the capacitor with a parallel inductor.

Low-pass butterworth filter can be seen in figure 3,

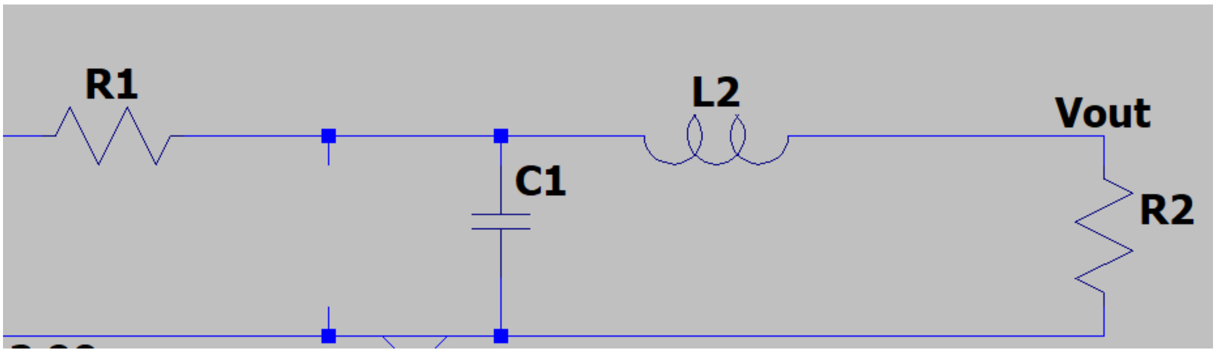

Figure 3: Overall Design of a Low-Pass Butterworth Filter

Table 1: Order Table of the Butterworth Filter

n	b_1	b_2	b_3	b_4	b_5	b_6	b_7	b_8
1	2.000							
2	1.4142	1.4142						
3	1.0000	2.0000	1.0000					
4	0.7654	1.8478	1.8478	0.7654				
5	0.6180	1.6180	2.0000	1.6180	0. 6180			
6	0.5176	1.4142	1.9319	1.9319	1.4142	0.5176		
7	0.4450	1.2470	1.8019	2.0000	1.8019	1.2470	0.4450	
8	0.3902	1.1111	1.6629	1.9616	1.9616	1.6629	1.1111	0.3902

The order is chosen as 2 therefore,

$$b_1 = C_1 = 1.4142$$

$$b_2 = L_2 = 1.4142$$

Since R = 50 ohms,

$$C_1 = \frac{1.4142}{2\pi * 150 \text{ kHz} * 50} = 30 \text{ pF}$$

Equation 5

$$L_2 = \frac{1.4142 * 50}{2\pi * 150 \text{ kHz}} = 75uH$$

Equation 6

In Figure 4, the Low-Pass Butterworth filter with the specific component values is visible.

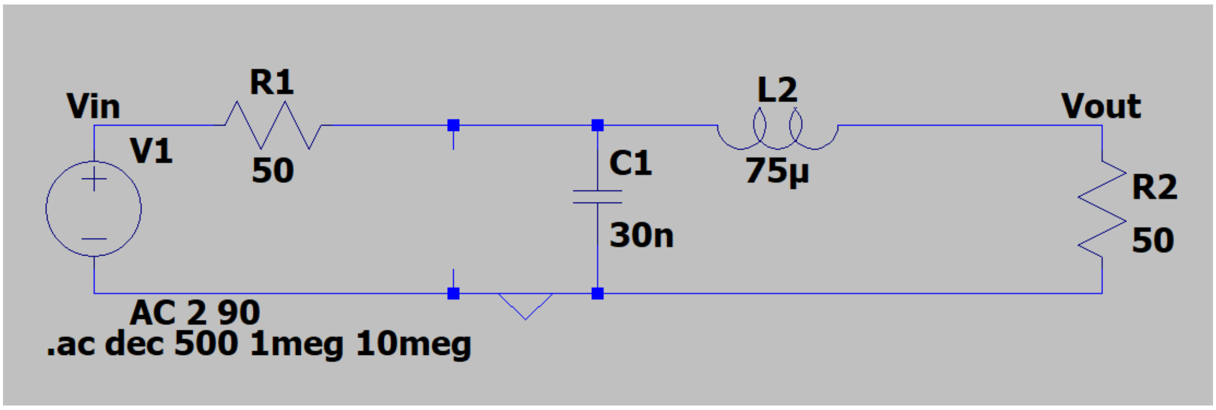

Figure 4: Butterworth Low-Pass Filter with the Specific Component Values

After achieving the Low-Pass Butterworth filter, we are done with the first step of completing the Butterworth filter. The inductor and capacitor must be tuned to achieve resonance at the center frequency of 3 MHz in the second stage. To do this, a parallel inductor L_1 will be connected near the capacitor C_1, and a series capacitor C_2 will be connected near the inductor L_2. This way L_1 will tune C_1 and C2 will tune L_2. Afterwards we will be done with completing the whole butterworth filter.

With using the formulas and knowing w = 2*pi*3MHz ,

$$L_1 = \frac{1}{w^2 * C_1}$$

Equation 7

$$C_2 = \frac{1}{w^2 * L_2}$$

Equation 8

C_2 and L_1 are found as,

$$L_1 = 94nH$$

$$C_2 = 37.7pF$$

After founding the values of C_2 and L_1, we are done with butterworth filter. The gain of the butterworth filter can be found by Equation 9,

$$A = 20 * \log\left(\frac{Voutput}{Vinput}\right)$$

Equation 9

Simulations:

Final circuit is seen in Figure 5,

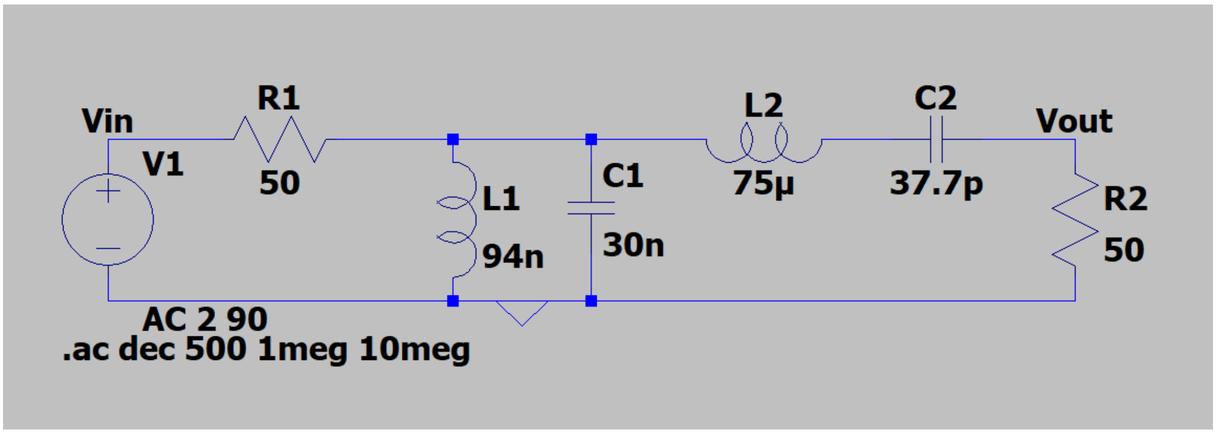

Figure 5: Final Butterworth Filter

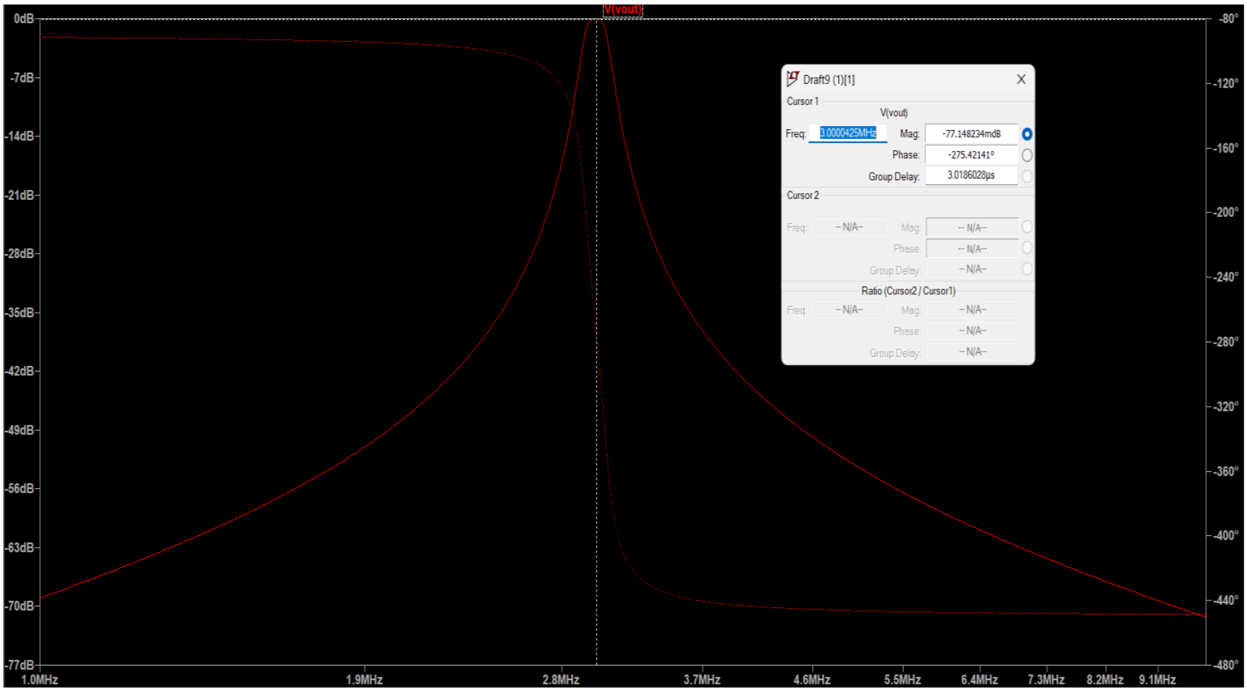

Figure 6: Central Frequency of the Band-Pass Filter, $f_0 = 3.000043\text{MHz}$

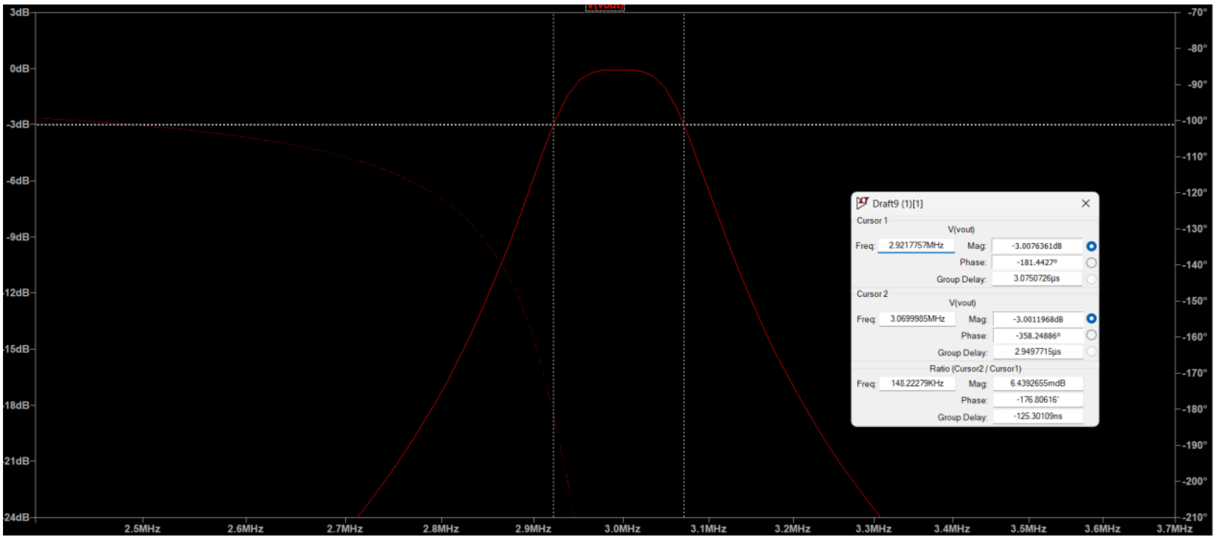

Figure 7: Cut-Off Frequency Points, $f_{c0} = 2.92MHz$, $f_{c1} = 3.07MHz$

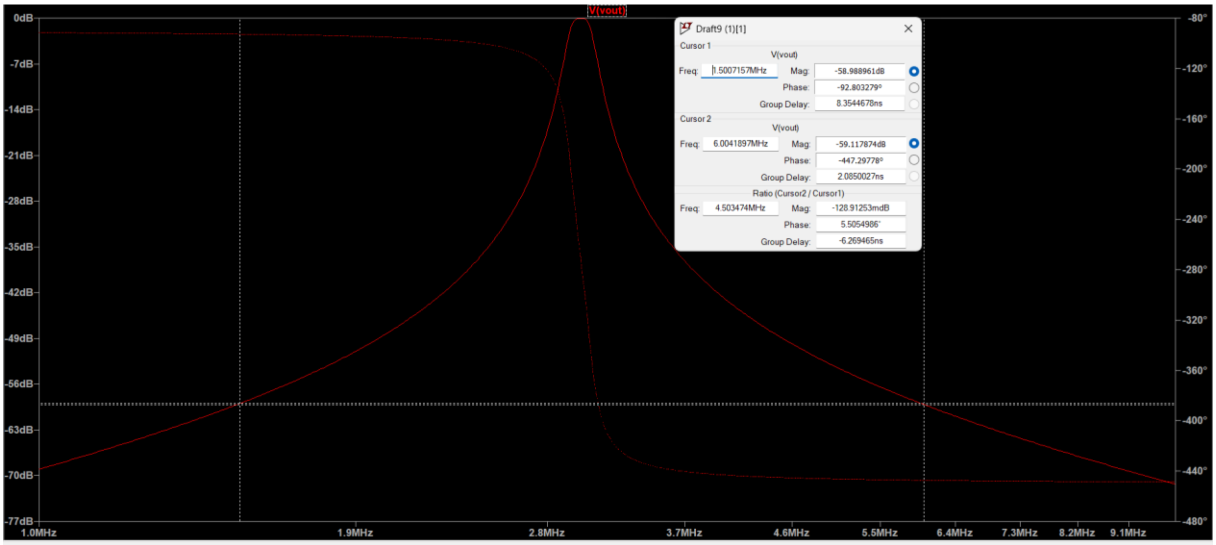

Figure 8: Frequency Responses of the Points $\frac{f_0}{2}$ and $2 * f_0$

Table 2: Frequency and Gain Values Learned from the LTSpice Simulation

	f_0	$f_{0/2}$	$2f_0$	f_{c0}	f_{c1}
Gain	-77.148mdB	-58.989dB	-59.117dB	-3.0076dB	-3.01dB
Frequency	3.000043MHz	1.5007MHz	6.004MHz	2.921MHz	3.069MHz

Table 3: Theory and Simulation Comparison Table

	Simulation Result	Theory Result	Check
Central Frequency (MHz)	3.000043	3	Satisfactory
Pass-Band Width (kHz)	148	150	Satisfactory error = %1.3
Gain at f_{c0}	≤3dB	2.921	Satisfactory
Gain at f_{c1}	≤3dB	3.069	Satisfactory error = %2.3

Hardware Lab:

In Figure 9, the hardware circuit is shown:

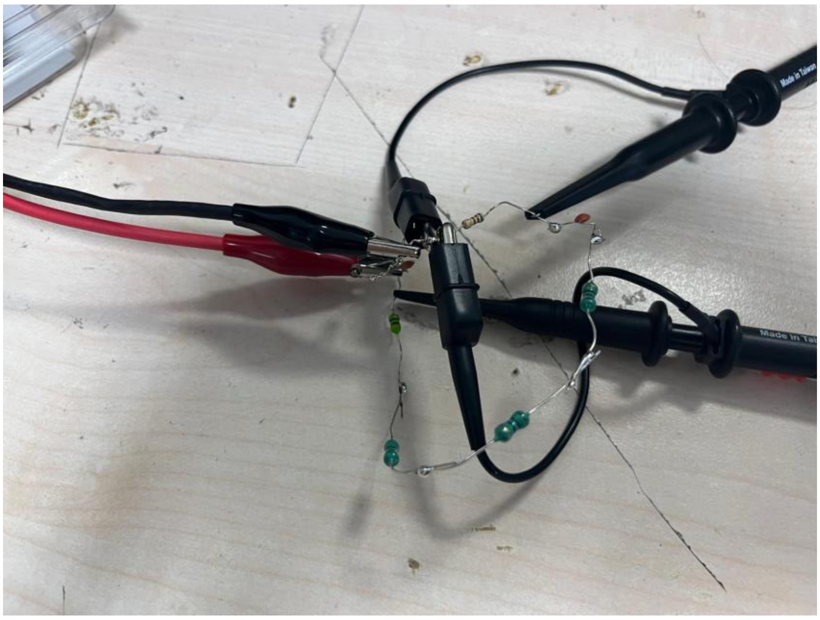

Figure 9: The Hardware Circuit

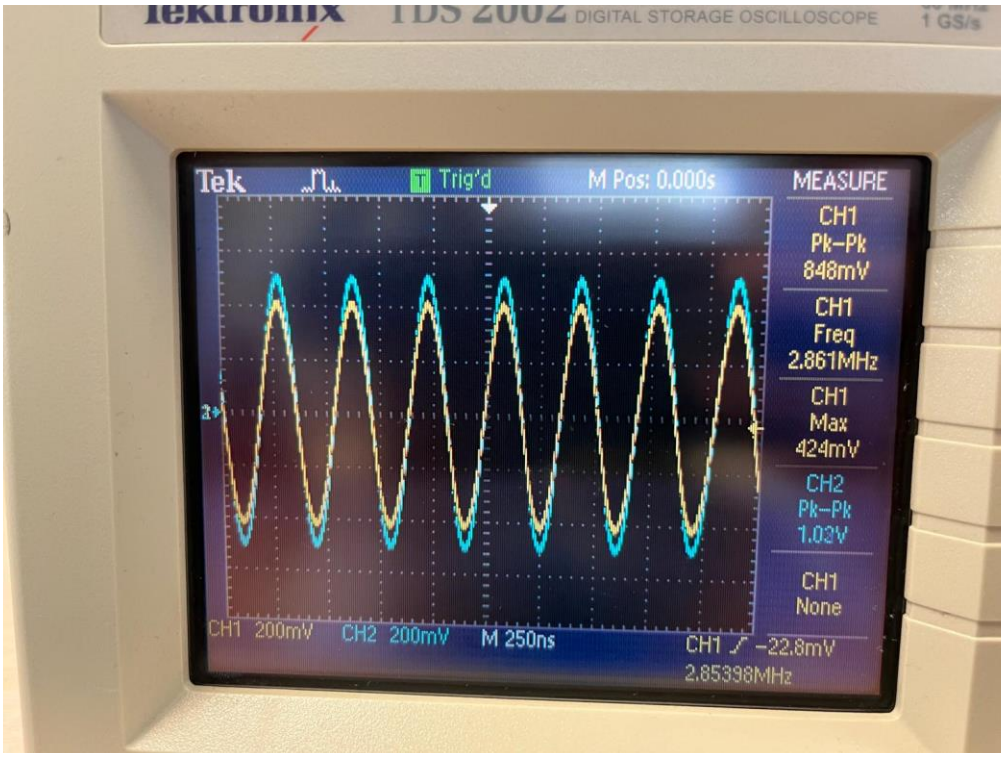

Figure 10: Central Frequency = 2.8539 MHz, Vin=1.02V pk-pk, Vout=848 mV

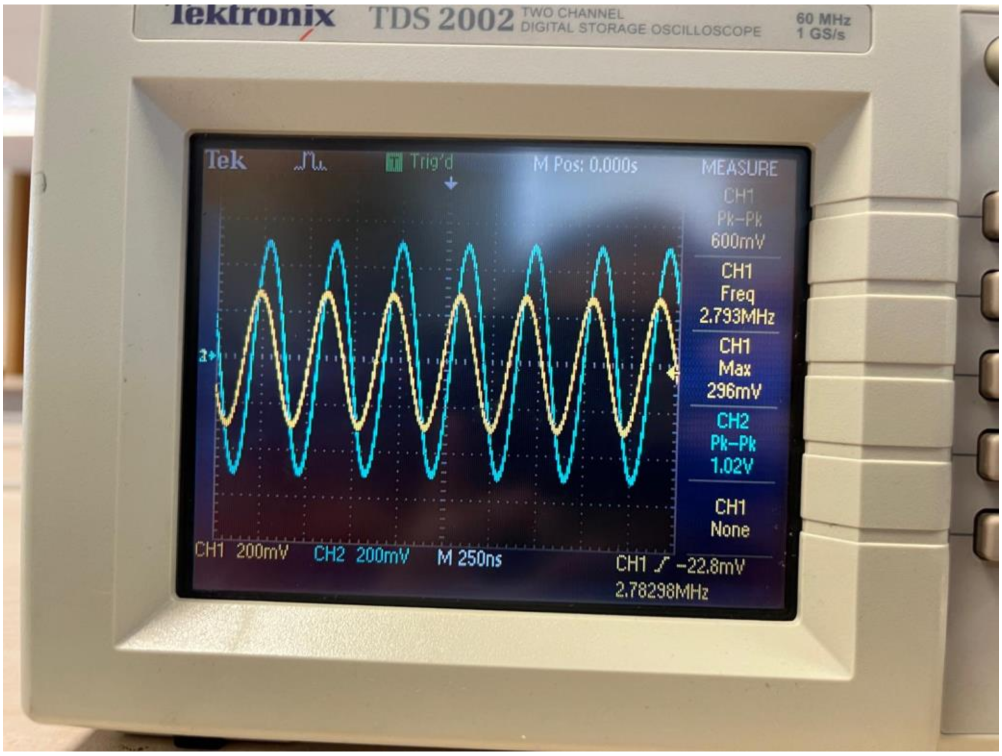

Figure 11: At $f_{c0} = 2.783MHz$, Vin= 1.02V pk-pk, Vout = 600mV peak to peak

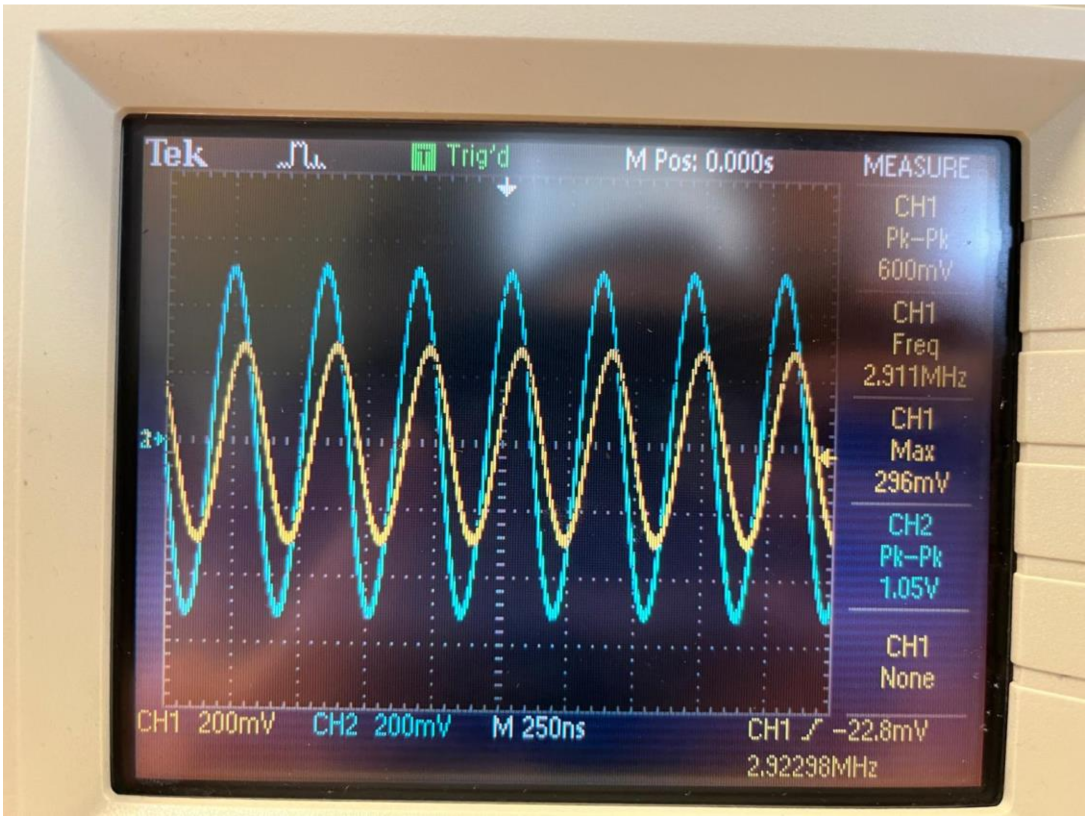

Figure 12: At $f_{c1} = 2.923MHz$, Vin = 1.05 V pk-pk , Vout = 600mV pk-pk

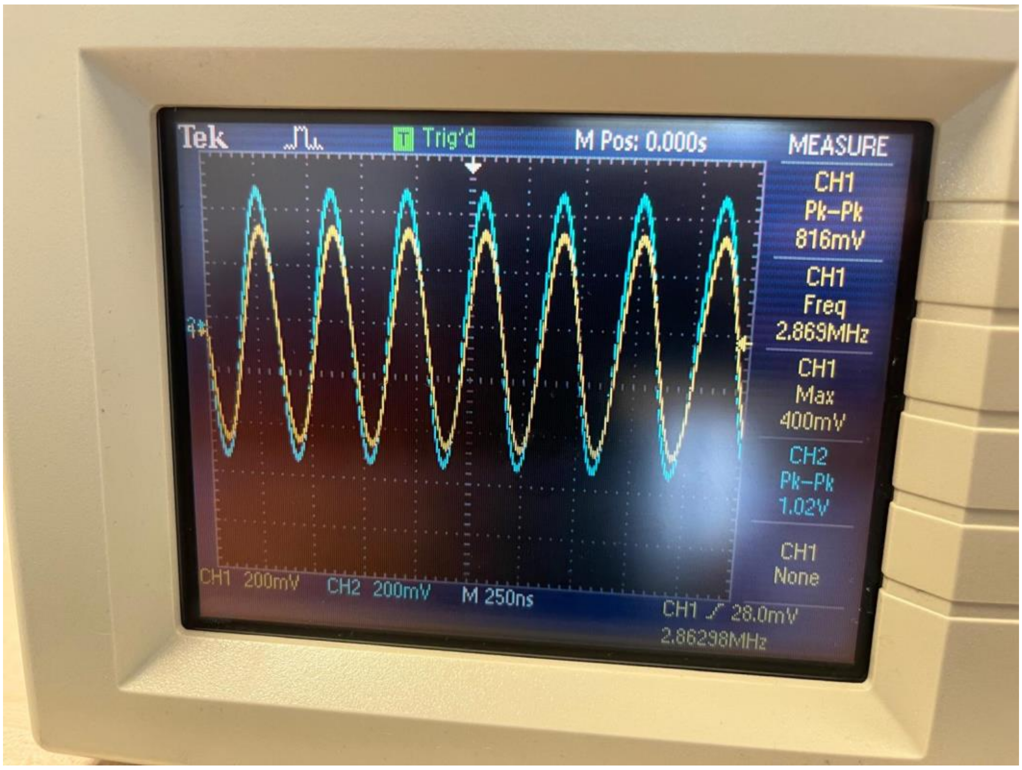

Figure 13: At f = 2.8629MHz, Vin = 1.02V pk-pk, Vout= 816mV pk-pk

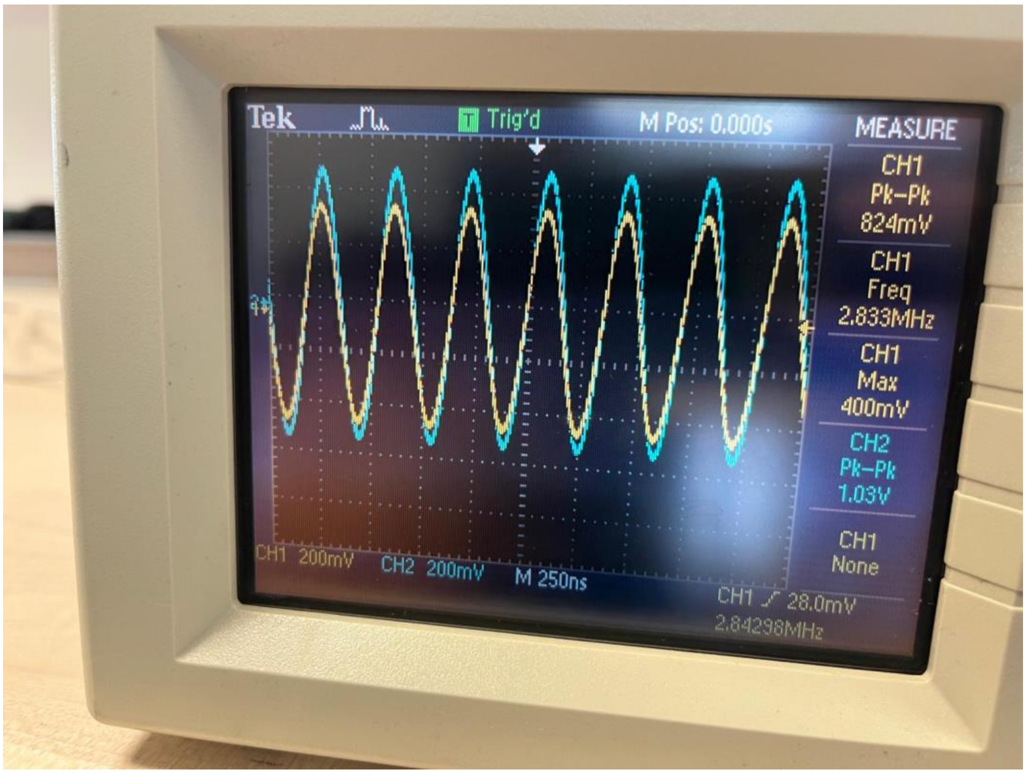

Figure 14: At f = 2.8429MHz, Vin = 1.03V pk-pk, Vout= 824mV pk-pk

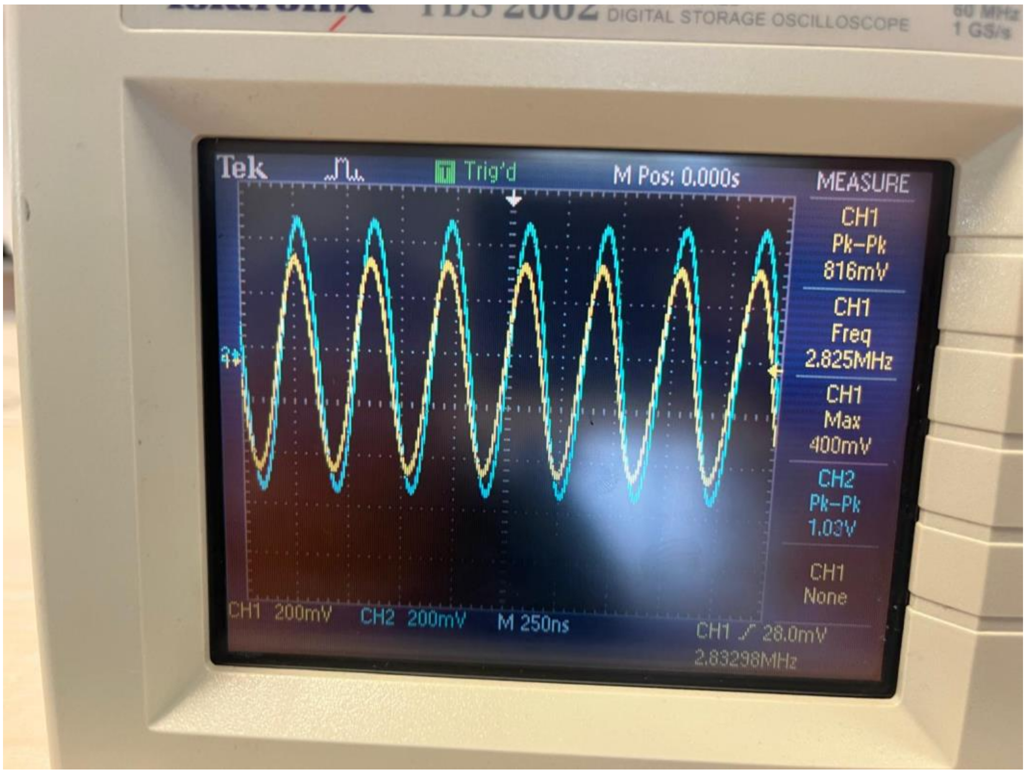

Figure 15: At 2.8329MHz , Vin= 1.02V pk-pk, Vout=816mV pk-pk

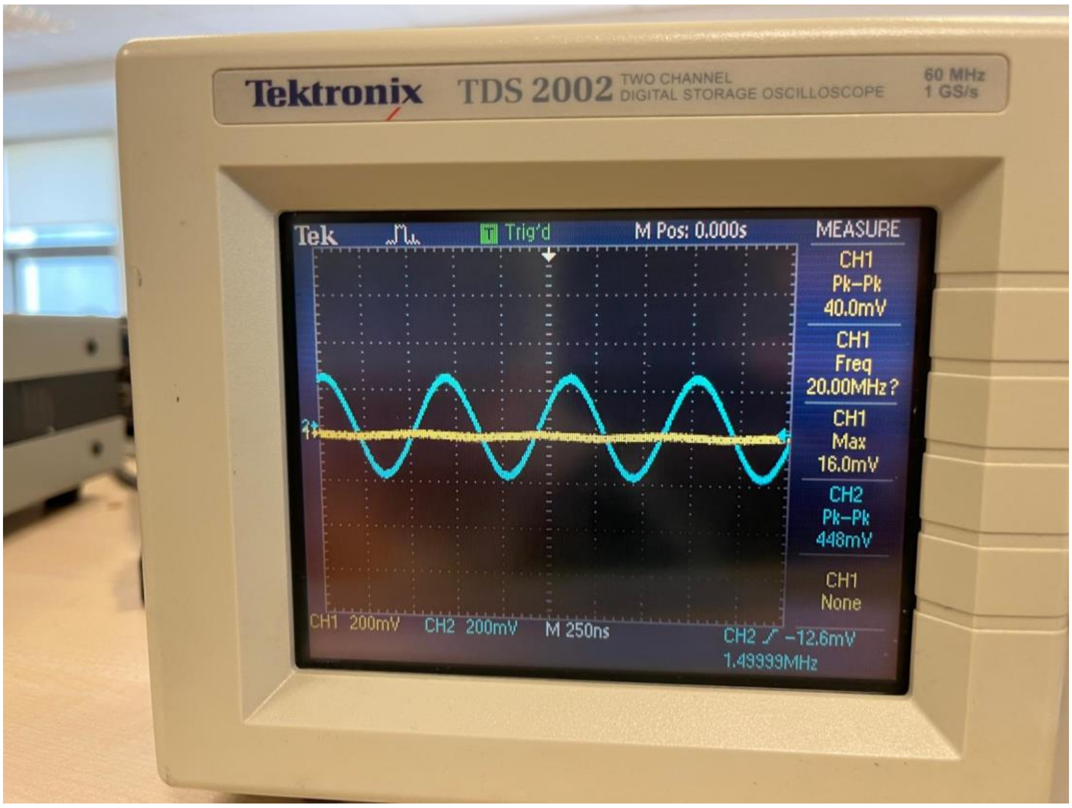

Figure 16: At $\frac{f0}{2}$= 1.5MHz, Vin=436mV pk-pk, Vout= 40mV pk-pk

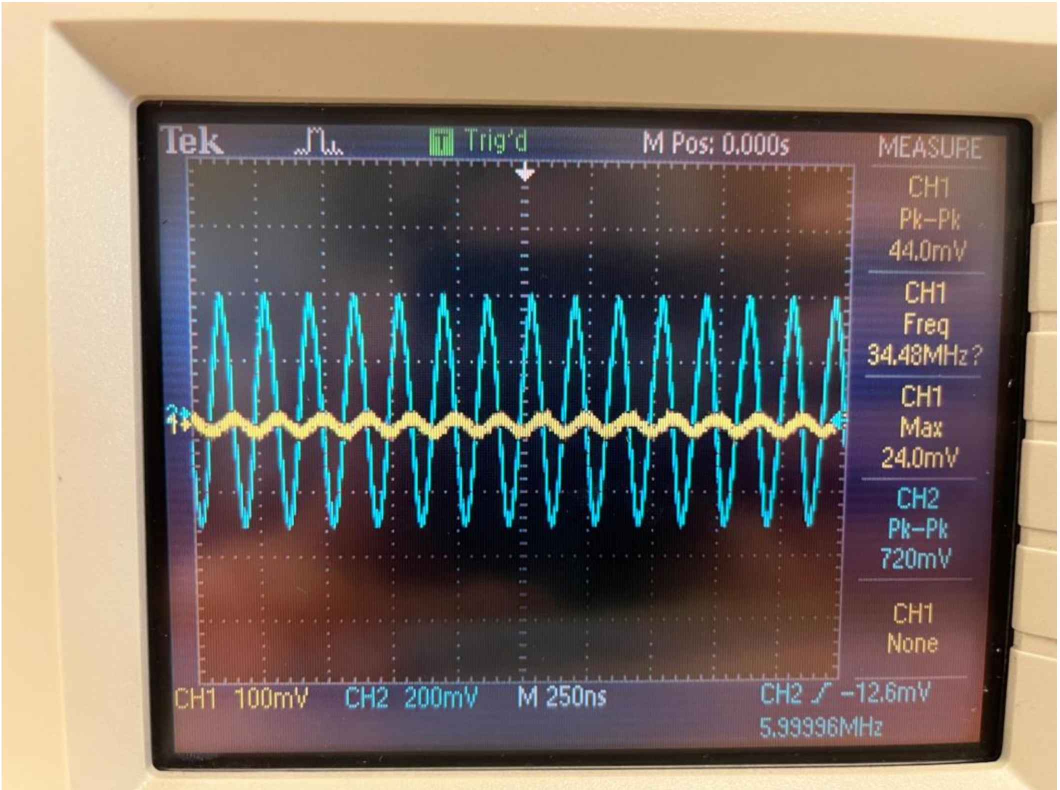

Figure 17: At 2*f0 = 6 MHz, Vin=720mV pk-pk, Vout= 44mV pk-pk

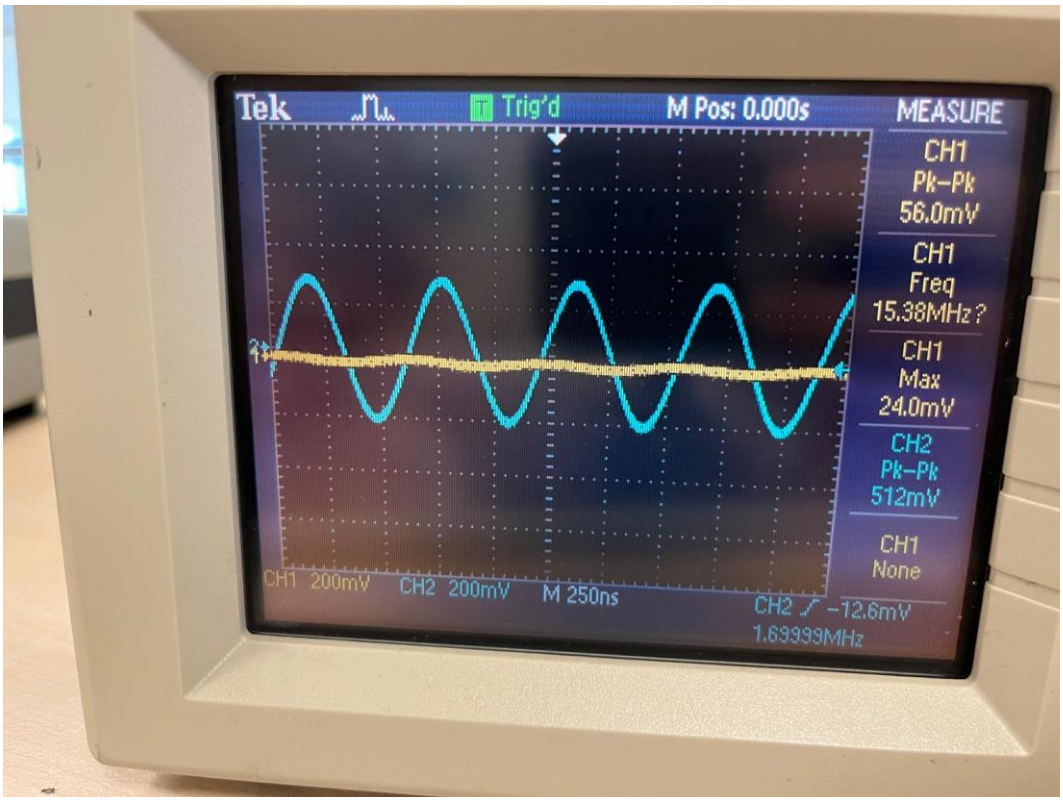

Figure 18: At f = 1.7 MHz, Vin=512mV pk-pk, Vout= 56 mV pk-pk

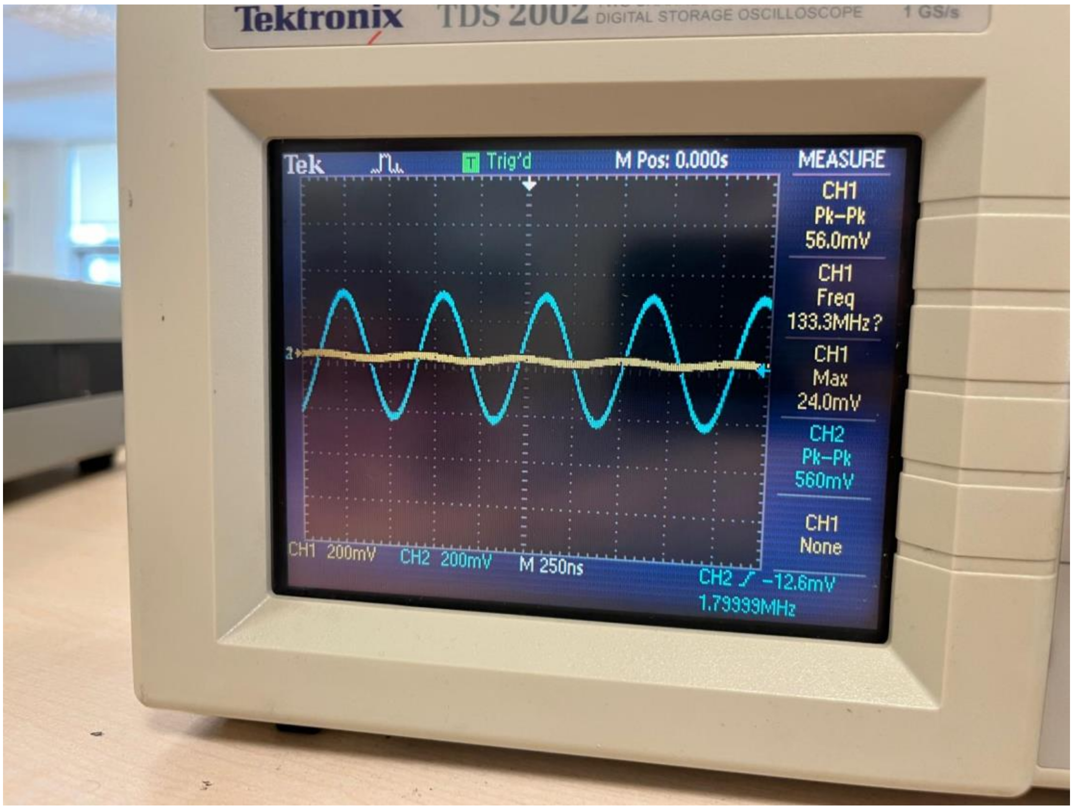

Figure 19: At f = 1.8 MHz, Vin=560mV pk-pk, Vout= 56 mV pk-pk

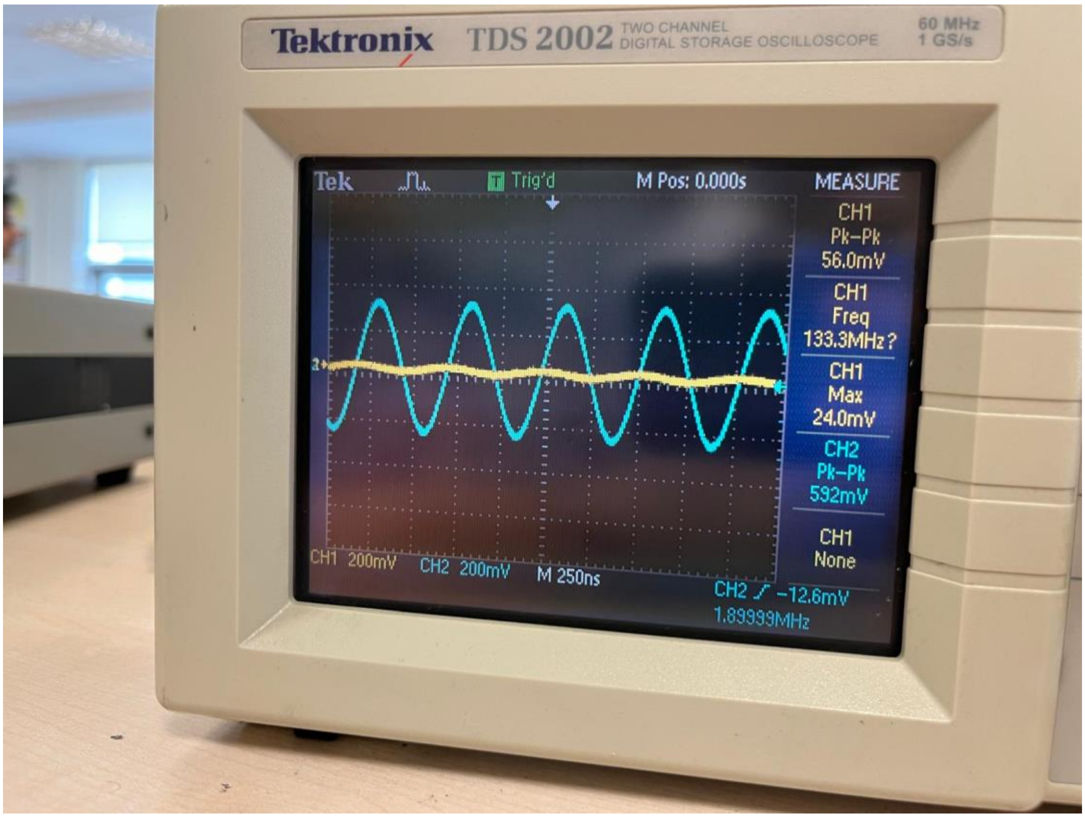

Figure 20: At f = 1.9 MHz, Vin=592mV pk-pk, Vout= 56 mV pk-pk

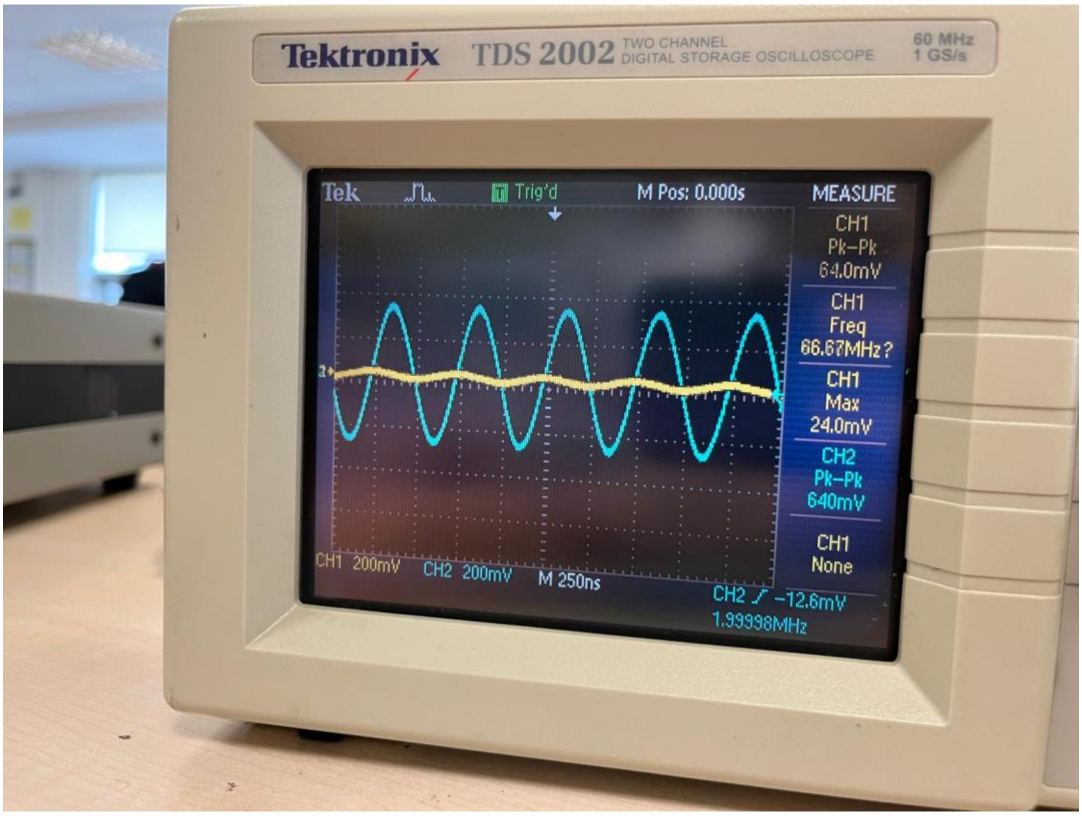

Figure 21: At f = 2.0 MHz, Vin=640 mV pk-pk, Vout= 64 mV pk-pk

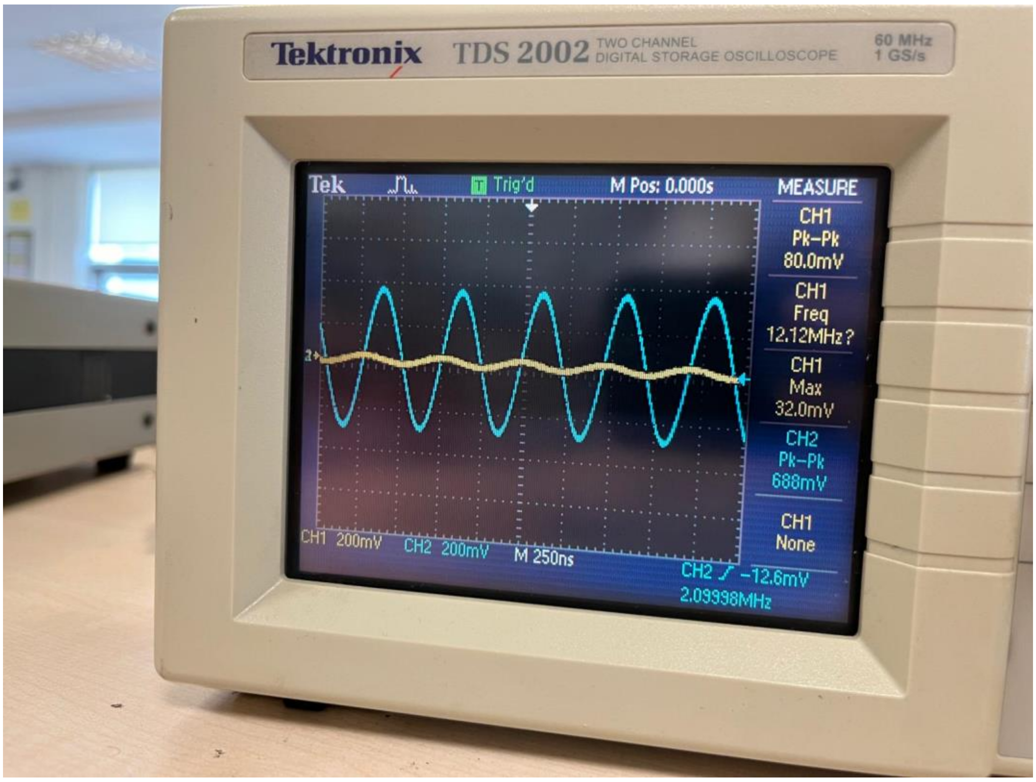

Figure 22: At f = 2.1 MHz, Vin=688 mV pk-pk, Vout= 80 mV pk-pk

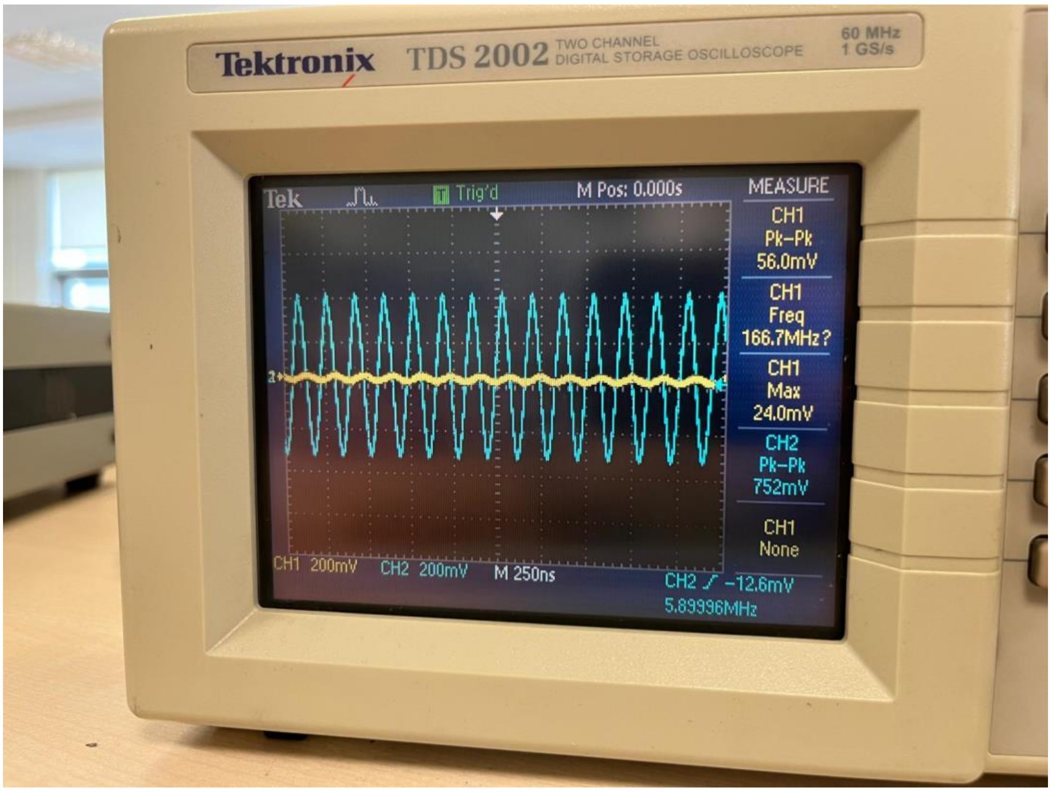

Figure 23: At f = 5.9 MHz, Vin=752 mV pk-pk, Vout= 56 mV pk-pk

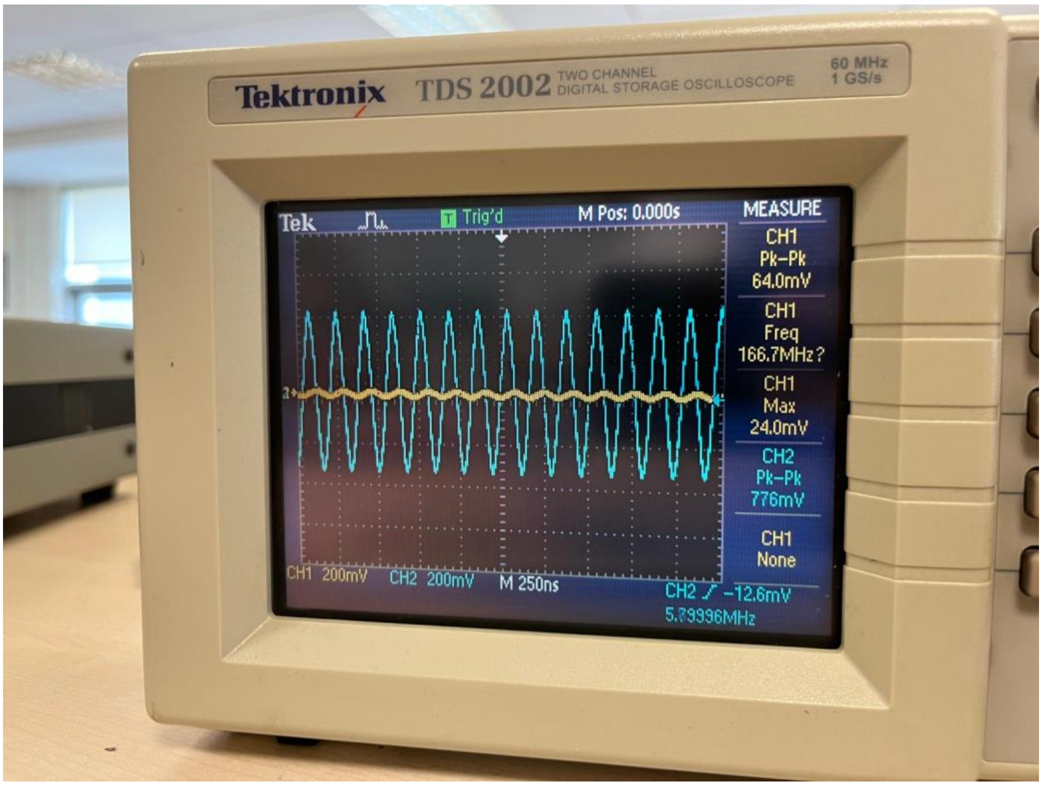

Figure 24: At f = 5.8 MHz, Vin=776 mV pk-pk, Vout= 64 mV pk-pk

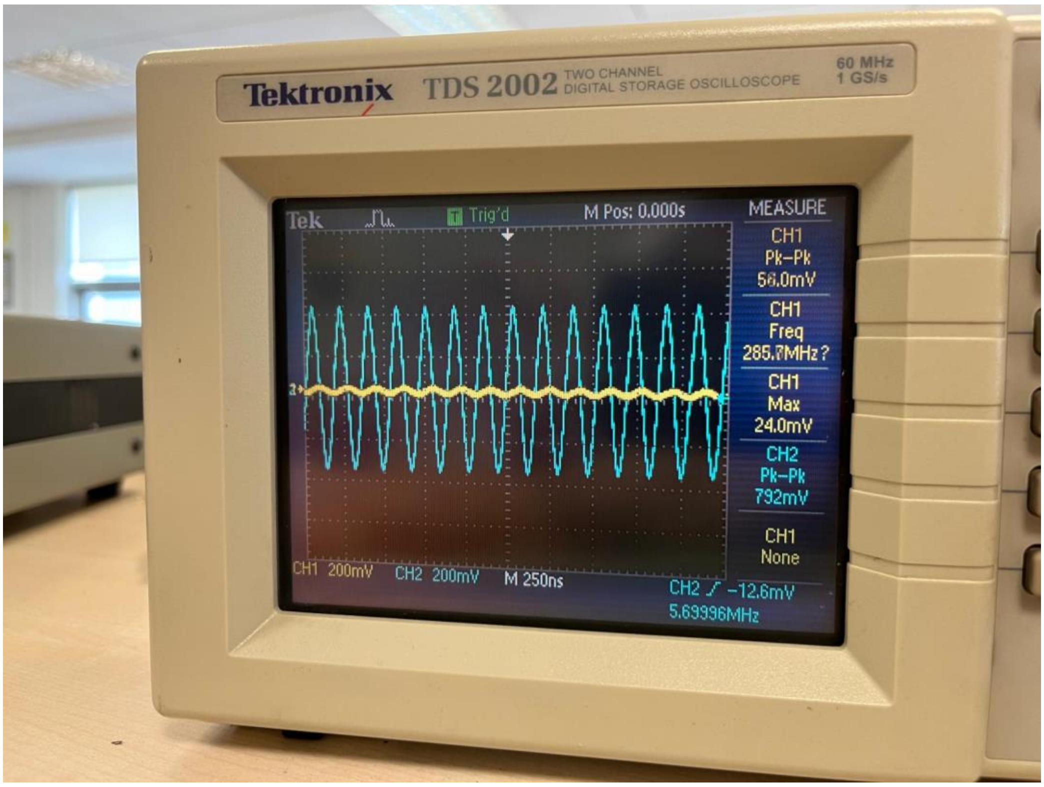

Figure 25: At f = 5.7 MHz, Vin=792 mV pk-pk, Vout= 56 mV pk-pk

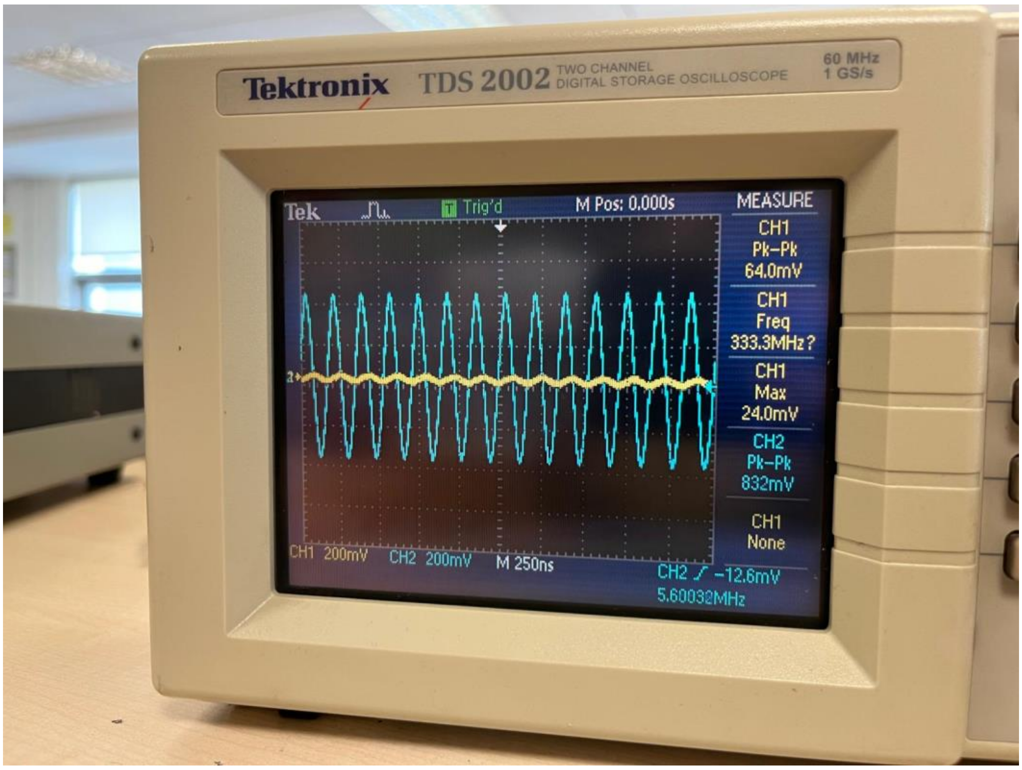

Figure 26: At f = 5.6 MHz, Vin=832 mV pk-pk, Vout= 64 mV pk-pk

Table 4: Frequency and Gain Table of Hardware Results

Band Type	Frequency (Mhz)	Gain (dB)
Stop-Band	1.5	-20.74
Stop-Band	1.7	-19.21
Stop-Band	1.8	-20.00
Stop-Band	1.9	-20.48
Stop-Band	2.0	-20.00
Stop-Band	2.1	-18.60
Pass-Band	2.783 (f_{c0})	-4.60
Pass-Band	2.82	-2.10
Pass-Band	2.8539 (f_0)	-1.60
Pass-Band	2.88	-2.43
Pass-Band	2.923 (f_{c1})	-4.86
Stop-Band	5.6	-22.28
Stop-Band	5.7	-23.00
Stop-Band	5.8	21.67
Stop-Band	5.9	-22.56
Stop-Band	6.0	-24.30

Table 5: Theory and Hardware Result Comparison Table

	Theory Result	Hardware Result	Check
Central Frequency f_0 (MHz)	3	2.783	Satisfactory Error = %7.23
Passband Width (kHz)	150	140	Satisfactory Error = %6.6
Gain at f_{c0}	≤-30dB	-4.60 dB	Satisfactory
Gain at f_{c1}	≤-30dB	-4.86 dB	Satisfactory

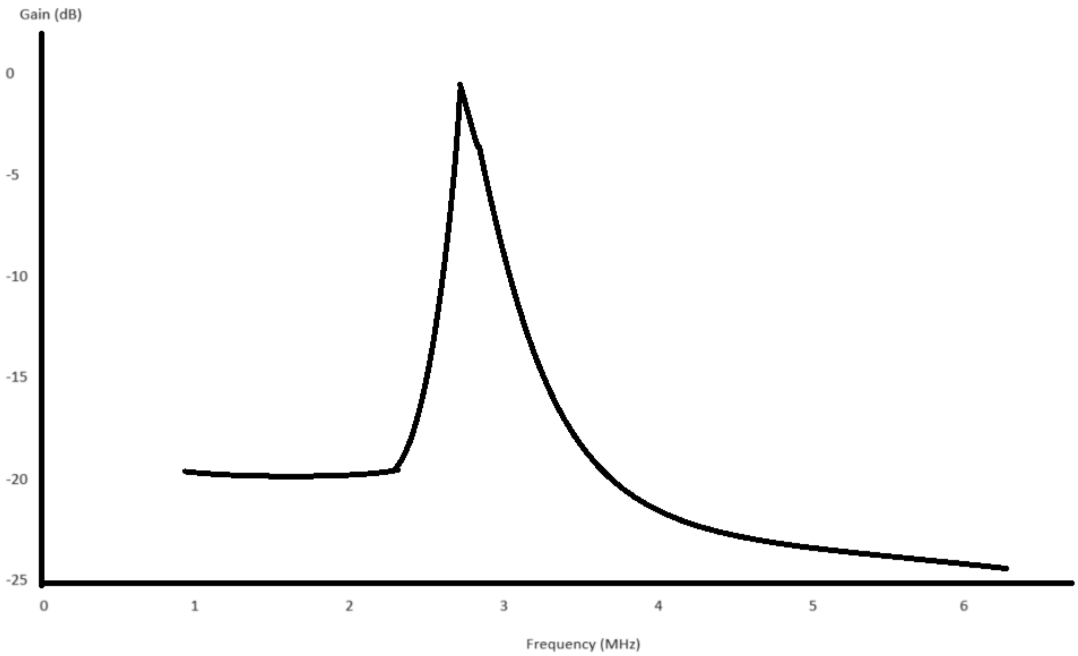

Figure 27: Gain and Frequency Plot of the Hardware Results

Conclusion:

Given that every requirement was met, the band-pass filter's software findings were encouraging. As anticipated, the central frequency was 3MHz, and the bandwidth was achieved as 148kHz with a small error %1.3. However, 2.783 MHz was the central frequency in the hardware lab where the largest gain was achieved. Since the inductances and capacitances were measured using series and parallel component combinations, it's possible that their precise values were not obtained, leading to the %7.23 error in the center frequency. Additionally, the lab's components contain internal resistances and tolerance levels. In order to determine the cut-off frequencies, the frequency was varied in order to seek for the -4.60dB value, which is 3dB less than the maximum gain, as opposed to the -3dB value.They were discovered to be 2.783 MHz and 2.923MHz. Therefore, the bandwidth was obtained with %6.6. The hardware met the remaining requirements as well. To sum up, this lab showed how to design a band-pass filter using both hardware and software. Because band-pass filters are essential circuits in electrical engineering, this lab helped me understand the idea in general.