Bilkent University

Electrical and Electronics Department

EE202-01 Lab 1 Report:

"Time-Domain and Frequency-Domain Analyses in LTSpice"

22/02/2024

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SOFTWARE LAB

Part 1: Transient (time-domain) Analysis

Part 1.1:

Introduction:

In Part 1.1, the purpose is to show that when R1, R2 and input voltage (Vin) values are in desired range, showing the output voltage which is the voltage of R2 in LTSpice and checking if it is correct by using voltage divider formula.

Analysis:

The requaried voltage divider formula is showed in Equation 1:

$$V_o = V_{in} * \frac{R_2}{R_1 + R_2}$$

Equation 1

To achieve the purpose, firstly the design of the circuit is done on LTSpice and run it. Then the voltage of V1 which is the input voltage and voltage of R2 which is the output voltage are seen on the graph and checked if they are correct. When the desired value for input voltage was 8V, 8 ohms for R1 and 15 ohms for R2, the mathematical result of Equation 1 is:

$$V_o = V_{in} * \frac{R_2}{R_1+R_2} = 8V * \frac{15}{8+15} = 5.217\text{V}$$

Simulation:

Here is the circuit design of Part 1.1:

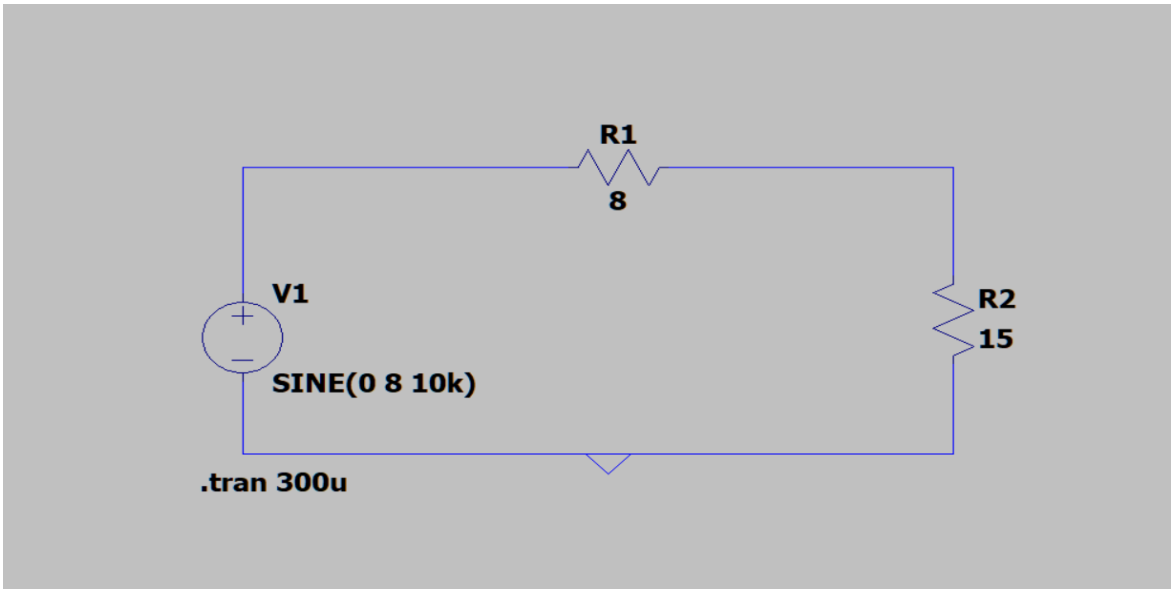

Figure1: A Simple Voltage Divider

Here is the graph of V1 which is the input voltage and output voltage which is the voltage of R2:

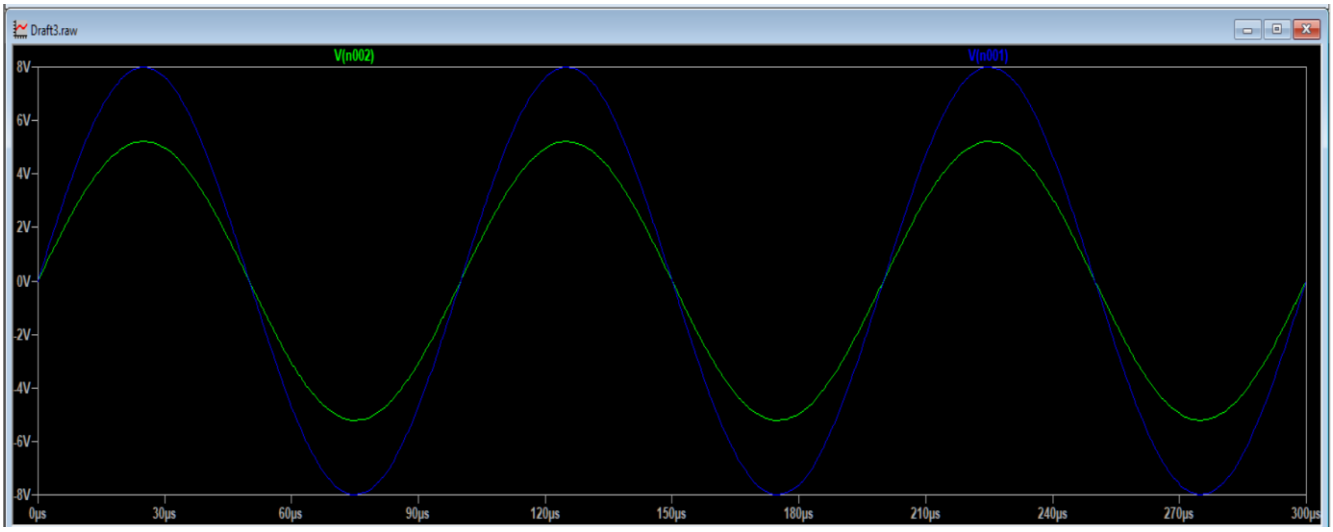

Figure 2: The Graph of V1(Vn001) and Voltage of R2(Vn002)

Here is the graph of output voltage of its maximum:

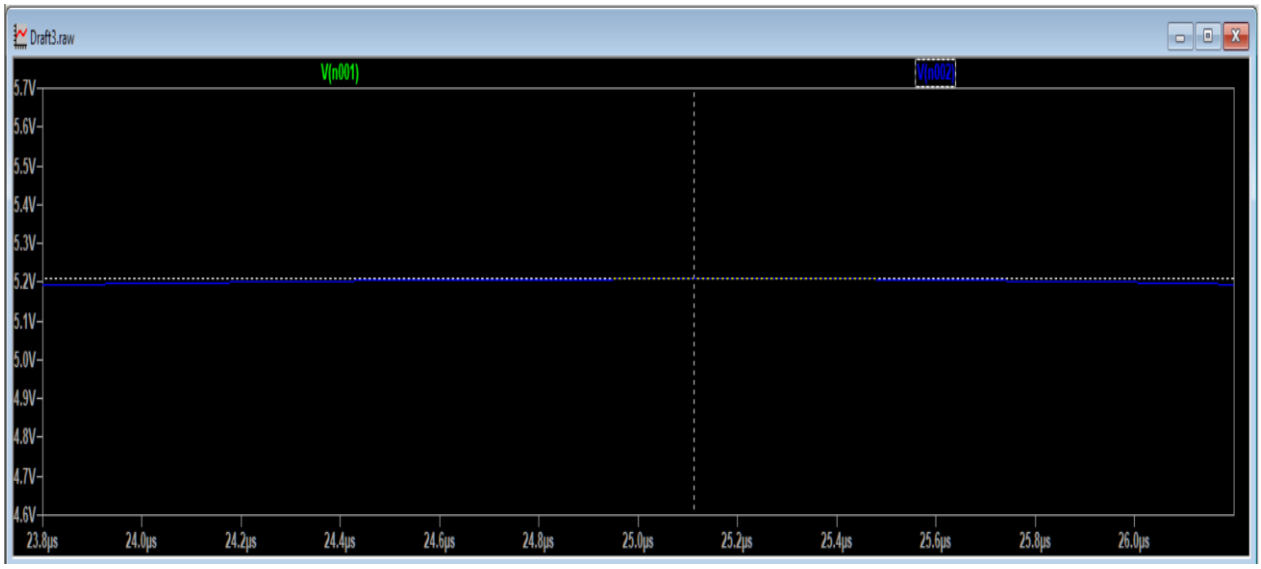

Figure 3: The Graph of output voltage at its maximum

The simulation result satisfies the mathematical result since the peak value for Vo is equal to 5.217 V and simulation result for peak value is nearly 5.2 V.

Part 1.2:

Introduction:

The purpose of Part 1.2 is to design an RL circuit by changing R2 with L1, and observing how the output voltage (Voltage of L1) changes by increasing the frequency and finding what kind of filter it is.

Analysis:

To achive the purpose, firstly the design of the circuit is done on LTSpice and run it. Then the voltage of V1 which is the input voltage and voltage of L1 which is the output voltage are seen on the graph then the frequency is increased and the process

is repeated. Equation 2 shows the mathematical equation which is supposed to be used for the mathematical value of output voltage.

$$V_o = V_{in} * \frac{jwl}{R + jwl} = V_{in} * \frac{1}{\frac{R_1}{jwl} + 1} \text{ when } w \to \infty, V_o \to V_{in}$$

Equation 2

Simulation:

Here is the design of circuit when frequency is 10kHz:

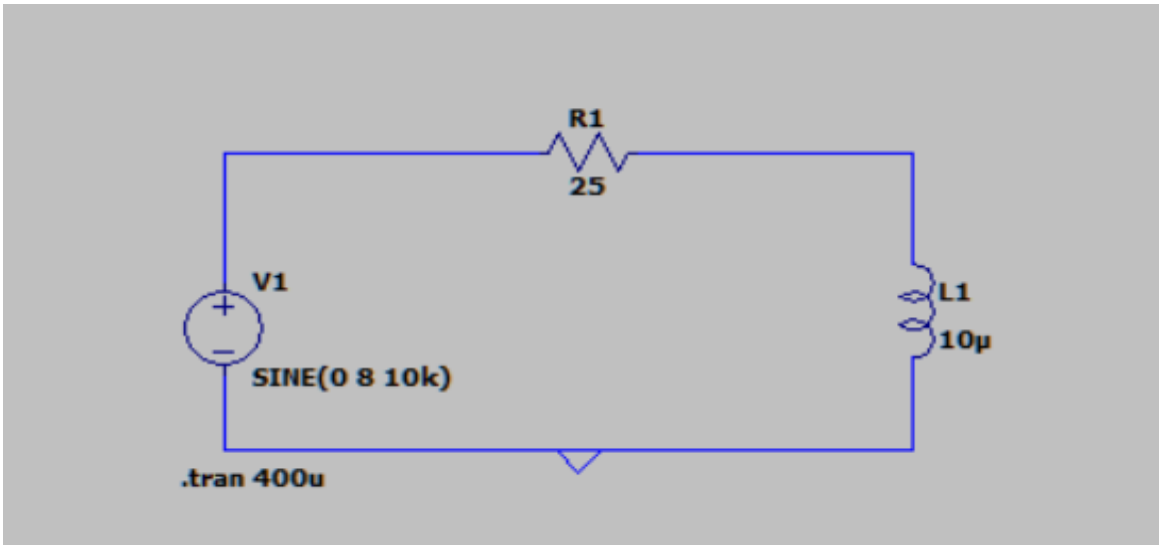

Figure 4: Design of RL circuit when frequency is 10kHz

Figure 5 shows the voltage graph of input voltage (Vn001) and output voltage (Vn002) when frequency is 10kHz:

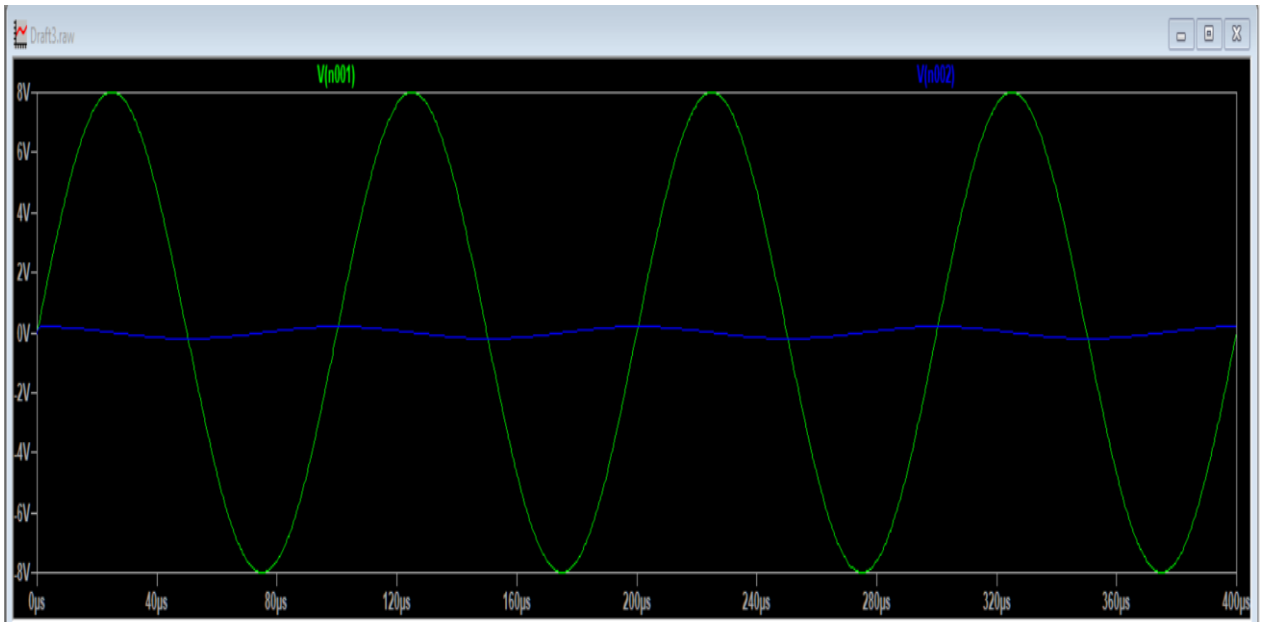

Figure 5: Voltage graph of RL curcuit when frequency is 10kHz

The top value for the output voltage is 200.98 mV when frequency is 10kHz.

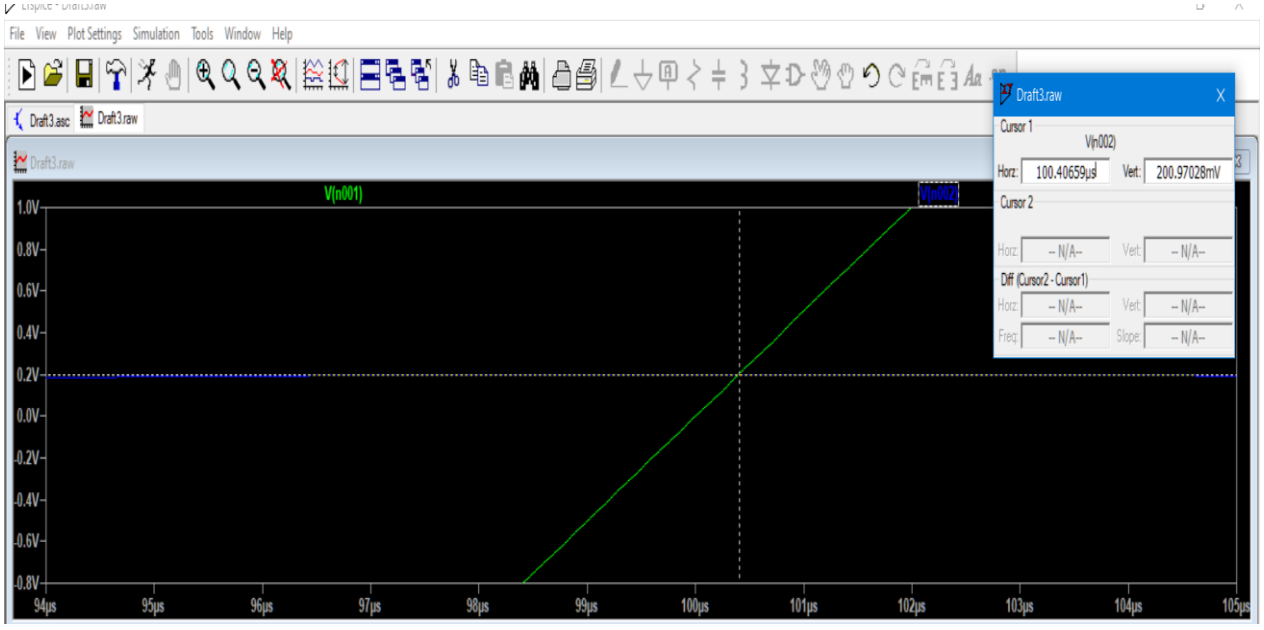

Figure 6: The maximum of output voltage

Figure 7 shows the circuit design and the graph of input and output voltage when frequency is 100kHz. As shown in the figure ,the value of output voltage is higher than the time when the frequency was 10kHz :

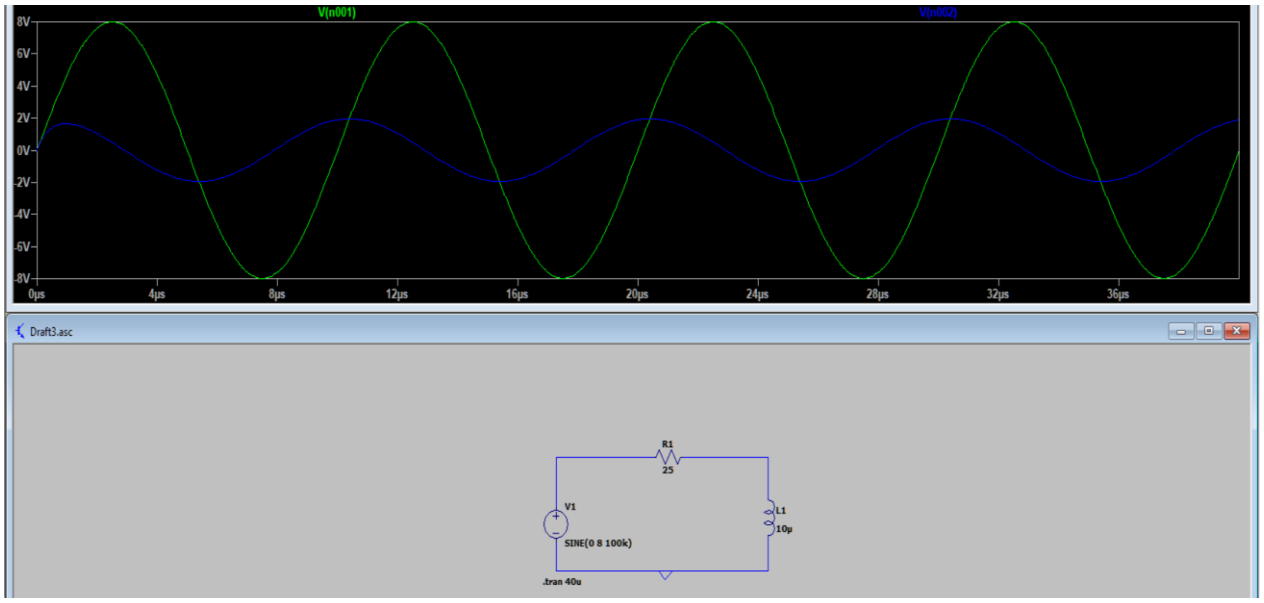

Figure 7: Voltage graph and circuit design when frequency is 100kHz

Here is the maximum value of output voltage which is about 1.95 Volts.

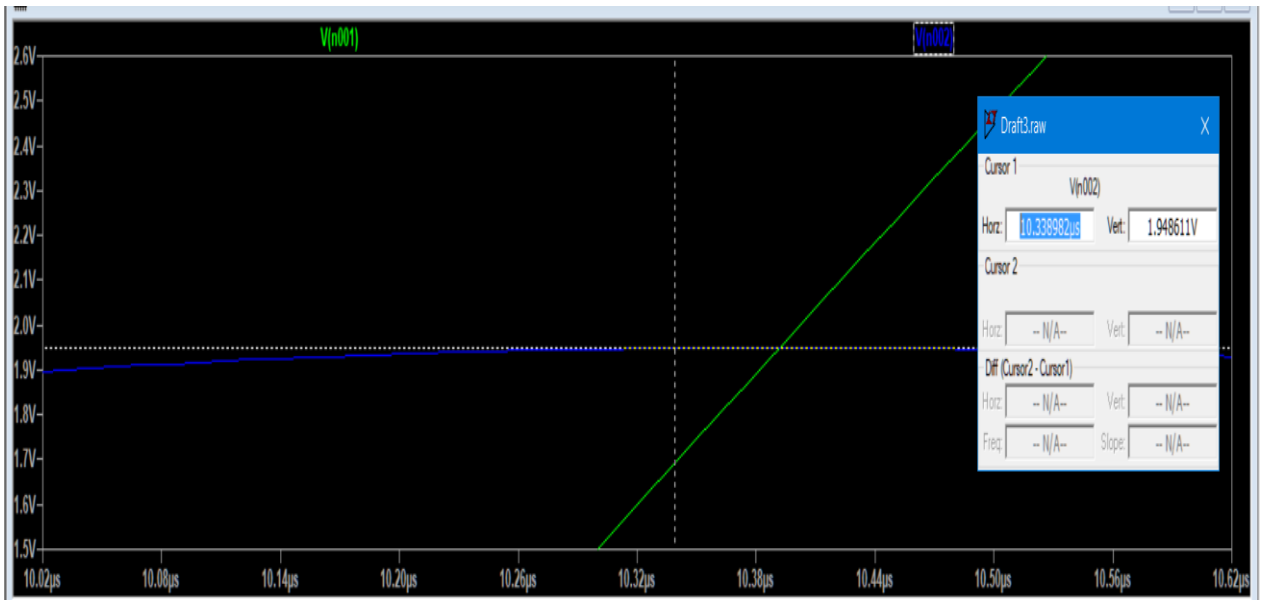

Figure 8: Voltage graph of output voltage (Vn002)

Here is the circuit design and the voltage graph when frequency is 500kHz.

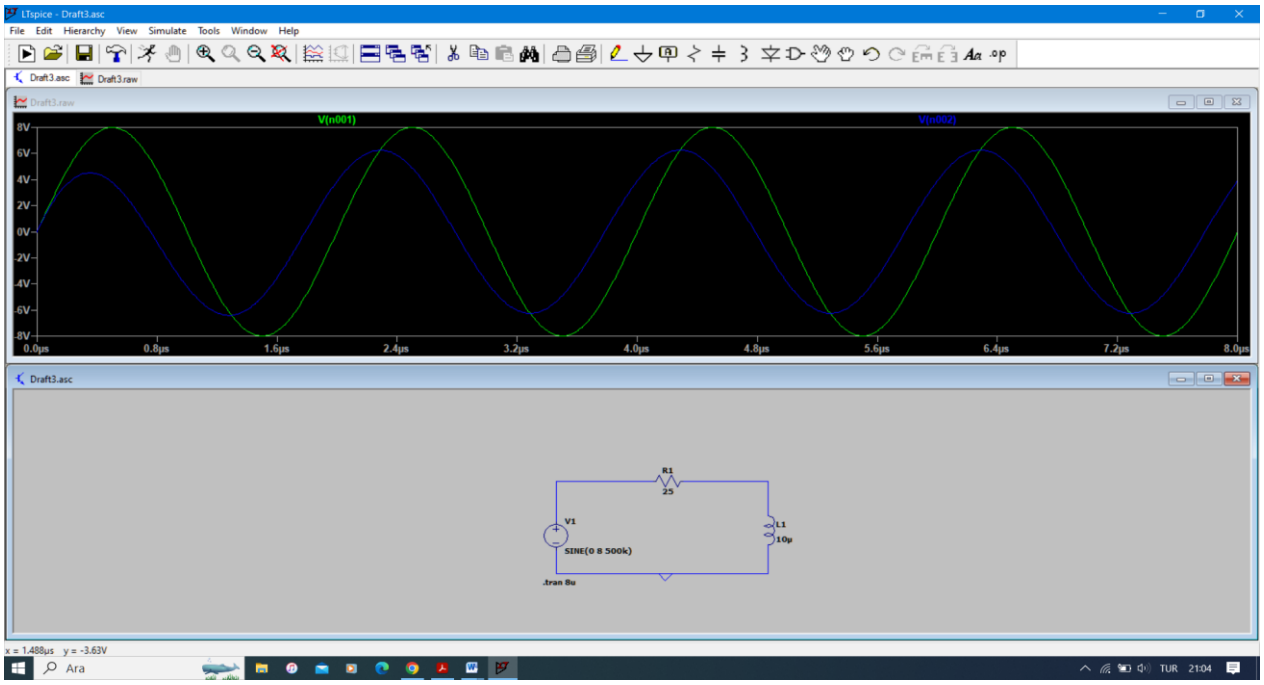

Figure 9: Circuit design and voltage graph of input (Vn001) and output (Vn002)

Here is the maximum of output voltage is nearly 6.25 volts which is much greater than the output voltage when the frequency was 100kHz or 10kHz:

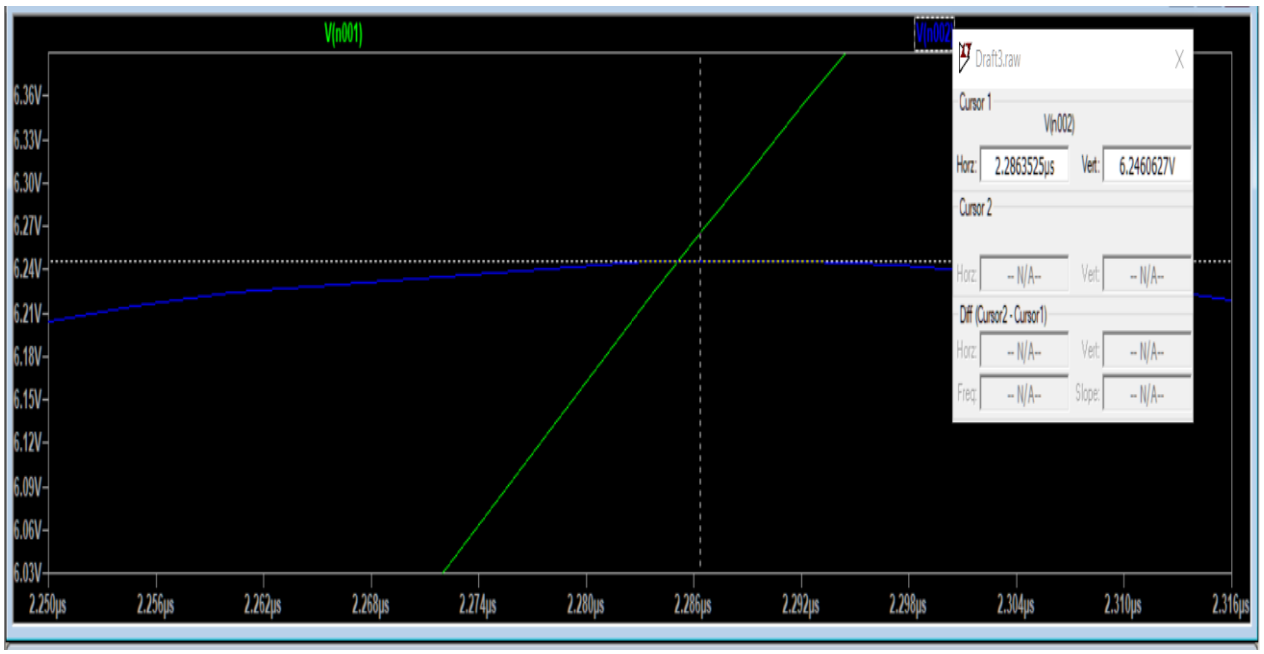

Figure 10: The Maximum of Output Voltage (Vn002)

From Part 1.2, it can be said that when frequency is getting higher the output voltage gets closer to the input voltage which is 8 volts. To check, when frequency was 10 kHz, the maximum of output voltage is 200.98mV, when frequency was 100kHz it was 1.95V and when frequency was 500kHz, it was 6.25 V. Therefore this is a high-pass filter. Additionally, to double check the simulation results, Equation 2 can be used:

$$V_o = V_{in} * \frac{jwl}{R_1 + jwl} = V_{in} * \frac{1}{\frac{R_1}{jwl} + 1} \text{ when } w \to \infty, V_o \to V_{in}$$

Therefore, simulation result satisfies the mathematical result since when frequency gets higher, output voltage gets higher and gets close to the input voltage.

Part 2: AC (frequency-domain) Analysis

Part 2.1 and 2.2:

Introduction:

In this part, the purpose of the project is to perform frequency-domain analysis of a RL circuit. And observing that the behaviour of the circuit changes with frequency. However, as it is hard to simulate the circuit at each frequency, it is better to see its behaviour in a frequency range in logarithmic plots.

Analysis:

The expected result is the same with the Part 1.2 because the only change is the type of the graph and the domain so the Vo should get higher and get close to Vin as the frequency gets higher. And this will prove that our RL circuit is a high-pass filter.

Simulation:

Here is the circuit design of RL circuit in LTSpice.

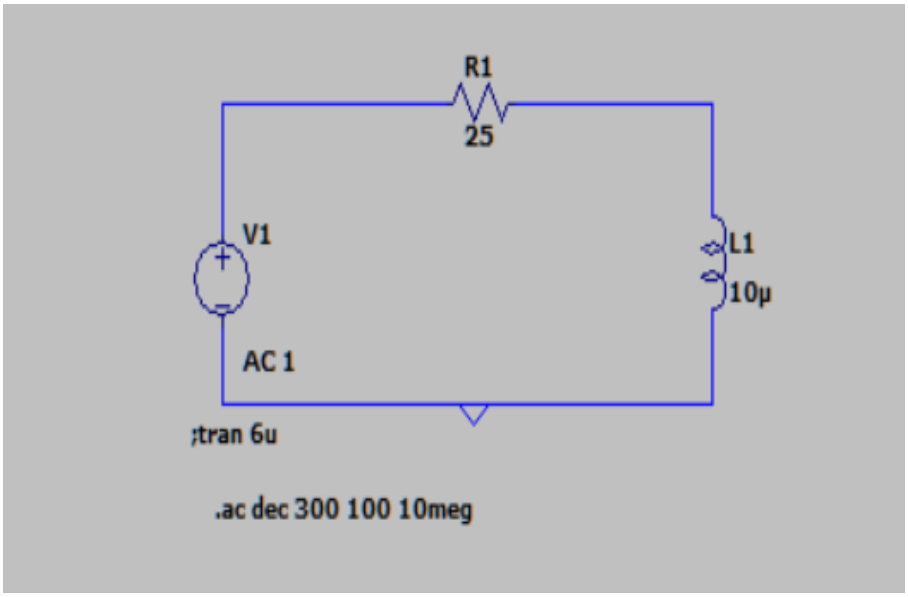

Figure 11: RL Circuit Design

Here is the logarithmic plot of output voltage (Vn002) which is the voltage of L1.

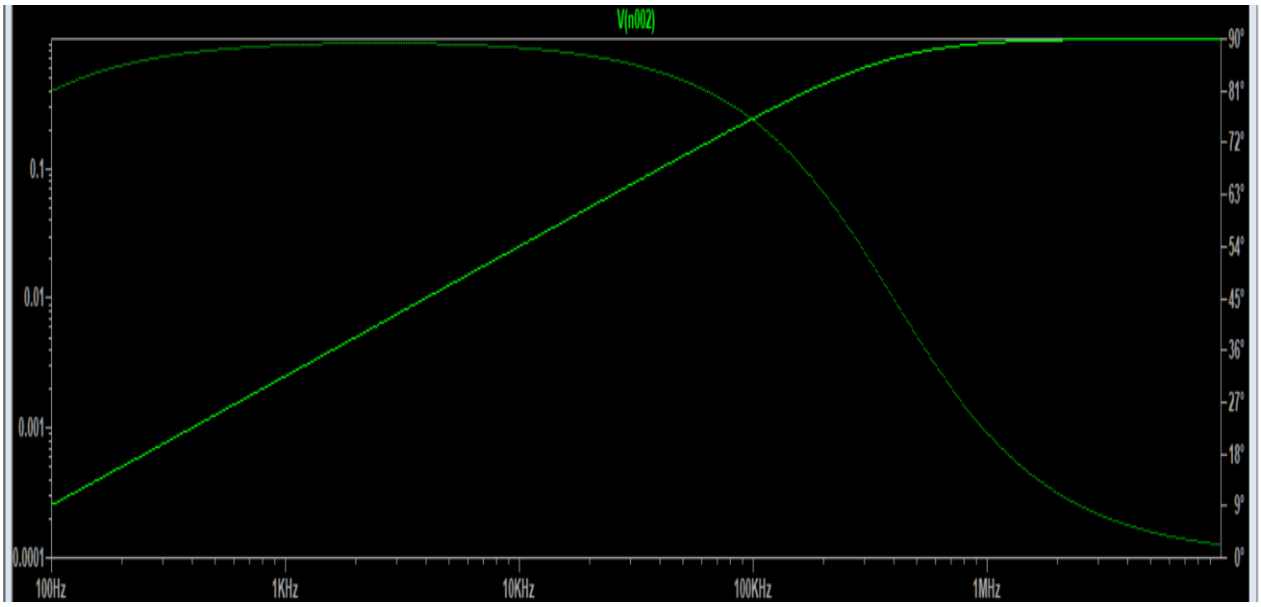

Figure 12: Logarithmic Plot of Part 2.1

As it can be seen from Figure 12, the RL circuit works as a high-pass filter. Because when the frequency get higher, the output voltage gets higher.

Part 2.3:

Introduction:

In our hardware labs, the signal generator has a serial output resistance of 50 ohms. Therefore, to get consistent results between my design and its hardware implementation, I needed to consider this resistance in LTSpice. As the result, 50 ohms of resistor R2 is added before the resistor R1. What is expected here is that, the RL circuit will stay as a high-pass filter but the amplitude of the output voltage will decrease.

Analysis:

Here is the necessary formula Equation 3, which is derived from Equation 1 and Equation 2:

$$V_o = V_{in} * \frac{jwl}{R_1 + R_2 + jwl}$$

Equation 3

Simulation:

Here is the following LTSpice RL circuit:

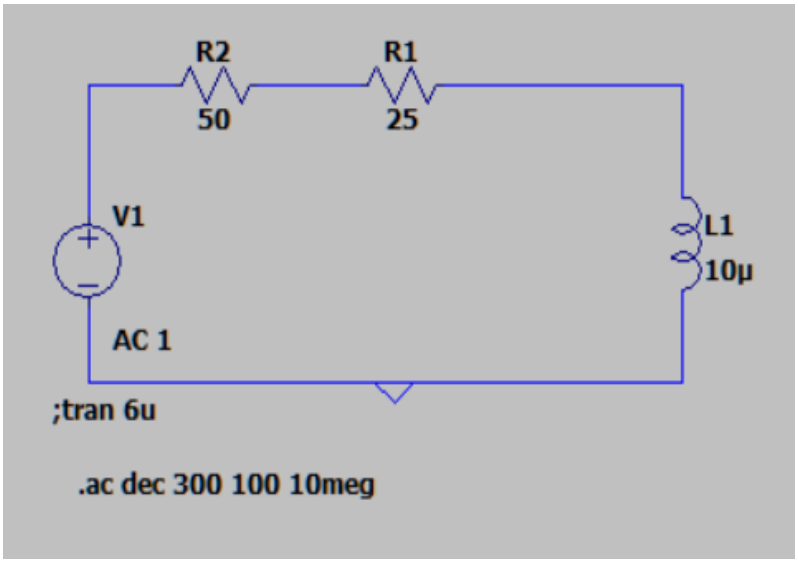

Figure 13: The Modified RL Circuit

Here is the logarithmic plot of output voltage (Vn002) which is the voltage of L1 for the modified circuit.

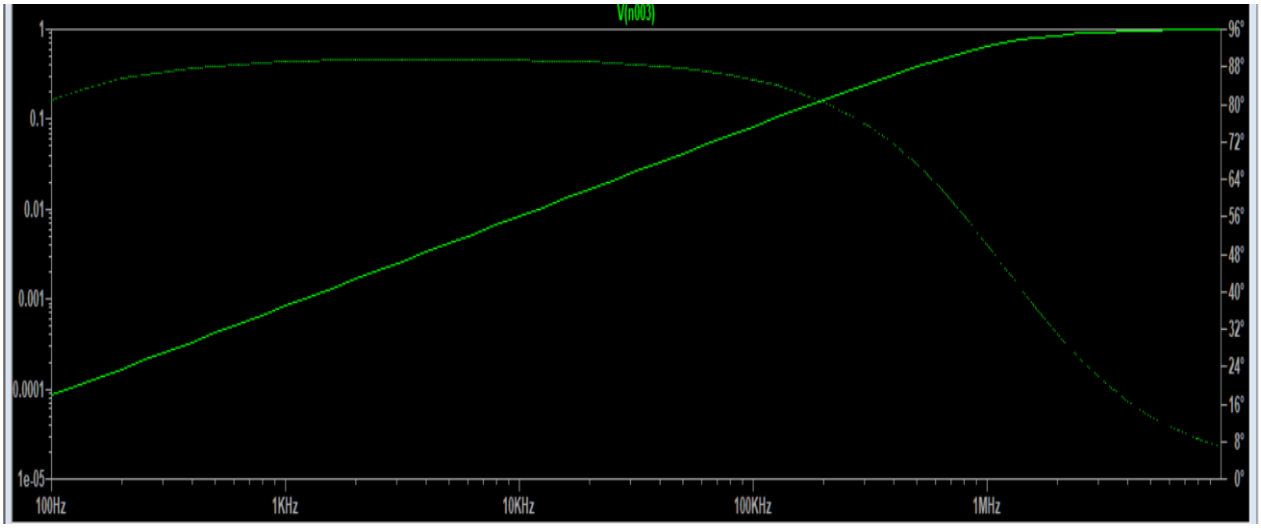

Figure 14: Logarithmic Plot of Part 2.3

And here is the graph for the comparison of logarithmic values for the modified and unmodified RL curcuits:

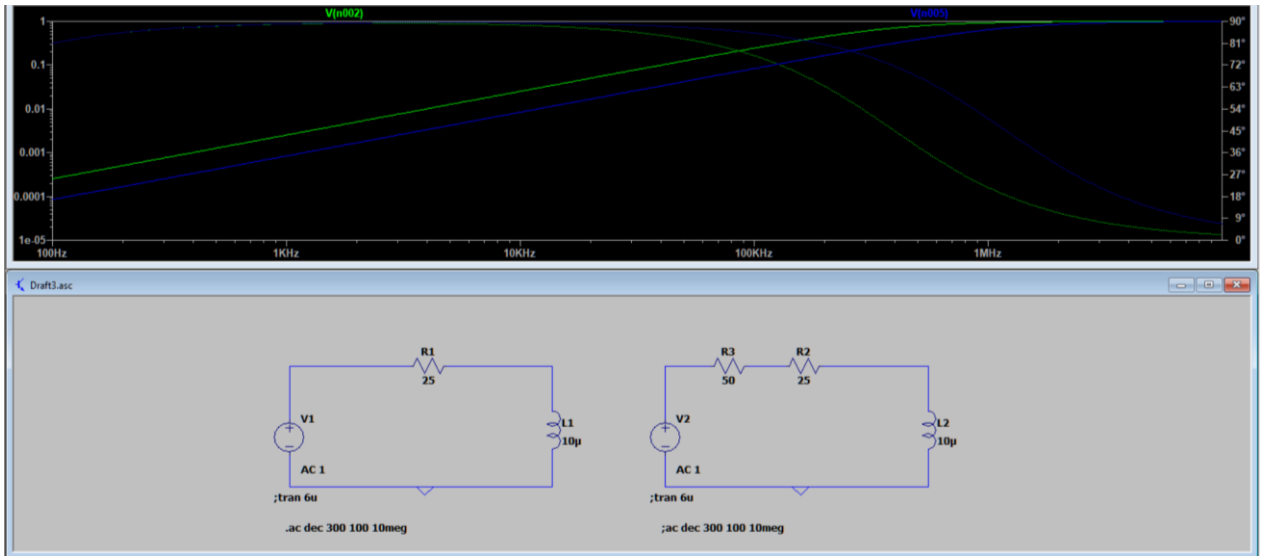

Figure 15: Logarithmic Plot and Designs of Modified and Unmodified Curcuits

As it is seen in Figure 15, the output voltage (blue lines) of the circuit is decreased after the modification as it is interpreted in the Equation 3. Therefore, the voltage gain decreases. It is clearly seen from the results that it is a High-Pass filter. While its frequency is approaching to the infinity output voltage gets closer to the input voltage 8V.

Part 2.4:

Introduction:

The purpose of this part is to deepen the understanding of the circuit's behavior by analyzing how the output voltage changes relative to different reference points within the circuit. This analysis helps in gaining insights into how the circuit responds to different conditions or inputs.

Analysis:

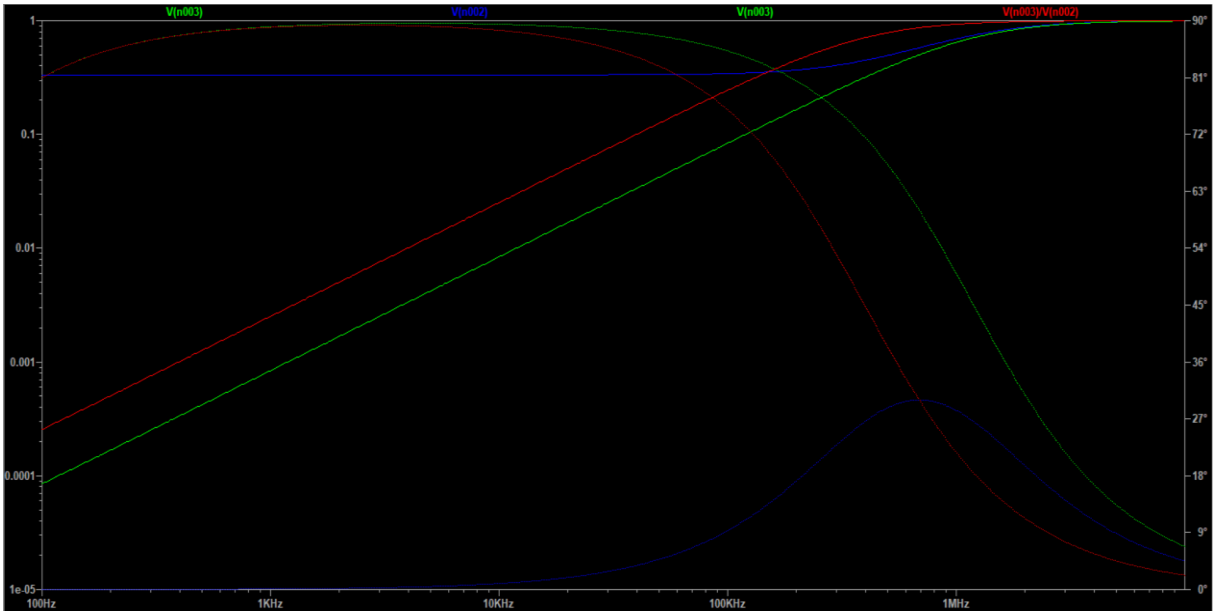

Figure 16: Voltage Comparison Graph in Logarithmic Scale

It is evident that the magnitude and phase of Figures Figure 16 and Figure 12 are identical. This indicates that the ratio of the input to the output of the original circuit—the circuit without a serial 50 Ω resistance—is the same as the ratio of the output voltage to the voltage at the output of the realistic signal generator model in the modified circuit. As we previously noted, the gain of the output relative to the input would drop with the addition of a 50 Ω serial resistance. We wouldn't experience this kind of gain loss if we thought of the input node as the realistic signal generator model's output.

Part 3:

Introduction:

The purpose of Part 3 is to familiarize students with the analysis of basic operational amplifier (OPAMP). There is a basic OPAMP circuit in Figure 17. Other purposes are simulating the circuit with a sinusoidal input signal and observing the amplified output to identify the type of OPAMP circuit. Changing the input signal to a square wave and repeating the simulation to observe the behavior.

Increasing the ratio of R2 to R1 to observe the saturation of the OPAMP. Modifying the circuit by changing resistor values and replacing a resistor with a capacitor, then simulating it with a square wave input to observe the output and determine the type of OPAMP circuit.

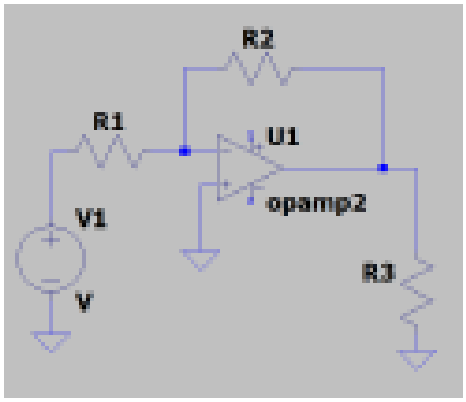

Figure 17:Basic OPAMP Circuit

Analysis:

In Figure 19, there is the output (green) and input (blue) voltage graph. As it is seen here, the output voltage is equal to the multiplication of input voltage and -3 V. Since the inverting input (-) is connected to the input signal through the input resistor (R1), the output voltage of the opamp adjusts in such a way that it produces a voltage at the inverting input (-) terminal that matches the voltage at the non-inverting input (+) terminal. This configuration results in an output voltage that is the inverted and amplified version of the input signal. Therefore, this is an inverting amplifier.

The gain of the inverter opamp circuit is determined by the ratio of the feedback resistor (R2) to the input resistor (R1). The formula for the gain (A) is typically given by Equation 4:

$$A = -(R2/R1)$$

Equation 4

Simulation:

Part 3.1, Part 3.2 and Part 3.3 (Inverter):

In figure 18, there is the desired OPAMP circuit on LTSpice for the Part 3.1, 3.2, and 3.3.

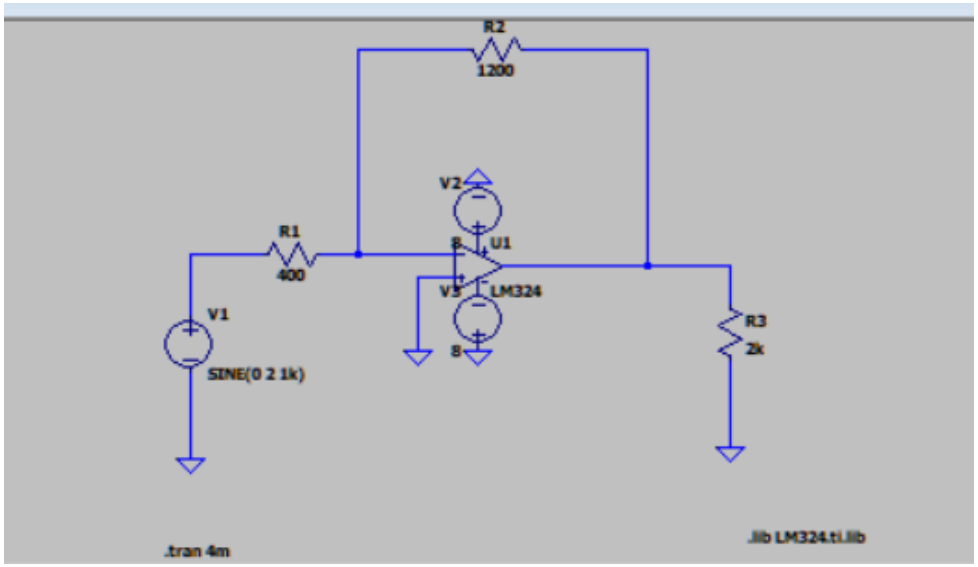

Figure 18: Desired OPAMP Circuit

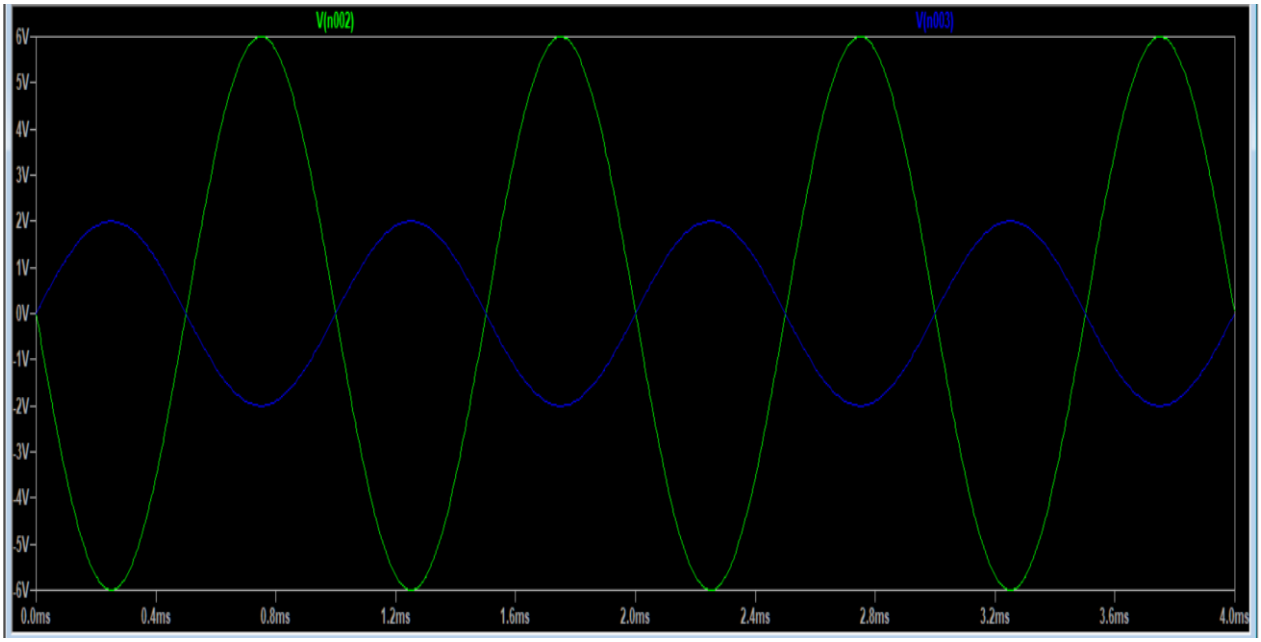

Figure 19: Input and Output Voltage of the Inverting Amplifier

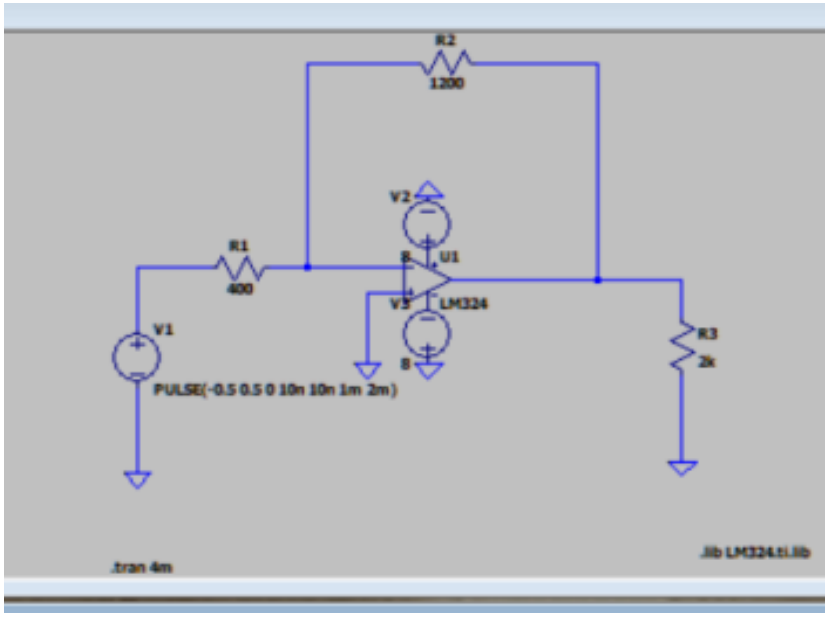

Figure 20: Inverting Opamp With a Square Wave Input

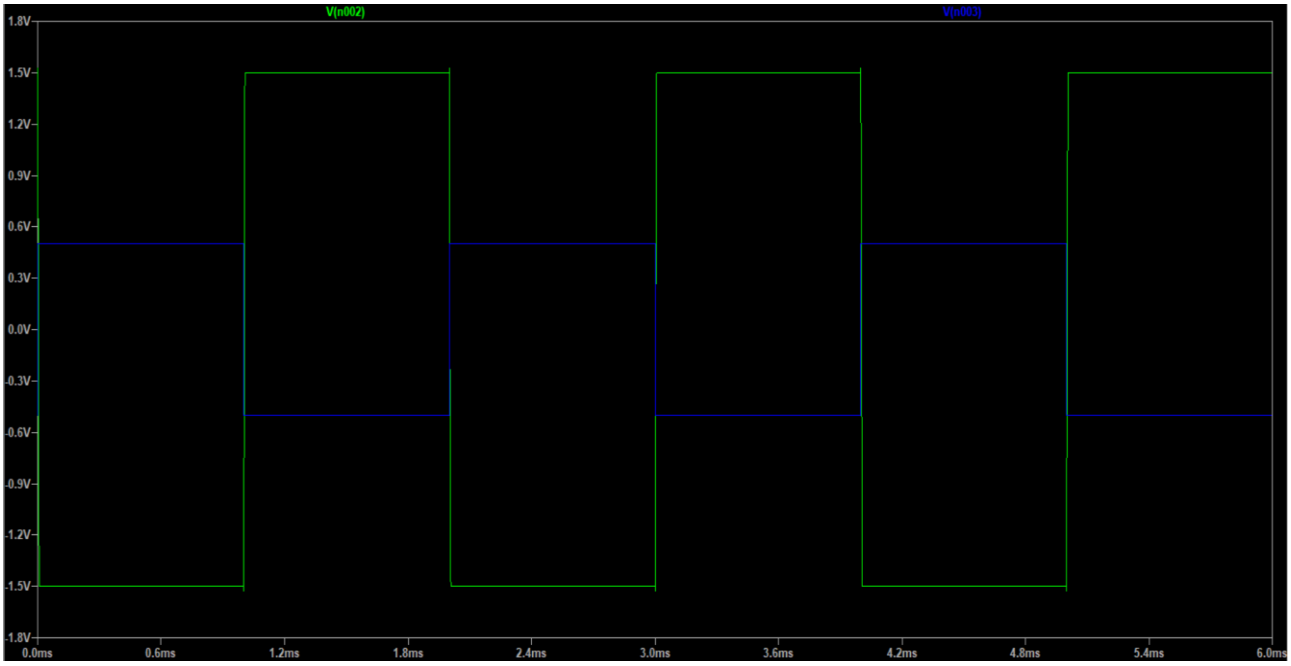

Figure 21: The Transient Analysis of Inverting OPAMP (input is in square wave)

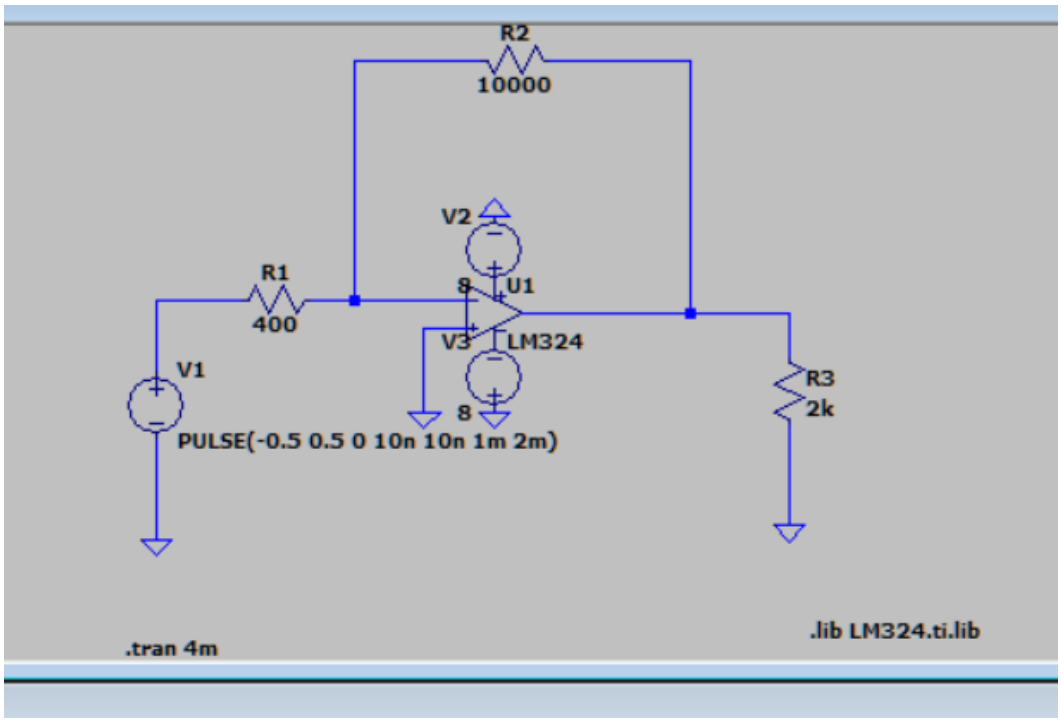

Figure 22:Saturated Inverting Opamp

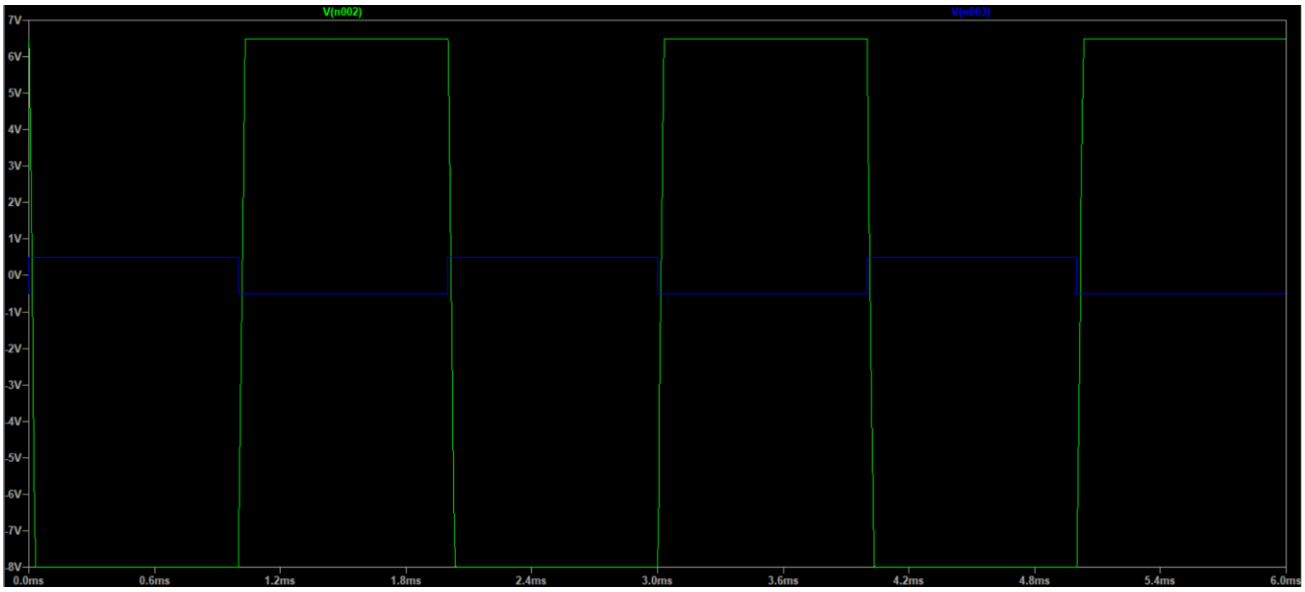

Figure 23: The Saturated Transient Analysis of Inverting OPAMP (input is in square wave)

Replacing R2 with a capacitor was the last task for the third and final software lab section. Figure 24 shows the updated circuit, and Figure 25 shows the input/output plot. This circuit functions as an integrating circuit; Equation 5 shows how the OPAMP integrates the input voltage to produce the output voltage. This is because we installed a capacitor in place of R2.

$$\frac{V1 - V2}{R1} = C\frac{dVc}{dt} = C\frac{d(V2 - Vout)}{dt}$$

$$Vout(t) = Vout(0) - \frac{1}{R1C}\int_0^t V1(\tau)d\tau$$

Equation 5

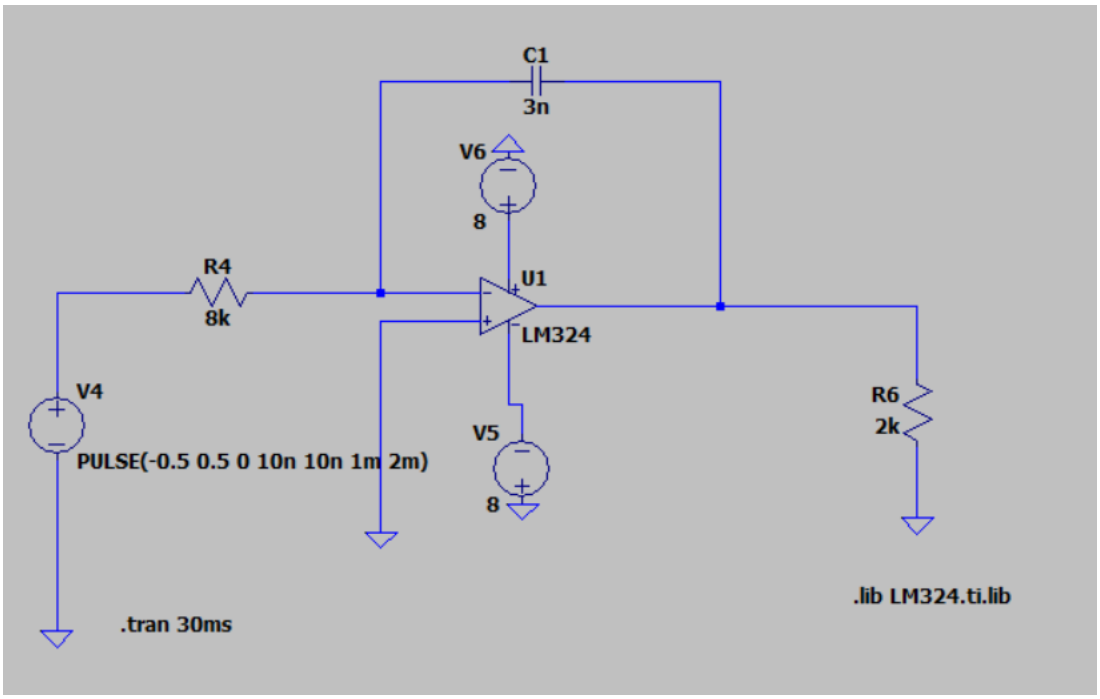

Figure 24: The integrator OPAMP circuit

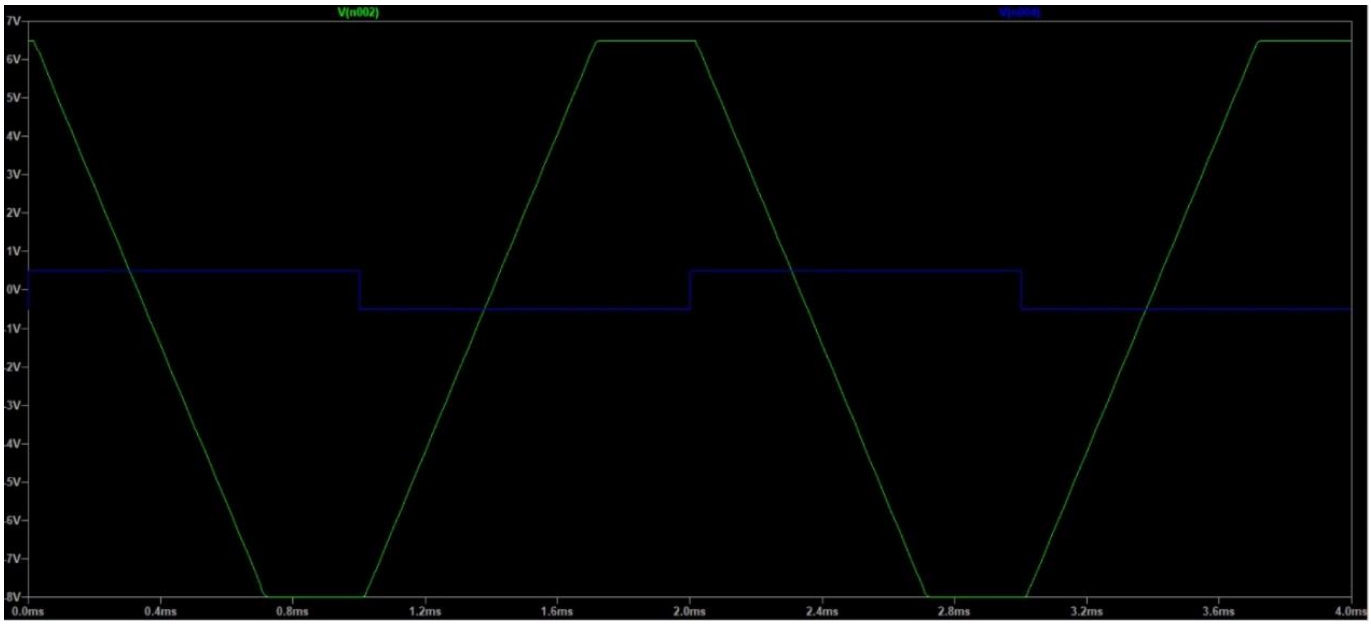

Figure 25: Input and Output Voltage Graph of the Inverter OPAMP

HARDWARE LAB:

Part 1: RL Circuit

We were tasked with putting the RL circuit we built in software lab part 1.2 into practice in the first hardware lab section. The constructed circuit, the output voltage's frequency response, and a table and graph of the collected data are all shown here.

With a tiny margin of error, the results were almost exactly in line with the LTSpice simulation. Here is the gain formula:

$$Gain(dB) = -20\log(\frac{\text{Vout}}{\text{Vin}})$$

Equation 6

Results:

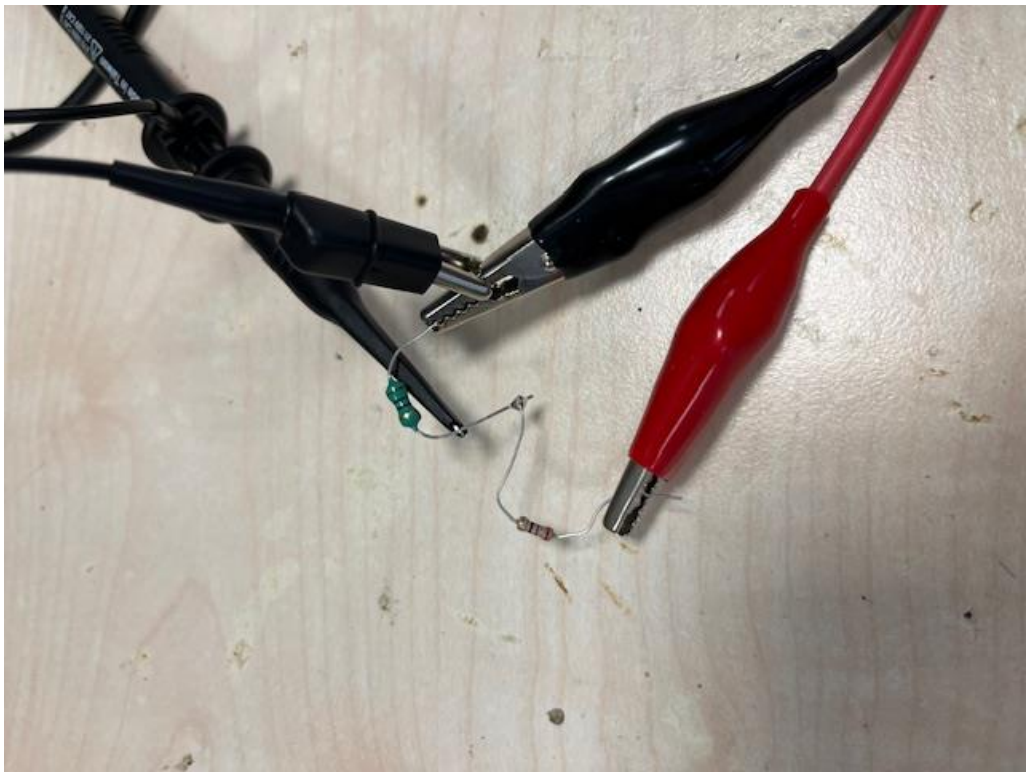

Figure 26: RL Circuit with Physical Components

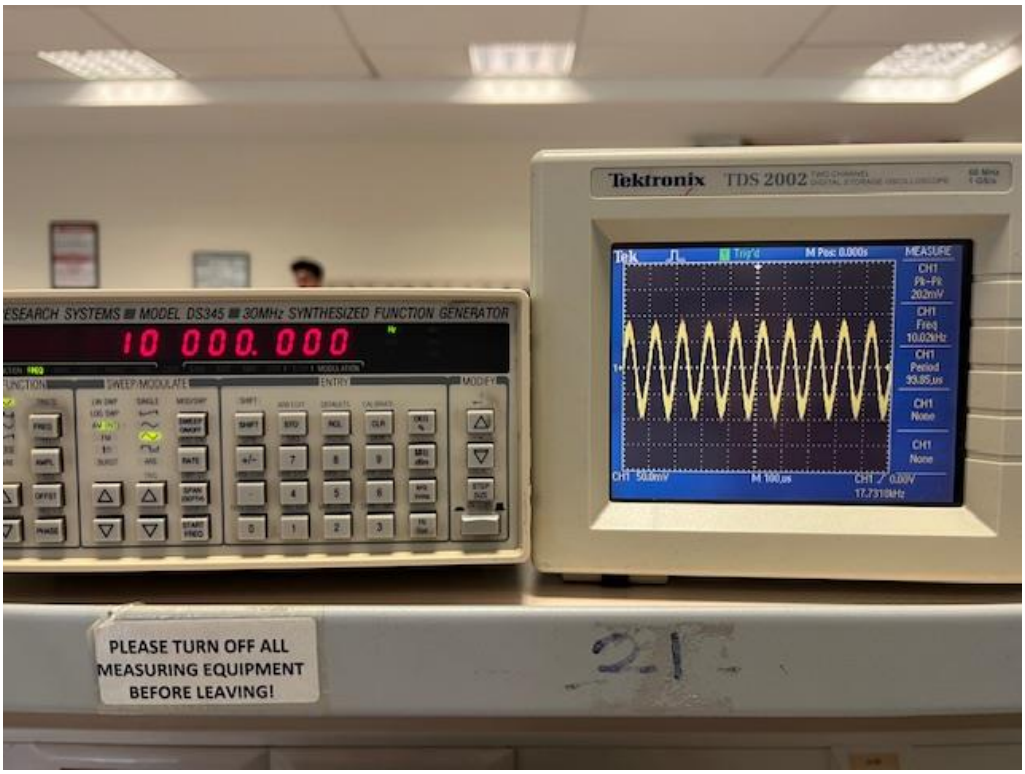

Figure 27: The Output Voltage Graph when f=10kHz and Vpp=0.202V

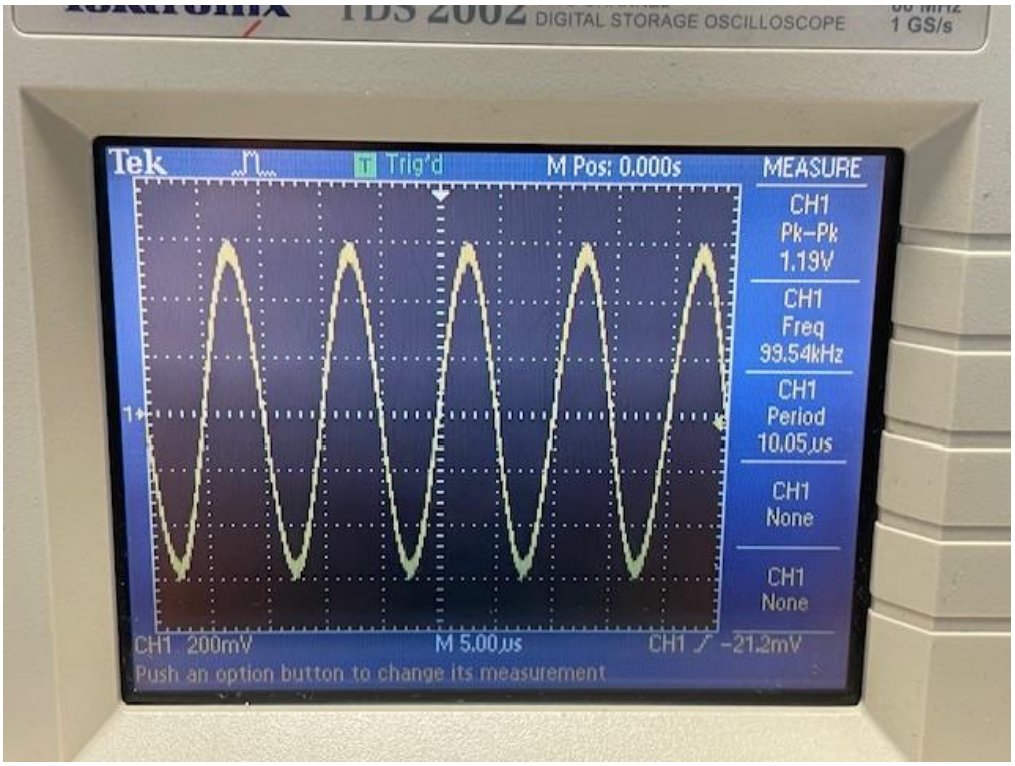

Figure 28: The Output Voltage Graph when f=100kHz and Vpp=1.19V

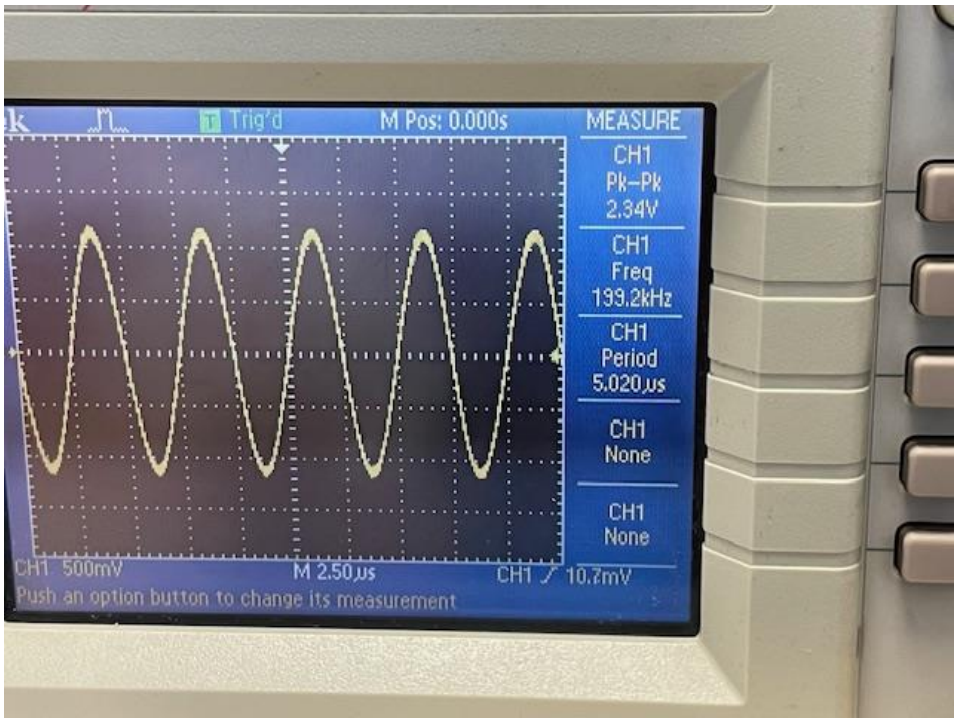

Figure 29: The Output Voltage Graph when f=200kHz and Vpp=2.34V

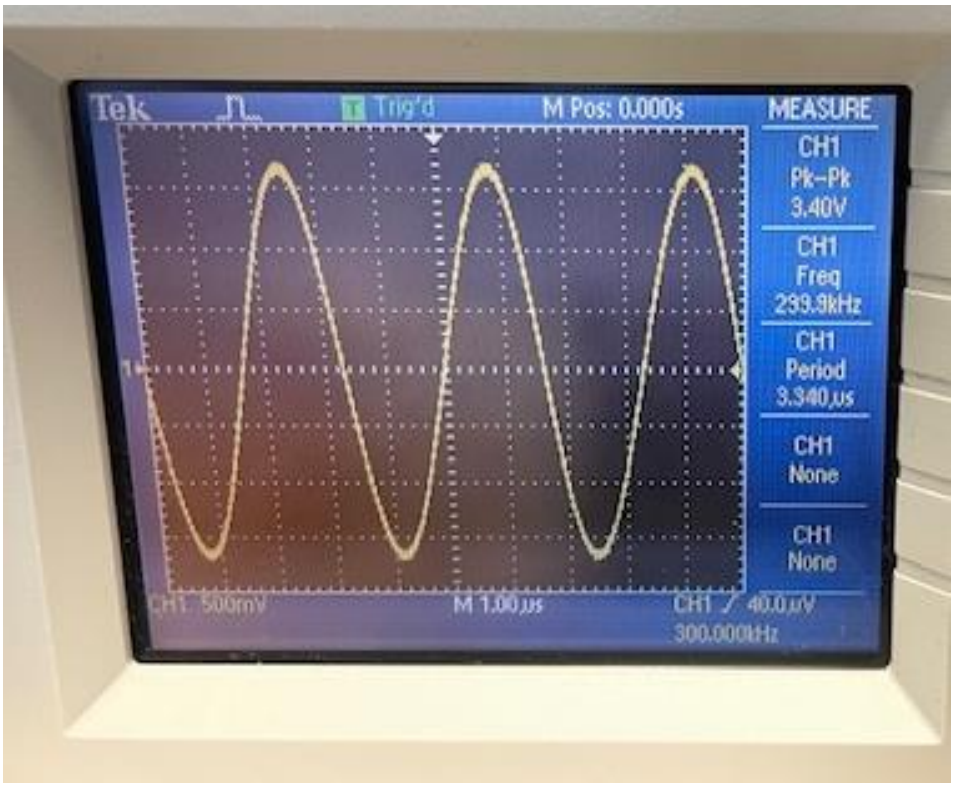

Figure 30: The Output Voltage Graph when f=300kHz and Vpp=3.40V

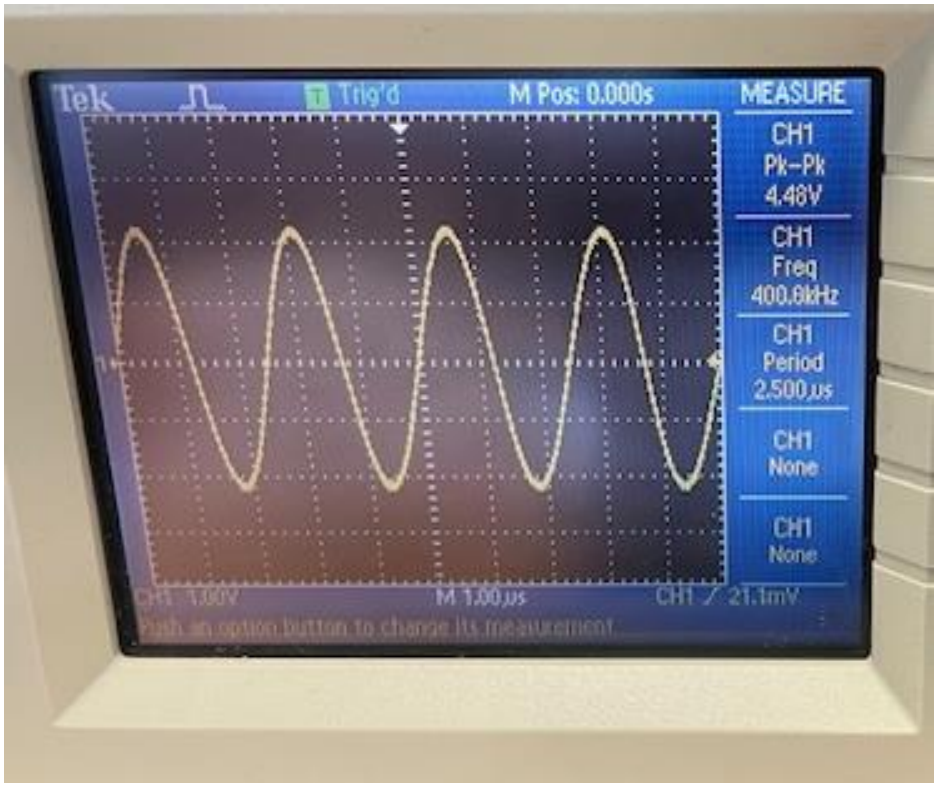

Figure 31: The Output Voltage Graph when f=400kHz and Vpp=4.48V

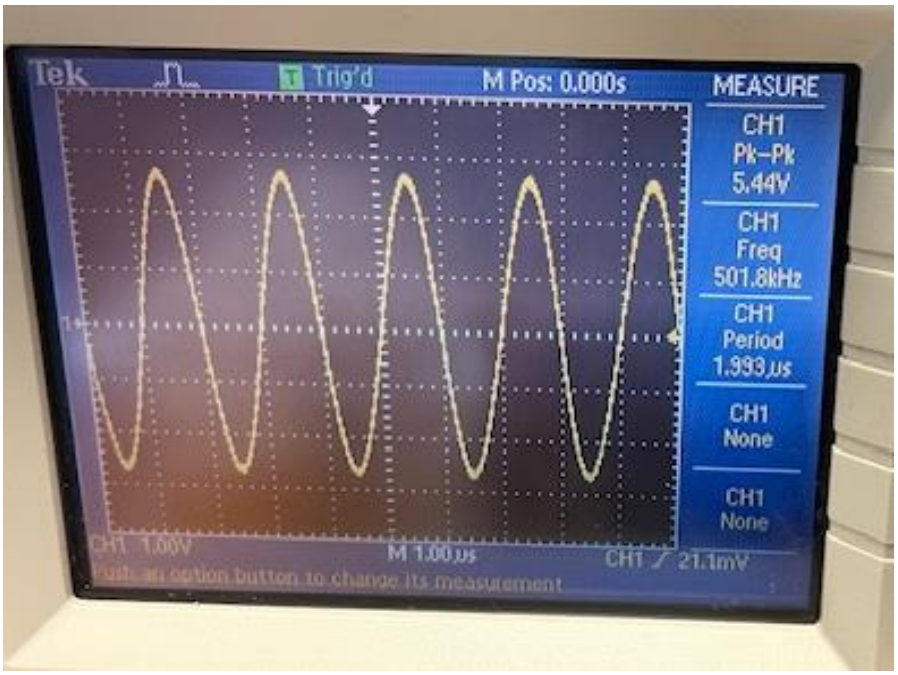

Figure 32: The Output Voltage Graph when f=500kHz and Vpp=5.54V

Frequency	Max Output Voltage	Gain (dB)
10kHz	0.101V	-37.9
50kHz	0.205V	-31.8
100kHz	0.595 V	-22.6
200kHz	1.17 V	-16.6
300kHz	1.7 V	-13.4
400kHz	2.24 V	-11.1
500kHz	2.77 V	-9.3

Table 1: Frequency-Max Output Voltage- Gain Table

As the frequency increases, gain decreases and output voltage gets closer with the input voltage which is 8 V. And satisfies with the software results.

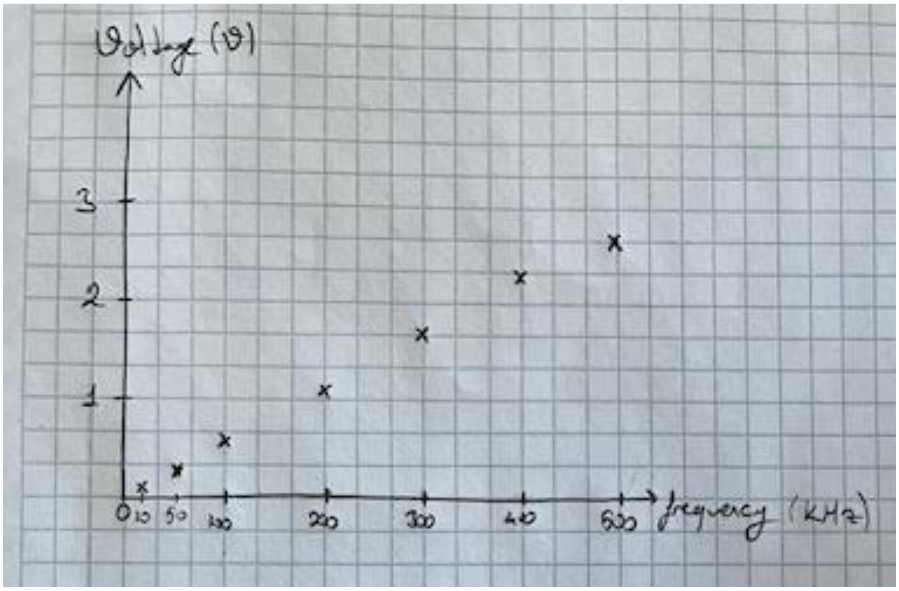

Table 2: A Rough Voltage-Frequency Graph with the Values From Table 1

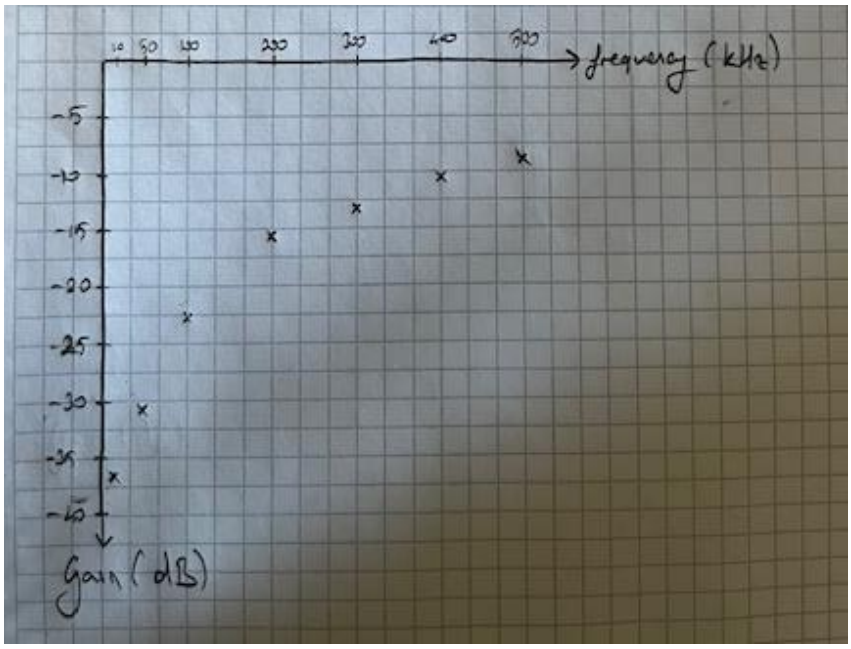

Table 3: A Rough Gain-Frequency Graph with the Values From Table 1

As it is wanted in the instructions, the rough graphs of voltage-frequency and gain-frequency are drawen. And the results are consistent with the software lab with minor errors. The reasons of these minor errors could be human errors, ossciloscope problems or the resistor of components.

Part 2:Opamp Circuit:

We were given the task of building the two distinct OPAMP circuits—the integrating amplifier circuit and the inverting amplifier circuit—that we had constructed in the software lab for part two of the hardware lab. Here are the output voltage data and the built circuits for both kinds of amplifier circuits. We note that in both types of circuits, our experimental results agree with the computational data. The equation to find the inverting coefficient:

$$\text{Inverting Coefficient} = \frac{Vout}{Vin}$$

Equation 7

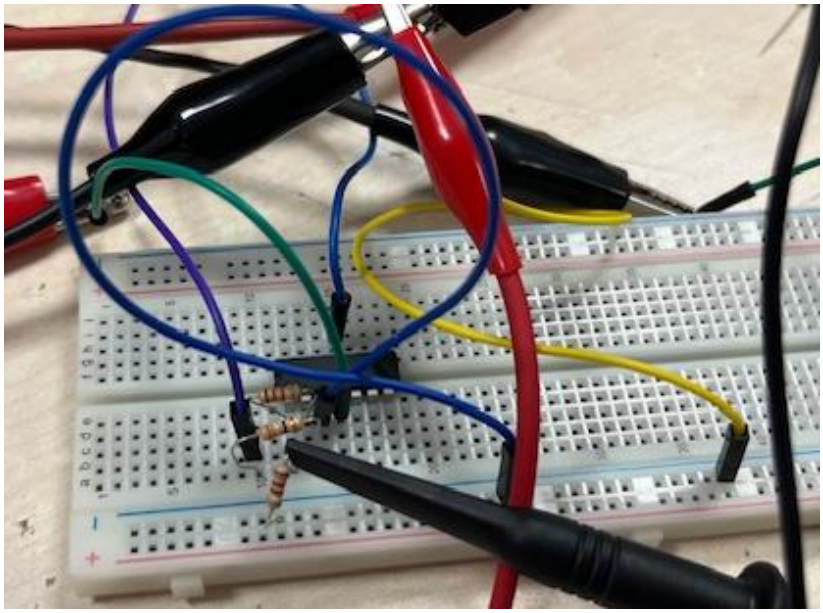

Figure 33: The Hardware Design of the Inverting OPAMP

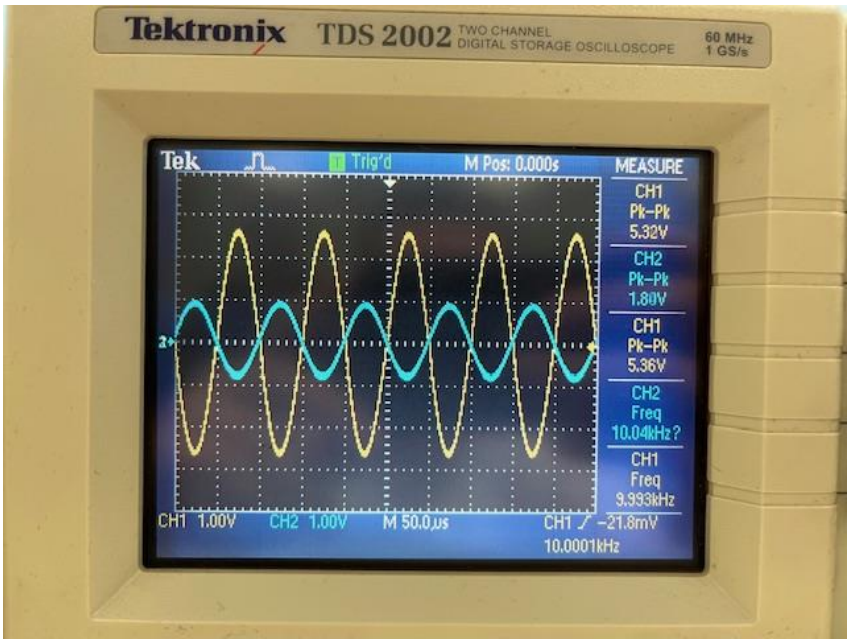

Figure 34: Input and Output Voltage Graph of Inverting OPAMP

This hardware result satisfies the software result since the output voltage is -2.96 times of input voltage. In the software result, it was -3 times of input voltage but they are satisfyingly close.

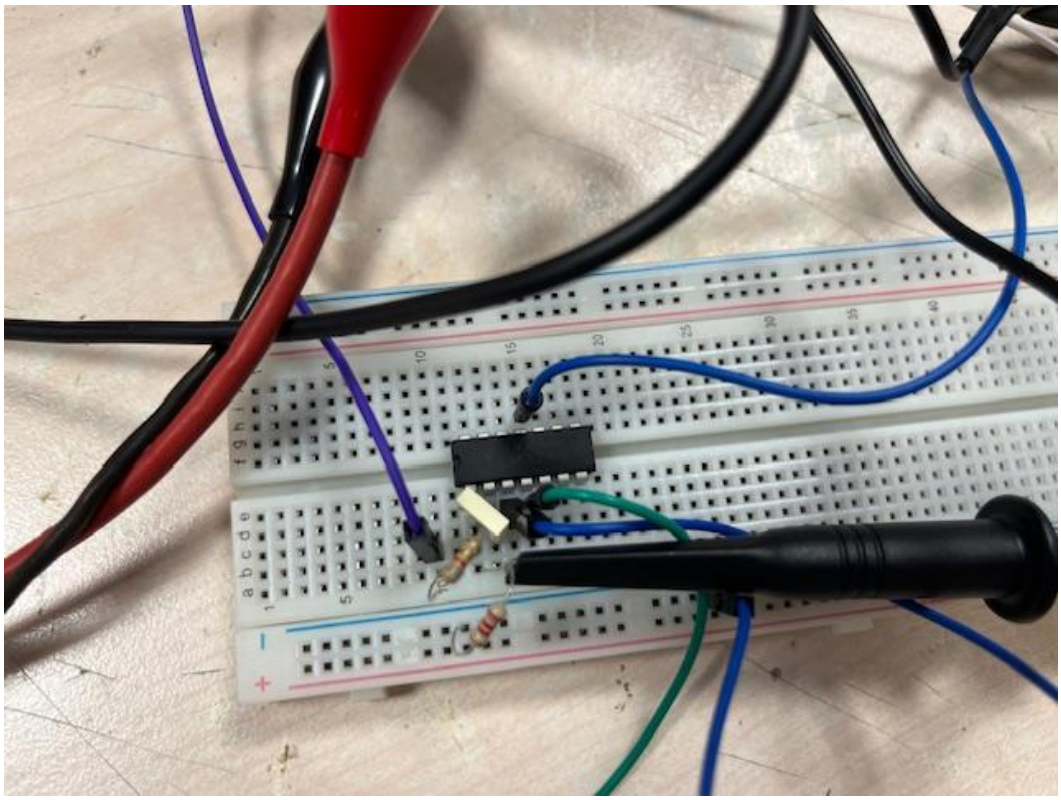

Figure 36: The Hardware Design of the Integrating OPAMP

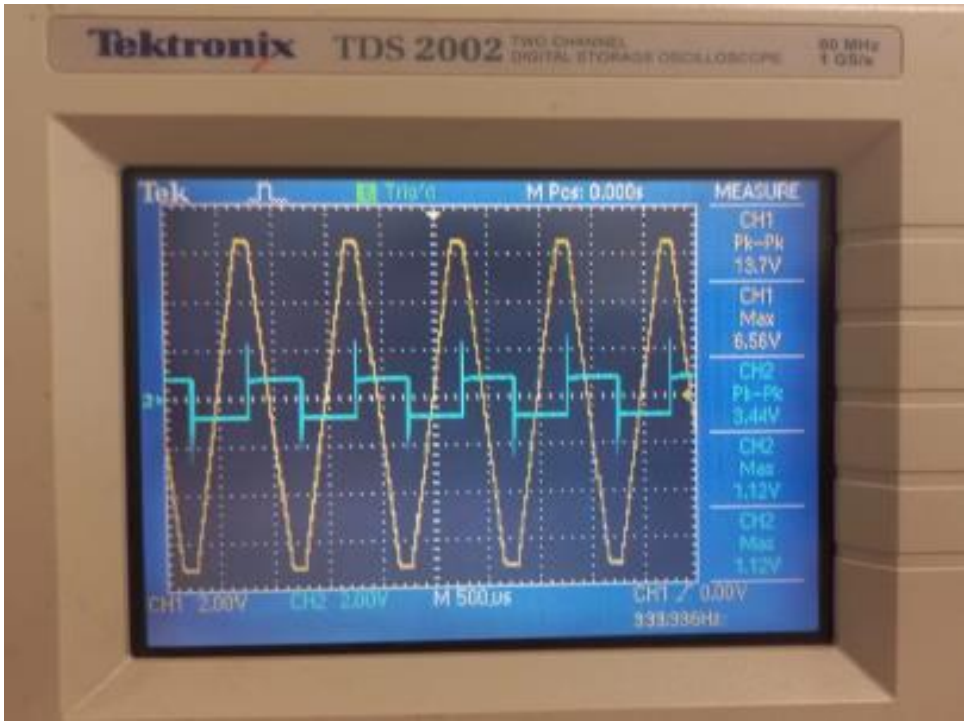

Figure 37: Output Voltage of the Integrating OPAMP

Conclusion:

The primary goal of this lab assignment's software part was to use LTSpice to conduct time and frequency domain evaluations. We created both OPAMP and RL circuits. The experiment's hardware and software components both performed as planned, however the hardware lab did have a few negligible little errors, mistakes in analog equipment, such as internal wire resistance or oscilloscope inaccuracy could be the source of these mistakes.

We gained faster and more efficient LTSpice skills throughout the lab. Since we will be using LTSpice software, this will undoubtedly aid us in both our academic and professional lives. Overall, this was really beneficial lab to get familiar to the next labs.