Bilkent University Department of Electrical and Electronics Engineering

EEE202 Circuit Theory Lab 3

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EE202-03

SOFTWARE LAB:

Introduction:

Lab 2's objective is to develop a circuit that uses a peak 5 V square wave as a source to produce the voltage waveform shown in Figure 1. Through the report the circuit design process, the findings, and the computations will be clearly explained. First, the Lt Spice simulation will be used to test the design, and the outcomes will be reviewed. Additionally, the expected Δt values in Figure 1 are $\Delta t0=2$, $\Delta t1=2$, $\Delta t2=3$, $\Delta t3=2$.

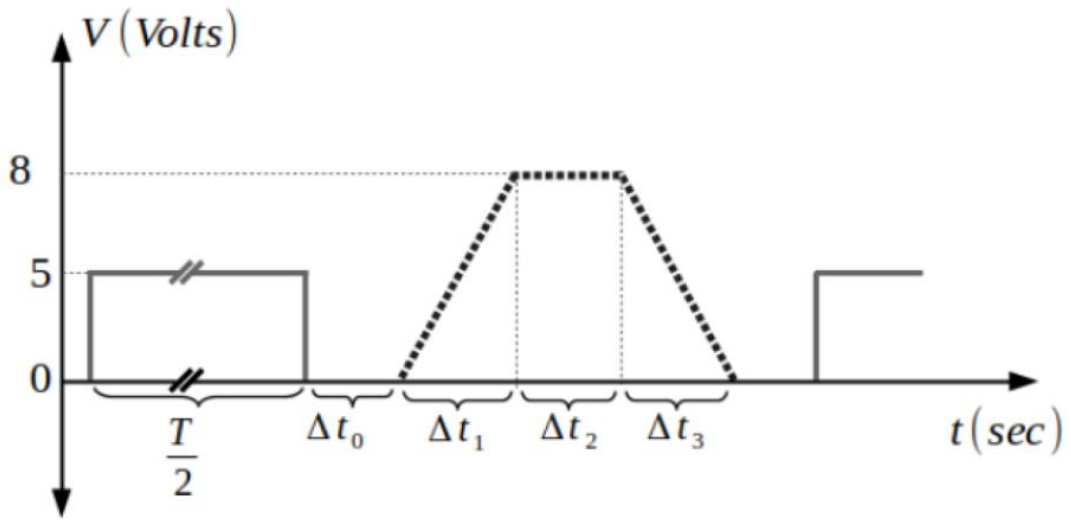

Figure 1: Expected Input and Output Voltage Graph with Respect to Time

Additionally, as per the laboratory specifications, the input frequency must not exceed 50 Hz, or have a duration of less than 2 milliseconds. To adhere to these criteria, the design approach will involve shifting, integrating, and subtracting processes. Specifically, the input voltage will undergo independent shifts of 2 milliseconds ($\Delta t0=2$) and a total delay of 9 milliseconds ($9= \Delta t0 + \Delta t1 + \Delta t2 + \Delta t3$) in the initial phase (shifting), facilitated by two comparator OPAMPs. Subsequently, the two delayed signals will reach the integration stage. It is imperative to incorporate the integration component to generate the desired output. Lastly, the 9 ms delayed signal will be subtracted from the 2 ms delayed signal using one subtracting OPAMP. The intended output signal in Figure 1 will be the final OPAMP's output.

Analysis:

First Step (Creating Delays):

In order to have 2 different delays, there is a need to have two comparator OPAMPs. If the voltage of the positive port of the OPAMP (V+) is larger than the reference voltage, then the OPAMP is saturated positively. . If the voltage of the positive port of the OPAMP (V+) is less than the reference voltage, then the OPAMP is saturated negetively. In the Figure 2 and Figure 3, the comparator OPAMPS can be seen.

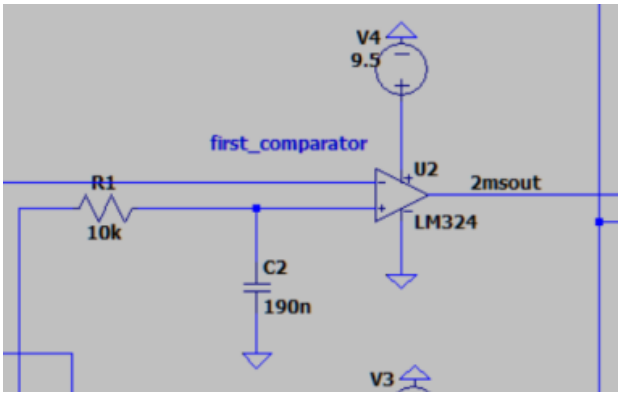

Figure 2: Schematics of the First Comparator

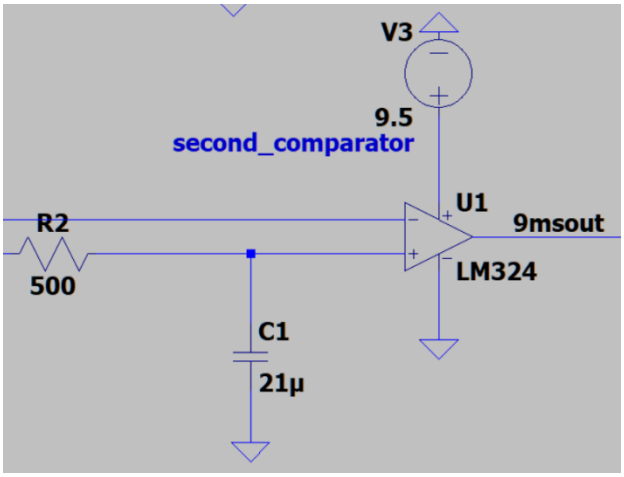

Figure 3: Schematics of the Second Comparator

The wires that are connected to the negative port of the OPAMPs are also connected to the comparator voltage and the wires that are connected to the positive port of the OPAMPs are connected to the input voltage.

Here are the computations:

By the Kirchhoff's Current Law at the positive port (V+),

$$\frac{dVc}{dt} * C = \frac{Vin - Vc}{R}$$

Equation 1

By using Equation 1, $Vc(t)$ is found as :

$$-5e^{\frac{-t}{R*C}} + 5 = Vc$$

Equation 2

When the values t=2ms, Vc=2.5V and, $R1 * C2 = 2.88 * 10^{-3}$

The values 10Kohms for R1 and 228nF for C2 satisfies the condition $R1 * C2 = 2.88 * 10^{-3}$ When the values t = 9ms, Vc = 2.5V, R2 * C1 =0.0129

The values C1=3nF, R1=10Kohm satisfies the condition R2*C1=0.0129

The integrator op-amps in the following stage may cause the overall output delays to beyond the specified limit, even though the determined values for the comparator OPAMPs alone may be accurate in theory. Therefore, the R * C computation needs to be lowered in order to satisfy the output delay requirements. For comparator 1, which has a delay of 2 ms, appropriate values can be determined as follows: $R1 * C2 = 1.9 * 10^3$, leading to R1 = 10 KOhm and C2 = 190 nF. Similarly, for comparator 2 with a delay of 9 ms, suitable values are found with R2 * C1 = 0.0105, resulting in R2 = 500 Ohm and C1 = 21uF.

Second Step (Integrator OPAMPs):

The subsequent phase involves designing two same integrator circuits by determining the component values. The upper wire corresponds to the output of the comparators, while the lower wire represents the reference voltage in Figure 4.

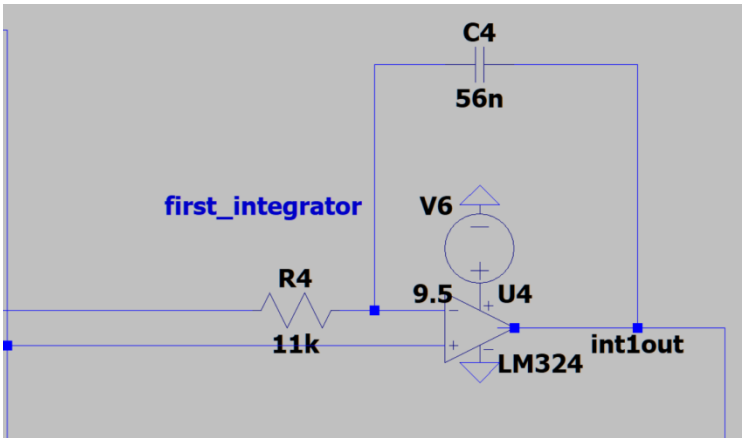

Figure 4: First Integrator Circuit in LTSpice

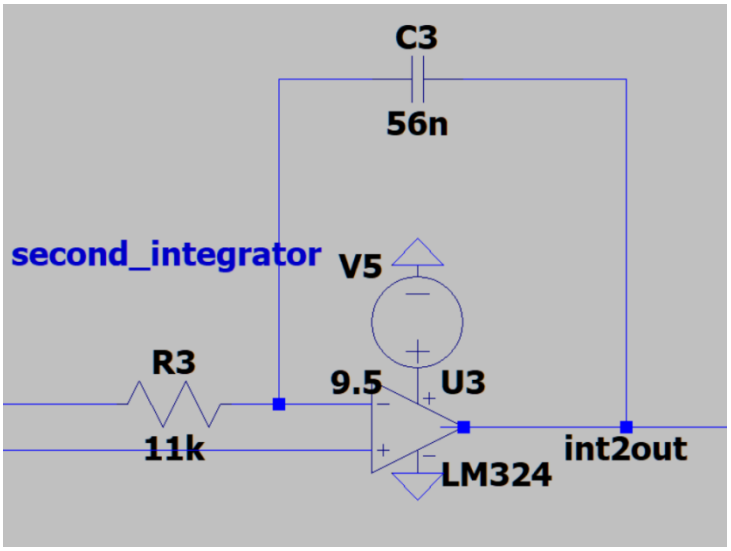

Figure 5: Second Integrator Circuit in LTSpice

By using the Kirchhoff's Current Law at the negative port (V-):

$$\frac{Input - V^{-}}{R\,.\,C} = dVc$$

Equation 3

Equation 4 is derived by taking the integral of Equation 3:

$$Vc = A + \frac{Input - V^+}{R.C}.t$$

Equation 4

Equation 5 is found for the desired values, Vc=0, A=0, t=0:

$$Vc = \frac{Input - V^+}{R.C}.t$$

$$Vc = \frac{2.5}{R.C}.t$$

Equation 5

Equation 6 is found for the desired values Vc=V, t=2:

$$3.2 = \frac{2m}{R.C}$$

$$RC = 6.25 * 10^{-4}$$

Equation 6

The values R = 11Kohm and C = 56nF

Third Step:

The third step is to create a subtractor OPAMP circuit to subtract the output voltages of two integrator OPAMPs. The desired subtractor OPAMP can be seen in the Figure 6.

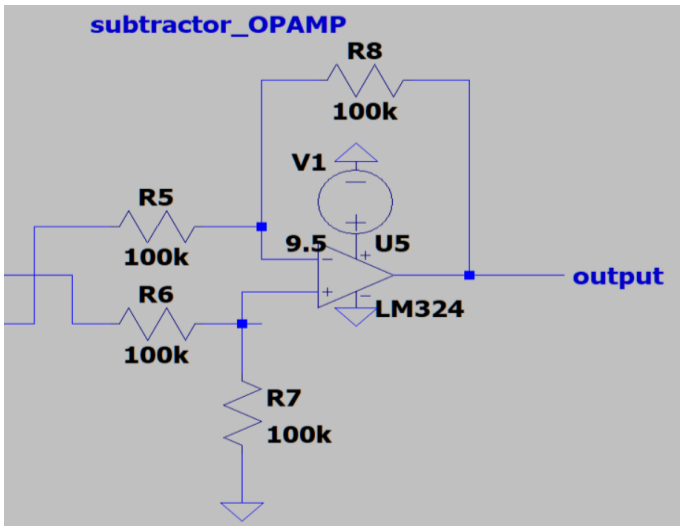

Figure 6: Substractor OPAMP circuit in LTSpice

In the Figure 6, the below wire is connected with the 9 ms delayed signal and the upper wire is connected with the 2 ms delayed signal.

By the Kirchhoff's Current Law in the negative port of the subtractor OPAMP (V-), Equation 7 is found:

$$\frac{input_9}{R5} = \frac{V^- - Vout}{R8}$$

$$V^- = \left(\frac{Input_9}{R5} + \frac{Vout}{R8}\right) * \frac{1}{\left(\frac{1}{R8} + \frac{1}{R5}\right)}$$

Equation 7

By the Kirchhoff's Current Law in the positive port of the subtractor OPAMP (V+), Equation 8 is found:

$$\frac{-V^- + input_2}{R6} = \frac{V^+}{R7}$$

$$V^+ = \frac{input2}{R6 * \left(\frac{1}{R7} + \frac{1}{R6}\right)}$$

Equation 8

By assuming the OPAMP to not be saturated, V+ is equal to V-:

$$\frac{input2}{R6*\left(\frac{1}{R7}+\frac{1}{R6}\right)} = \left(\frac{Input_9}{R5}+\frac{Vout}{R8}\right) * \frac{1}{\left(\frac{1}{R8}+\frac{1}{R5}\right)}$$

Equation 9

One can set the same values for all resistors, which are 100Kohm.
Then is found that:

$$V_{input2} - V_{input9} = V_{out}$$

Equation 10

After all of the computations and circuits are done, the final circuit is achieved in the Figure 7.

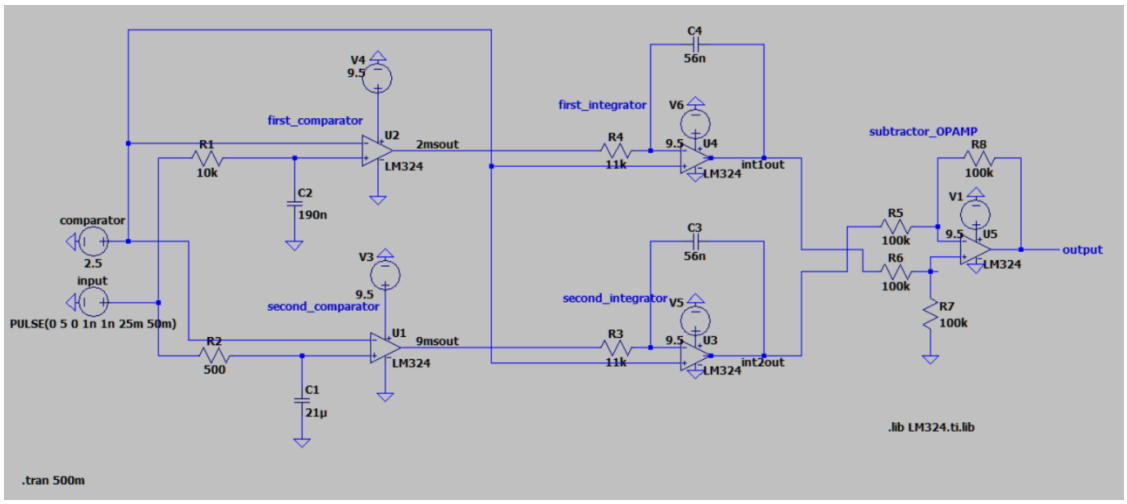

Figure 7: The Final Circuit

Simulation:
In the simulation part, the LTSpice simulation results will be provided.

Delay of the first comparator OPAMP is shown in Figure 8. The desired delay had to be less than 2ms because of the delay of the integrator OPAMP.

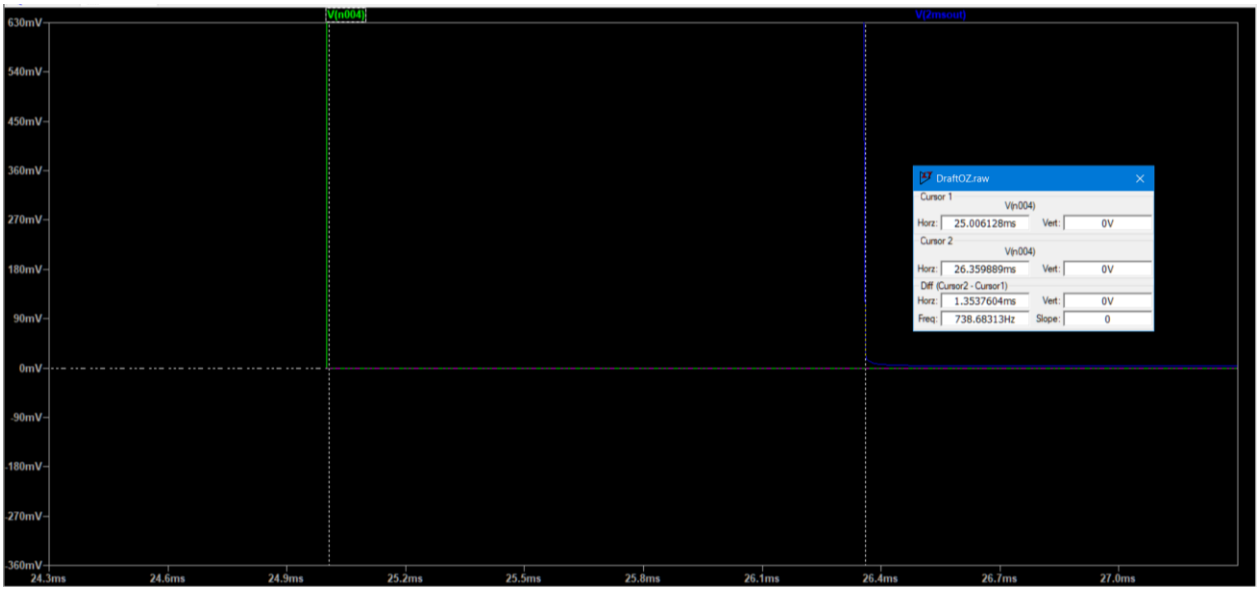

Figure 8: Delay of the First Comparator OPAMP is 1.3 ms

Delay of the second comparator OPAMP is shown in Figure 9. The desired delay had to be less than 7ms because of the delay of the integrator OPAMP.

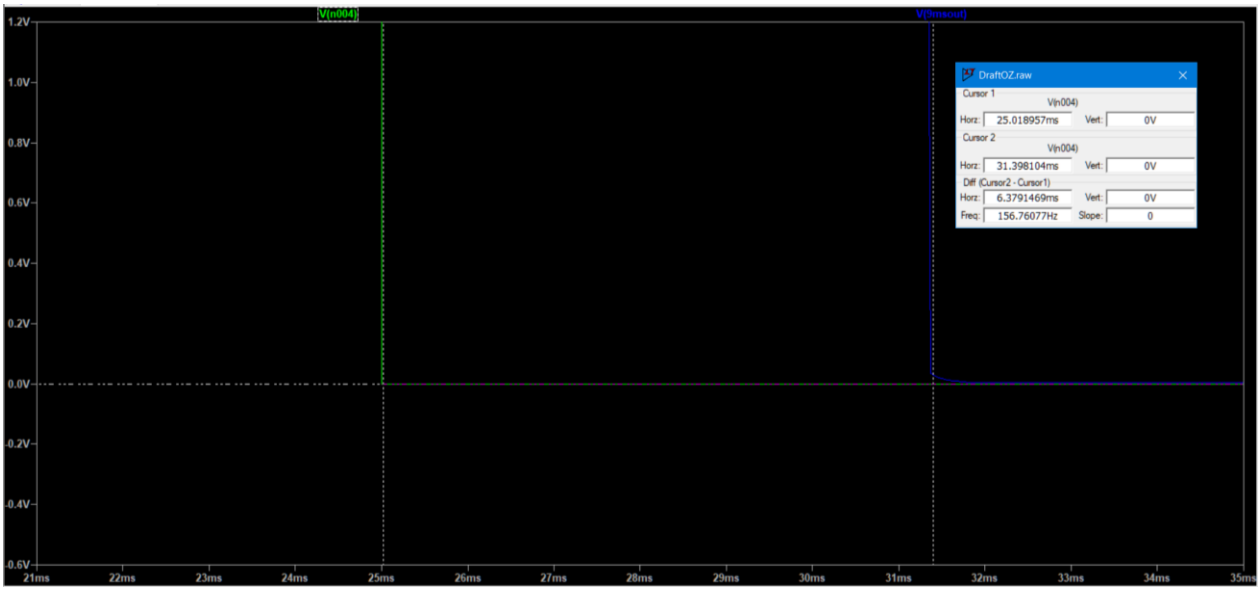

Figure 9: Delay of the Second Comparator OPAMP is 6.4 ms

Delay of the first integrator OPAMP is shown in Figure 10. The desired delay was 2ms. And the simulation result was satisfactory.

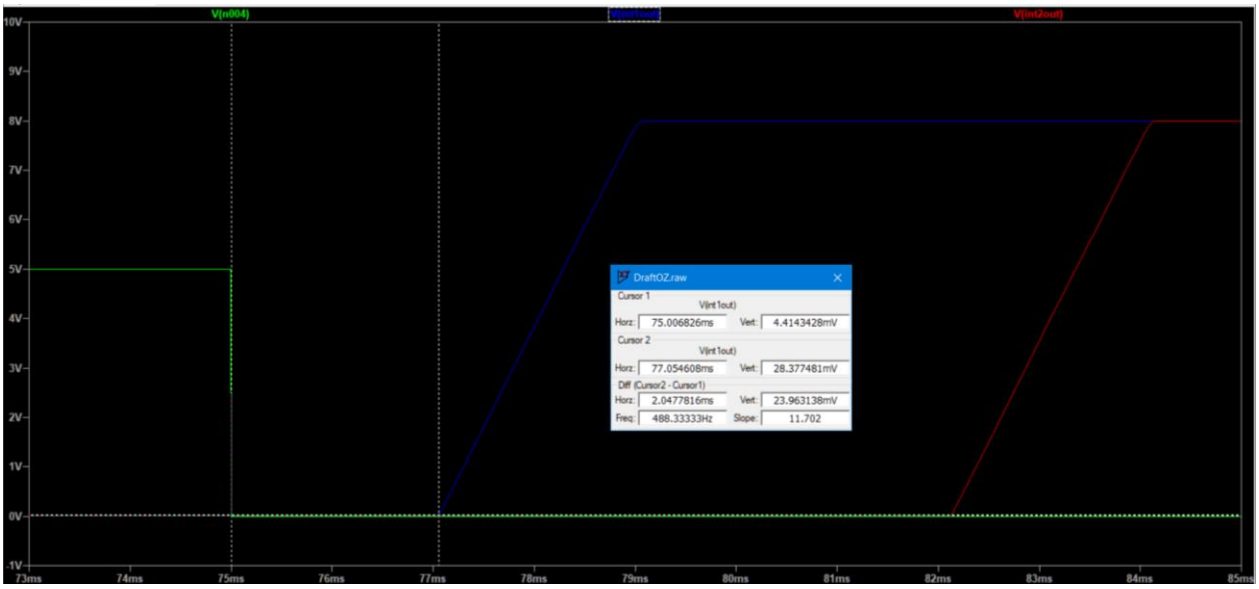

Figure 10: Delay of the First Integrator OPAMP is 2.04ms

Delay of the second integrator OPAMP is shown in Figure 11. The desired delay was 9ms. And the simulation result was satisfactory.

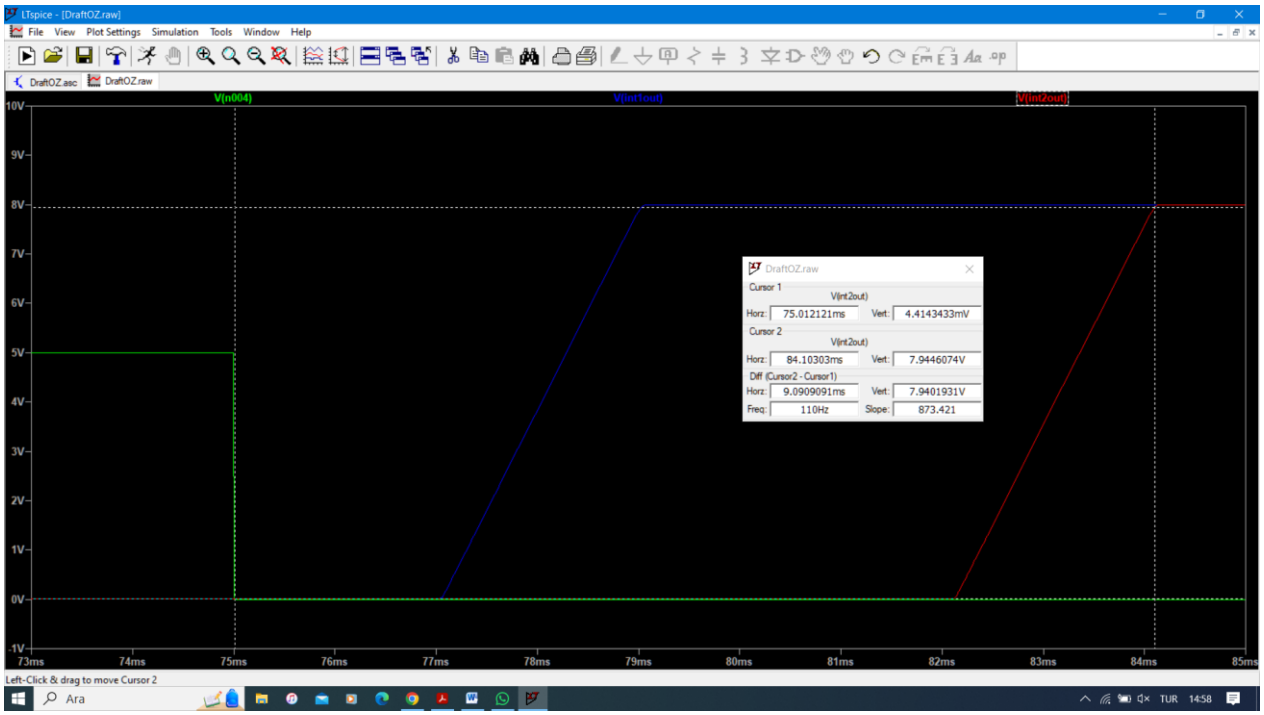

Figure 11: Delay of the Second Integrator OPAMP is 9.09ms

In the Figure 12, the skew line from the first integrator OPAMP can be seen.

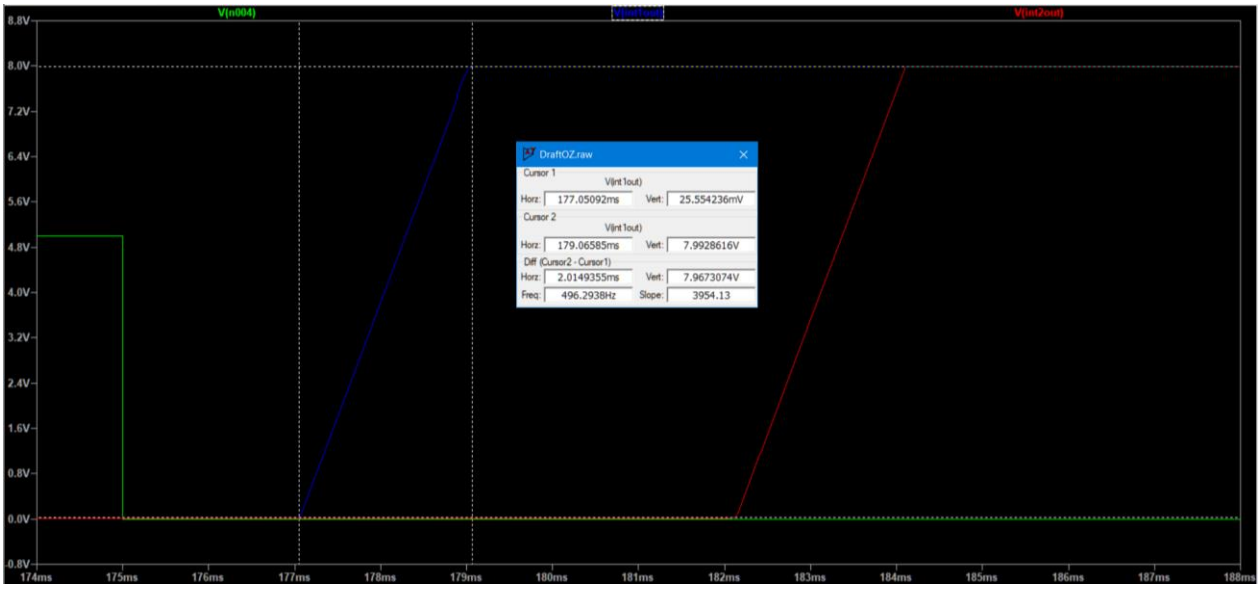

Figure 12:First skewed waveform created by the first integrator OPAMP with slope= 8V/2ms

In the Figure 13, the skew line from the second integrator OPAMP can be seen.

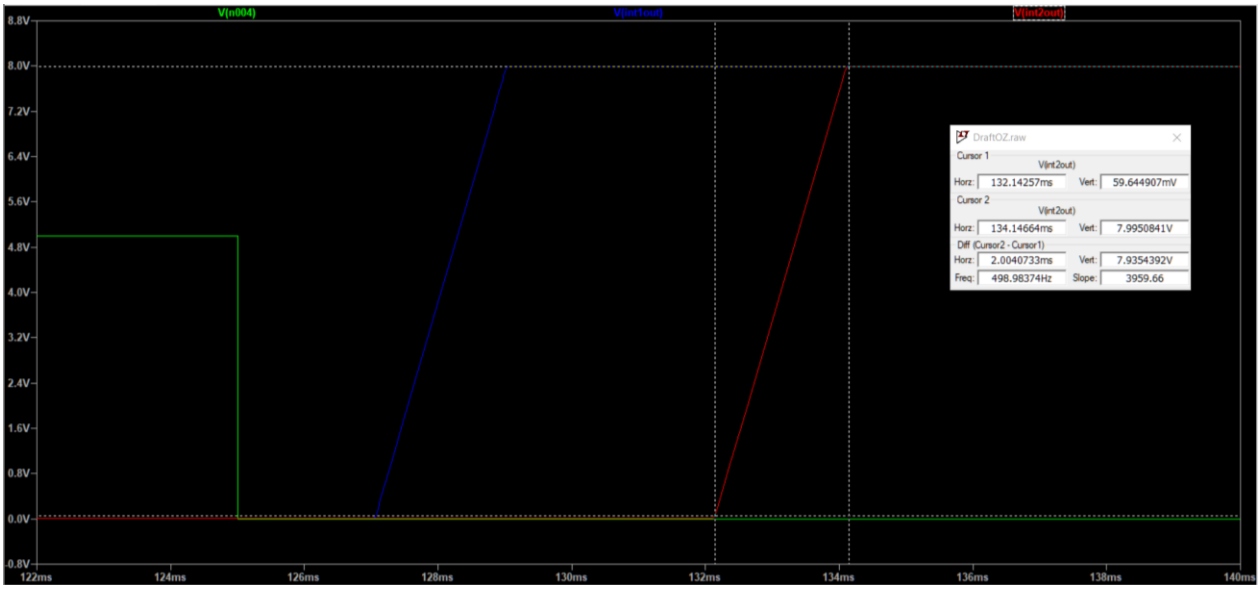

Figure 12:Second skewed waveform created by the second integrator OPAMP with slope= 8V/2ms

In Figure 13, the output of the subtractor OPAMP and the input signal can be seen.

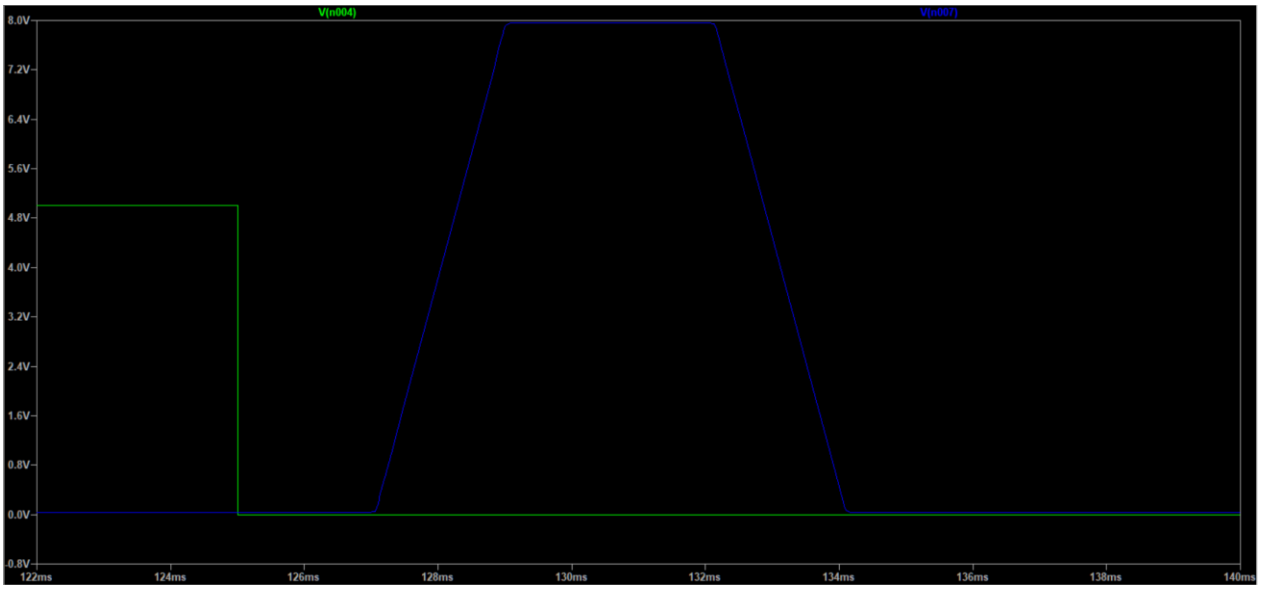

Figure 13: Output Signal from Subtractor OPAMP and Input Signal

The detailed results of the output of the subtractor OPAMP can be seen in the following figures.

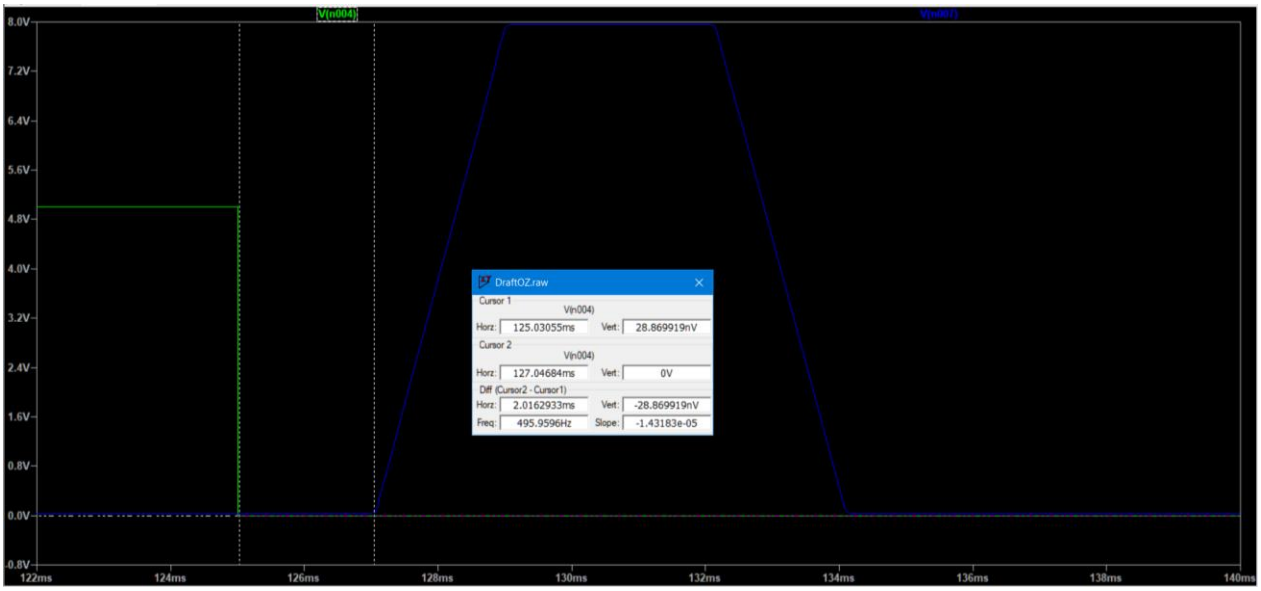

Figure 14: $\Delta t0$=2.01ms

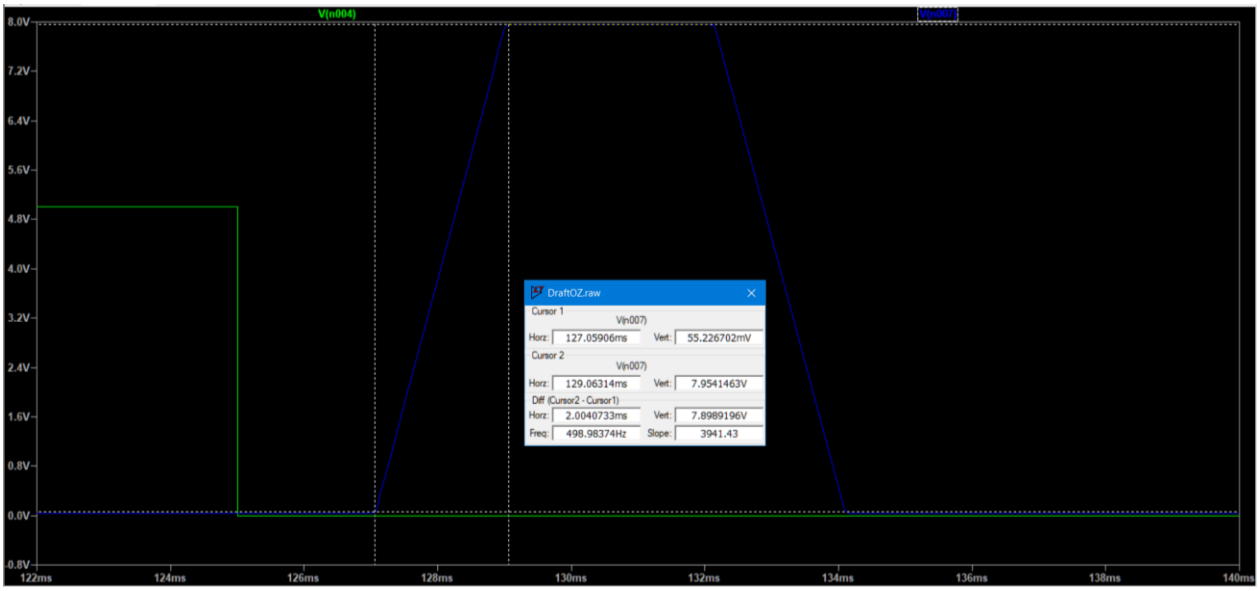

Figure 15: $\Delta t1$= 2.004ms

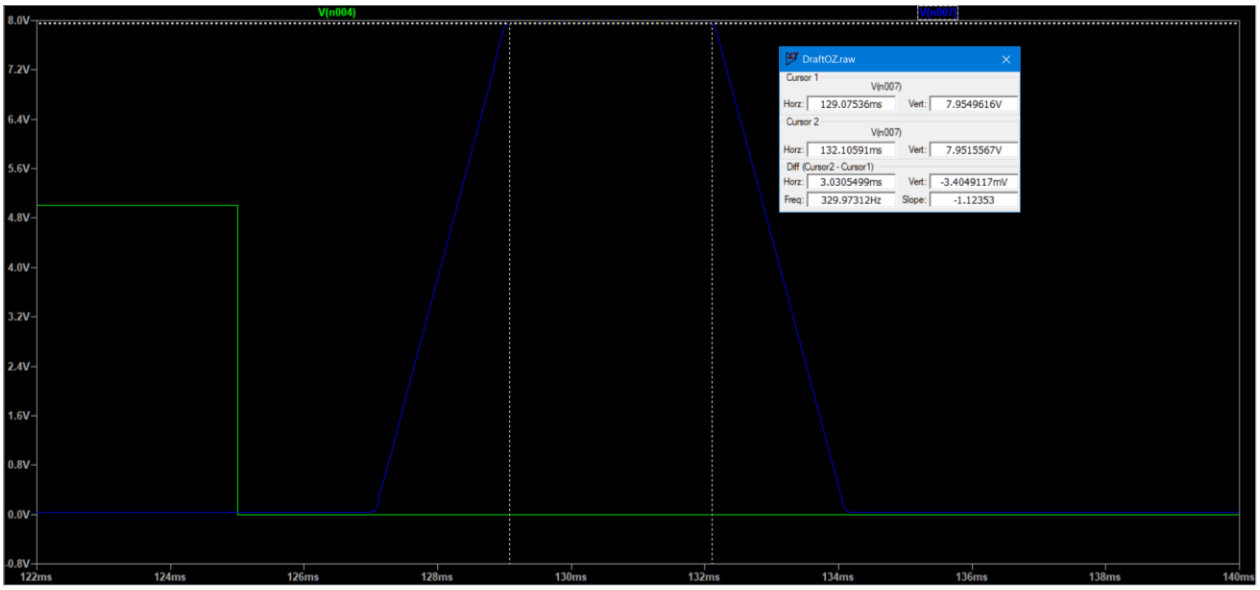

Figure 16: $\Delta t2$= 3.03ms

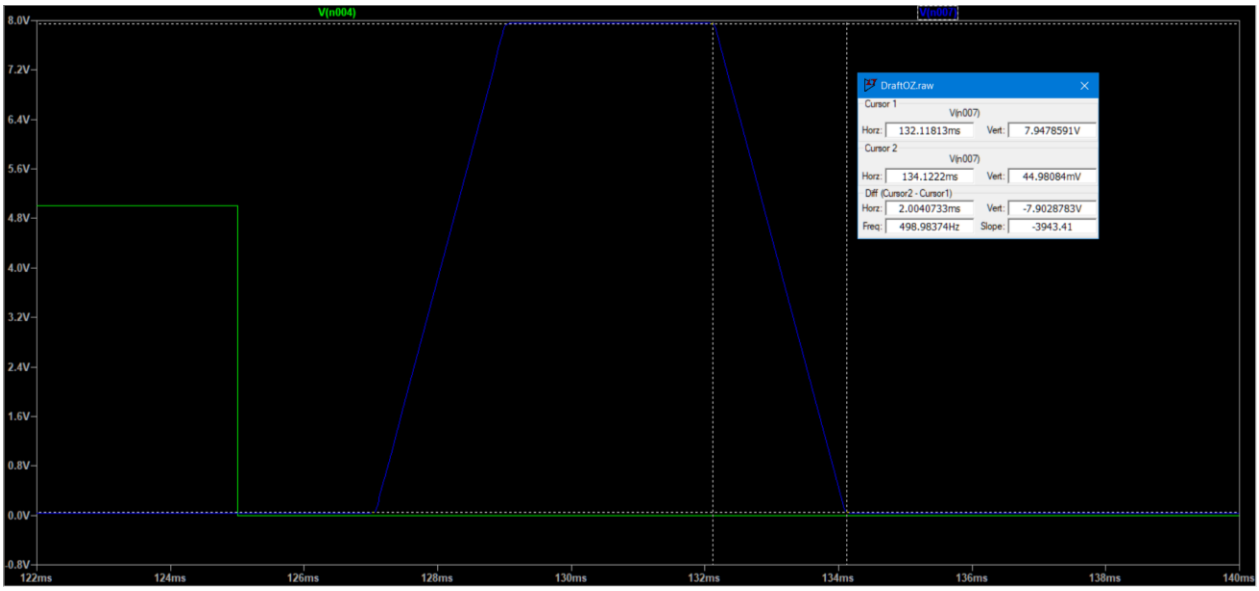

Figure 17: $\Delta t3$= 2.004ms

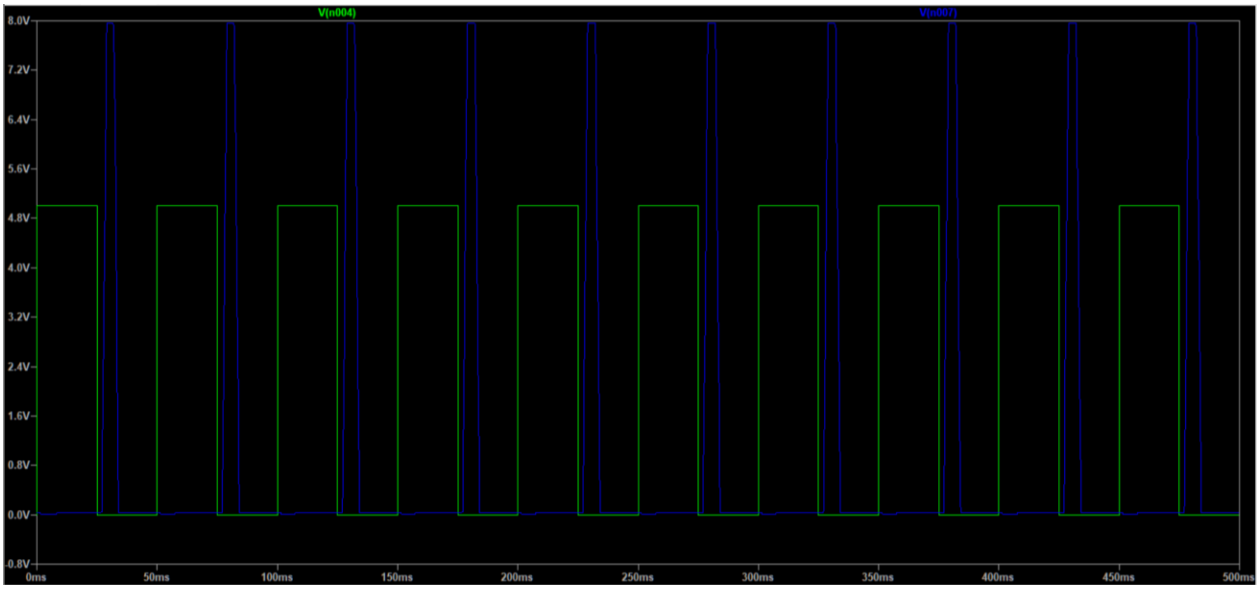

Figure 18: Output Signal from Subtractor OPAMP and the Input Signal

Note that there are delays due to integrator and comparator circuits. The final delays were measured after the integrator circuit in Figures 10 and Figure 11, not after the comparator circuits.

The summary of software simulation results and errors can be visible in Table 1.

	$\Delta t0$	$\Delta t1$	$\Delta t2$	$\Delta t3$
Desired Values	2(ms)	2(ms)	3(ms)	2(ms)
Result Values	2.01(ms)	2.004(ms)	3.03(ms)	2.004(ms)
Error Percentage	0.5	0.2	1.5	0.2

Table 1: Desired Values, Result Values ,and Error Percentage Table

The results are satisfactory since all of the error percentages were lower than the limit 10%.

Hardware Lab:

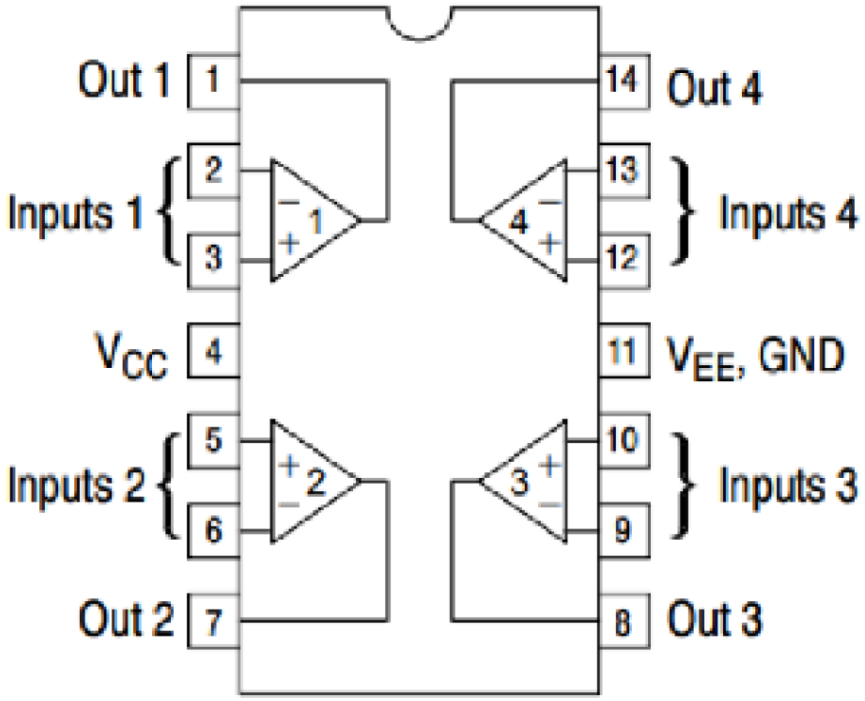

Figure 19: Integrated Circuit of LM324 OPAMP

There are two LM324s employed, and 9.5V is provided to them. The specified Vcomp is 2.5 V. Due to the absence of exact values for components in the lab, minor adjustments have been made to the component values. The signal generator produces a square wave with 2.5 V pp, 20 Hz, and 1.25V offset voltage.

The hardware circuit can be seen in the Figure 20.

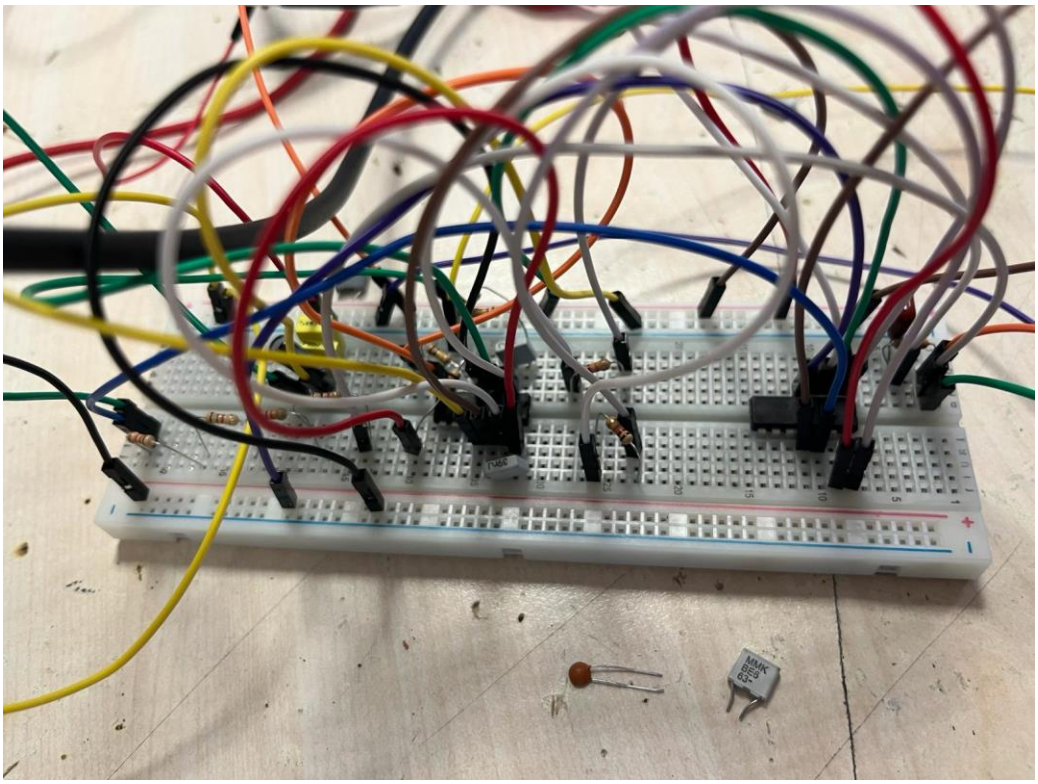

Figure 20: The Hardware Circuit

Integrator OPAMPs' output signals are examined and showed in the Figures 21,22.

Yellow lines are for the first integrator and blue lines are for the second integrator.

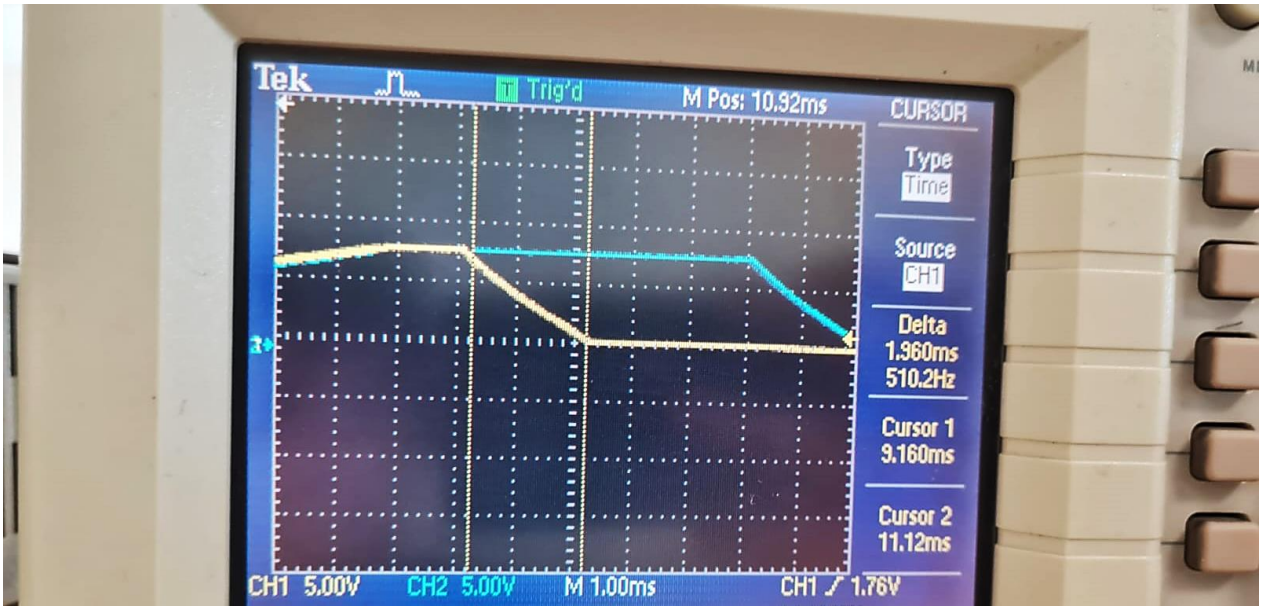

Figure 21: Skew Line from the First Integrator and Δt is 1.96ms

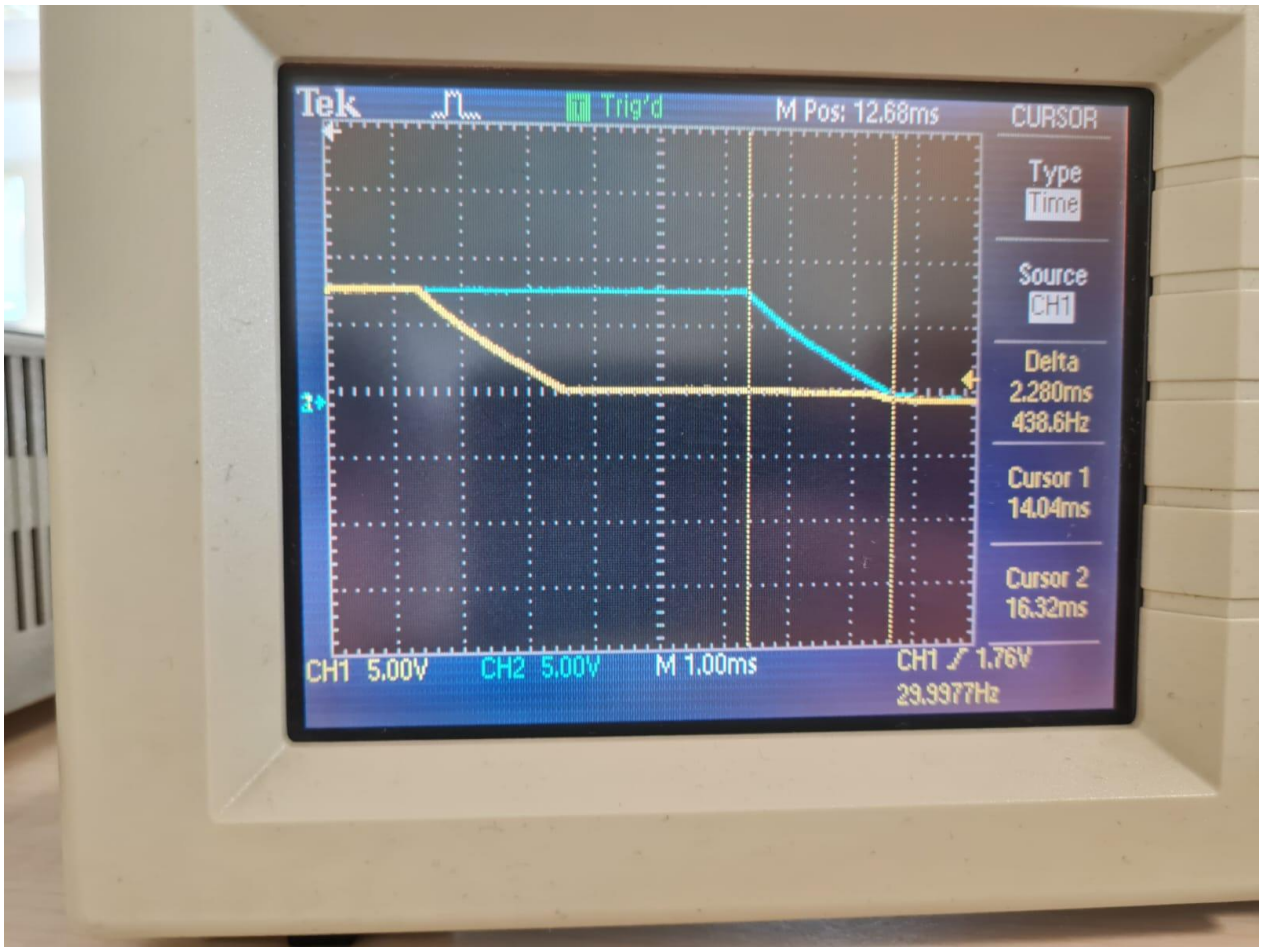

Figure 22: Skew Line from the Second Integrator and Δt is 2.28 ms

In the Figures 23,24 ,and 25, the output signal of the subtractor OPAMP and input signal can be seen.

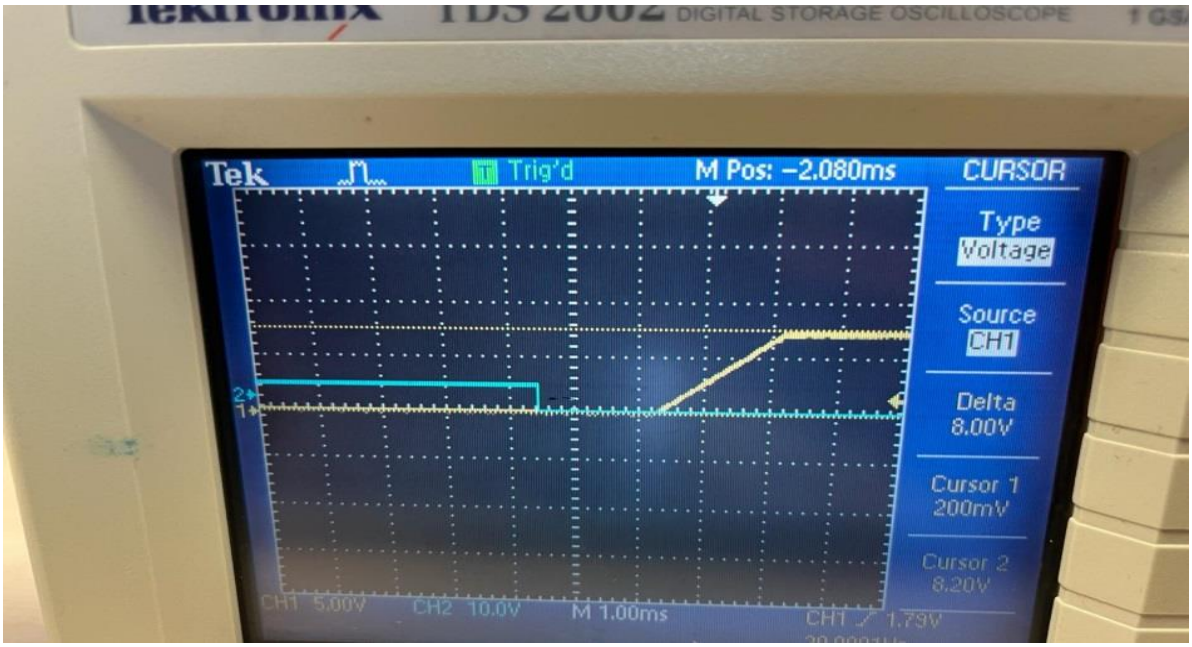

Figure 23: Peak Value of the Output Voltage is 8V

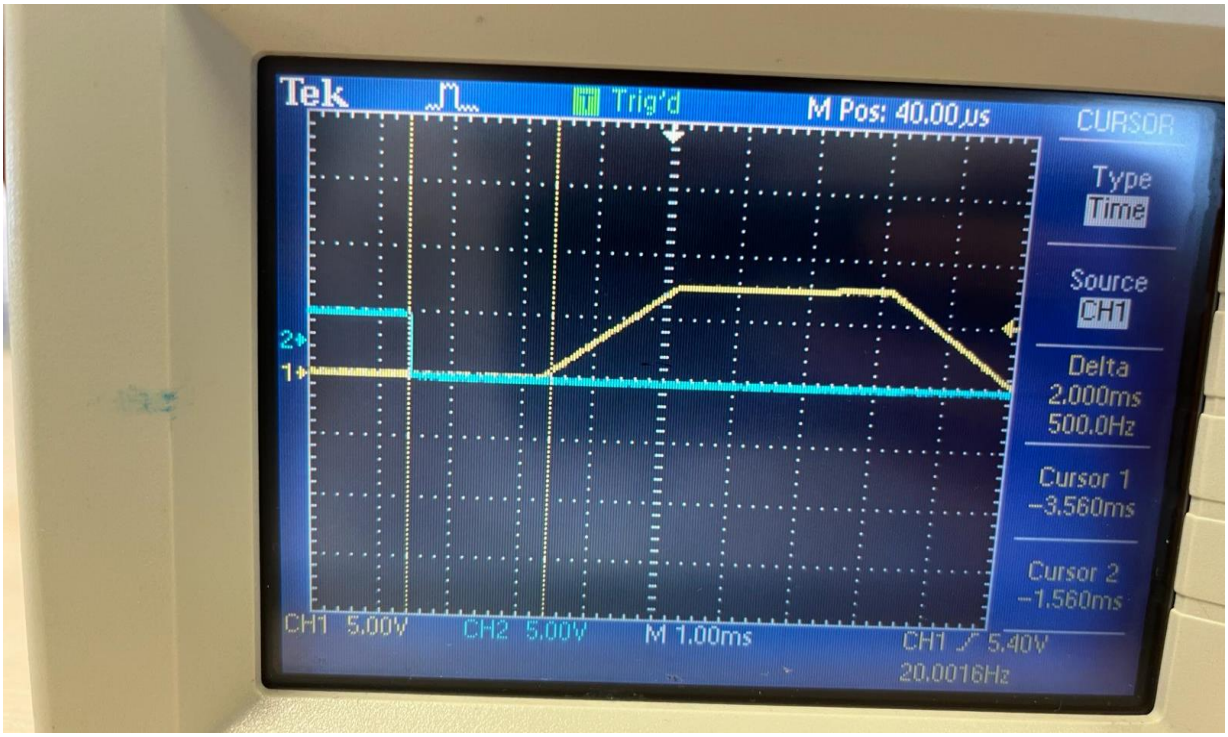

Figure 24: $\Delta t0$ = 2ms

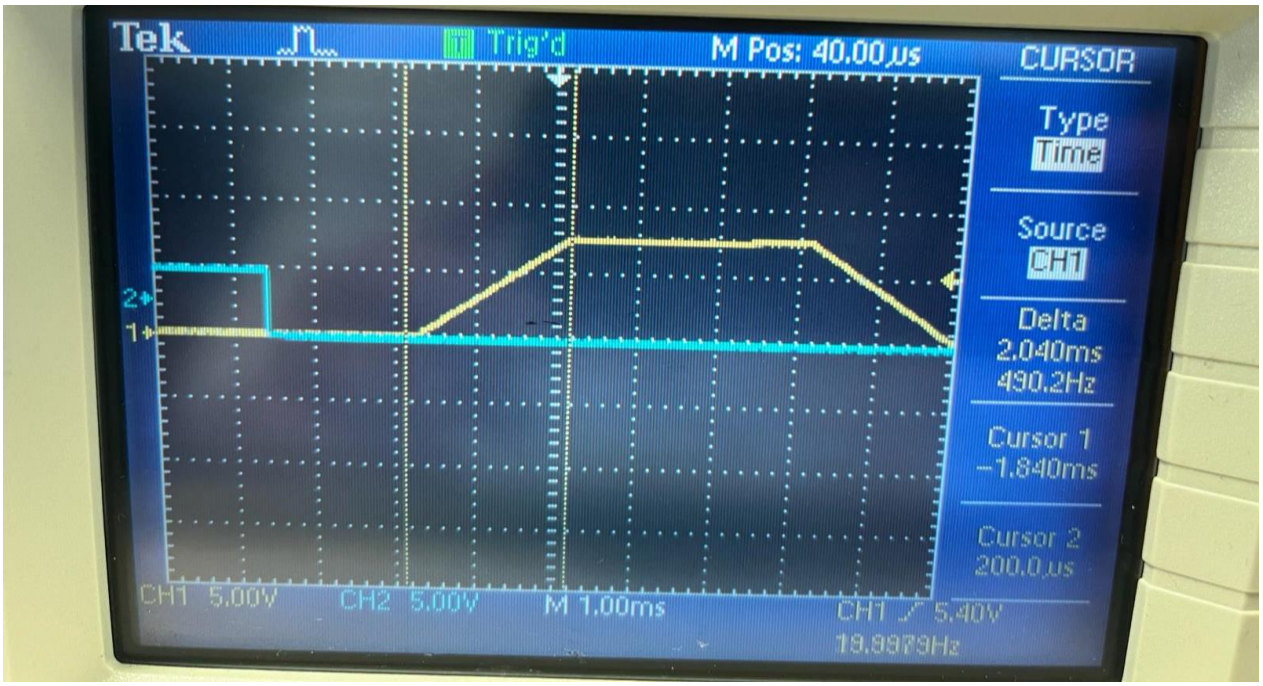

Figure 25: $\Delta t1$ = 2.04ms

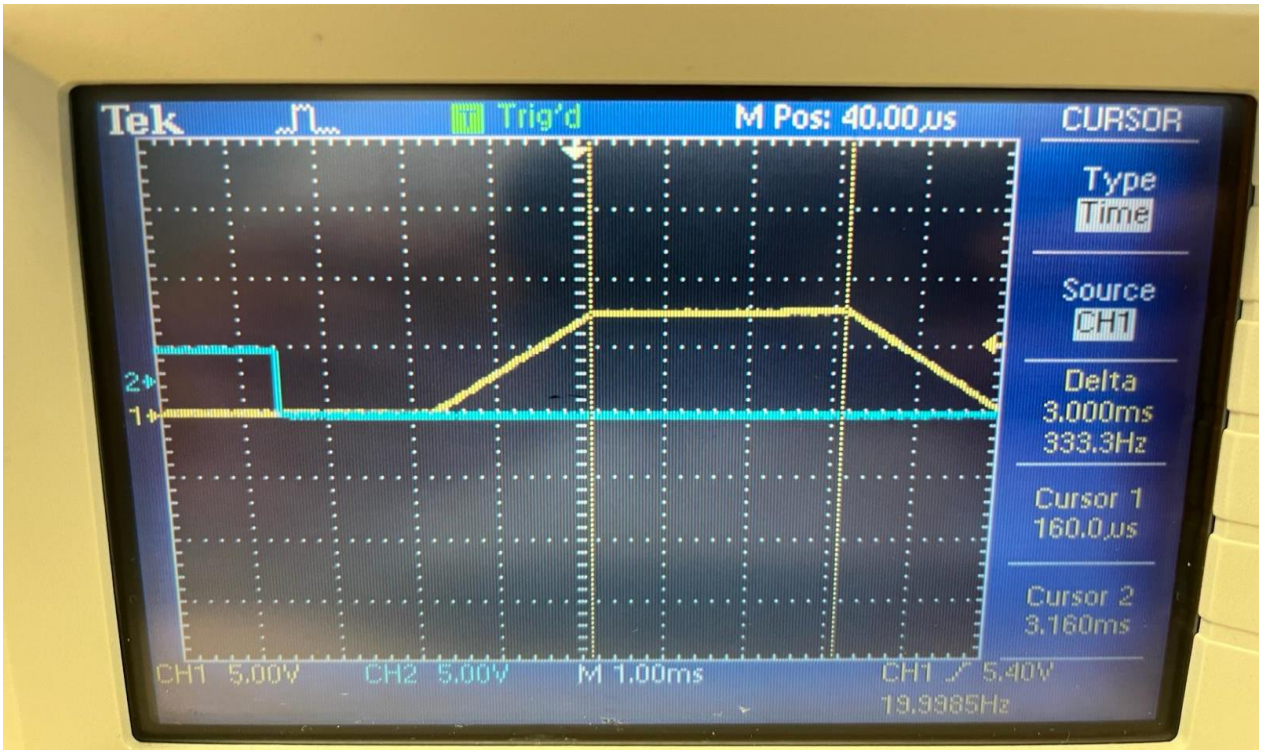

Figure 26: $\Delta t2$ = 3ms

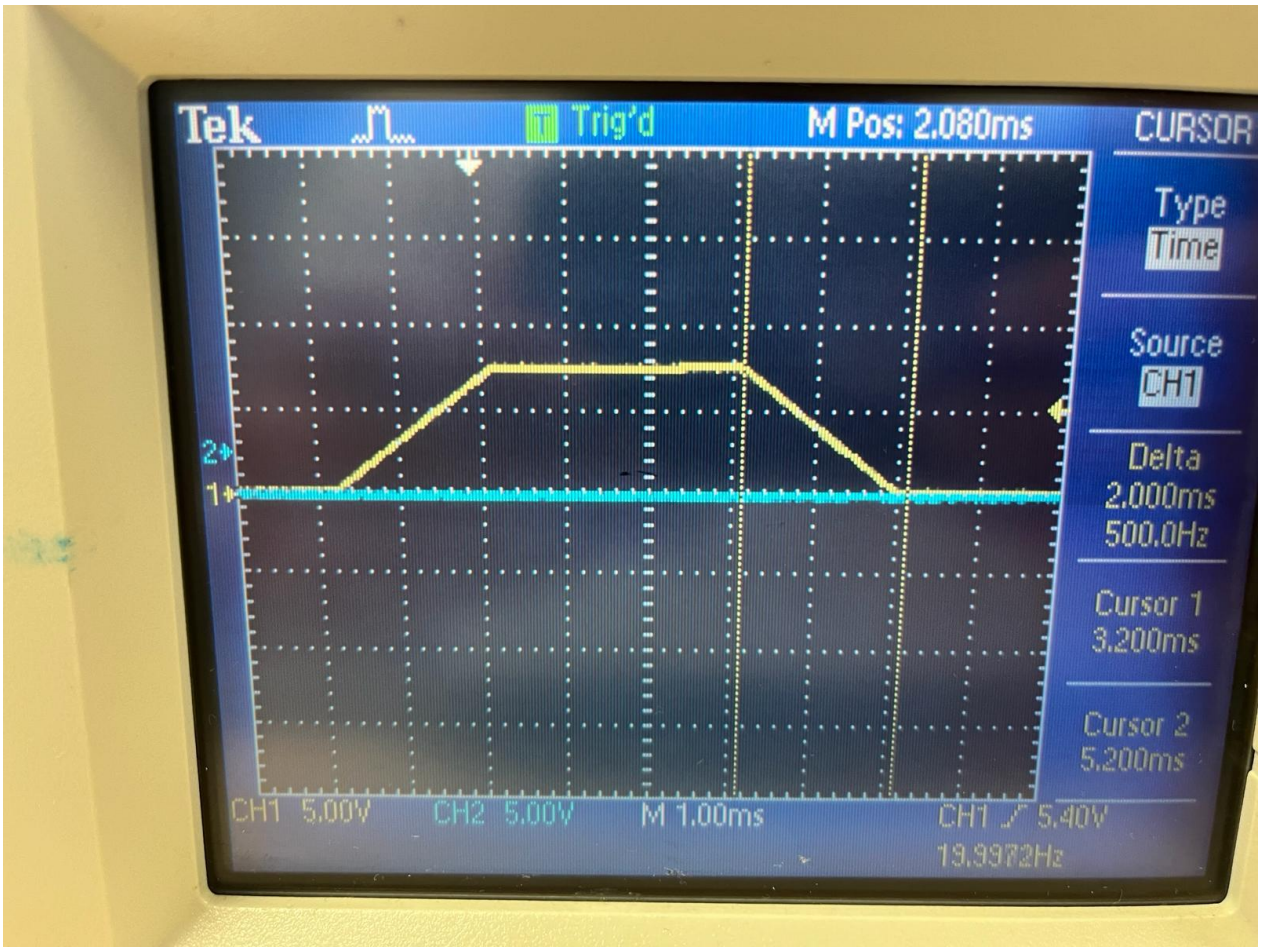

Figure 27: $\Delta t4$ = 2ms

	$\Delta t0$	$\Delta t1$	$\Delta t2$	$\Delta t3$
Desired Values	2(ms)	2(ms)	3(ms)	2(ms)
Hardware Values	2(ms)	2.04(ms)	3(ms)	2(ms)
Error Percentage	0	2	0	0

Table 2: Desired Values, Hardware Values ,and Error Percentage Table

The results are satisfactory since all of the error percentages were lower than the limit 20%.

Conclusion:

The objective of this laboratory experiment was to generate peak voltage of 8 volts trapezoidal waveform using a square input signal with a peak voltage of 5 V. Three configurations of operational amplifiers (OPAMPs), namely comparator, integrator, and subtractor, were utilized to accomplish this task. Nevertheless, discrepancies and inaccuracies surfaced in both software and hardware components. Software errors may have arisen due to the selection of standard resistor and capacitor values, which may not precisely align with the calculated values. Nonetheless, all discrepancies remained below 10%. Smaller errors occurred in the Hardware results. Moreover, Lab 3 achieved success in instructing and enabling practice in the manipulation of a circuit according to specific objectives.