Zhe **Li**

FPGA Engineer

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"Talk is cheap. Show me the code."

Education

Southeast University — *Nanjing, China*

M.Eng. in Electronic Engineering — *Sep. 2021 - Jun. 2024*

- Merit Graduate Student award, Transcom Microwave Scholarship

Southeast University — *Nanjing, China*

B.S. in Information Engineering — *Sep. 2017 - Jun. 2021*

- Merit Undergraduate Student award, Ye Jing and Liu Fang Scholarship
- National first price of TI Cup Undergraduate Electronics Design Contest (Top 2% of 50,000 participants)

Skills

EDA Tools	Vivado, HLS, Vitis, Wireshark, Questasim, Verdi
Programming	SystemVerilog, Chisel, TCL, Python, C/C++, Scala, MATLAB, LaTeX
Languages	English, Chinese

Experience

ByteDance Ltd. — *Shanghai, China*

FPGA Intern — *Sep. 2023 - Nov. 2023*

- Investigated packet scheduling algorithms and its' hardware implementation published in IEEE/ACM SIGCOMM, NSDI, etc.
- Designed a fully pipelined implementation of priority queue based on PIFO (SIGCOMM '16). Overcame the limitation of priority coding thus achieved 5x better timing performance than original PIFO design. The implementation was designed in SystemVerilog and tested with cocotb.
- Delivered a lecture about my design that was attended by 50+ engineers in RDMA NIC team.

Akuna Capital — *Shanghai, China*

FPGA Intern — *Jan. 2023 - Feb. 2023*

- Acquired in-depth understanding of FPGA development flow, low-latency system architecture, and fundamental knowledge of trading system.
- Implemented the ICMP and ARP protocols in network test chip. From dissecting Ethernet and IP packets to assembling IP and Ethernet frames. Designed and verified with SystemVerilog and SVA. Wrote Python scripts to configure registers.
- Successfully passed on the first attempt in the FPGA board bring-up process, and achieved the goal two weeks ahead of schedule.

Hesai Technology — *Shanghai, China*

FPGA Intern — *Jun. 2021 - Sep. 2021*

- Participated in the R&D of FMCW LiDAR. Responsible for the coding and debugging of various peripherals, including ADC, DAC, light switch, etc.
- On a collaborative effort with hardware engineers, successfully established the communication link between the laser probe and bottom house to transmit point cloud data.
- Implemented a 4096 points FFT algorithm with Vivado HLS, achieved 2x throughput rate than Xilinx FFT IP core after pipeline, throughput, resource and area optimization.

Research

Neural network implementation on Versal VCK190 board

Nanjing, China

Independent developer, Github — *Nov. 2022 - May. 2023*

- Developed pipelined systolic arrays based fully connected neural network in Chisel for digital predistortion.
- Parameterized the configuration including number of layers, neurons, fixed-point position, and activation functions.
- Used URAM for Sigmoid function and DSP58 as processing element.
- Running at 245.76 MHz with polyphase ability to linearize 983.04 MHz baseband bandwidth.
- Achieved nearly the same performance as software floating point models.

Memory polynomial hardware implementation

Nanjing, China

Independent developer, Github — *Sep. 2022 - Nov. 2022*

- The only open-source digital predistortion algorithm hardware implementation in Github.
- Developed the implementation with configurable memory depth and LUT depth in SystemVerilog.
- Achieve nearly 20 dBc ACPR reduction for GaN Power amplifier.
- Successfully passed on the first attempt in the FPGA board bring-up process, and achieved the goal two weeks ahead of schedule.

ADC-DAC radio frequency signal processing platform

Shanghai, China

Core developer — *Jun. 2021 - Sep. 2021*

- Built radio frequency signal processing platform with Xilinx ZCU102/VCK190, ADI AD9173 RF-DAC, and AD6688 RF-ADC
- Used JESD204B protocol and GTH transceiver to establish the communication link between converter and FPGA.
- Used NoC and DMA in Versal to transfer baseband DAC/ADC data from/to DDR, used LwIP in CIPS to make network connection with MATLAB (as host) in PC.

Paper

AI-based RF-Input RF-Output Digital Predistortion for RF Power Amplifiers with Neural Network FPGA Implementation — Sep. 2023

Zhe Li, Yucheng Yu, Peng Chen, Ziming Wang, and Chao Yu*

IEEE Transaction on Microwave Theory and Techniques (Under Review)

A Digital Predistortion System Based on Versal ACAP — Jul. 2023

Zhe Li, Chao Yu* — Chengdu, China

2023 National Conference of Microwave Spectrum and Control System

Envelope Added Time-Delay Neural Network-based Digital Predistortion of Wideband Envelope Tracking Power Amplifiers — May. 2021

Zhe Li, Xueya Yi, Peng Chen, Xiao-Wei Zhu, Chao Yu* — Nanjing, China

2021 International Conference on Microwave and Millimeter Wave Technology