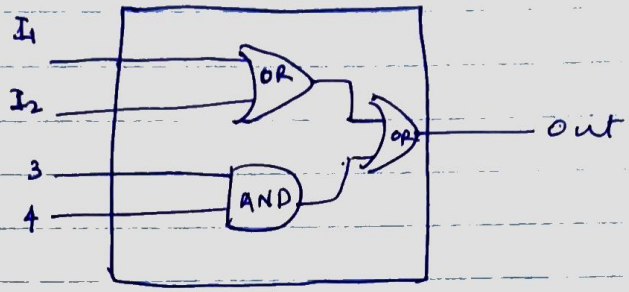
- PROJECT : ML model will be implemented on an FPGA, specifically targetting the MNIST dataset. This model will inherently be accelerated on the FPGA.

MNIST dataset - handwritten digits.

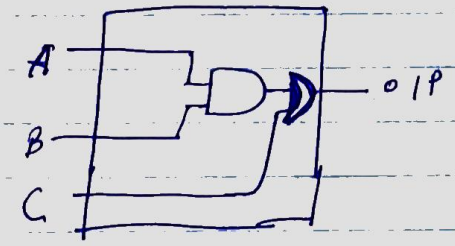
EPGA : Field Programmable Gate Array



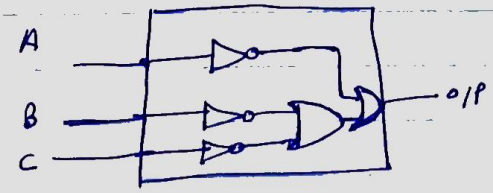

All gates can work parallely on the same dataset.

FPGA programming - verilog lang.

→ O/P = A.B + C



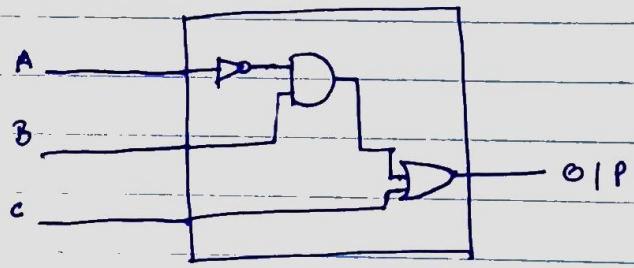

→ O/P = $\bar{A} + \bar{B} + \bar{C}$

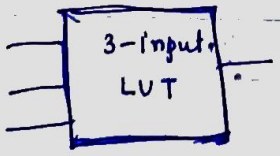


| A | B | C | OUT |
|---|---|---|---|
| 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |

→ $OUT = (\bar{A} \cdot \bar{B}) + C$

$= (\bar{A} \cdot B) + C$



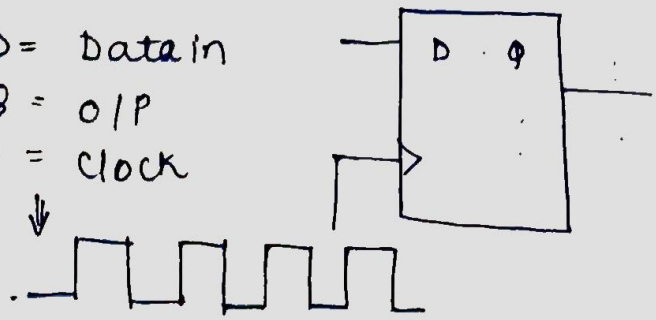

LUT: Look up Table

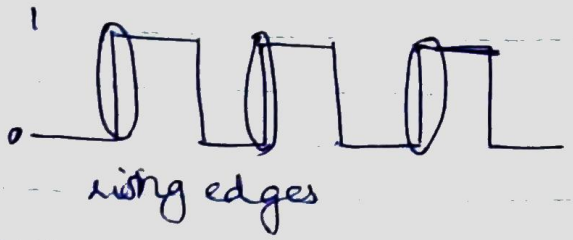
→ **D flip flops in FPGA**

D = Data in

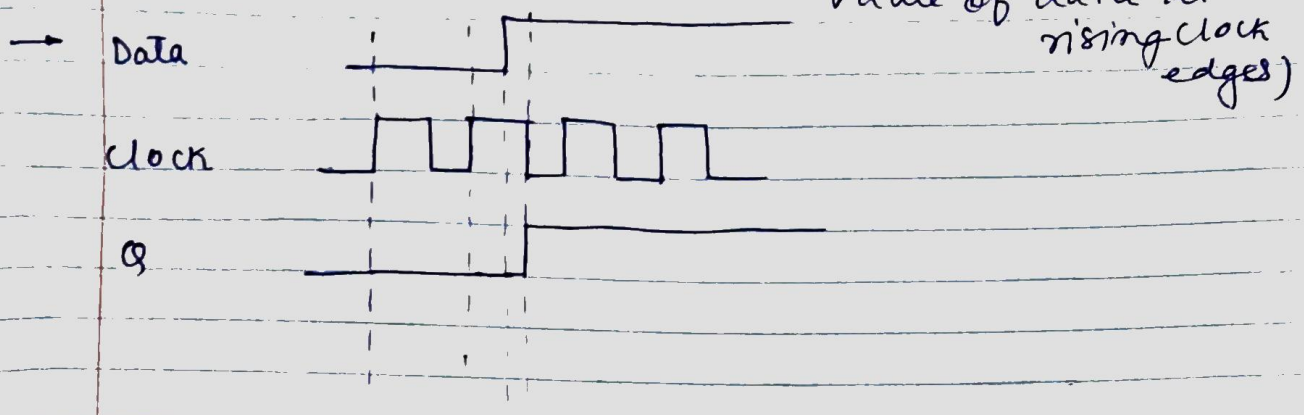
Q = O/P

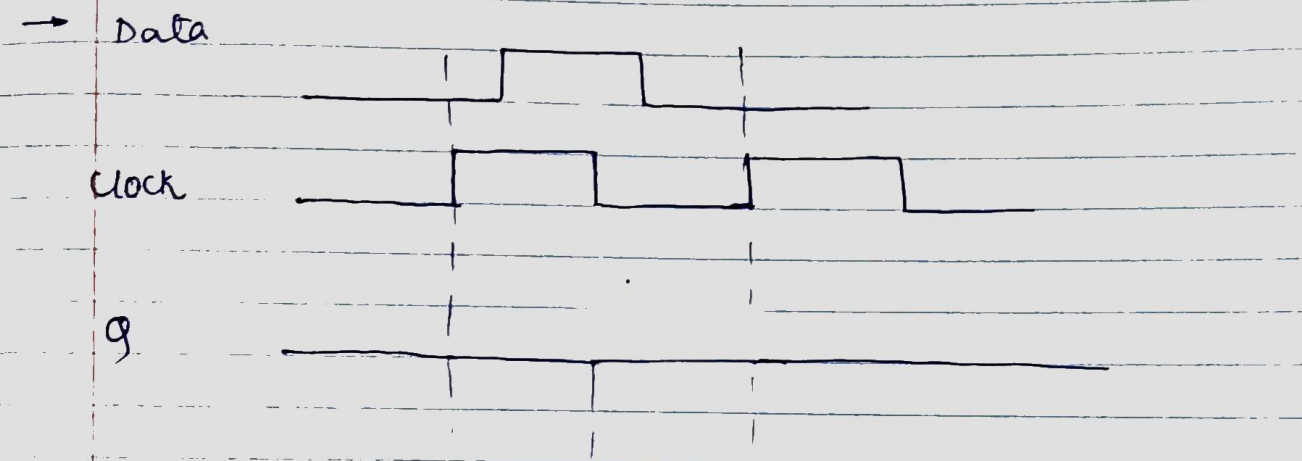
> = Clock

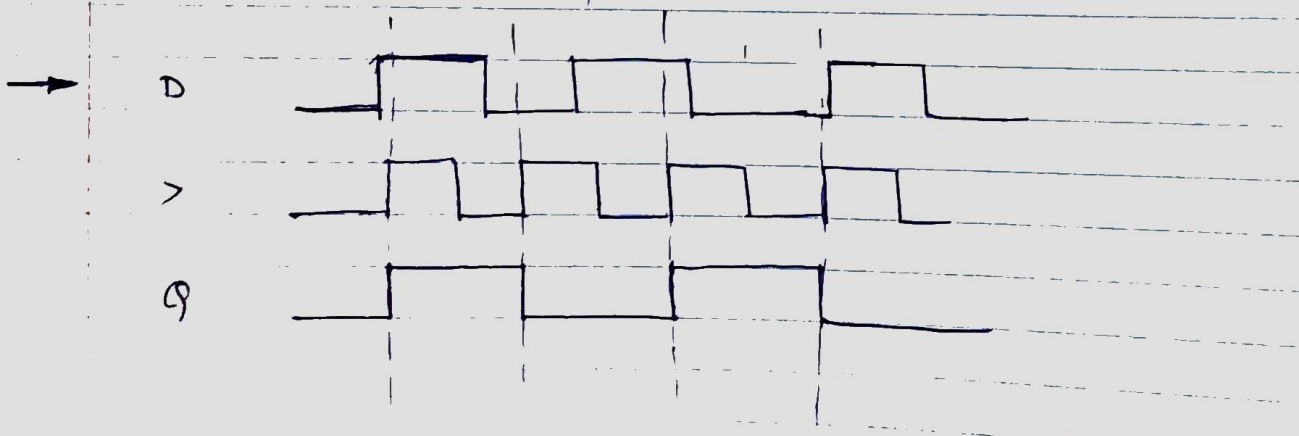





(check the instantaneous value of data at rising clock edges)



- **Two Flip Flops**