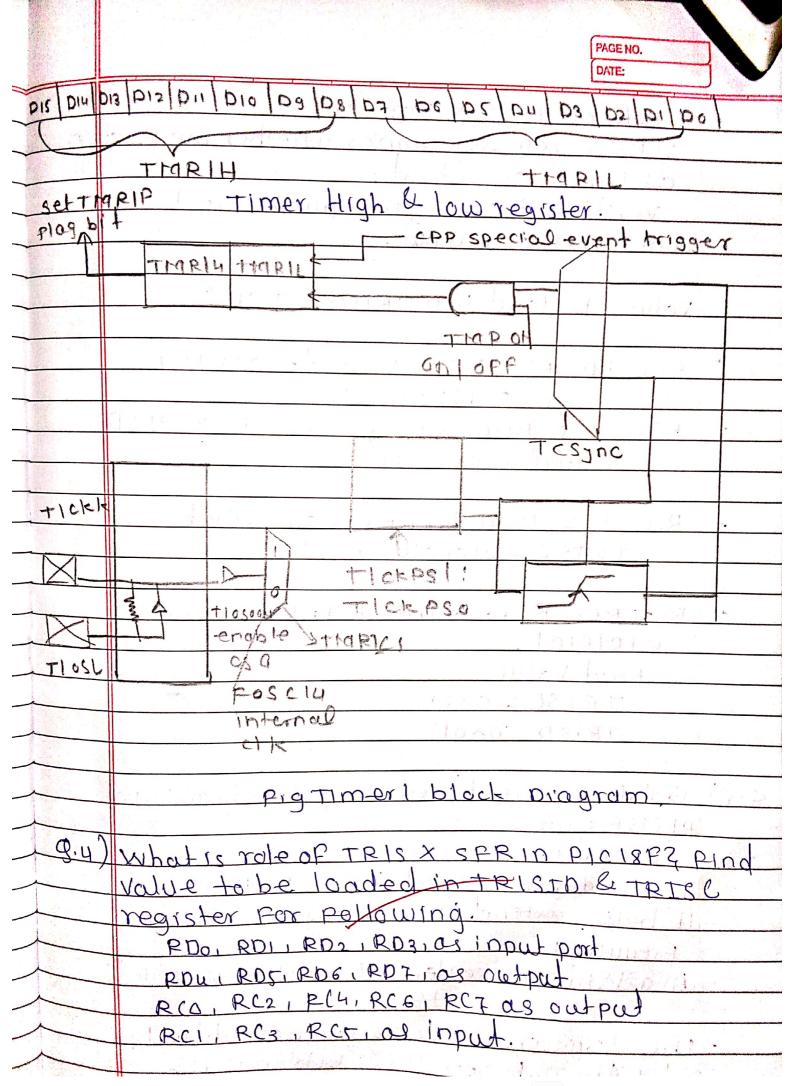
PAGE NO. Assignment No:-2 g. 1) Name SPRS associated with each TIO part of PTCI8F What is role of PORTX SFR? SPRS associated with the post in PICISF-In picisf series, each 110 postis controlled by Serveral special function register. 1) PORT -> Register -> stores actual 110 date oppost. 2) TRISX Register -> configures each pin ageither input (1) or output (0). 3) LAT & Register > used for latching of Pralues to reduce read-modify write issue 9) ANSEL x Register -> copique pin as analog or digited. ROLE OF PORTX SPR-It act as buffer that stores current state of post. When reaching it show actual logic Level at pin & when witing it changes output value. 9.2) Calculate total delay generated by timero if (FFFI) H is loaded into it. Assume Crystal Prequency = 10 MHz. Given, constal freq = 10MHz Timer o prescaler=1 Timer OTS 18 bit Firmer load value = PPFIH (65521in decimal) - Timer clack Freg = Ftimer = Foscillator = 18 MH2 = 25 MHZ

-Timer clock period 2.5MH2 trount = 65536 - instial value = 65536-65521 delay = Tcount x +1 mer =15X0.4 =6Ms 9.3) Explain Working of PICISF +1 mer with help OF suitable diagram Timer is 16 bit timer bits 16 bit register is split into 2 bytes refer as traRIL & TraRIH -timer I can be programmed 16 bit mode only & unlike timer oit does not support & bit made, timer o it does not support & Timer I also has ticoH register in addition to trripe Flag bit goes high when THARIL OVERFLOW From FFFFTO 0000 timer 1 also has prescaler option builty only supports perctors of 1:1,1:2,1:481:8



DATE: > Role of TRIS X Register --trts x reg determines whether pin function as input or output. - Writing I configures pin as input & o configures as output. Values to load into TRISD & TRISC-RDO, RD, IRD2, RD3, as input -> TRISD= 00001111 =0x0F RBU, RDS, RDG, RD7 as output ->TRISD Remains agoalli RCO, RC2, RC4, RC6, RC7, as output -TRTS C = 010/010/ = 0x55 RCI, RC3, RCT. as input-TRISC remains 01010101 Find Value-TRISC= 0X55 TRISD - OXOF 9.5) Explain in detail presculing & posts caling of PICISF timer. > prescaler-- It divides input clock before reeding it to Himer - It helps extend timer range by reducine Frequency - Available prescaler value -1:2,1:4,1:8,1:6 The druision Pactor is programmble typicould through specific bite in times control

PAGE NO. DATE: register. A higher prescaler value result in slower Hmor increment rate, which is useful for measuring longer duration but reduce timers resolution \* post-scal-er-It operates after time counting register & Frequency of intermosph generation by dividing no of times overplow required to trigger an interrupt. similar to prescaler, postscaler division Pacter is programmble via specific bit in times control register. teg-Timer in PICL8FUTTO allow For a posts culer setting ranging from 1:1 to 9.6) Drag format or to coH register & explain fundianality of each bit PSA TOPS TOPS Hame TrapooH TOSBIT TOCS TOSE Big. Formal of to cott red THEROOH ( bit 7) - enable timero (1=0H30=0PP) to 88 tt (bit 6) -1 - 8 bit made, 0 = 16 bit tocs (bits)=1= external clk, o=internal (bitu) select edge for extercit

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Explain working of picisf timer o in 16 bit made with suitable diagram.  Timero-  It can be used as 8 bit or 16 bit timer  The 16 bit register of timer o is ascessed as hown  The 16 w byte & high byte as shown  register is called trapal.	F 1			4	,-	1		40
	Upolition Is control of the order of the order	The law byte ron is called thank & big	Tall the for the bull of the table of	The Is hit reals for the time of the police of the	It can be used as a bit or Is hit times	Timero-	mode with suitable diagram.	Explain Working of PICISP Homer Oin 1661

69 Can RA M0V1 180 440 +MO read Laoves 1110 of Hmer anj n-8-8-6 Jeg 13 ex F

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D 4 DIA DIS U 7 Di Pro Dio 0 High U 00 O 00 Do regis O 9 O 2 D P Ō Do

3

ROL

TRO