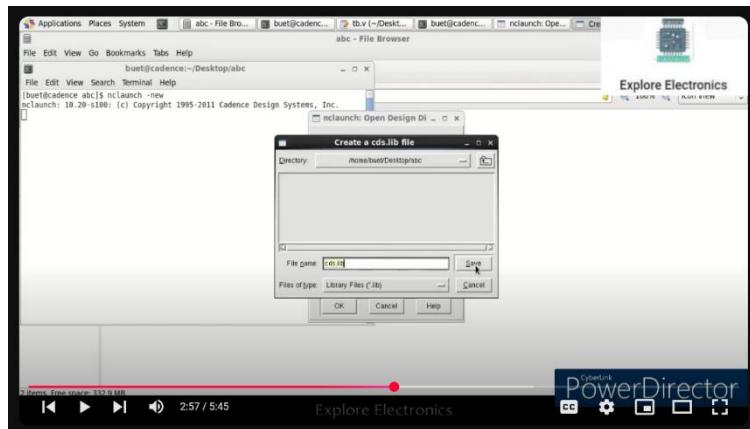
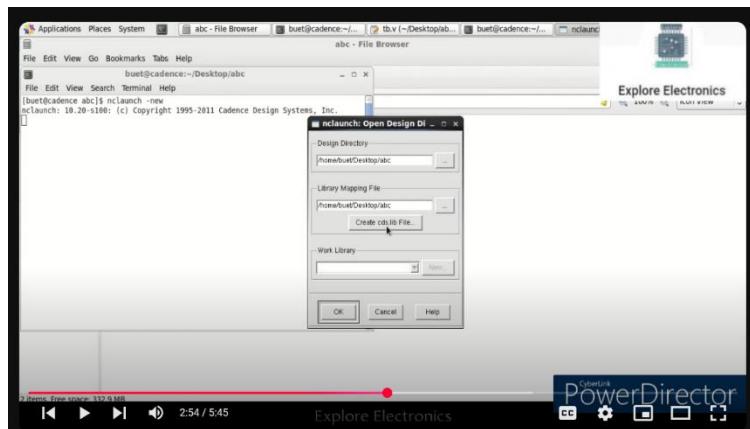
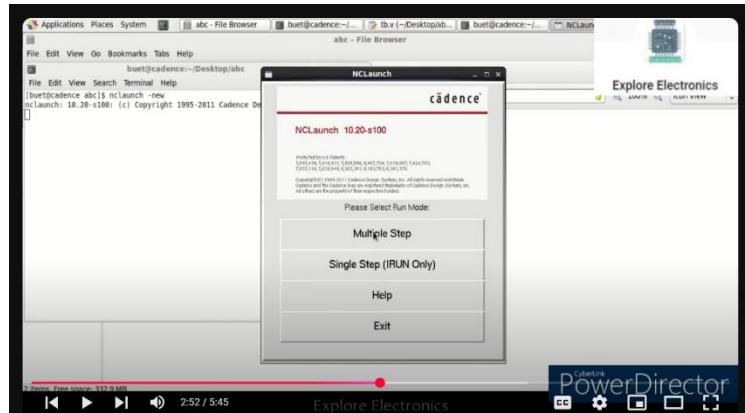
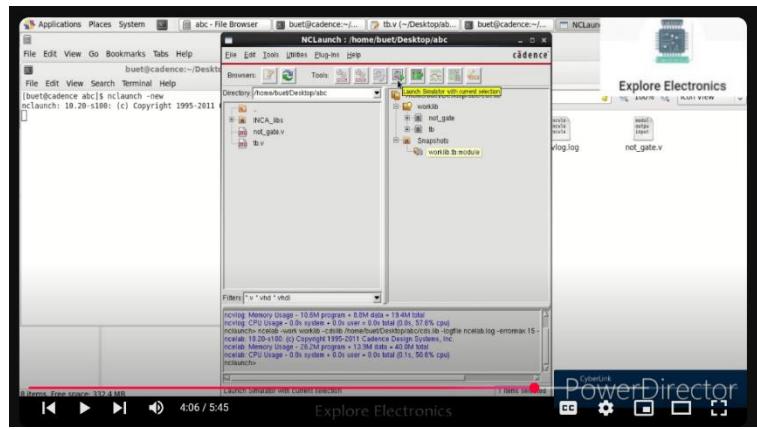
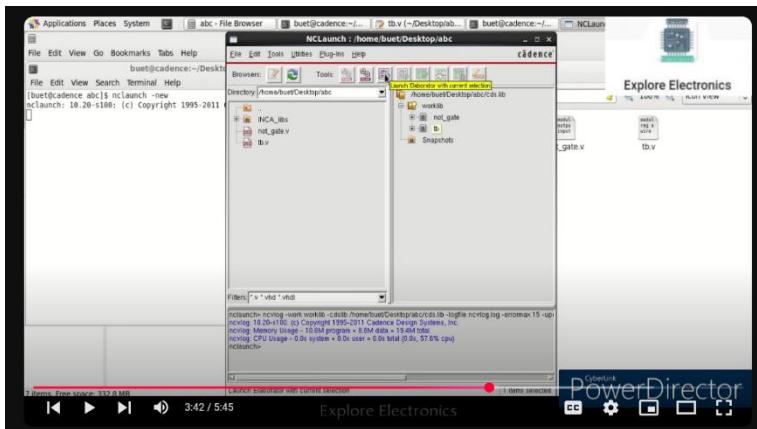
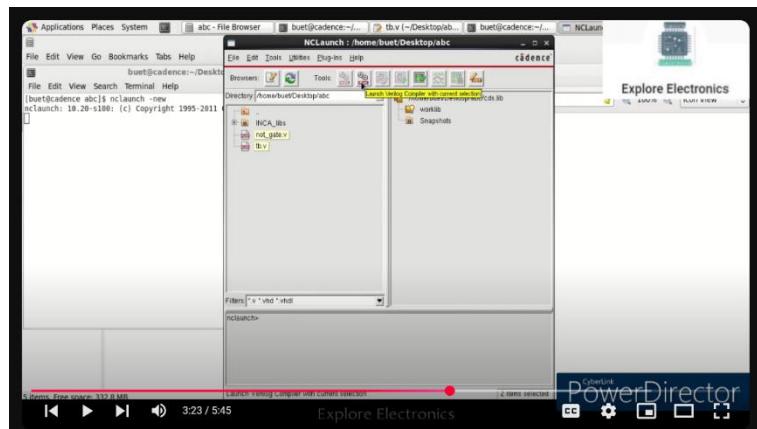
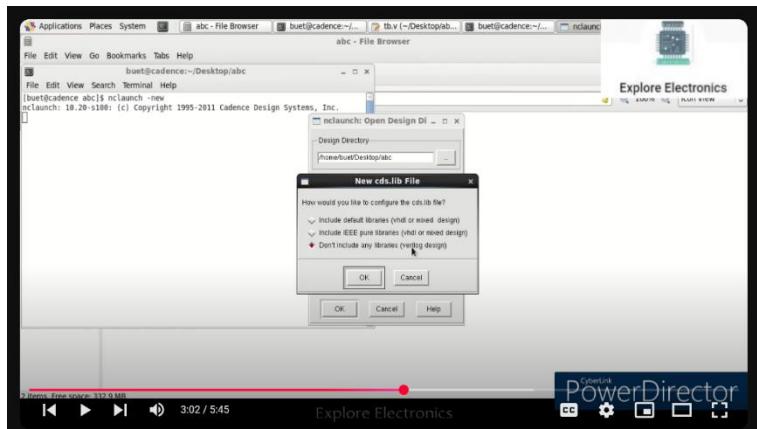


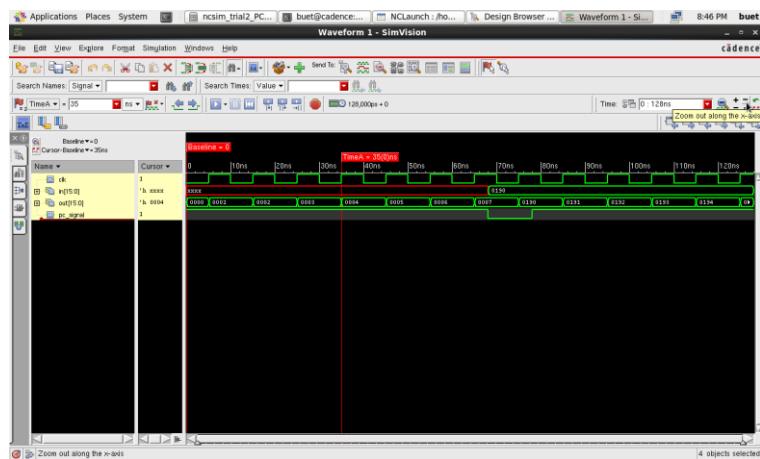
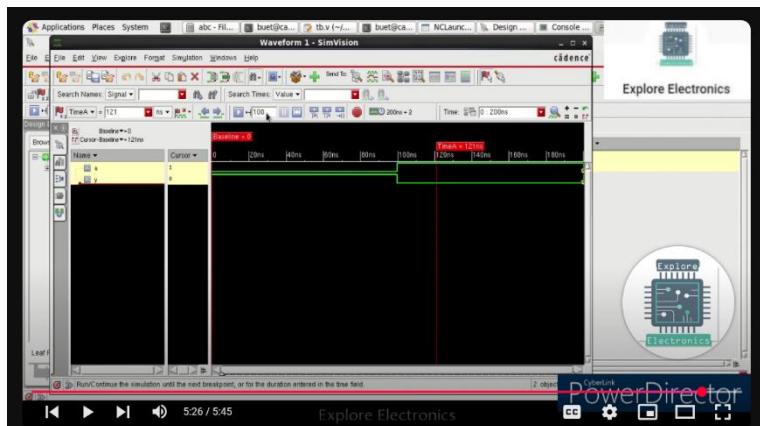
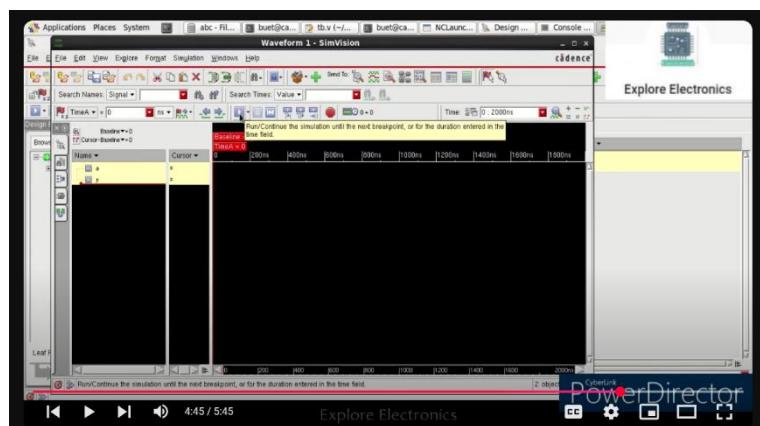
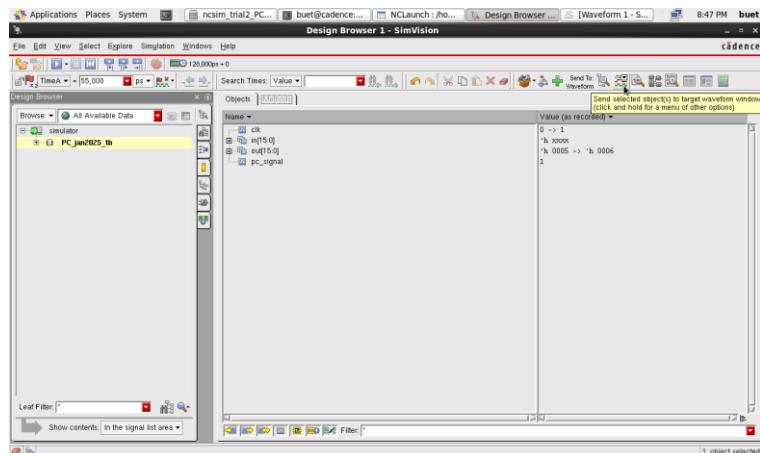
NCSIM STEPS

1. Source /home/install/cshrc
2. Nclaunch -new&
3. ===== window opens =====
4. **Multiple steps**
5. **Create cds.lib file**
6. **Save**
7. **Don't include any libraries**
8. **Ok**
9. ===== new window opens =====
10. Click both verilog files on lhs
11. Compile them using ncvlog
12. Click both compiled files on rhs
13. Elaborate them using ncelab
14. Only click elaborated testbench
15. Simulate it using ncsim
16. ===== new window opens =====
17. Click both files on lhs
18. **Send selected object to target waveform window**
19. ===== new window opens =====
20. Select all IO pins on LHS
21. Press the run simulation button

Create new folder (# don't leave space while naming folder / files), in that create 2 files – one for code and other for test bench, saves those files with .v extension, then open Terminal to invoke ncsim tool.

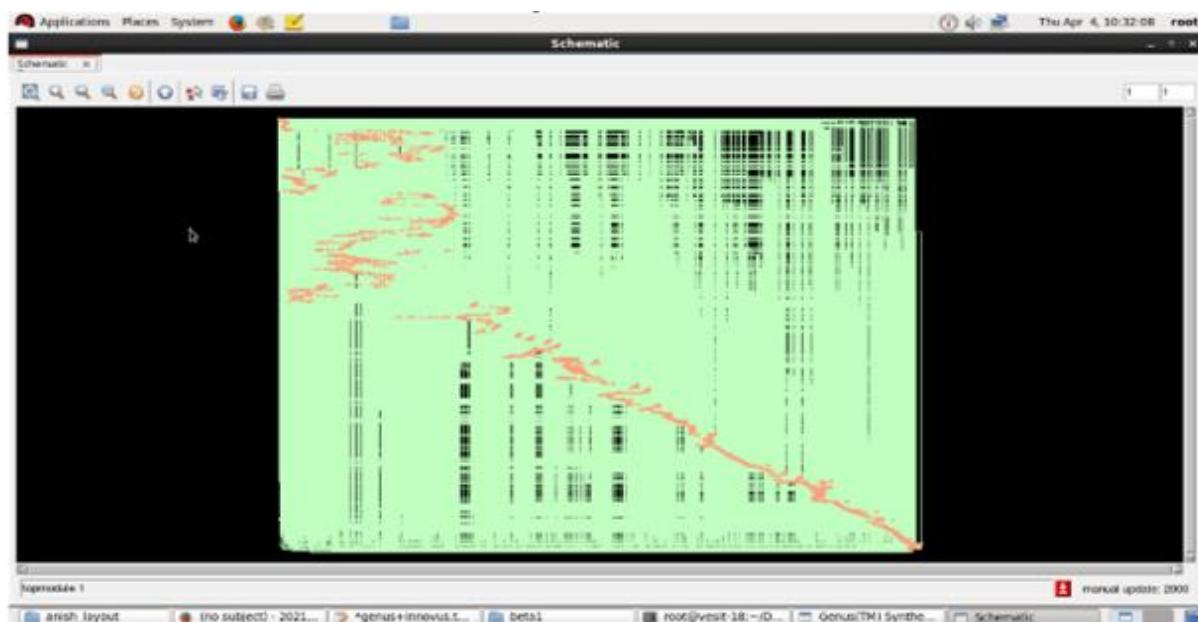






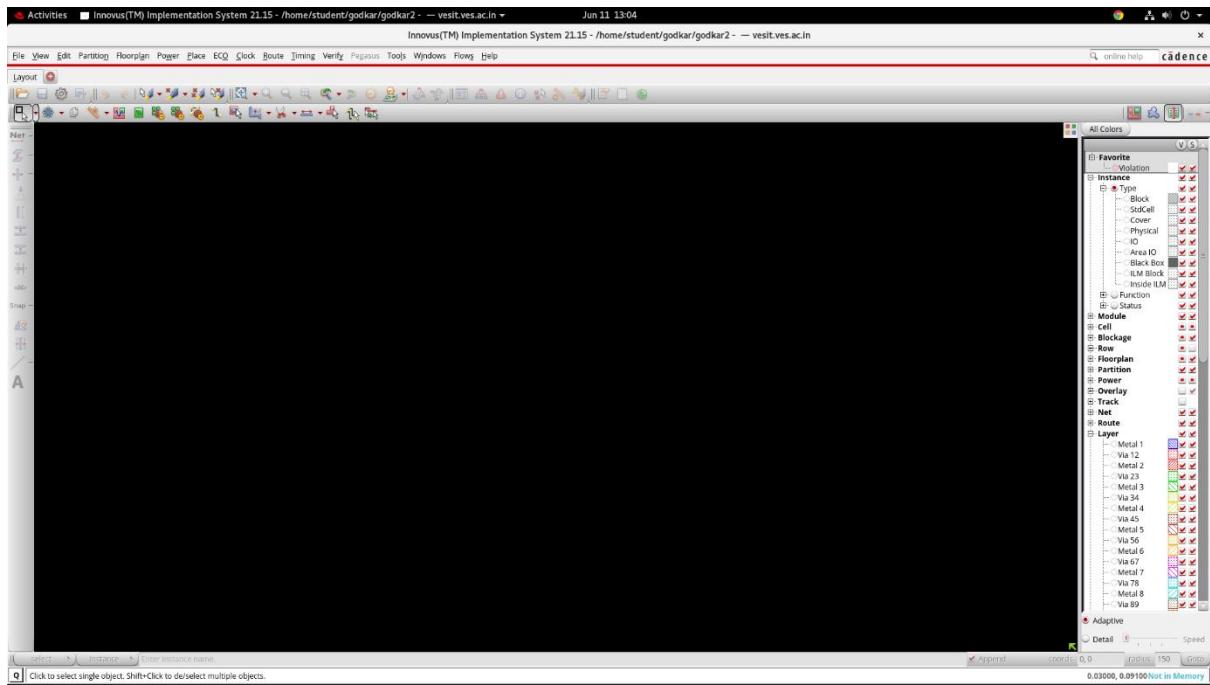
GENUS STEPS

1. source /home/install/cshrc
2. genus
3. read_lib slow.lib
4. read_hdl name.v
5. elaborate topmodule
6. syn_gen
7. syn_map
8. syn_opt
9. report area
10. report power
11. report gates
12. report timing -unconstrained
13. write_hdl > netlist.v
14. write_sdc > sdc.sdc
15. gui_show
16. gui_hide

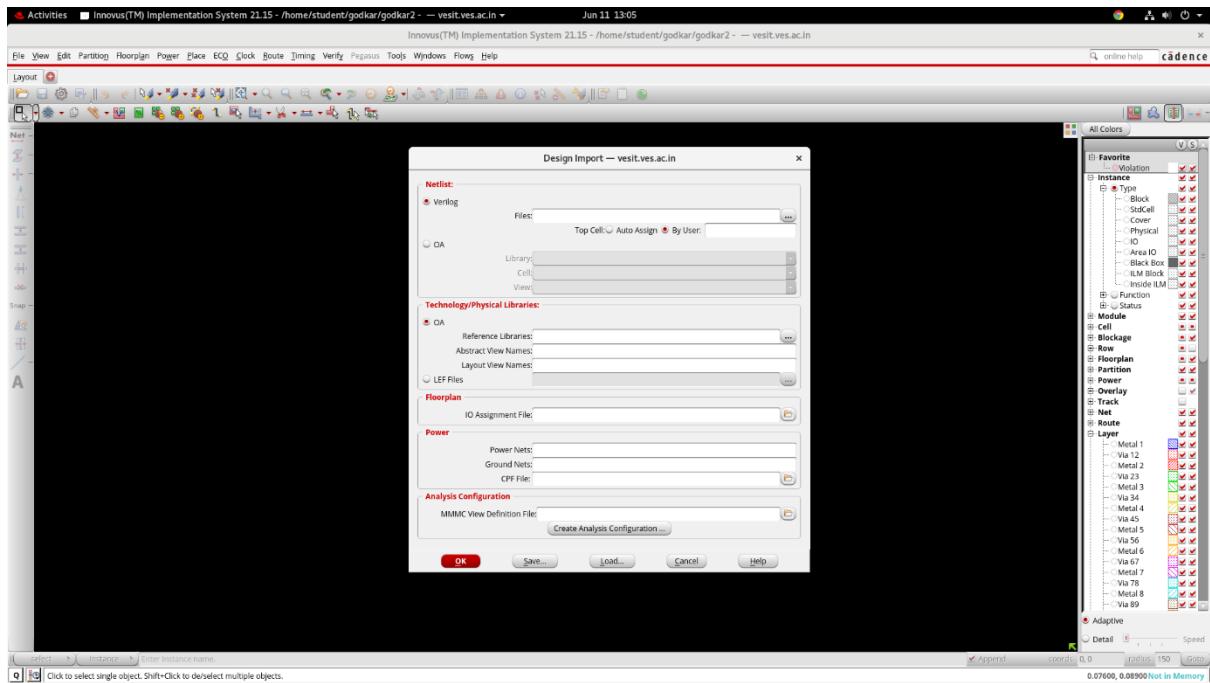


INNOVUS STEPS

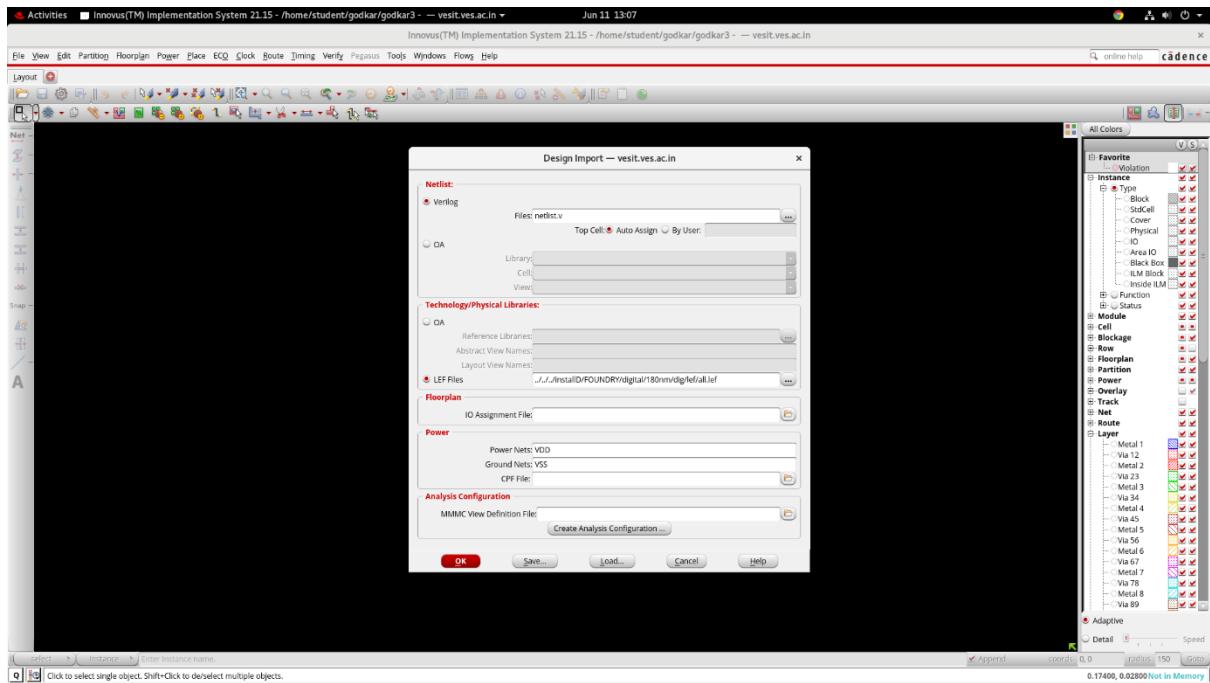
First launch innovus tool, gui will appear



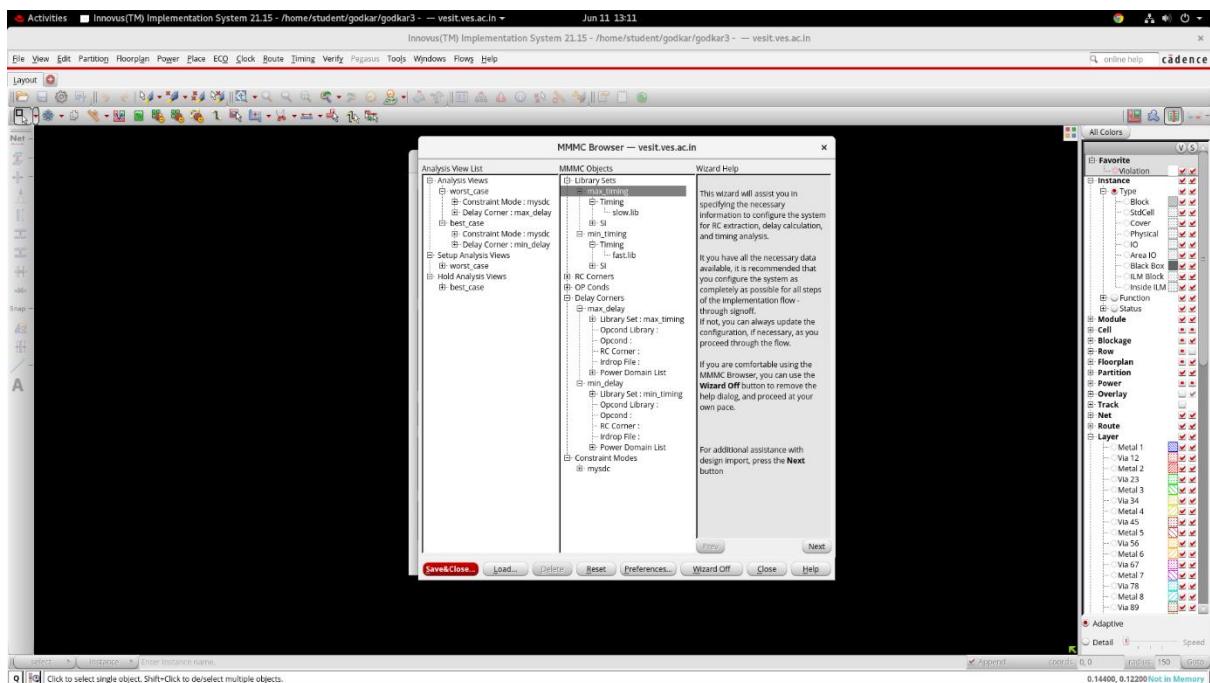
Click on file tab and press import design , drop down box appears



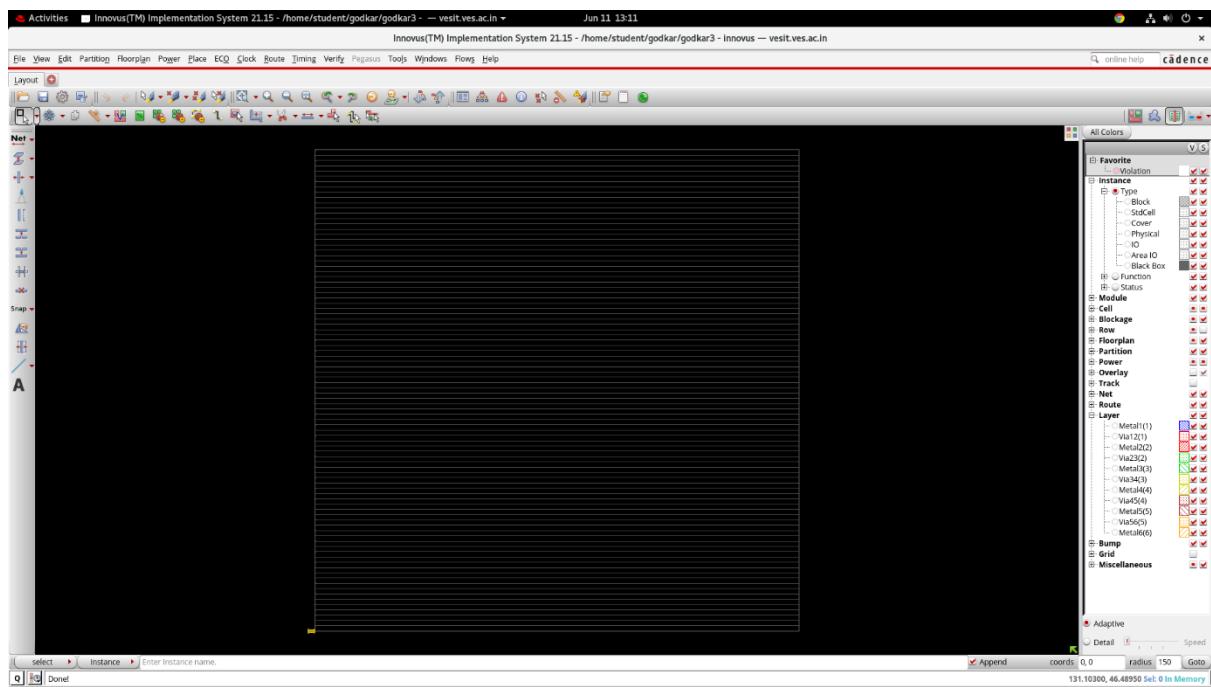
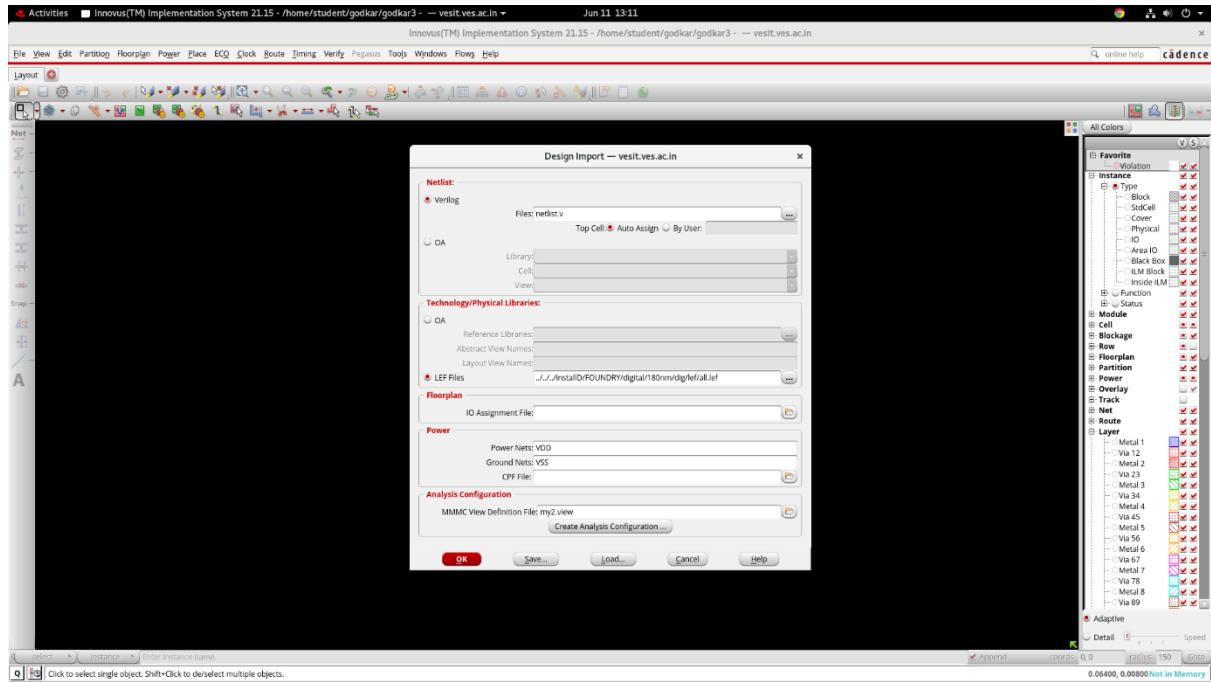
Select netlist file with .v extension that u made in genus tool. Top cell – auto assign. Select which ever leaf file is available from foundary. Type power net – VDD, ground net – VSS.



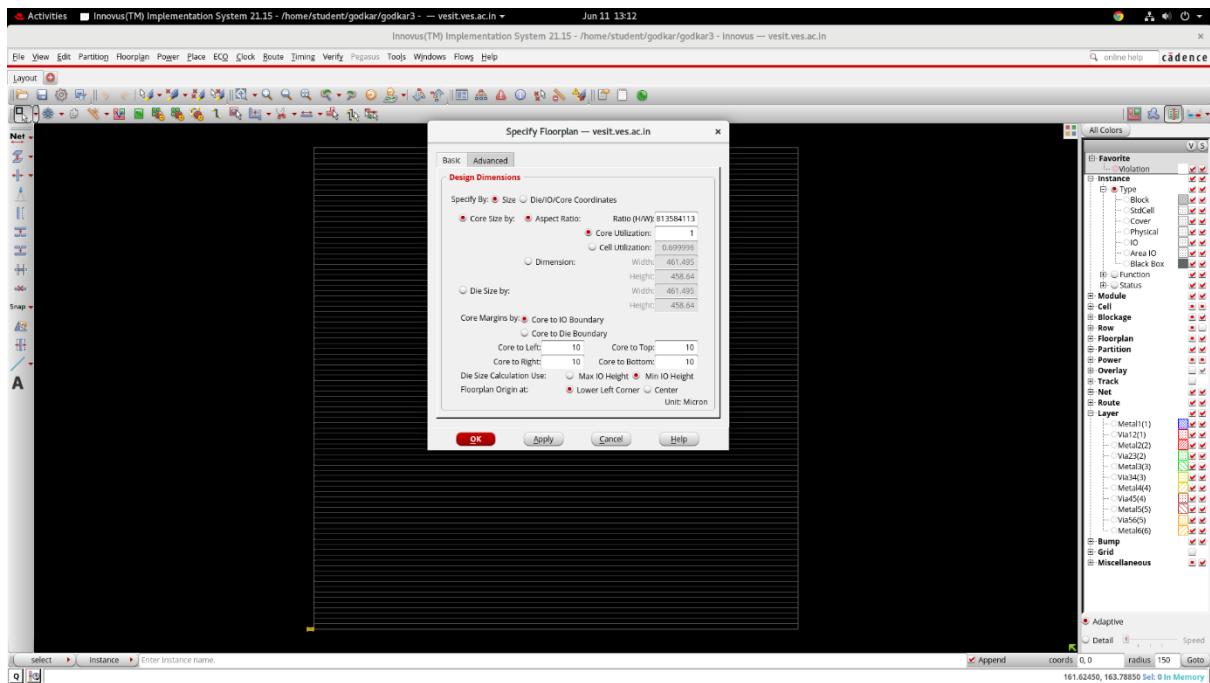
For Mmmc file – click create analysis configuration. A drop down box appears. Under library sets (name slow.lib as max_timing, name fast.lib as min_timing) under delay corners (name max_timing as max_delay, name min_timing as min_delay) under constraint modes (select sdc file obtained from genus tool) under analysis view (name max_delay as worst_case, name min_delay as best_case) under setup analysis view (select worst_case) under hold analysis view (select best_case). Now that everything is filled click save&close to save file with .view extension.



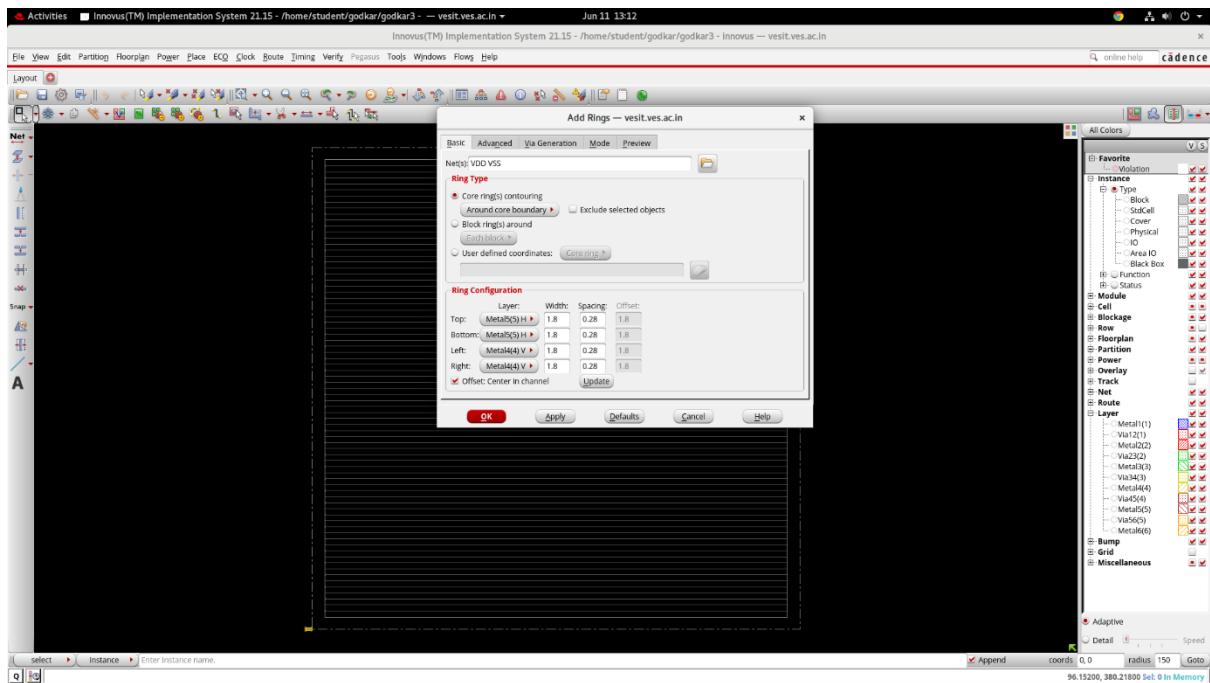
Now press save to save file with .globals extension. Now click ok. A die appears on screen

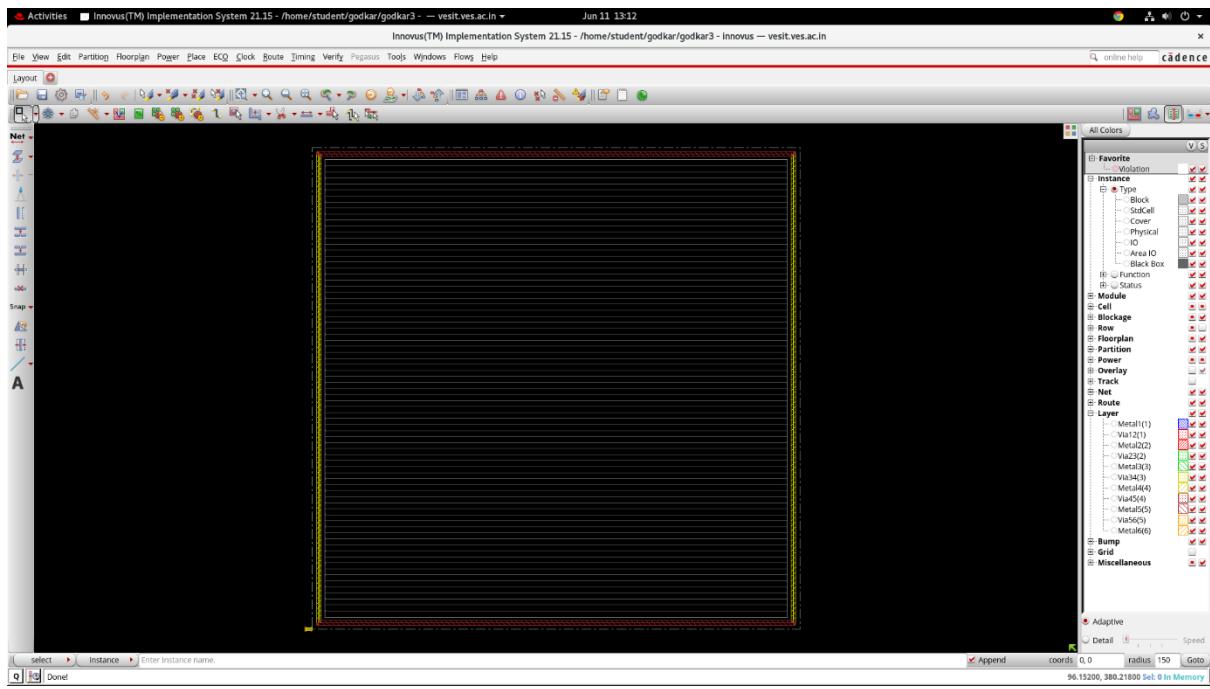


Now select floorplan > specify floorplan. If core utilization = 1 we get square shape die. If core utilization < 1 we get rectangle shape die. Core to left / right / top / bottom = 10. Press ok

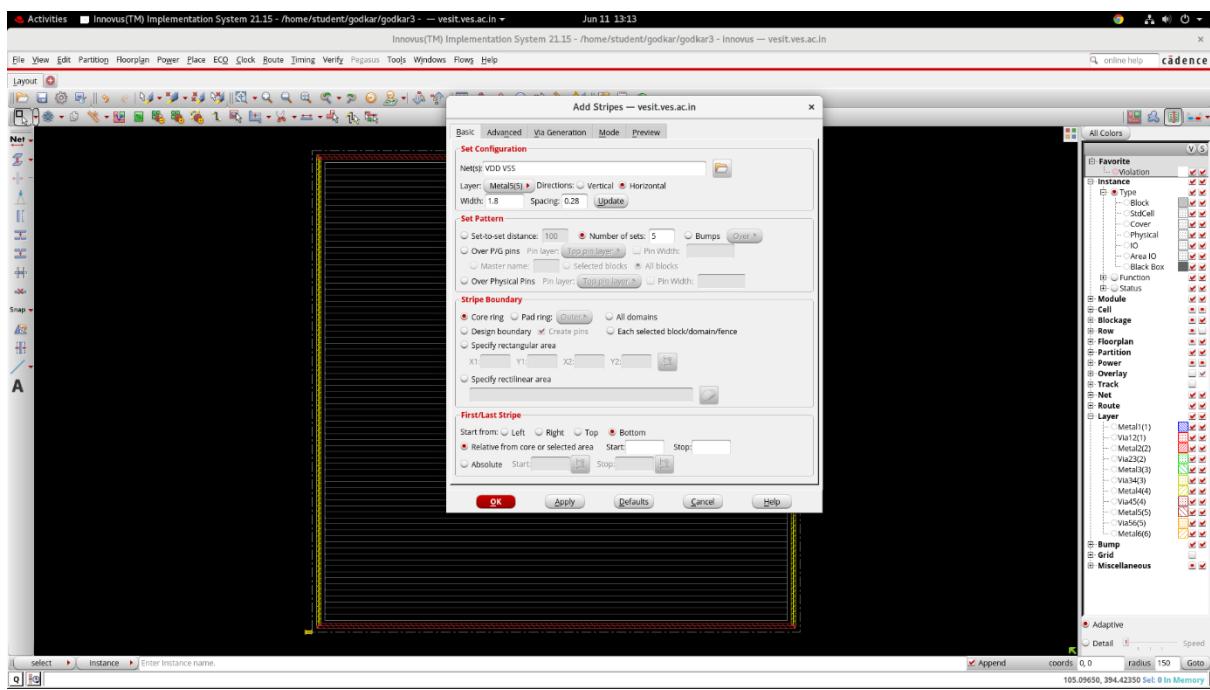


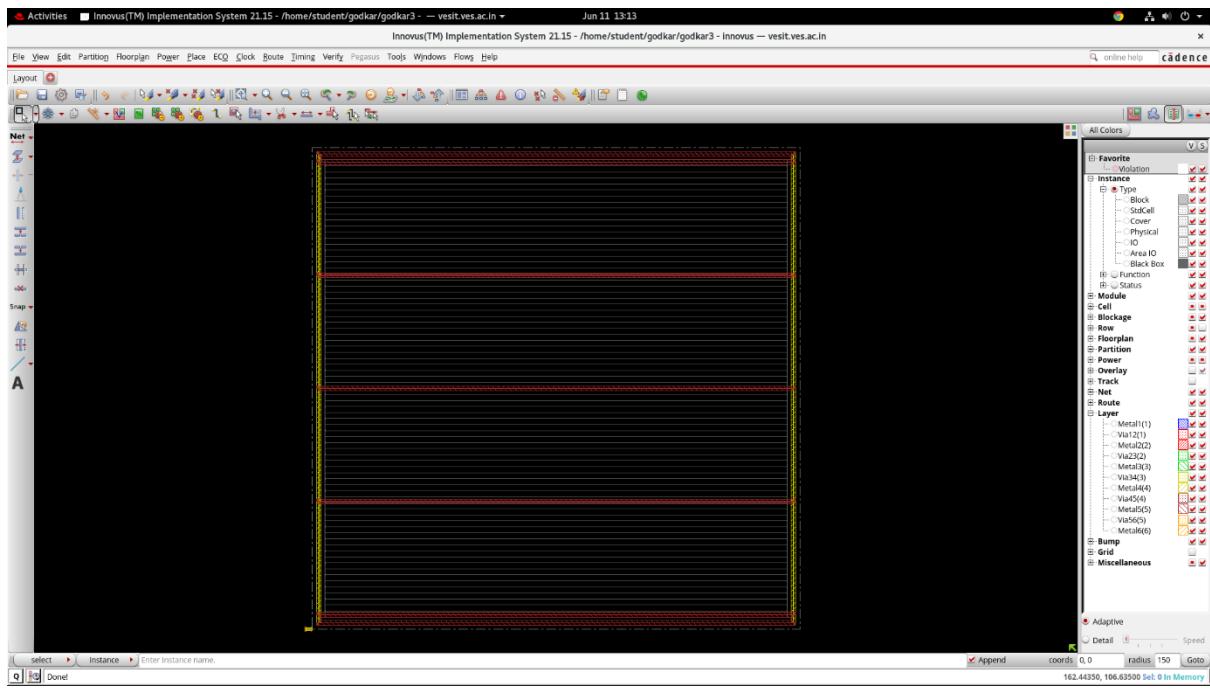
Now select power > power planning > add rings. Browse for VDD, VSS. Top / bottom metal 5. Left / right metal 4. Offset center in channel. Update. Ok.



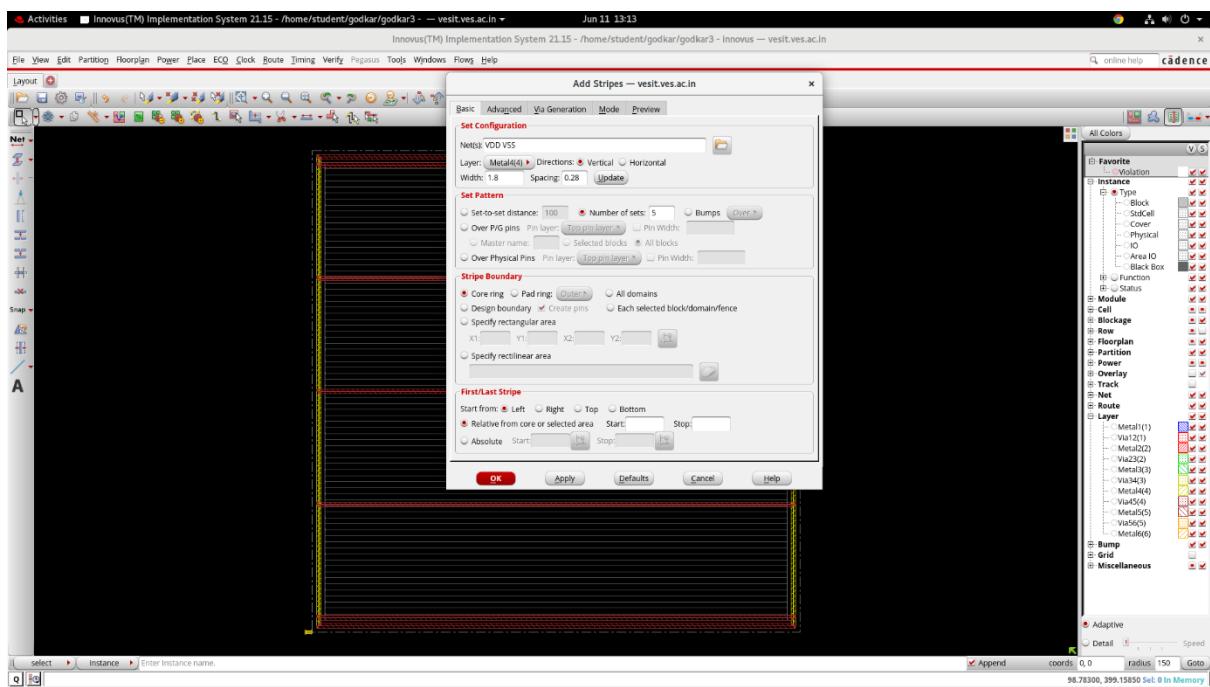


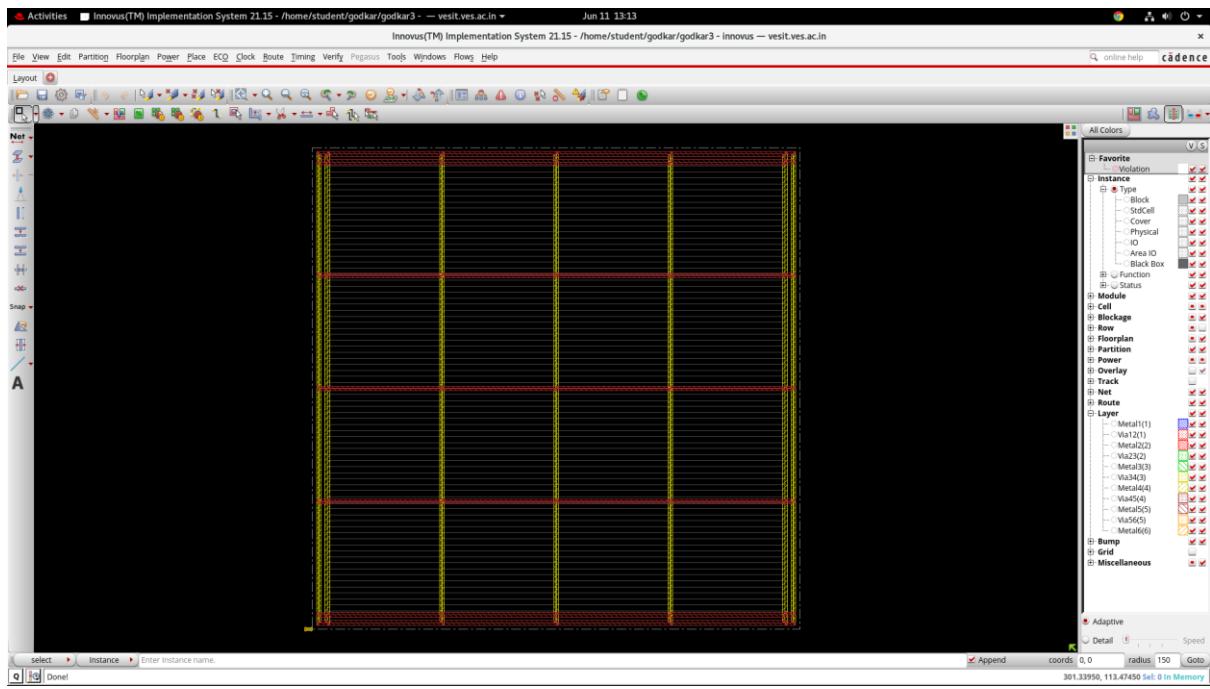
Now select power > power planning > power strips. Browse VDD VSS. Select metal 5 . horizontal. Update. Number of sets 5. Ok.



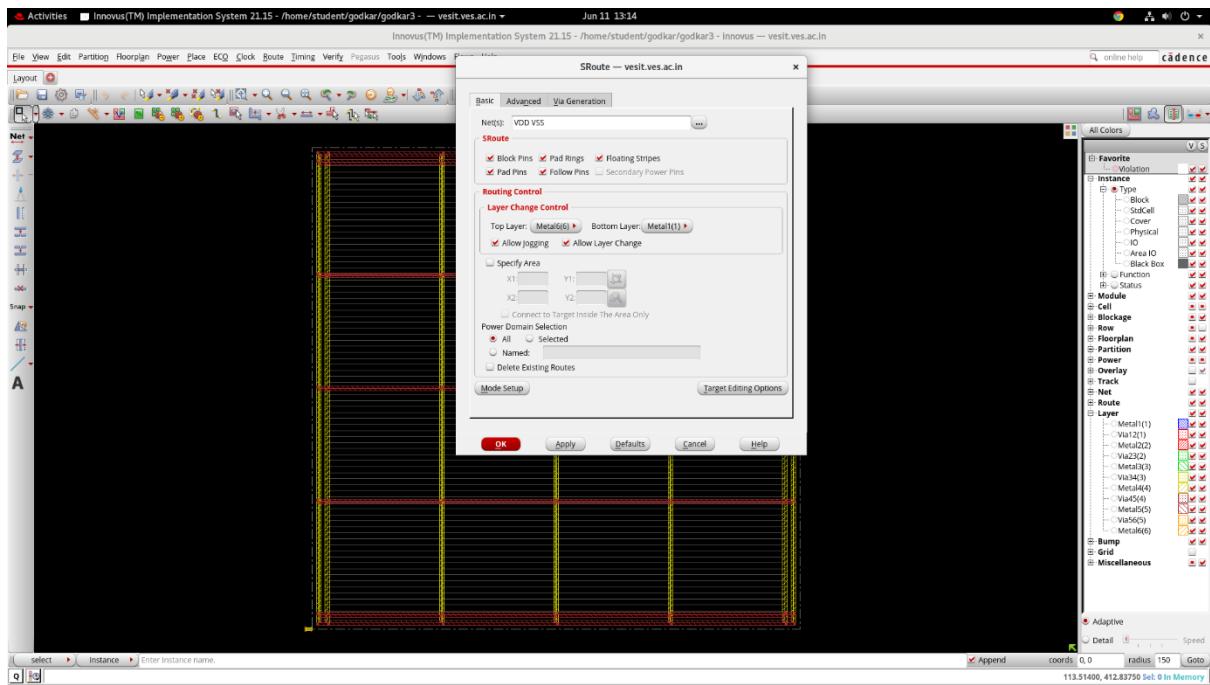


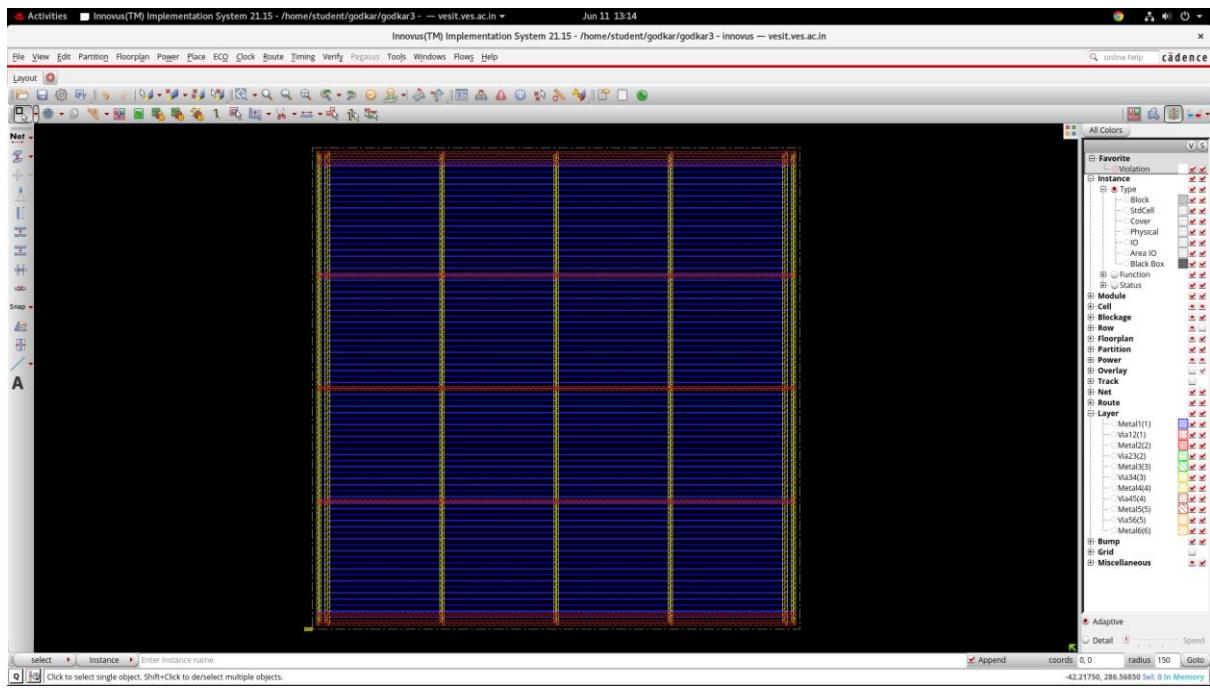
Again Now select power > power planning > power strips. Browse VDD VSS. Select metal 4 . vertical. Update. Number of sets 5. Ok.



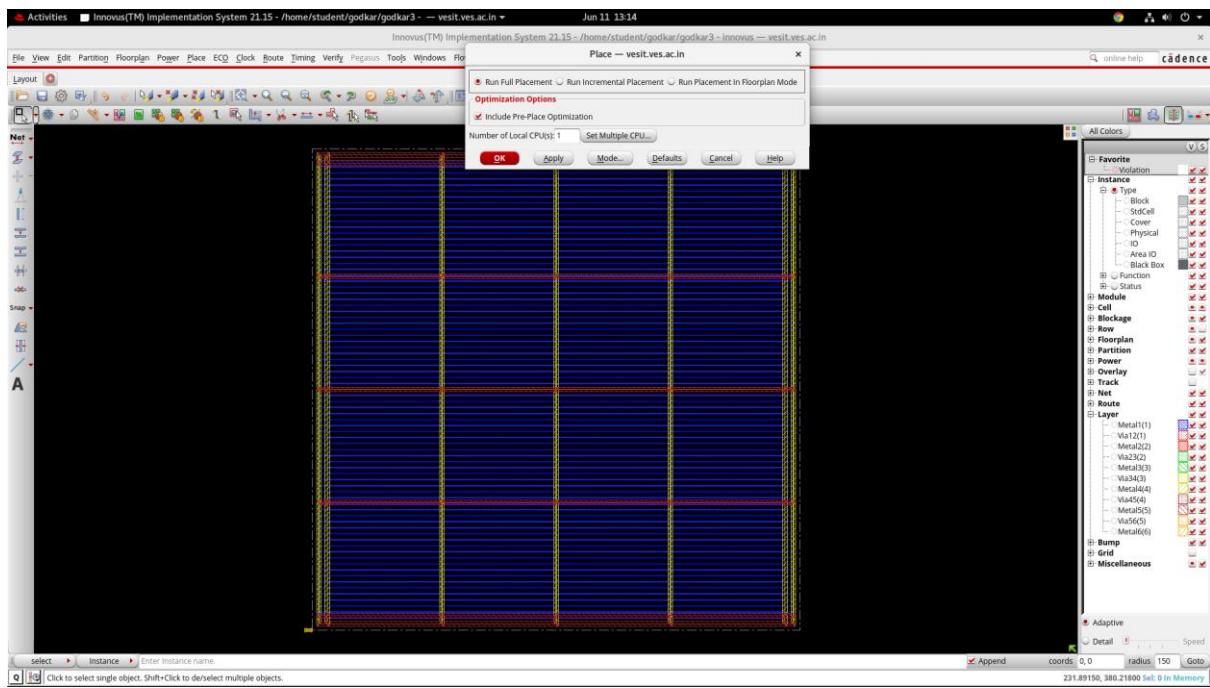


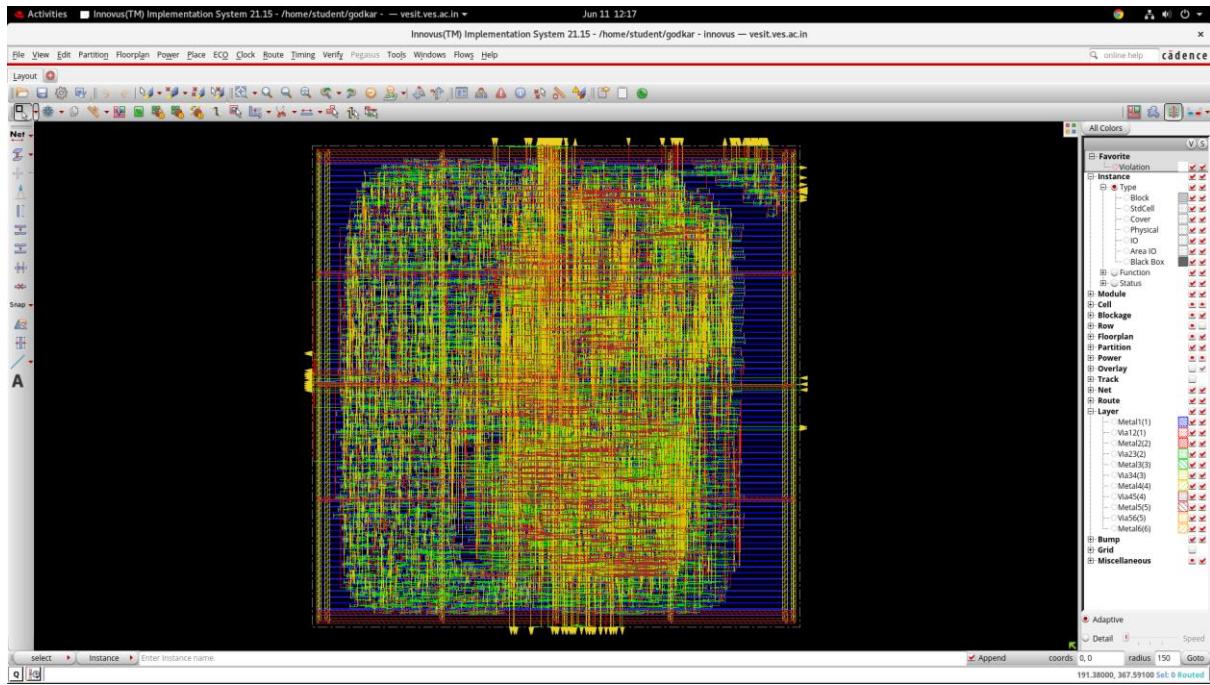
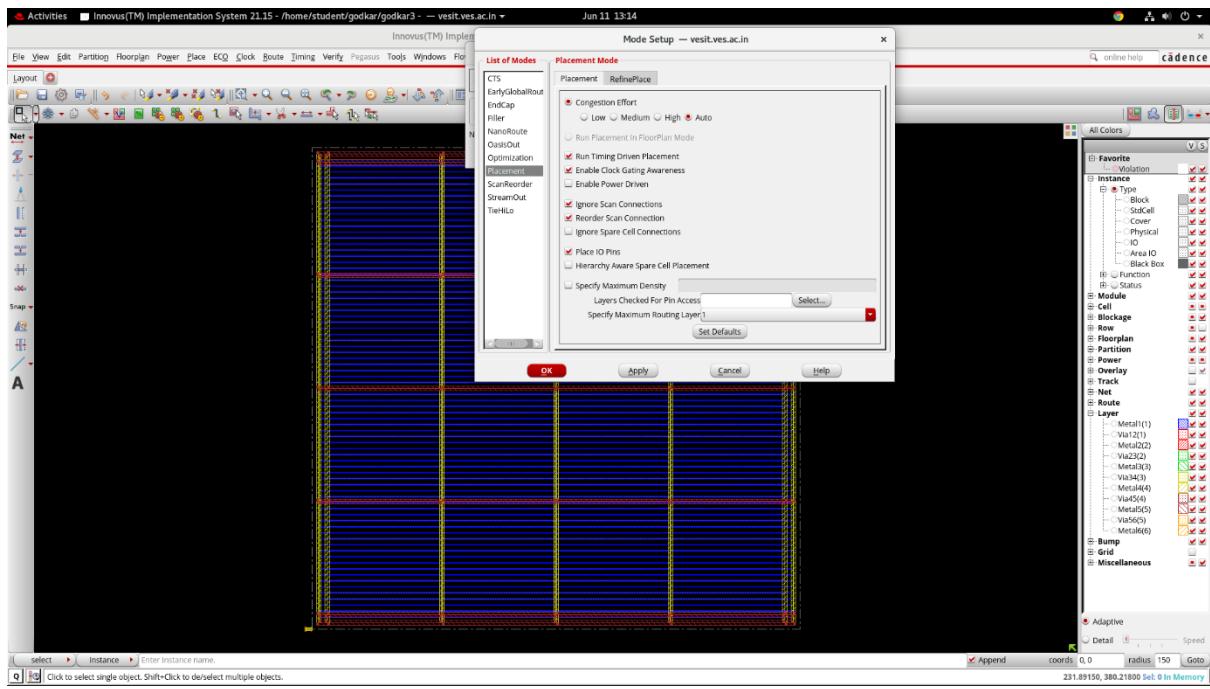
Select routing > special routing. Browse VDD VSS. Press ok.

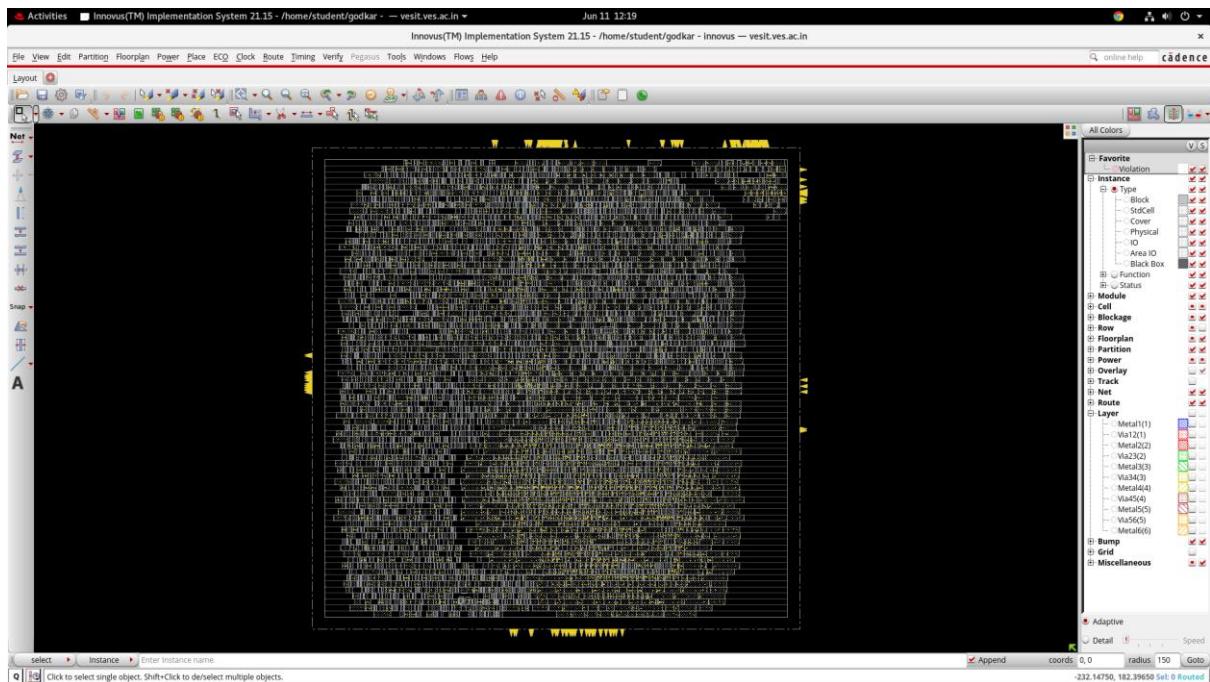




Now select placement > place std cells > run full placement > mode > place io pins > ok > ok. Once placement is complete u can turn off the layer option on RHS to view std cell which appear in gray color.







Now this is only die. We need to add IO pad ring to die to complete the chip. To do that in innovus we have to write .io file at the time of importing the design. There is another simpler way. To do that in virtuoso. For that we will first save this layout. File > save design > innovus > name.enc > ok. Now this layout can be opened any time. File > restore design > innovus , browse , select , ok. After saving layout next step is to export layout. File > save > GDS/OASIS > name.gds > ok. Now close innovus and open virtuoso. File > import > stream. A drop down box appears. Browse stream file . give name to library. Attach a existing technology file. Then press translate.

