

Design of 8 bit SAR ADC

Submitted in partial fulfillment of the
requirements of the degree of Bachelor of
Engineering

Group Number: BE-02	
Group Member Names	Roll No.
Vansh Dhoka	24
Atharva Godkar	25
Anish Godse	26
Anushri Kadam	50

By Supervisor:

Name of Guide: Dr. Jaymala Adsul



Department of Electronics Engineering
V.E.S. Institute of Technology

(Autonomous Institute Affiliated to University of Mumbai, Approved by AICTE & Recognized by Govt. of Maharashtra)

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CERTIFICATE

This is to certify that the project entitled "**Design of 8 bit SAR ADC in Cadence Virtuoso**" is a bonafide work of "**Atharva Godkar (25), Anish Godse (26), Vansh Dhoka (24), Anushri Kadam (50)**". Submitted to the V.E.S. Institute of Technology in partial fulfillment of the requirement for the award of the Bachelor of Engineering in **Electronics Engineering**.

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Principal

Project Report Approval for B.E

This project report entitled “**Design of 8 bit SAR ADC in Cadence Virtuoso**” is a bonafide work of “**Atharva Godkar (25), Anish Godse (26), Vansh Dhoka (24), Anushri Kadam (50)**” & is approved for the degree of the Bachelor of Engineering in **Electronics Engineering**.

Examiners

1. _____

2. _____

DECLARATION

We declare that this written submission represents our ideas in our own words and where others' ideas or words have been included, we have adequately cited and referenced the original sources. We also declare that we have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in our submission. We understand that any violation of the above will be cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

Atharva Godkar

Anish Godse

Vansh Dhoka

Anushri Kadam

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ABSTRACT

This project presents the complete design, implementation, and analysis of an 8-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) using Cadence Virtuoso and GPDK 180nm CMOS technology. The SAR ADC architecture was selected for its ideal trade-offs between speed, resolution, power efficiency, and design simplicity, making it suitable for moderate bandwidth and precision applications. The system is composed of four main building blocks: a Sample and Hold (S/H) circuit, a high-speed dynamic Comparator, a Successive Approximation Register, and an R-2R ladder-based Digital-to-Analog Converter (DAC). Each block was designed, optimized, and validated through rigorous schematic-level and post-layout simulations.

A key focus of the project was to overcome practical challenges typically encountered in analog and mixed-signal design, including issues like comparator delay, sample and hold charge injection, and DAC settling time. Strategies such as optimized MOSFET sizing, improved layout techniques (interdigitization and common centroid), removal of compensation elements for comparator speed improvement, and careful RC trade-offs in the DAC were employed. Post-layout simulation results validated the successful functioning of the ADC, achieving a Signal-to-Noise Ratio (SNR) of 43.76 dB, an Effective Number of Bits (ENOB) close to 7, and a Spurious-Free Dynamic Range (SFDR) of 50.23 dB, with a total power consumption of approximately 8.33 mW under a 3.3V supply.

Through this work, a complete bottom-up flow from schematic design to layout verification, parasitic extraction, and performance analysis was executed, providing valuable practical experience in analog IC design. The finalized SAR ADC demonstrates efficient operation at 10 MHz sampling rate with 8-bit resolution, making it a robust and effective solution for applications demanding moderate speed, low power consumption, and reliable signal conversion. The learnings from this project lay a strong foundation for advancing toward higher-resolution, lower-power, and faster ADC architectures in future work..

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Chapter 1: Introduction

Chapter 1: Introduction

In today's era of rapidly advancing technology, Analog-to-Digital Converters (ADCs) are critical components that bridge the analog and digital worlds. Whether in smartphones, medical devices, automotive sensors, or industrial automation, the accurate and efficient conversion of real-world analog signals into digital data is foundational for modern electronic systems. Among the various types of ADCs, the Successive Approximation Register (SAR) ADC stands out for offering an optimal balance between speed, resolution, power efficiency, and implementation complexity. This makes SAR ADCs a preferred choice for a wide range of medium-speed, high-precision applications.

This project focuses on the design and development of an 8-bit SAR ADC using Cadence Virtuoso with GPDK 180nm CMOS technology. The goal is to achieve a high-speed, low-power, and accurate ADC architecture suitable for real-time signal processing applications. The complete system is composed of four key sub-blocks: a Sample and Hold (S/H) circuit, a high-speed dynamic Comparator, a Successive Approximation Register, and a Digital-to-Analog Converter (DAC) based on an R-2R resistor ladder network. Each block was meticulously designed, simulated, and optimized to meet strict performance requirements under real-world constraints like parasitic effects, supply noise, and process variations.

The design methodology adopted for this project emphasizes a bottom-up approach, starting with transistor-level schematic design, followed by physical layout, post-layout parasitic extraction, and performance validation through detailed simulations. Key performance metrics like Signal-to-Noise Ratio (SNR), Effective Number of Bits (ENOB), and power dissipation have been evaluated, and challenges such as charge injection, clock feedthrough, comparator speed bottlenecks, and DAC settling issues were systematically overcome. Ultimately, this project not only demonstrates the practical aspects of mixed-signal circuit design but also serves as a stepping stone toward mastering advanced analog and VLSI system development. The insights gained pave the way for future improvements in SAR ADC architectures, including higher resolutions, asynchronous operation, and further power optimization.

Specifications of ADC -

1. Type = SAR ADC
2. Resolution = 8 bits
3. Sample Hold clock speed = 100 ns (10Mhz)
4. SAR register clock speed = 11.1111 ns (90MHz)
5. Conversion time = 8 bits * 11.1111 = 88.8888 ns
6. Supply voltage = 3.3v
7. Technology used = 180nm

Chapter 2: Literature Review

Chapter 2: Literature Review

Performance analysis of double tail dynamic comparators

[1] Analog and digital converters (ADCs) are the most inevitable part of today's high-speed human interacted devices. Continuous efforts are being made to improve their performance. Despite working for the improvement of the whole ADC, efforts to improve sub-modules are also significant. Comparators are also a vital part of ADC. In this work, we have proposed a design of an Asynchronous Successive Approximation Register (SAR) ADC. Dynamic comparators have a high input impedance, rail to rail swing, and almost zero static power consumption; they are widely used in industrial applications over static comparators. Depending on the application requirements, the circuit can be chosen which provides less delay, area or higher operating frequency. Designing the comparator with high precision, low voltage, high dynamic range, lower power dissipation, high speed, robust and less offset voltage is a critical challenge for present and future applications. The Circuit behavior was observed over a large supply voltage range. When the input voltage becomes lesser than the resolution of the comparator, the wrong output gets latched at the output. This method helps in determining the offset voltage.

The specifications of the same are as follows:

Technology used - 180 nm

VDD - 1.8 V

Operating Freq - 500 MHz Offset

Power Consumption - 480 μ W

Delay - 310 ps

Designing of a high speed, compact and low power, balanced-input balanced-output preamplifier latch based comparator

[2] The conventional SAR ADC which is known to be the most energy-efficient ADC amongst various types of other ADCs, has medium speed, medium resolution, less power dissipation and lesser hardware complexity. The speed of such ADCs is known to be limited mainly by the time taken by comparator to resolve the applied inputs and is of the order of few MHz. Designing the SAR ADC using a comparator with high precision, low voltage, high dynamic range, lower power dissipation, high speed, robust and less offset voltage is a critical challenge for present and future applications. In this work, the author has proposed a novel high-speed Balanced-Input Balanced-Output (BIBO) preamplifier latch based comparator design, to be used for the designing of an Asynchronous Successive Approximation Register (SAR) ADC. The key point that makes this design different from other designs is that it uses latch made using two back to back connected inverters. These inverters are forming a positive feedback arrangement that prohibits the comparator from bursting into the oscillation. The Latch circuit uses three non-overlapping phases and dissipates less power when operated on a single 1V supply voltage.

The specifications of the same are as follows:

Technology - 500 nm Supply voltage -1V

Power consumption - 65 μ W

Speed - 2100 KSP (Kilo Samples per Second) = 2KHz

On The Design of Low Power CMOS (SA-ADCs) for Biomedical Applications

[3] Charge injection and clock feedthrough are considered two major problems that occur in basic S/H circuits. Charge injection occurs when the clock \emptyset goes high. The NMOS transistor turns ON, and the input voltage is sampled by the capacitor C_s . Due to the inverted channel, a charge under the gate oxide is produced. Then, when the clock \emptyset goes low, The NMOS transistor turns OFF. The charge will flow out from the NMOS gate into its source and drain creating an error in the sampled voltage. From this Thesis paper we understood that sample and hold circuit faces 2 problems i.e fluctuation in V_{gs} due changing V_{in} & charge injection. We use 2 additional circuits to solve these problems. Bootstrapped circuit to ensure that constant V_{gs} voltage is maintained. boosted driver circuit to shift supply voltage from 0-Vdd to Vdd - 2Vdd. This solves the Charge injection problem.

The specifications of the same are as follows:

resolution = 8 bit ,

technology= 90nm

power consumption 200nW

power supply = 1v

signal to noise ratio = 53.8 dB

DNL = +0.34/-0.3 LSB

INL = +0.79/-0.58 LSB

Design of a Low-Power Asynchronous SAR ADC in 45 nm CMOS Technology

[4] The asynchronous SAR ADC is called “asynchronous” because the blocks in this SAR system don’t operate with the same uniform clock signal. Each block produces a signal that signals another block to change state. The external clock only triggers the internal-clock generator to begin the conversion process. The generator produces 2 internal signals, “Clk_Sample”, which is a pulse used for the sampling phase by the sample-and-hold (S/H) block, and “Clk_SAR”, which controls the comparator and the SAR code that changes the DAC voltage. The conversion process starts with the S/H block sampling the input, then “Clk_SAR” goes high which prompts the SAR logic to apply the DAC code. From this paper we learned that ADCs are basically of 4 types - flash , SAR, Counting, Dual slope, pipeline, sigma delta etc. Amongst these sigma delta is used for applications requiring high resolution whereas Flash is used for applications requiring high BW. SAR adc has moderate BW & resolution. It is further classified into 2 types. Synchronous sar adc the sampling clock is given externally. Whereas in asynchronous sar adc sampling clock is generated internally.

The specifications of the same are as follows:

input signal = 1.2v

power consumption 49uW

power supply = 1v

signal to noise ratio = 46 dB

technology = 45nm

resolution= 8 bit

Chapter 3: Block Diagram and Working

Chapter 3: Block Diagram and Working

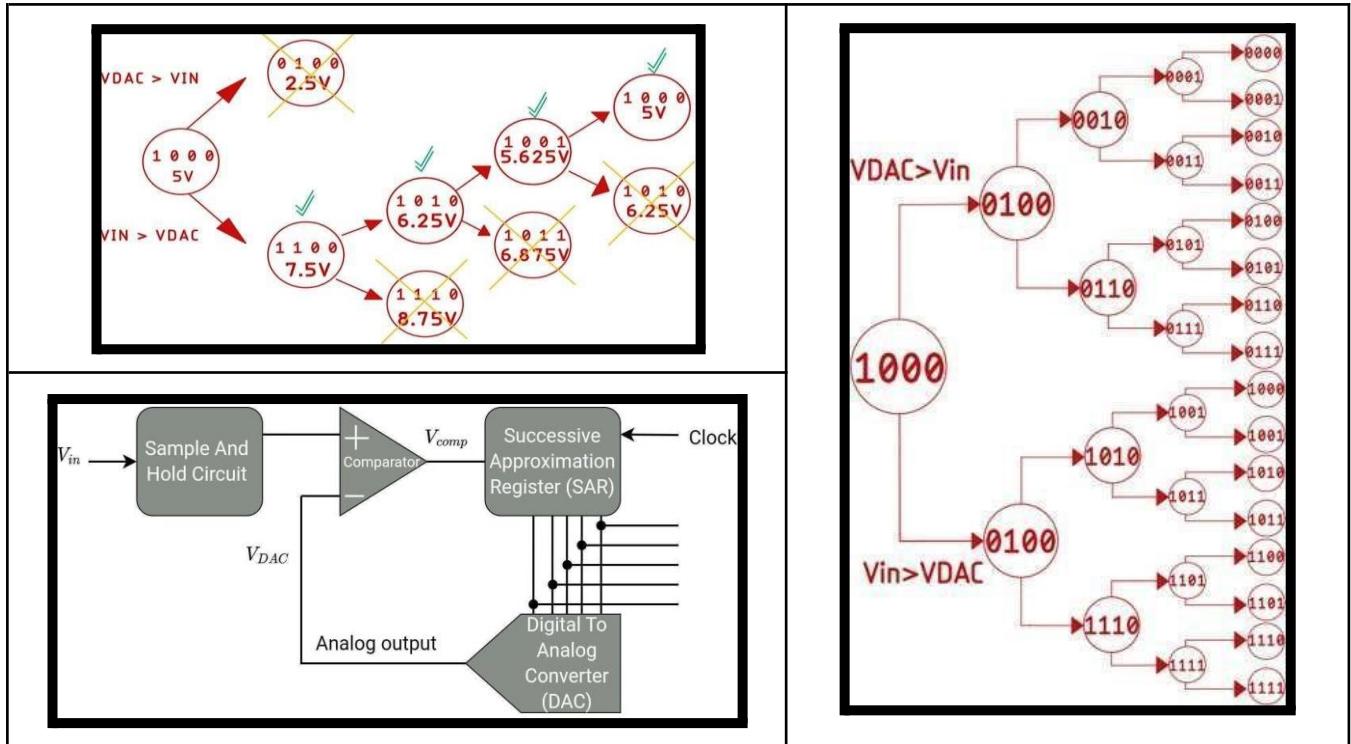


Fig. 3.1 Block diagram & working Principle

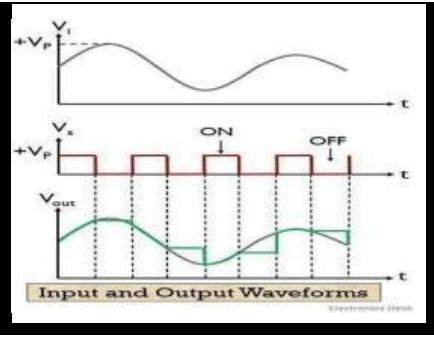
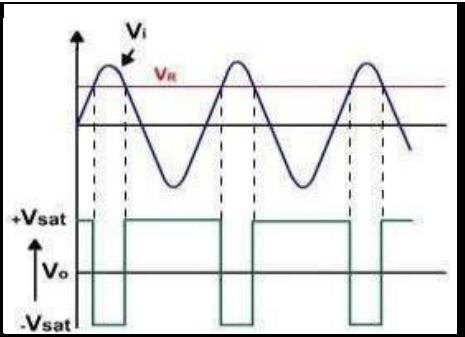
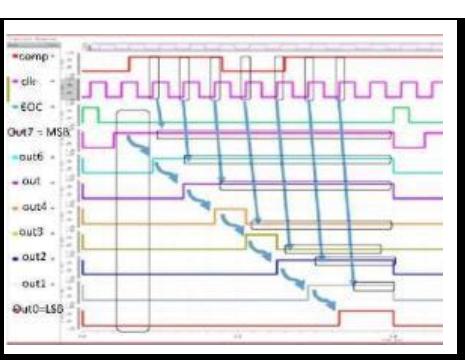
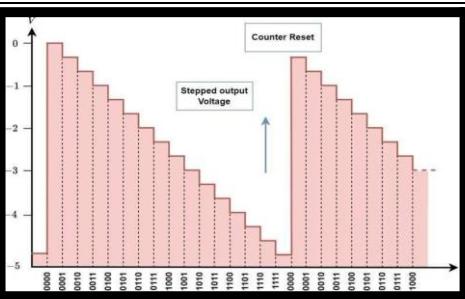
Working of the SAR ADC:

An ADC (analog-to-digital converter) has three main parts: a comparator, a digital to analog converter (DAC), and a successive approximation register with a control circuit. Whenever a new cycle starts, the sample and hold circuit samples the input signal which is compared with the specific output signal of the DAC. Also, the sampled signal is holded for a specific time period so that the subsequent circuit can compute the result. When the conversion starts, the successive approximation register sets the most significant bit to 1 and all other bits to zero. For example, for a 4-bit ADC, the value becomes 1000. Now let's say, the sampled input signal is 5.8V. For a 10V reference voltage, the DAC will produce a value of 5V which is half of the reference voltage. (The value will toggle between both extreme values.) Now this voltage will be compared to the input voltage and based on the comparator output, the output of the successive approximation register will be changed.

- This means if V_{in} is greater than the output of the DAC, the most significant bit will stay as it is, and the next bit will be set for a new comparison.
- Otherwise, if the input voltage is less than the DAC value, the most significant bit will be set to zero, and the next bit will be set to 1 for a new comparison.

This is how the successive approximation ADC changes 1 bit at a time to determine the input voltage and produce the output value. And whatever the value might be, in four iterations/cycles, we will get the output digital code from the input value. A n-bit SAR ADC will take n-iterations to convert the analog signal to digital value.

Table 3.1 - The SAR ADC is collectively made up of four blocks, which are described as below:

COMPONENT	EXPECTED OUTPUT
Sample and Hold Circuit: It takes samples from the analog input signal and holds them for a particular period of time and then outputs the sampled part of the input signal. Capacitor holds the sampled input signal and provides it at output according to command input.	
Comparator: The comparator determines whether the SHA output is greater or less than the DAC output. There are two signals input to the comparator, V_{in} is the analog input voltage that needs to be converted into a digital format and V_{ref} is the reference voltage against which V_{in} is compared. If $V_{in} > V_{ref}$, the comparator outputs a logic HIGH and if $V_{in} < V_{ref}$, the comparator outputs a logic LOW.	
Successive Approximation Register (SAR): The SAR ADC uses a SAR to determine the digital output that represents the analog input voltage. It sequentially approximates the input analog voltage by setting and clearing bits in a shift register based on comparisons with the DAC output. This iterative process results in a digital output that accurately represents the analog input voltage.	
Digital to Analog Converter (DAC): A R-2R DAC is used here to convert digital signals back into analog form for comparison with the input signal. In an R-2R DAC, resistors are arranged in a ladder network where the values follow a binary weighting scheme.	

Working of the SAR Block :

SAR block uses a binary search algorithm to successively approximate the analog input signal to produce equivalent Binary output. It performs a series of steps to determine the digital code that represents the input signal by setting each bit of the digital output starting from the most significant bit (MSB) to the least significant bit (LSB). The SAR logic controls the Digital-to-Analog Converter (DAC) and Comparator. The SAR logic updates the approximation register depending upon the comparator's result (whether the DAC output is higher/lower than the input voltage). Once all bits are processed, the final binary equivalent value in the approximation register represents the digital equivalent of the analog input voltage.

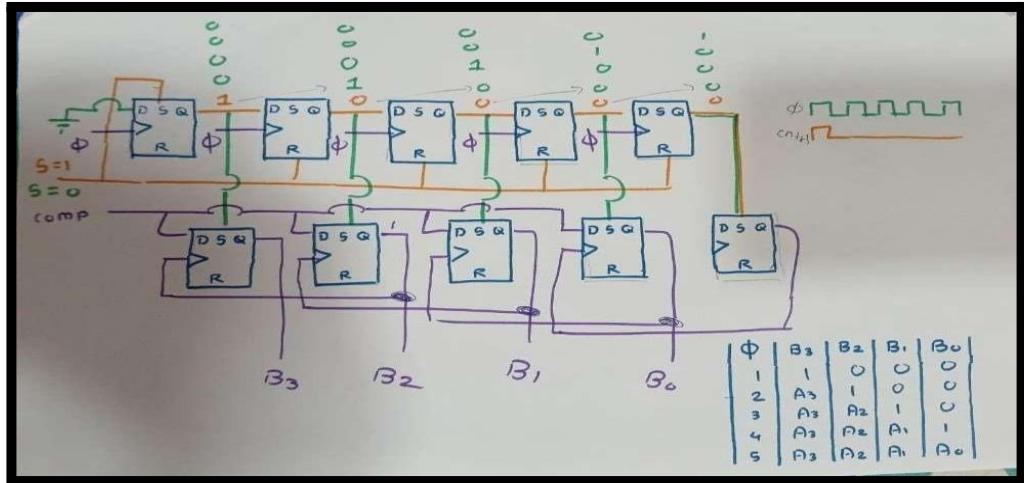


Fig 3.6 SAR register hand drawn circuit

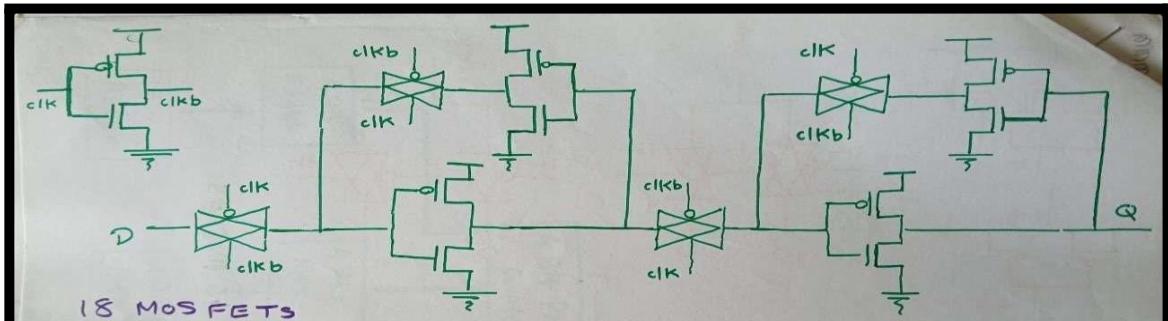


Fig 3.7 conventional D flip flop hand drawn circuit

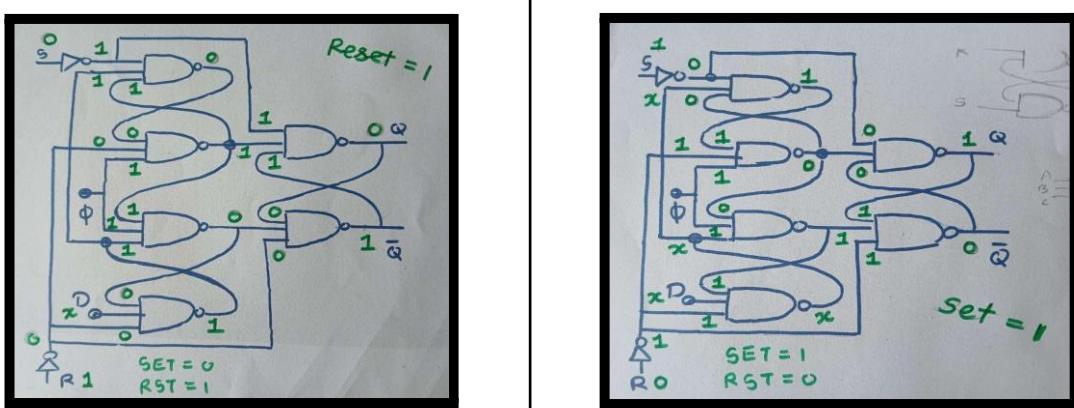


Fig 3.8 upgraded D flip flop hand drawn circuit

SAR block construction

SAR circuit is made up of 18 D flip flops. It is basically a combination of SISO shift register and PIPO shift register. SAR circuit takes input from comparator and gives output to R-2R DAC. SAR works on principle of Binary Search Algorithm. It generates output from LHS to RHS i.e from MSB to LSB. We are designing 8 bit SAR. so we will require total 9 clock cycles to generate output. At the start of conversion we reset SAR circuit i.e we store 1000,0000 inside the circuit. For next 8 clock cycles we keep this reset signal low. During these 8 clock cycles the input given by comparator is pushed into shift register. Some SAR circuits use additional signals like SOC (start of conversion) & EOC (end of conversion).

D flip flop - Working

The D flip flop used in the SAR circuit is positive edge triggered. It has active high SET & reset pins. It is Synchronous FF - set / reset action takes place only at a positive edge of clock. Both set and reset pins should not become HIGH simultaneously. It is invalid . This FF is made using 3 input NAND gates and 1 input NOT gates. At the positive edge of clock, output of FF = input to the FF. provided $S = R = 0$. Rest in all other cases the output of FF is retained, it does not change. When the set is HIGH output goes 1, irrespective of input given to FF. When reset is HIGH output goes 0 , irrespective of input given to FF. Outputs Q and $\sim Q$ are complementary to each other. Bottom - Up design approach is used to make the SAR circuit. SAR circuit is made using Semi Custom Design methodology

OPAMP construction

OP AMP circuits can be of 2 stage, 3 stage, or even 4 stage. The circuit given above is a 2 stage OP-AMP circuit. The first stage comprises an PMOS differential amplifier. The second stage comprises a common source NMOS amplifier. MOSFET M2 & M3 act as PMOS constant current sources. They are given external biasing (Vbias). 2 capacitors are used i.e Cc compensation capacitor & C1 load capacitor. MOSFET M4 & M5 form a differential pair circuit. Differential pair circuits can have passive load like resistor or active loads like current source & current mirror. In this circuit we have taken the current mirror as load. MOSFET M6 & M7 form NMOS current mirror circuit. Some OP-AMP circuits have a buffer stage on LHS while some do not have a buffer stage on LHS. For the buffer we use a common drain amplifier circuit. Our circuit is an buffered OPAMP circuit. MOSFET M1 & M8 make buffer.

OPAMP Working

Working of OP-AMP circuit The op-amp uses a single supply configuration, meaning it operates between voltages: VDD (positive) and GND (negative). for single supply OPAMP we cannot use NMOS differential pair, otherwise output will get clipped, hence we use PMOS differential pair. This allows the op-amp to amplify both positive and negative input signals, resulting in an output that can swing both above and below ground. Compensation Capacitor (Cc) To ensure stability, a compensation capacitor is placed between the output of the first and second stages. This provides frequency compensation, which helps maintain the phase margin and prevent oscillations in the op-amp. MOSFET M2, M3 act as PMOS current source. They ensure constant current flows through both the stages of OPAMP. MOSFET M4, M5 act as PMOS differential pair circuits. This circuit amplifies the difference between inputs Vin1 & Vin2. The common-mode rejection ratio (CMRR) is high due to the current mirror and the fact that any common-mode signal results in minimal change in output. differential amplifier & current mirror together make the 1st stage of OP-AMP. It offers high gain but low output current due to high output impedance provided by active load. MOSFET M6, M7 act as PMOS current mirror circuit. This circuit copies the current flowing through M4 into the current flowing through M5. it ensures that current coming from M2 gets equally distributed in both branches. MOSFET M6 is in diode configuration (because its gate and drain terminal are tied together). M9 is a single stage CS amplifier with PMOS current source as load (M3). this 2nd stage of OP-AMP. It provides high output current due to low output impedance, however gain decreases.

Table 3.2 - OPAMP design Parameters

open loop gain (AOL) - The gain of the op-amp without any feedback. Higher gain improves accuracy in analog processing. Important for low offset, high precision applications. Typically reduces with frequency. Affects DC performance and settling behavior. AOL = $20\log_{10}(V_{out} / V_{in})$. The unit is dB.
gain bandwidth product (GBP) - The frequency at which the op-amp's gain becomes 1. Product of DC gain and bandwidth. Key metric for comparing amplifier speed. Important in switched-capacitor circuits. Relates to how fast the op-amp can settle in a feedback loop. GBP = BW * Av . unit is Hz
unity gain frequency (UGBW) - The frequency where gain = 1 or 0 dB. Indicates how fast the op-amp can respond in unity-gain configuration. Must be higher than the system's operating frequency. Used in determining phase margin and loop stability. Influences transient response. UGBW = BW * AOL . unit is Hz
phase angle - Phase of the op-amp output relative to input at a certain frequency. At UGF, it helps determine phase margin. Should stay far from -180° for stability. Related to system response and oscillation risk. Measured during AC analysis.
phase margin - Stability margin in degrees from -180° at UGF. Higher PM ensures stable operation without overshoot. Too low → ringing or oscillation. Too high → sluggish response. Balanced PM ($\sim 60^\circ - 70^\circ$) is usually ideal. Typically measured from a Bode plot, no specific formula. unit is degrees.
slew rate - The maximum rate of voltage change at op-amp output. Important for large, fast signal transitions. Affects settling time in sampling systems. Limited by internal current and compensation. Measured during transient simulation. SR = $\Delta V_{out} / \Delta t$. unit is V/ us
OPAMP power consumption - Total power drawn by the op-amp during operation. Must be minimized for battery or low-power designs. Depends on bias current and architecture. Trade-off exists between power, speed, and linearity. Should be within the system power budget.
Bandwidth (BW) - The frequency range over which the op-amp can amplify signals without significant attenuation. BW = UGBW / AOL. The unit is Hz.
Power Supply Rejection Ratio (PSRR) - The ability of the op-amp to reject variations in the power supply voltage. PSRR = $20\log_{10}(V_{supply} / V_{out})$. unit is dB
Common-Mode Rejection Ratio (CMRR)- The ability of an op-amp to reject common-mode signals (signals present at both inputs). CMRR = $20\log_{10}(Av / Acm)$. The unit is dB.

Table 3.3 - ADC design Parameters

effective number of bits (ENOB) - Effective Number of Bits indicates the actual resolution when noise and distortion is considered. Lower than ideal due to non-idealities. Derived from SINAD using a standard formula. Reflects true usable accuracy of the ADC. Useful for comparing ADCs with different architectures.
Signal-to-Noise Ratio (SNR) - it compares the desired signal power to background noise. Does not include harmonic distortion. Higher SNR means cleaner signal conversion. Impacts overall system fidelity and signal quality. Decreases in presence of thermal, quantization, or flicker noise
Spurious-Free Dynamic Range (SFDR) - it measures how far the strongest spur is below the fundamental tone. Reflects the linearity and spectral purity of the ADC. Important in communication and RF systems. Can be affected by DAC mismatches, glitches, or layout. Higher SFDR implies fewer distortion components.
Signal-to-Noise and Distortion Ratio (SNDR) - it includes both noise & harmonic distortion. It is used to compute ENOB. More comprehensive than SNR alone. Affected by DAC nonlinearity & comparator kickback. Good SNDR ensures high signal fidelity
resolution - Defines how finely the analog input is quantized into digital levels. Higher resolution increases ADC accuracy. Determines number of quantization steps: $2^{N_2} \times 2^{N_1}$. Impacts comparator design, DAC size, and settling time. More bits require better matching and noise performance
sampling rate - The rate at which the ADC samples the analog input signal. Determines the ADC's bandwidth and max input frequency. Must satisfy the Nyquist criterion for the target signal. Affects conversion time and settling requirements. Trade-off exists between speed, resolution, and power
supply voltage - The operating voltage for the ADC circuit. Affects signal swing, power consumption, and linearity. Lower voltages reduce dynamic range and headroom. Needs to be chosen according to technology limits. Impacts the design of analog front-end blocks like DAC, op-amp.
ADC power consumption - Represents the total power drawn by the ADC during operation. Crucial for battery-powered and low-power systems. Depends on comparator type, DAC switching, and digital logic. Affected by supply voltage and clock frequency. Must be balanced with performance metrics like speed and resolution.

Sample and Hold Circuit Working:

In a SAR ADC, the S/H circuit is responsible for capturing the input analog signal at a specific moment in time and holding that value steady during the conversion process. It operates by successively narrowing down the value of the input signal through a series of comparisons with reference voltages. Before this process begins, the S/H circuit samples the analog input voltage when a control signal, usually a clock pulse, is triggered. This allows the S/H circuit to take a snapshot of the input signal, ensuring that the voltage remains constant throughout the subsequent conversion steps.

During the sample phase, the S/H circuit's switch (often a transistor or FET) is closed, connecting the input signal to a capacitor. This capacitor temporarily stores the sampled voltage. The timing of this sampling is critical; it must occur just before the ADC's conversion process to ensure that the input voltage accurately reflects the value that needs to be converted. The switch remains closed for a short duration, allowing the capacitor to charge to the input voltage level.

Once the sampling is complete and the control signal is removed, the switch opens, and the S/H circuit enters the hold phase. In this phase, the capacitor holds the voltage steady, isolating it from the input signal. This stability is crucial because the SAR ADC now begins the conversion process, comparing the held voltage against a series of reference levels to determine the corresponding digital output. The integrity of the voltage held by the capacitor must be maintained during this phase to avoid errors in the digital conversion.

The effectiveness of the S/H circuit directly influences the performance of the SAR ADC. Key factors include the accuracy and speed of the S/H circuit, as well as the time it takes for the capacitor to charge and hold the voltage. A high-speed S/H circuit ensures that the ADC can operate at faster sampling rates, while a high-accuracy circuit minimizes quantization errors and improves the overall resolution of the ADC. Additionally, after the hold phase, it's important that the capacitor discharges slowly enough to prevent voltage droop, which can occur if the load on the output is too large. To mitigate this, output buffers are often used to stabilize the output voltage and isolate it from load variations.

Working of DAC:

Digital-to-Analog Converters (DACs) are crucial components in various electronic systems, responsible for converting digital signals, typically represented in binary form, into corresponding analog voltages or currents. This conversion is essential in applications ranging from audio playback to video rendering and control systems. At its core, a DAC takes a binary input—such as a series of 1s and 0s—and produces an analog output that reflects the magnitude of that digital signal. The primary function of a DAC is to create a continuous analog representation from discrete digital values, allowing for smooth transitions and outputs.

The R-2R ladder DAC consists of only two resistor values: R and 2R. This simplicity reduces the complexity of the design and makes it easier to create precise resistor values, which is crucial for accurate operation. The structure consists of a series of resistors connected in a ladder-like formation, with switches that connect to the digital input bits.

The output voltage is determined by the weighted contributions of each active bit, with the most significant bit (MSB) contributing the most to the output. This design allows the DAC to produce a continuous analog voltage that corresponds to the digital input, facilitating its use in various applications such as audio and control systems.

Working of Comparator:

The comparator has two input terminals, often referred to as the inverting input (-) and the non-inverting input (+). When a voltage is applied to these inputs, the comparator continuously monitors the two levels. If the voltage at the non-inverting input (+) exceeds the voltage at the inverting input (-), the output of the comparator switches to a high state (often close to the supply voltage). Conversely, if the voltage at the inverting input exceeds that at the non-inverting input, the output switches to a low state (near ground).

This output is typically a digital signal, which makes comparators useful in various applications such as analog-to-digital conversion, zero-crossing detection, and threshold detection. Comparators can be implemented using operational amplifiers (op-amps) configured in open-loop mode, allowing them to provide fast response times and high sensitivity. Some comparators also feature hysteresis to prevent rapid switching of the output due to noise or small fluctuations in input voltages, enhancing stability and reliability in practical applications.

Layout

Before we start making the layout we have to prepare our schematic. Minor changes need to be made before proceeding for layout. First we start by replacing the resistor from the analog library with a poly resistor from the GPDK 180 library. Similarly we replace the capacitor from analog library with mim capacitor from GPDK 180 library. This is done because only those components which are present in GPDK 180 library have ready made layouts. Our resistor is of 1.47 K ohm, and has a width in the range of 100 - 500 um. This generates a layout which is very long as compared to other components like MOSFETs. So we added 20 segments, which divided width by 20. Now in the capacitor case there is no issue of dimension , but there is an issue of value. Maximum value of the mim capacitor is 100 f. But most of our capacitors have value in pico fard range. So we connected multiple capacitors in parallel so that their values get added up.

Table 3.4 - mim capacitor values for layout

Block in which C is present	Required value	Solution
Capacitor in DAC	100 f	Only 1 capacitor
Capacitor in Sample & Hold OPAMP	1p	5 capacitors in parallel
Capacitor in sample & Hold TG	2p	10 capacitors in parallel

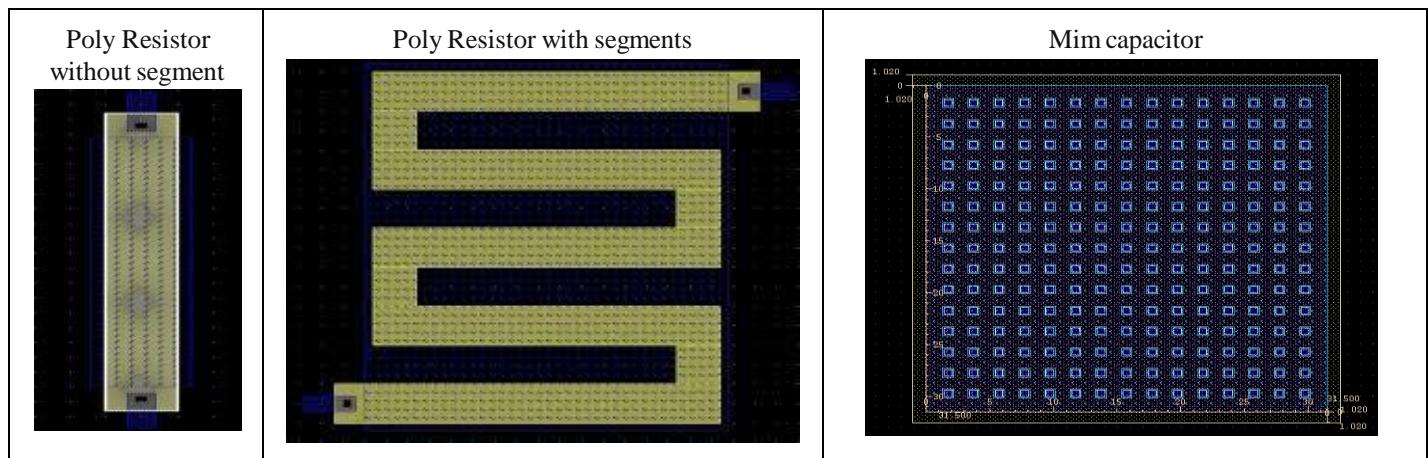


Fig 3.9 mim capacitor and poly resistor layout

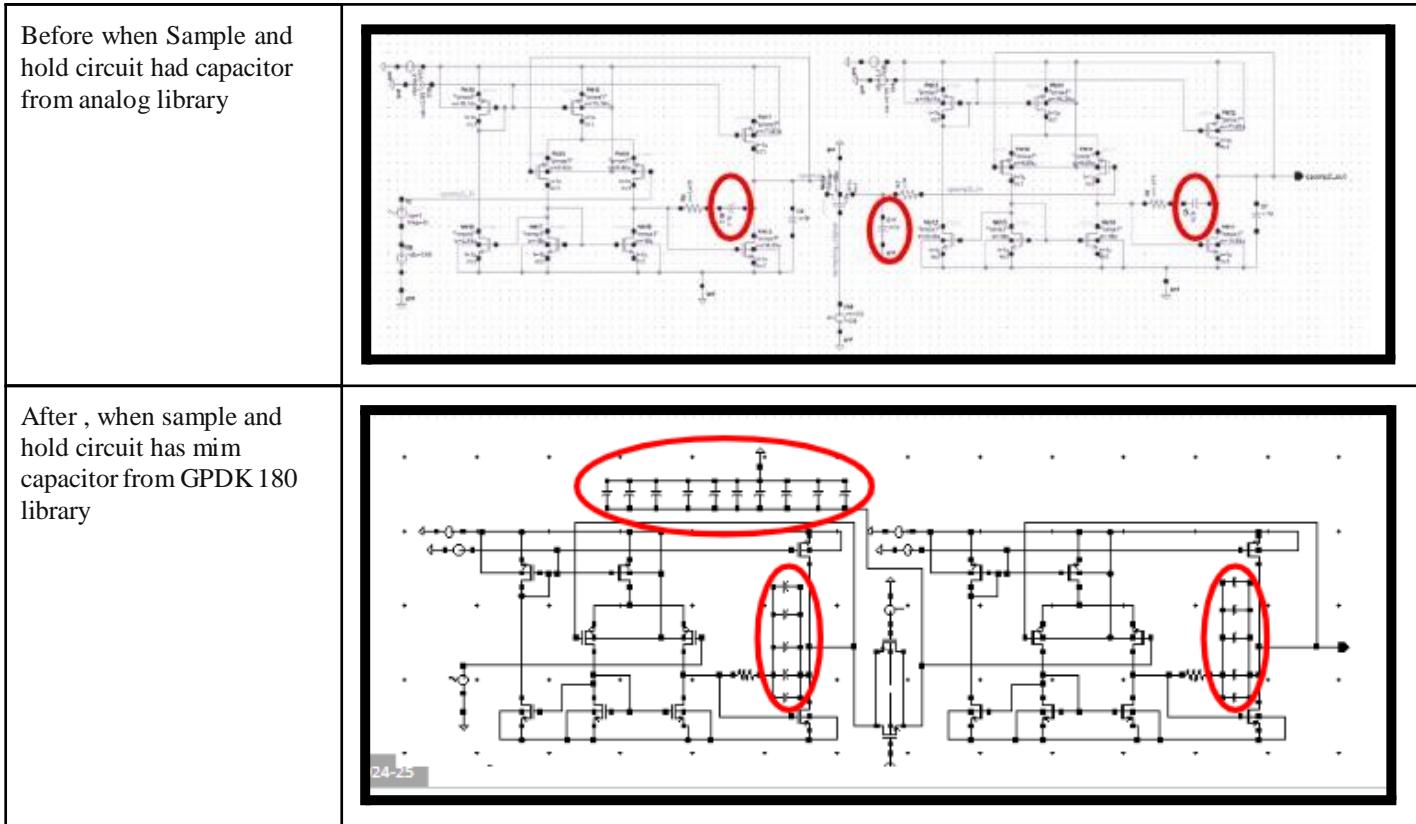


Fig 3.9 replacing analog library C with GPDK 180 library C

MOSFET in the OPAMP are of varying Widths. This creates problem in layout. We need to bring all MOSFETs to same width. For this we use multiplier option. Suppose A has width = 10 um and B has width = 2 um. Then we break A into 5 small parts each having width = 2 um. Number of multiplier required is 5. However this is not the case always, let say A has width = 7 um then we won't be able to break it exactly into 2 um. In this case we go for nearest possible value. In our OPAMP circuit smallest PMOS is M4 M5 having width = 6.65 um. So rest all PMOS will be converted to this width. Similarly smallest NMOS is M8 having width = 2.46 um. So rest all NMOS will be converted to this width.

Table 3.4 - adding multiplier to MOSFET

MOSFET	M2	M4 M5	M6 M7	M9	M1	M8	M3
LENGTH	1u	1u	1u	1u	1u	1u	1u
TOTAL WIDTH	76.39u	6.65u	10u	14.55u	18.14u	2.46u	71.2u
WIDTH OF EACH MULTIPLIER	6.365u	6.65u	2u	2.425u	6.046u	2.46u	5.93u
NUMBER OF MULTIPLIER	12	1	5	6	3	1	12

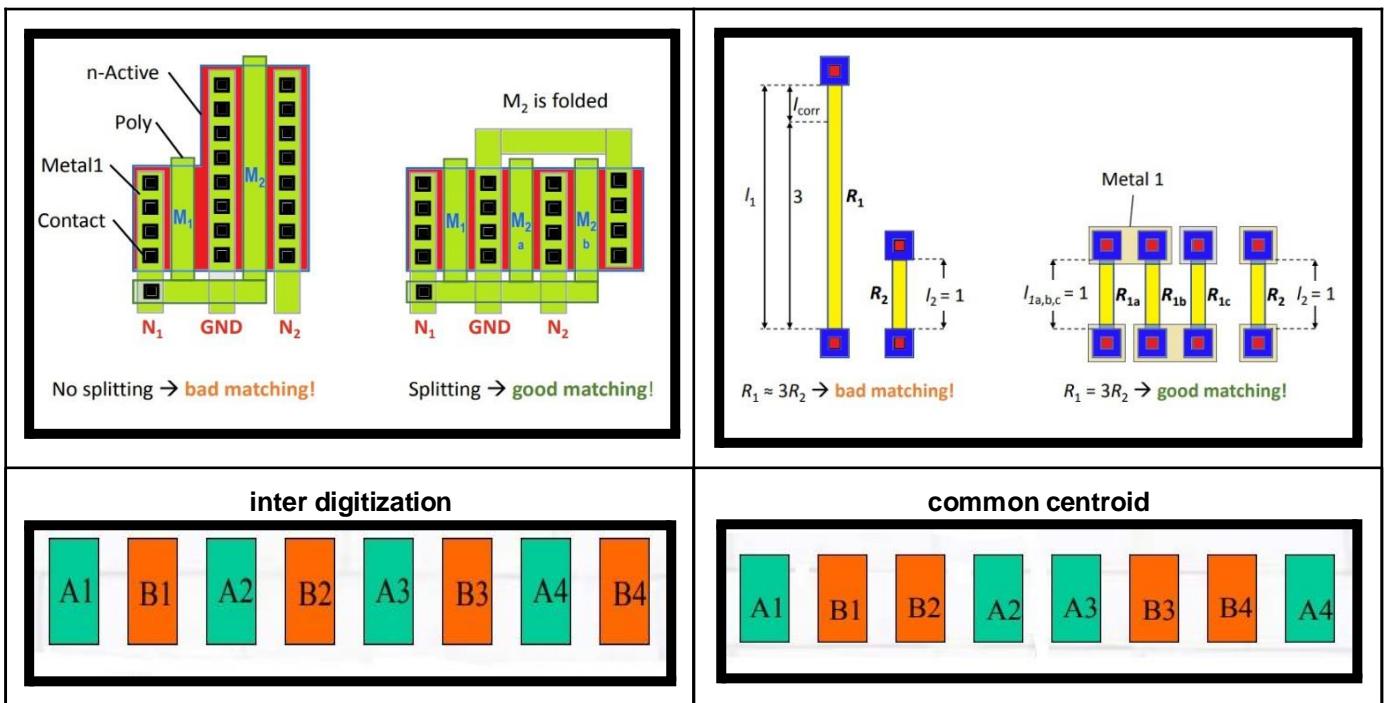


Fig 3.10 inter digitization & common centroid concept

Multiplier is one way of dividing the width of the MOSFET. There other way is to use fingers. The difference is that In multiplier we get separate MOSFET of small widths , whereas is finger we get a single MOSFET of small width. This single MOSFET cannot be used for inter digitization or common centroid technique. So we prefer multiplier over finger. These techniques are used in analog IC design, especially when you're designing matched pairs of devices, like in current mirrors, differential pairs, etc. Reduce Transistor mismatches (in W/L, threshold voltage, mobility, etc). They cancel out the effects of process gradients (e.g., doping variation, oxide thickness gradients) and temperature gradients across the chip. They ensure better symmetry in routing and parasitics, which leads to better performance. In inter digitization we place MOSFETs alternately. In common centroid we place MOSFETs symmetrically around a central point.

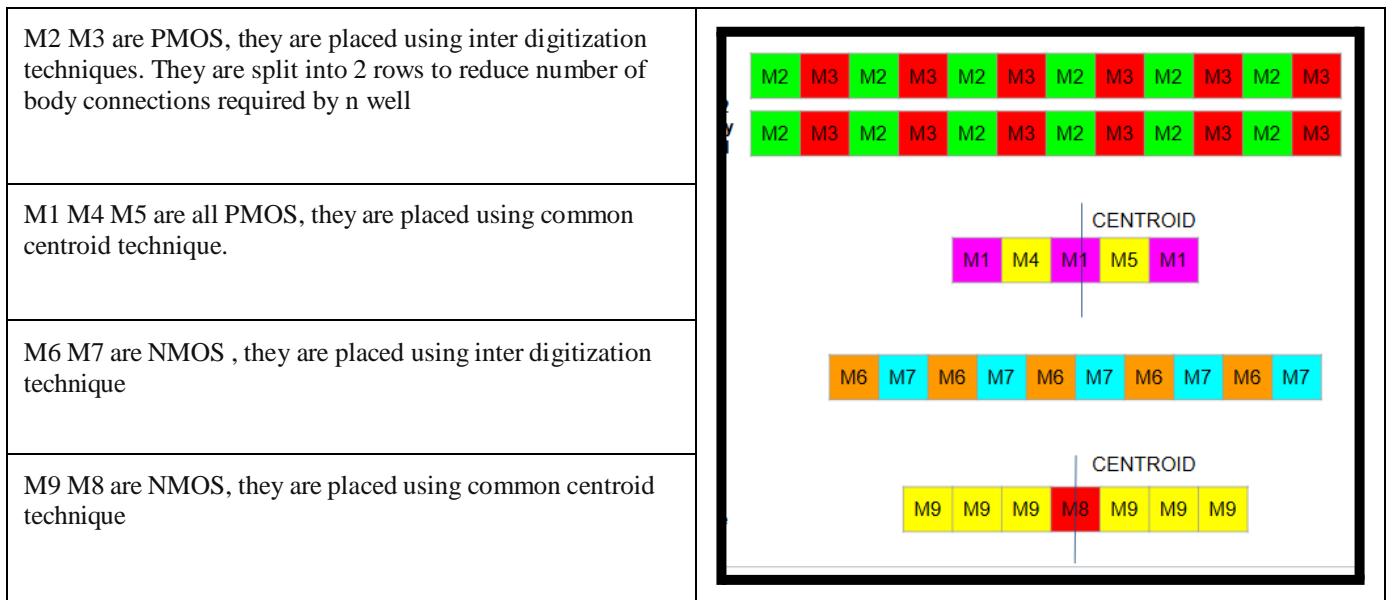


Fig 3.11 inter digitization & common centroid, theoretical implementation

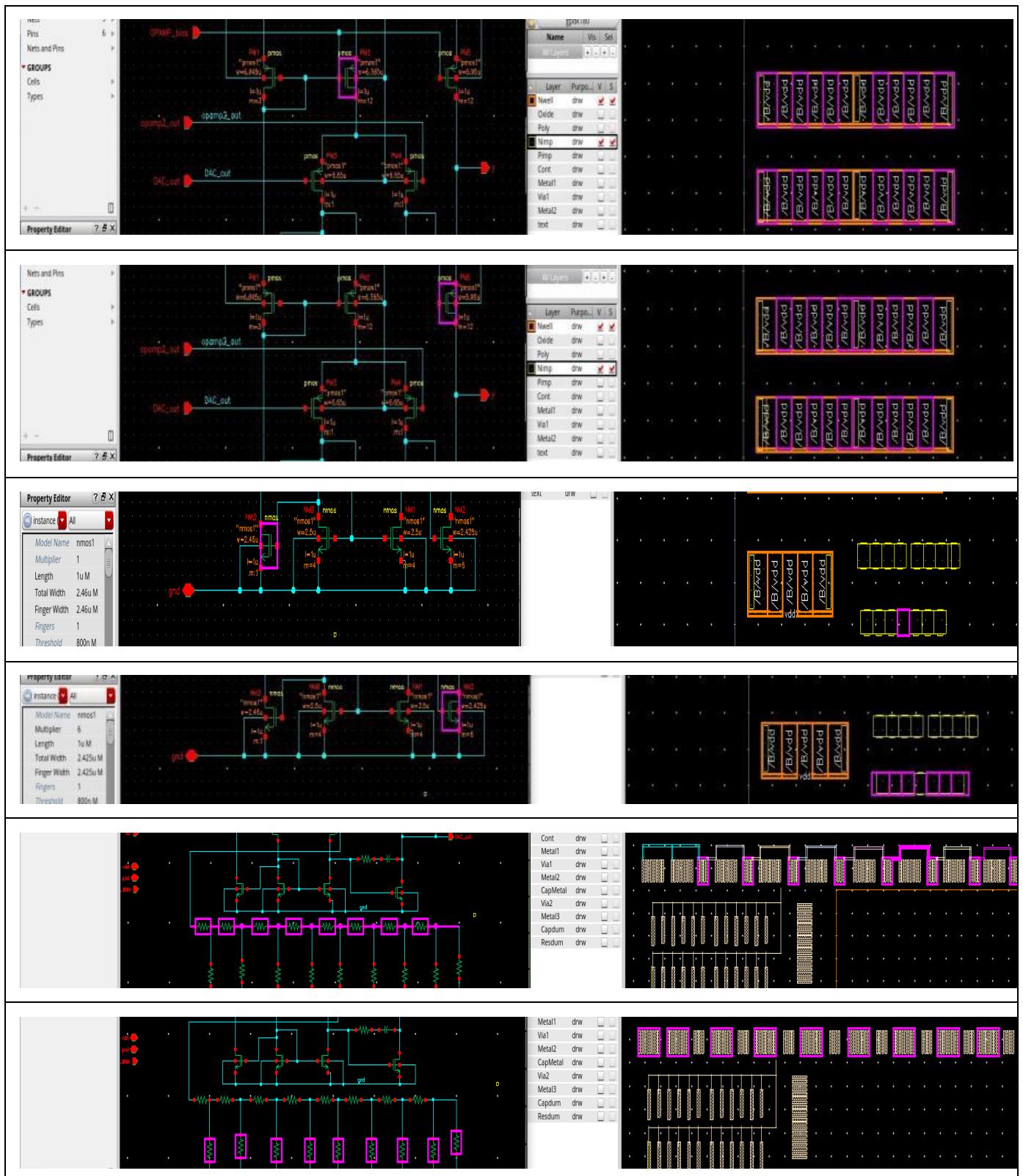


Fig 3.12 inter digitization & common centroid, practical implementation

Layout Verification Methods

DRC ensure the layout follows all the geometric and spacing rules defined by the semiconductor foundry. It Checks, Minimum metal width and spacing, Via and contact enclosure, Transistor gate enclosure, Well spacing and overlaps, Density rules (e.g., metal fill density). Violating any of these rules can lead to fabrication issues, reduced yield, or outright chip failure.

LVS ensure that the layout and schematic represent the same circuit — both in connectivity and device types/sizes. It Compares Netlist extracted from layout vs schematic netlist. it compares Device sizes, connections, and counts. it compare Ports and hierarchy. An LVS mismatch means your layout might be functionally incorrect, even if it passes DRC. LVS is always performed DRC check is successful.

Parasitic extraction provides resistance (R) and capacitance (C) values from the layout interconnects. It Provides RC values for each net or path, Coupling capacitance between net, Can also include inductance (RLC extraction in high-speed designs). These parasitics are fed into post-layout simulations to accurately model delays and power. Cadence tool Quantus is used for this purpose.

Post layout simulation is used to simulate the behavior of the circuit after including layout parasitics (resistance, capacitance). It Includes extracted RC values from layout. It May show delay, signal degradation, or functional changes that weren't visible in schematic simulation. It is Used For Functional verification & Performance validation (speed, power, delay). Cadence tool spectre is used for this purpose.

PVT analysis. PVT stands for process voltage temperature. It is used to evaluate circuit performance across all expected manufacturing and operating corner cases. Key Corners are - Process: TT (Typical), SS (Slow), FF (Fast), SF, FS. Voltage: Min/typical/max supply voltage. Temperature: -40°C to 125°C . Circuit must function reliably in real-world environments, not just under ideal lab conditions.

Thermal analysis is used to check for heat buildup in the chip, especially in dense or high-power regions. It Checks Temperature gradients across layout, Hot spots due to power-hungry blocks, Impact of temperature on performance / lifetime. Excess heat can cause timing failures, device degradation, or electromigration. Cadence tool called Celcius is used for performing this Thermal analysis.

Crosstalk analysis is used to identify undesired coupling between neighboring signal nets due to parasitic capacitance. Effects of crosstalk - Signal delay, False switching or glitches, Noise injection into sensitive analog circuit. Generally used for design of High-speed digital buses & Analog-mix-signal blocks. Cadence tool Tempus is used for this purpose.

STA analysis stand for static timing analysis. It is used to ensure all timing paths in a digital design, meet setup and hold time requirements without running dynamic simulations. It Checks - Setup time violations, Hold time violations, Clock skew, Worst-case paths (critical path delay). STA gives fast, corner-based timing verification across all PVT corners without running full simulations. Cadence tool Tempus is used for this purpose.

Chapter 4: Software Requirements

Chapter 4: Software Requirements

Software	Description
Cadence Virtuoso	Cadence Virtuoso is a widely used electronic design automation (EDA) software suite primarily used for designing and verifying complex integrated circuits (ICs) and semiconductor devices.

Library	Description
GPDK180	The GPDK (Generic Process Design Kit) 180 library is a commonly used set of design rules, models, and data for semiconductor device design and simulation. It is typically associated with 180-nanometer (nm) semiconductor manufacturing technology nodes.



Fig 4.1 Cadence tool

Chapter 5: Equipment Detail

Chapter 5: Equipment Details

5.1 Cadence Virtuoso

Cadence Virtuoso is a suite of electronic design automation (EDA) tools primarily used for designing integrated circuits (ICs) and other electronic systems. It's one of the most widely used tools in the semiconductor industry, offering a comprehensive set of features for design, simulation, verification, and layout of analog, digital, and mixed-signal circuits. Here's a detailed breakdown of its components and functionalities:

Schematic Entry: Virtuoso provides a user-friendly environment for creating schematics of electronic circuits. Engineers can draw circuit diagrams using a variety of predefined symbols representing components such as transistors, resistors, capacitors, and integrated circuit blocks. This schematic entry tool allows for hierarchical design, where complex circuits can be divided into smaller, more manageable blocks.

Simulation: Virtuoso includes powerful simulation engines for analyzing the behavior of circuits under different conditions. It supports various types of simulations including:

Analog Simulation: This involves simulating the behavior of analog circuits, such as amplifiers, filters, and oscillators. Common simulation techniques include transient analysis, AC analysis, DC sweep, and Monte Carlo analysis for statistical variations.

Digital Simulation: Virtuoso supports digital simulation for verifying the functionality of digital circuits, such as logic gates, flip-flops, and microprocessors. It can perform timing analysis, gate-level simulation, and functional verification.

Mixed-Signal Simulation: Virtuoso allows for the simulation of mixed-signal circuits, where analog and digital components are integrated. This is crucial for verifying the interaction between analog and digital domains in modern IC designs.

Layout Design: Virtuoso offers a layout editor for creating physical layouts of integrated circuits. Engineers can place components and interconnects on a silicon substrate while adhering to design rules and constraints. The layout editor provides features for routing signals, adding metal layers, and performing design rule checks (DRC) and layout versus schematic (LVS) checks to ensure the layout matches the schematic.

Design Rule Checking (DRC): DRC is a critical step in the design process where the layout is checked against a set of design rules specified by the semiconductor foundry. Virtuoso's DRC tool identifies violations such as minimum spacing, minimum width, and other geometric constraints to ensure the layout meets the foundry's requirements.

Layout vs. Schematic (LVS) Verification: LVS verification compares the schematic netlist with the layout netlist to ensure they match accurately. This helps identify any discrepancies between the intended circuit design and its physical implementation. Virtuoso's LVS tool ensures that the layout faithfully represents the original circuit design.

Custom IC Design Flows: Virtuoso supports custom IC design flows tailored to specific technologies and design methodologies. It provides flexibility for integrating third-party tools, scripting, and automation to streamline the design process and improve productivity.

Integration with Other Tools: Virtuoso integrates with various other EDA tools and design environments to provide a comprehensive IC design solution. This includes tools for synthesis, place and route, physical extraction, and electromagnetic simulation, among other

5.2 GPDK 180nm technology:

The GPDK180 process library, short for "Generic Process Design Kit 180nm," is a standardized semiconductor process technology offered by semiconductor foundries and design tool vendors, including Cadence, for designing integrated circuits (ICs). It provides a set of design rules, device models, and technology files tailored for the fabrication of CMOS (Complementary Metal-Oxide-Semiconductor) ICs with feature sizes down to 180 nanometers.

Detailed description of the GPDK180 process library:

Feature Size and Technology Node: The "180nm" in GPDK180 refers to the minimum feature size, typically the gate length of transistors, which is 180 nanometers. This represents the critical dimension of the semiconductor manufacturing process used to fabricate ICs. While 180nm technology is considered relatively mature compared to more advanced nodes like 65nm or 7nm, it remains widely used for various applications, particularly in the fields of analog and mixed-signal design.

Design Rules: The GPDK180 process library defines a comprehensive set of design rules that specify the constraints and guidelines for designing IC layouts. These rules cover parameters such as minimum feature sizes, spacing requirements, layer stack-ups, and other geometric constraints essential for ensuring manufacturability and reliability of the fabricated ICs. Designers must adhere to these rules to avoid potential manufacturing defects and ensure compatibility with the semiconductor foundry's manufacturing processes.

Device Models: GPDK180 provides accurate models for various semiconductor devices used in IC design, including MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors), resistors, capacitors, and diodes. These models describe the electrical behavior of devices under different operating conditions, such as DC bias, AC signals, and temperature variations. The accuracy of these device models is crucial for simulation and verification of IC designs using tools like Cadence Virtuoso.

Process Design Kits (PDKs): The GPDK180 process library is typically distributed as a Process Design Kit (PDK), which includes technology files, device models, design rules, and documentation necessary for IC design. Designers use these PDKs within EDA tools like Cadence Virtuoso to develop, simulate, and verify their IC designs. The PDKs provide a standardized framework that enables designers to work seamlessly across different design environments and foundries, ensuring design portability and interoperability.

Analog and Mixed-Signal Design Support: GPDK180 is well-suited for analog and mixed-signal IC design due to its mature process technology and comprehensive device models. Designers can leverage this process library to create high-performance analog circuits such as amplifiers, filters, voltage regulators, and data converters. Additionally, the library supports the integration of analog and digital circuits on the same chip, enabling the development of complex mixed-signal systems-on-chip (SoCs) for applications in communications, automotive, and industrial electronics.

Manufacturing Compatibility: The GPDK180 process library is designed to be compatible with the manufacturing processes of semiconductor foundries offering 180nm CMOS fabrication services. This ensures that IC designs developed using GPDK180 can be readily manufactured without requiring significant process modifications or adjustments. It also facilitates the seamless transition from design to fabrication, reducing time-to-market and overall development costs for semiconductor products.

In summary, the GPDK180 process library provides a robust and standardized platform for designing CMOS ICs with feature sizes down to 180 nanometers. It offers comprehensive design rules, accurate device models, and manufacturing compatibility, making it a preferred choice for analog and mixed-signal IC design in various industries. Designers can leverage GPDK180 within EDA tools like Cadence Virtuoso to develop high-performance and reliable semiconductor products for diverse applications.

Chapter 6: Project Implementation Schedule

Chapter 6: Project Implementation Schedule

The schedule for our Project was planned and executed as follows:

Table 6.1 plan of implementation

Timeline	Task
September 2024	reading research papers & doing literature review
October 2024	designing SAR register
November 2024	designing OPAMP
December 2024	using OPAMP to make comparator , DAC, SH
January 2025	connecting all 4 blocks to complete ADC
February 2025	doing Layout of ADC

Chapter 7: Project Methodology

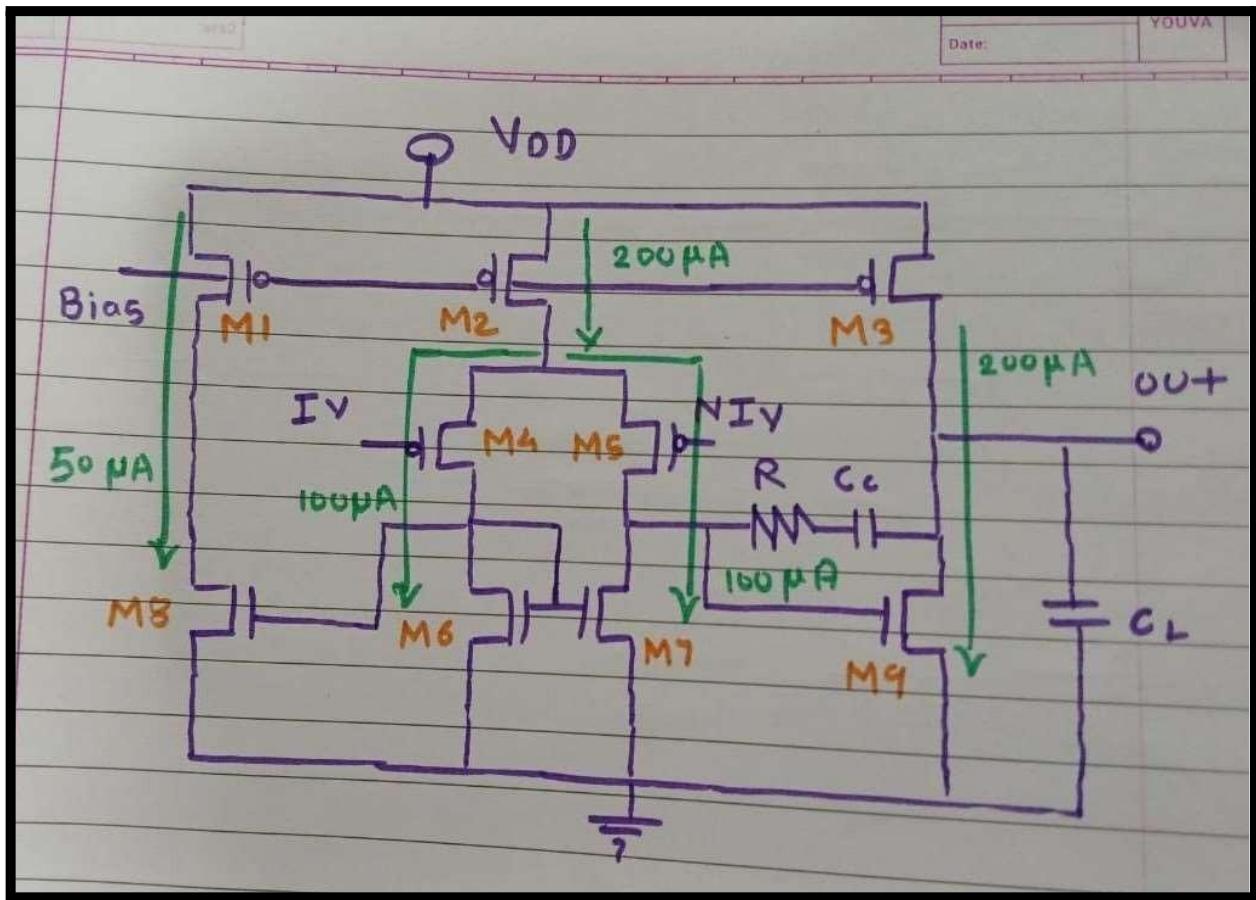


Fig 7.1 OPAMP hand drawn circuit

Table 7.1 - OPAMP - MOSFET sizing table

MOSFET	M2	M4 M5	M6 M7	M9	M1	M8	M3
LENGTH	1u	1u	1u	1u	1u	1u	1u
TOTAL WIDTH	76.39u	6.65u	10u	14.55u	18.14u	2.46u	71.2u

MOSFET Sizing Procedure

let the open loop gain > 60 dB
 phase margin has to be > 60 degree for stability
 conversion time < 60 ns

let us fix power dissipation

< 2 mW P < 2 mW

VI < 2 mV

I < 2 / 3.3 = 606 mA

let us fix our total current to be 450 mA

the distribution of current flowing via different MOSFETs is as

follows current via M1 M8 is 50 uA

current via M2 is 200 uA

current via M4 M6 M5 M7 is

100 uA current via M3 M9 is

200 uA

Table 7.2 - MOSFET M2 (PMOS)

$V_{gs} < V_{th}$	$V_{ds} < V_{gs} - V_{th}$	V_g	W
$V_{sg} > V_{th}$	$-V_{sd} > -V_{sg} - V_{th}$	2.6	+ 100 μ
$V_s - V_g > V_{th}$	$-V_d > -V_g - V_{th}$	2.50	58.53 μ
$3.3 - V_g > 0.5$	$-3 > -V_g - 0.5$	2.55	76.39 μ
$V_g < 2.8$	$V_g > 2.5$		

Table 7.3 MOSFET M4 M5 (PMOS)

$V_{sg} > V_{th}$	$-V_d > -V_g - V_{th}$	V_s	V_d	W
$V_s - V_g > V_{th}$	$-V_d > -1.65 - 0.5$	3	0.6	6.65 μ
$V_s - 1.65 > 0.5$	1.65 is mid value of 3.3	3	0.65	6.65 μ
1.65 is mid value of 3.3	$-V_d > -2.15$	3	0.7	6.66 μ
$V_s > 2.15$	$V_d < 2.15$			
Form above table $V_s = 3$ which satisfy the condition				

Table 7.4 MOSFET M6 M7 (NMOS)

$V_{gs} > V_{th}$	$V_{ds} > V_{gs} - V_{th}$	V_g	W
$V_g - V_s > V_{th}$	$V_d > V_g - V_{th}$	0.6	12.97 μ
$V_g - 0 > 0.5$	However $V_g = V_d$	0.65	10.43 μ
$V_g > 0.5$	$V_g > V_g - 0.5$	0.7	18.51 μ
		0.75	21.37 μ

Table 7.5 MOSFET M9 (NMOS)

$V_{gs} > V_{th}$	$V_{ds} > V_{gs} - V_{th}$	V_g	W
$V_g - V_s > V_{th}$	$V_d > V_g - V_{th}$	0.72	14.52 μ
$V_g - 0 > 0.5$	1.65 is mid value of 3.3		
$V_g > 0.5$	$1.65 > V_g - 0.5$		
	$V_g < 2.15$		

Table 7.6 MOSFET M3 (PMOS)

V _{sg} > V _{th} V _s - V _g > V _{th} 3.3 - V _g > 0.5 V _g < 2.8	-V _{sd} > -V _{sg} - V _{th} -V _d > -V _g - V _{th} -1.65 > -V _g - 0.5 1.65 is mid value of 3.3 -V _g < -1.15 V _g > 1.15	V _g 2.55	W 71.13 u
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Table 7.7 MOSFET M1 (PMOS)

V _{sg} > V _{th} V _s - V _g > V _{th} 3.3 - V _g > 0.5 V _g < 2.8	-V _{sd} > -V _{sg} - V _{th} -V _d > -V _g - V _{th} However V _d = V _g -V _g > -V _g - 0.5 V _g < V _g + 0.5	V _g 2.50 2.55	W 13.63 u 18.14 u
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Table 7.8 MOSFET M8 (NMOS)

V _{gs} > V _{th} V _g - V _s > V _{th} V _g - 0 > 0.5 V _g > 0.5	V _{ds} > V _{gs} - V _{th} V _d > V _g - V _{th} V _d > V _g - 0.5	V _g	V _d	W
		0.6	2.5	2.46 u
		0.6	2.55	2.42 u
		0.65	2.5	1.19 u
		0.65	2.55	1.17 u

$$R = (C_l + C_c) / G_m * C_c$$

$$R = (1p + 1p) /$$

$$1.36533 * 1p R =$$

$$1.47K$$

Chapter 8: Applications

Chapter 8: Applications

1. Consumer Electronics

SAR ADCs are frequently used in various consumer electronic devices like smartphones, tablets, digital cameras, and audio equipment. In these applications, they play a crucial role in converting analog signals from sensors, microphones, and other analog interfaces into digital signals that can be processed by digital circuits. For example, in digital audio systems, SAR ADCs convert analog audio signals into digital data for processing, enhancing audio quality and enabling features like noise cancellation.

2. Medical Devices

In medical instrumentation, SAR ADCs are used in devices such as electrocardiogram (ECG) machines, blood pressure monitors, and pulse oximeters. These devices rely on accurate and fast analog-to-digital conversion to monitor patients' vital signs. For instance, in ECG machines, the SAR ADCs convert the electrical signals from the heart into a digital form, allowing doctors to analyze the heart's rhythm and detect abnormalities. Their high resolution and precision make them ideal for capturing subtle variations in biological signals.

3. Automotive Applications

The automotive industry also leverages SAR ADCs in various systems for both safety and convenience. They are used in advanced driver-assistance systems (ADAS) such as lane-keeping assist, parking sensors, and collision detection. SAR ADCs convert signals from sensors like radar, lidar, or ultrasonic transducers into digital data that can be processed by onboard computers for real-time decision-making. In electric vehicles, SAR ADCs are essential for monitoring battery voltages and current, ensuring safe and efficient battery operation.

4. Industrial Automation

In industrial control systems, SAR ADCs are used for process monitoring, automation, and control. Many industrial applications require the conversion of analog signals from temperature sensors, pressure sensors, or flow meters into digital signals to control machinery or trigger safety mechanisms. SAR ADCs' speed and resolution make them suitable for these applications, where precise data conversion is crucial for optimizing performance and ensuring safety in real-time operations.

Chapter 9: Results and Discussion

9.1 Results

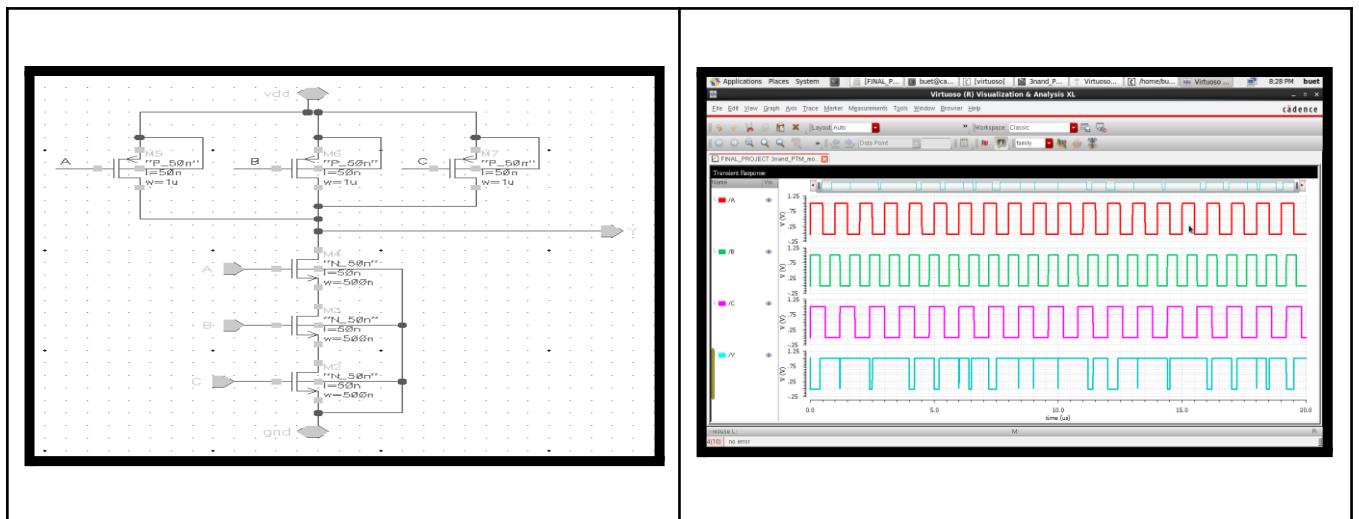


Fig 9.1 three input nand gate circuit

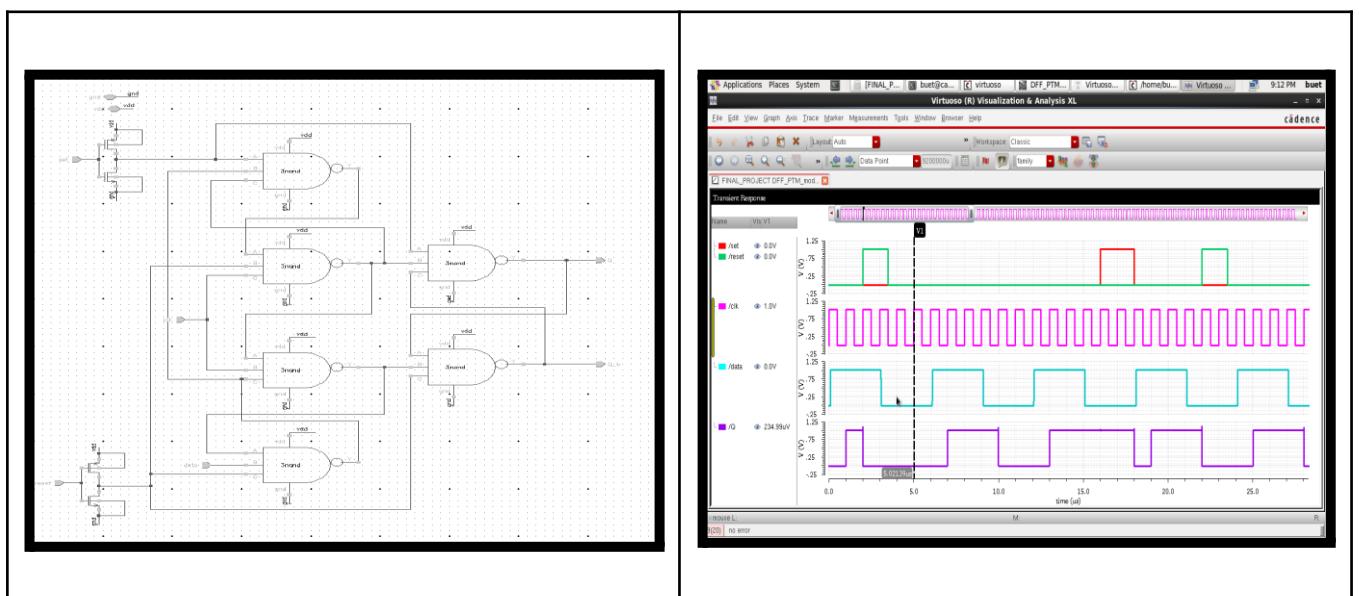


Fig 9.2 d flip flop circuit

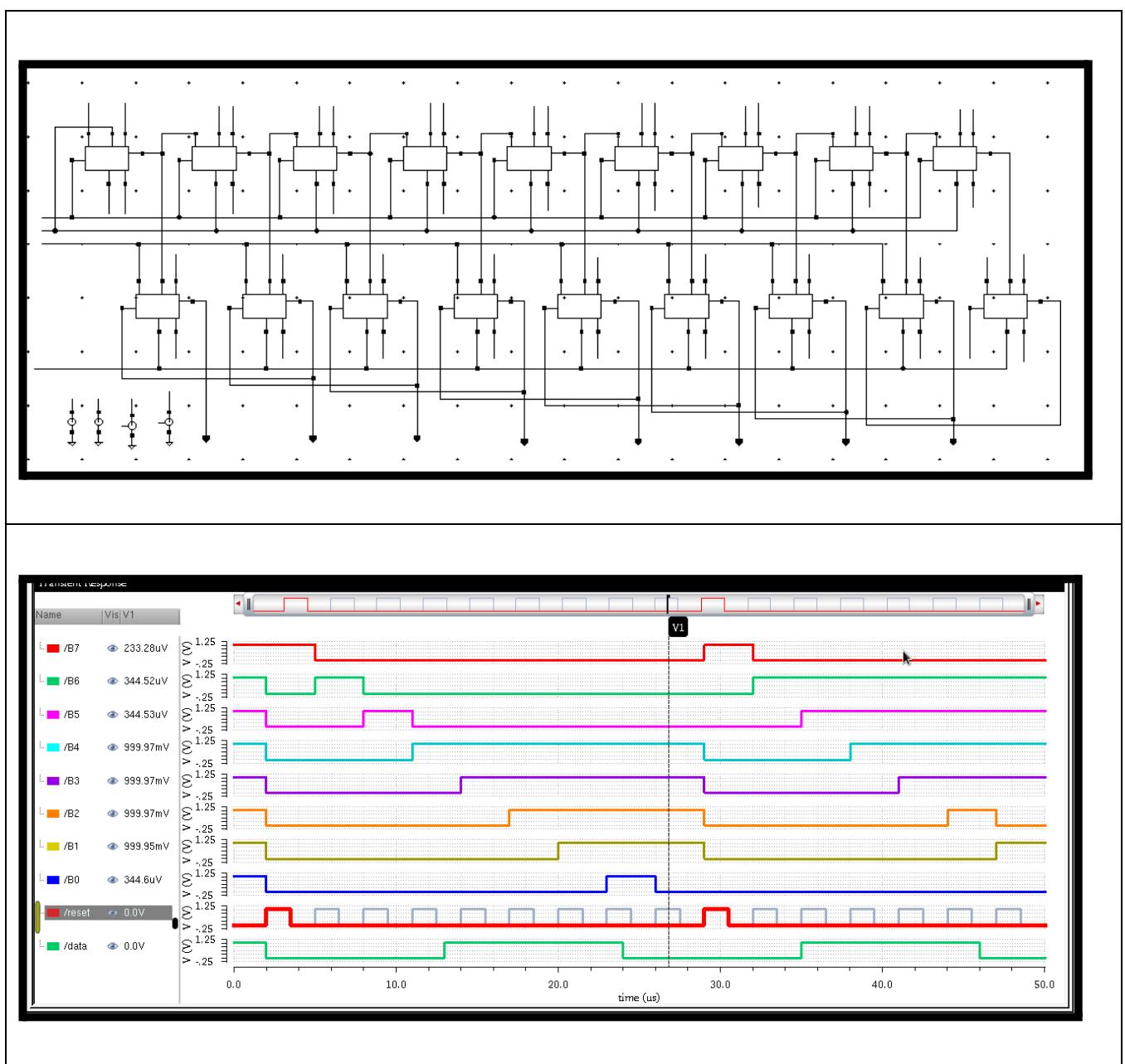


Fig 9.3 SAR register circuit

Table 9.1 OPAMP design parameters - theoretical & practical

Parameter	Theoretical Value	Practical value
Supply voltage	3.3 v	3.3 v
Phase margin	PM > 60 dB	180 - 94 = 86 dB
Power dissipation	PD < 2mW	= (50 + 200 + 200) * 3.3 = 1.485 mW
Settling time	Ts < 40ns	56.159 ns
gain bandwidth product	NA	33 MHz
open loop gain	NA	73.8 dB
unity gain frequency	NA	28.99 MHz
phase angle	NA	93.57 degree
slew rate	NA	4.808 KV / us

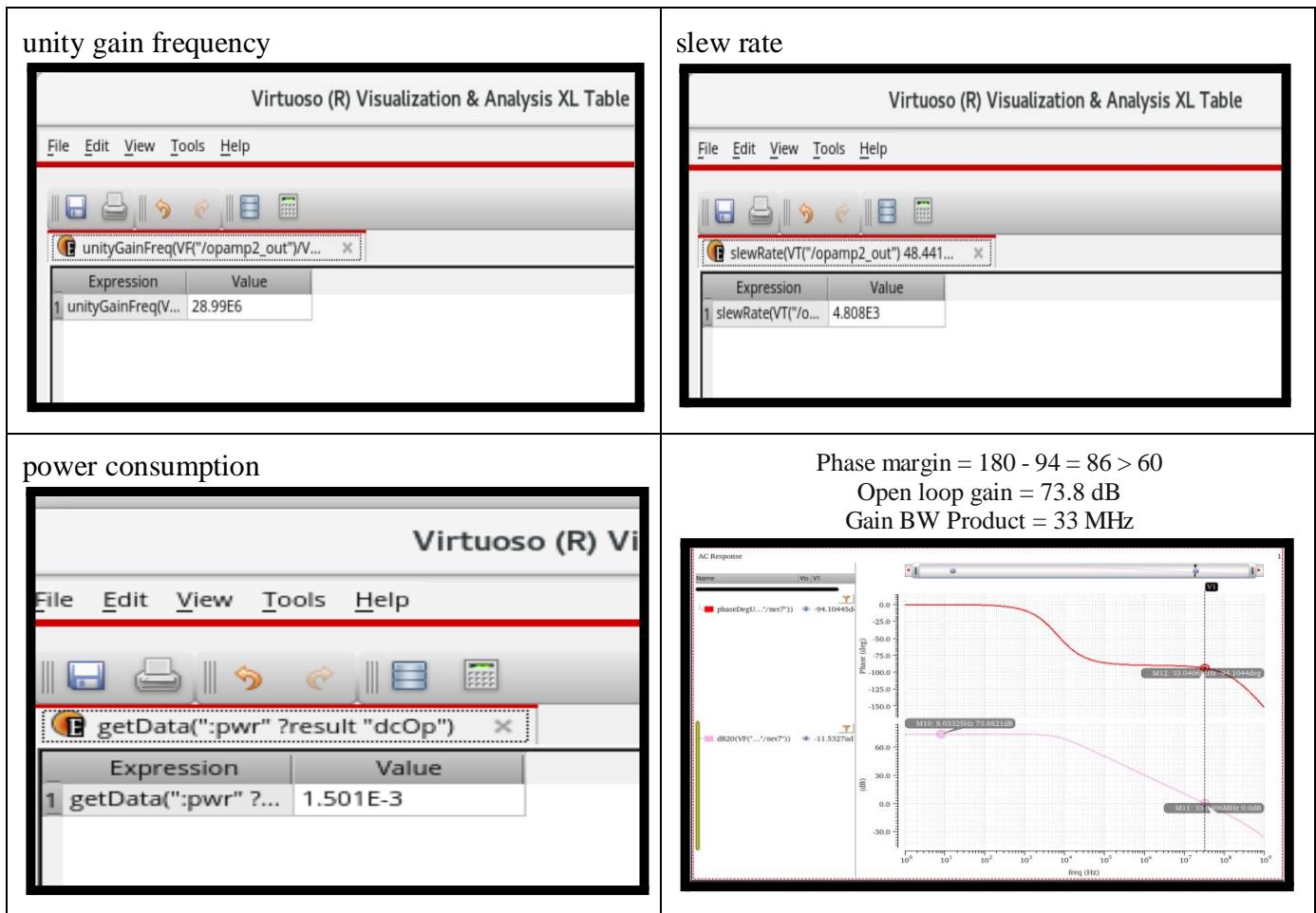


Fig 9.4 OPAMP results 1

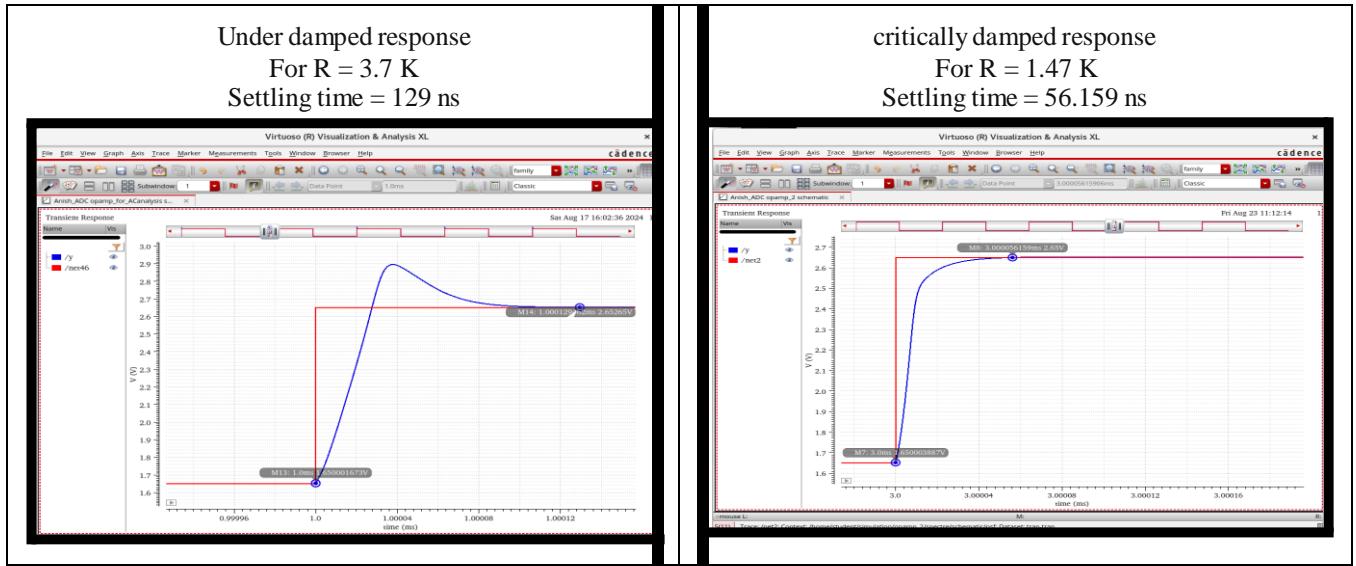


Fig 9.5 OPAMP results 2

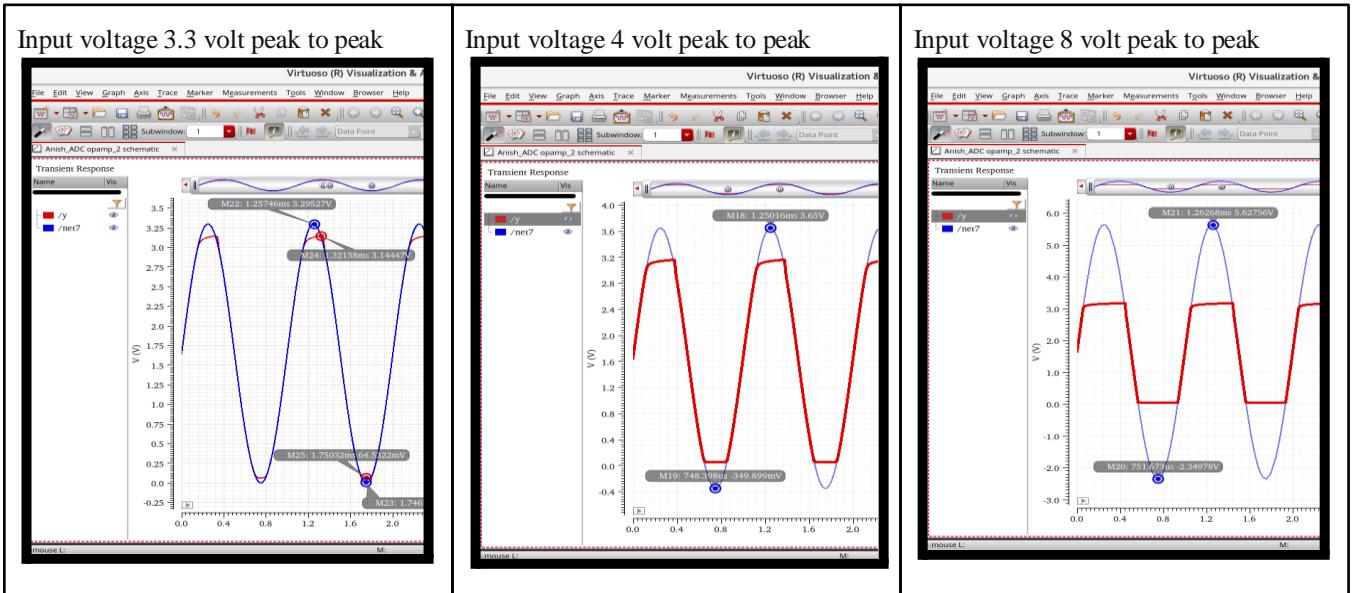


Fig 9.6 OPAMP results 3

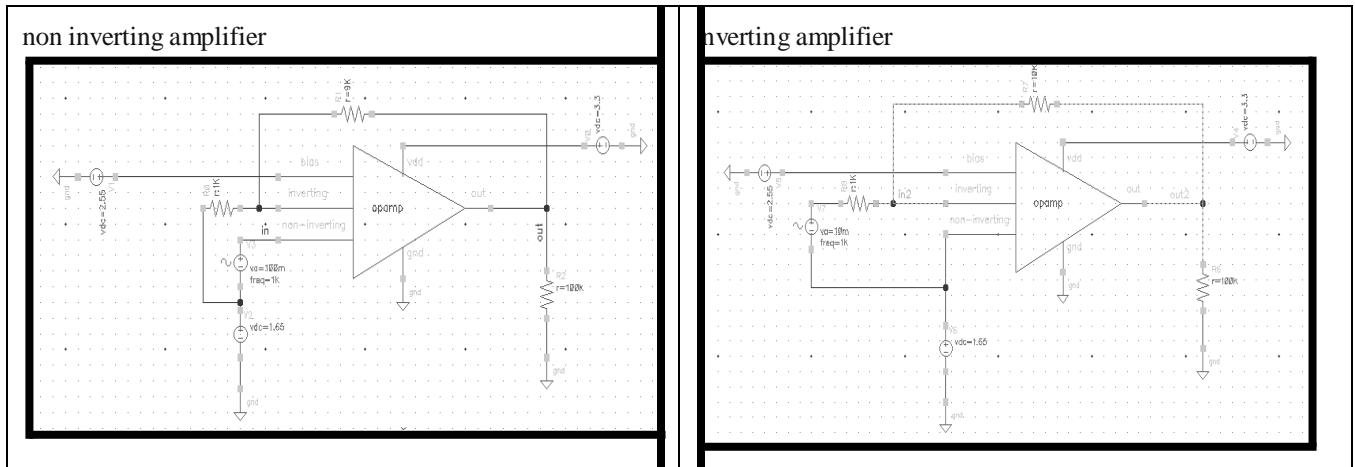


Fig 9.7 OPAMP results 4

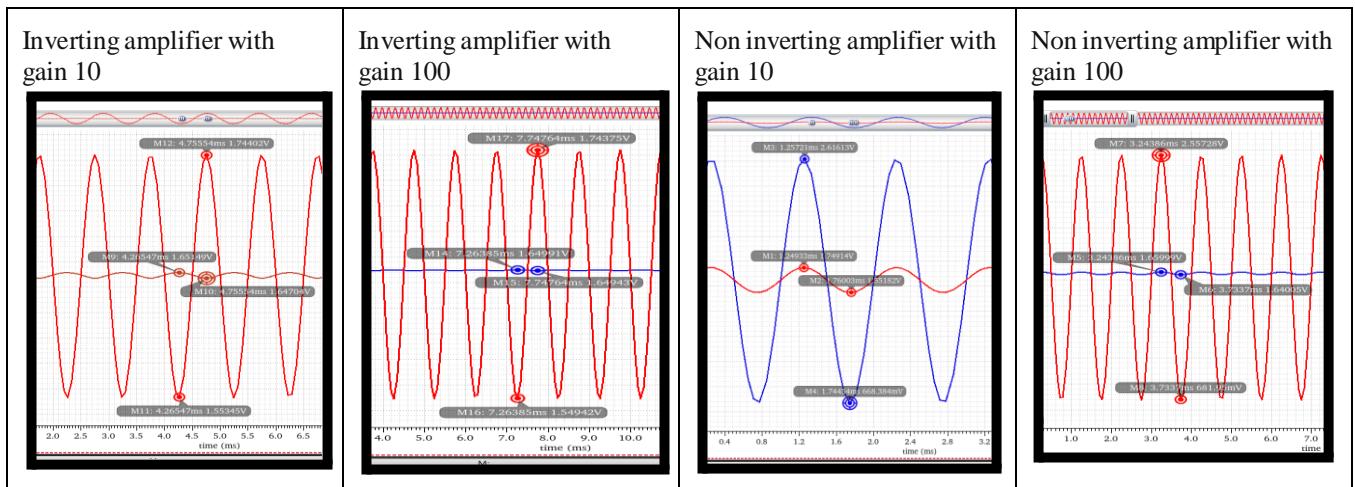


Fig 9.8 OPAMP results 5

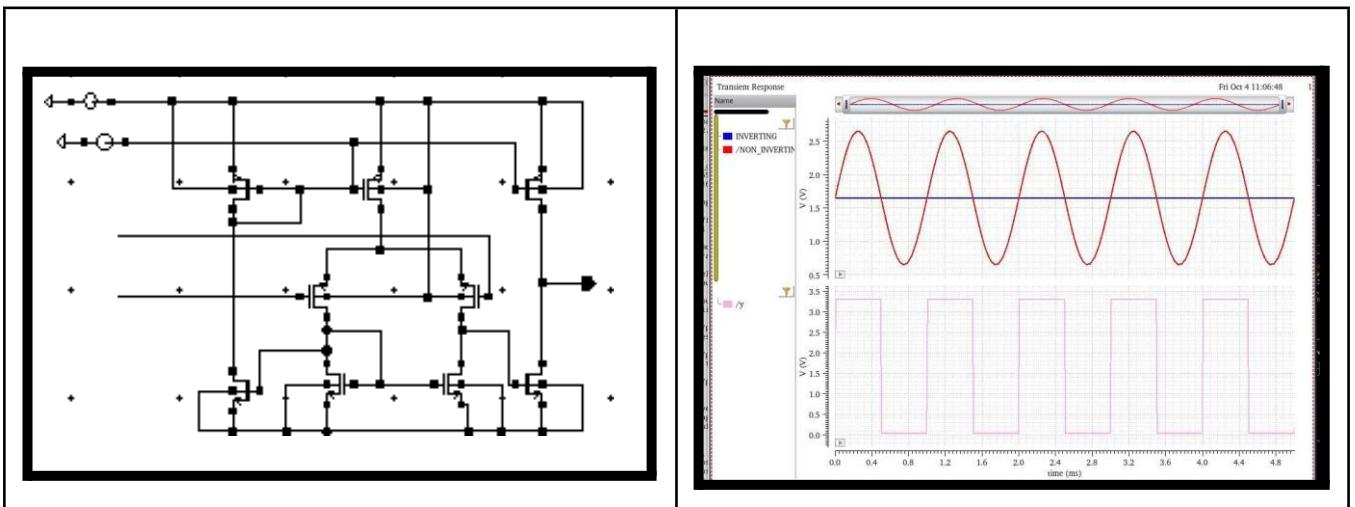
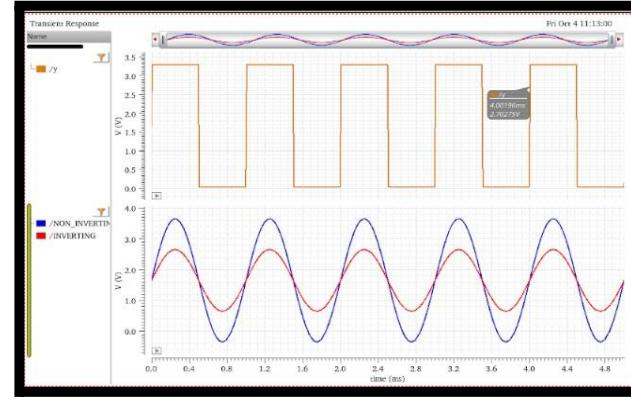


Fig 9.9 comparator results 1

Transient Analysis 1

If NIV > IV then output = 3.3

If NIV < IV then output = 0



time = 1.7212756 - 1.7161337 us

time = 0.0051419 us

time = 5.1419 n

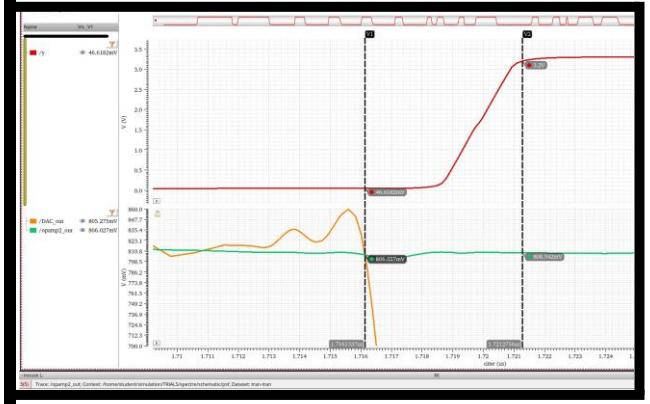


Fig 9.10 comparator results 2

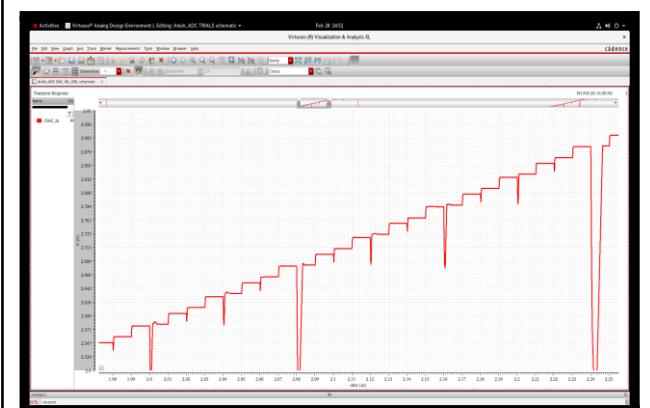
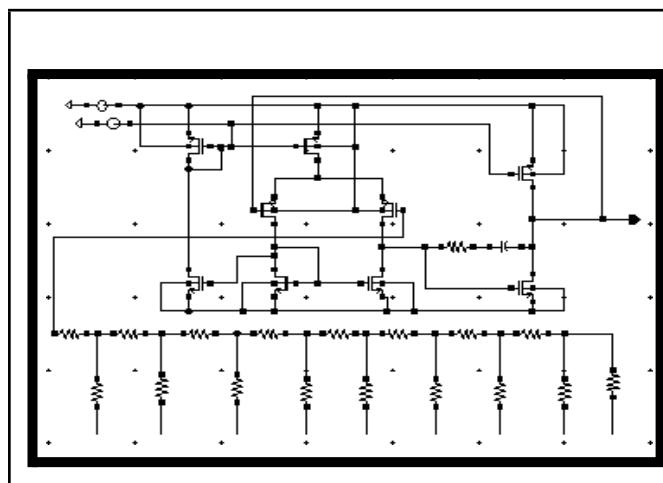
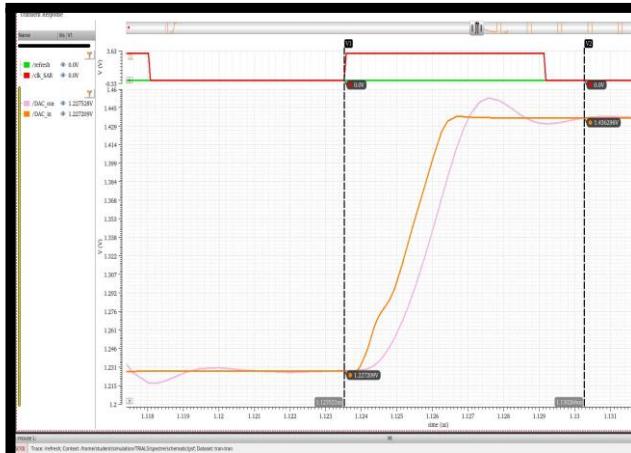


Fig 9.11 DAC results 1

Settling time = $1.130266 - 1.12352$ us
 Settling time = 0.006746 us
 Settling time = 6.746 ns



digital input = 0000,1111
 SB value = $1 * (3.3) / 256 = 0.01289$
 analog (theoretically) = $15 * (3.3) / 256 = 0.1933$ v
 analog (practically) = 0.194868 V

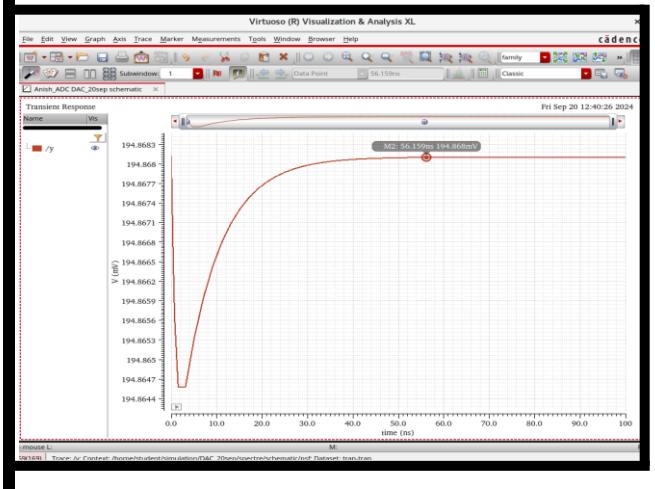


Fig 9.12 DAC results 2

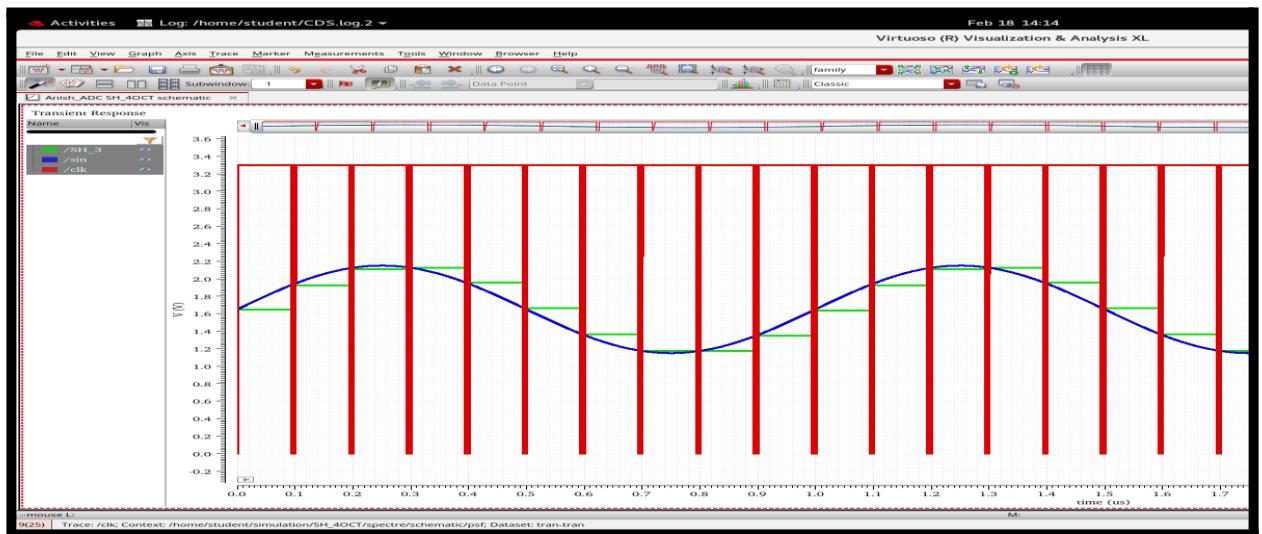
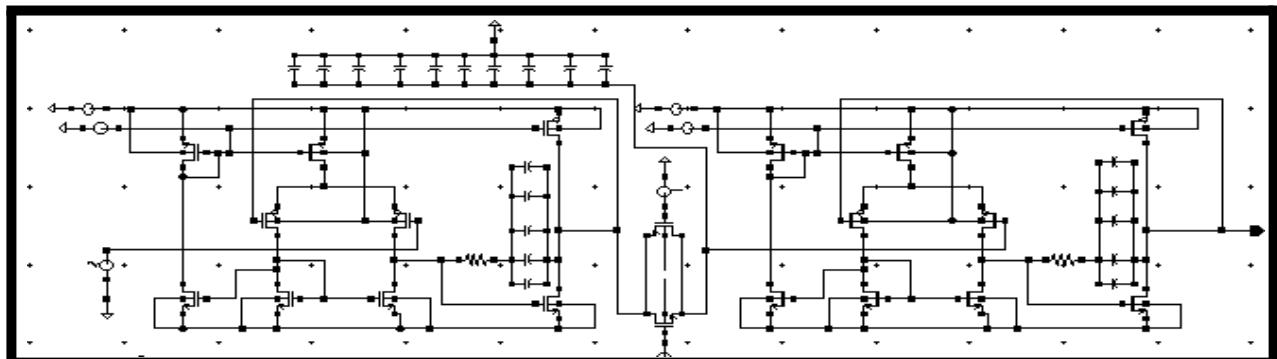


Fig 9.13 Sample & Hold result 1

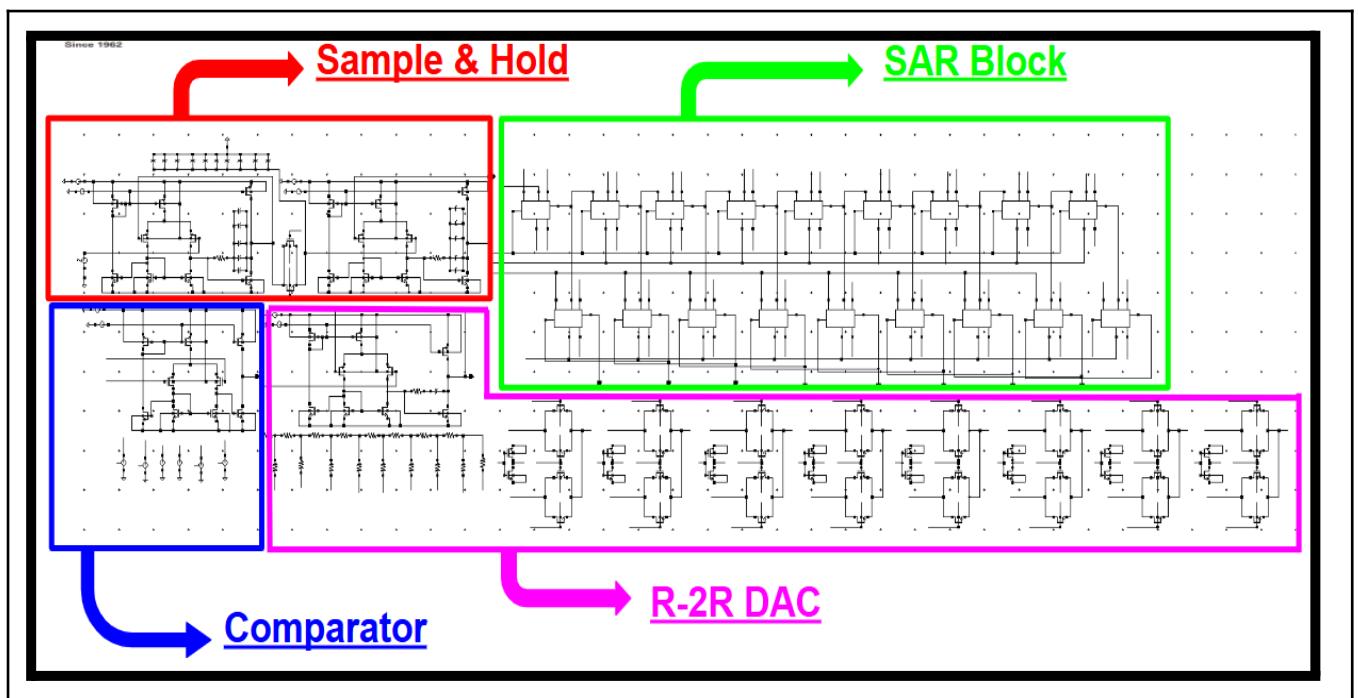


Fig 9.14 complete ADC circuit

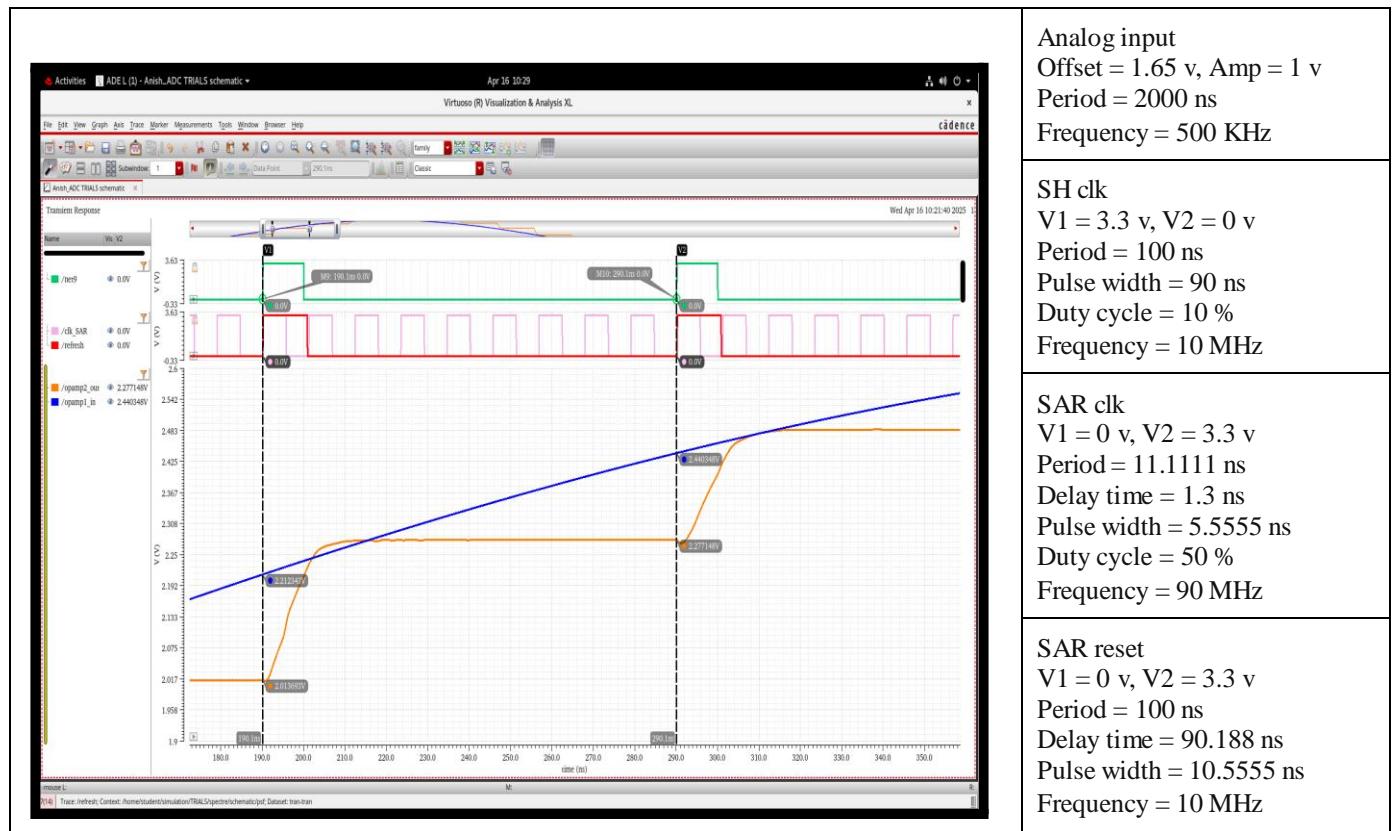


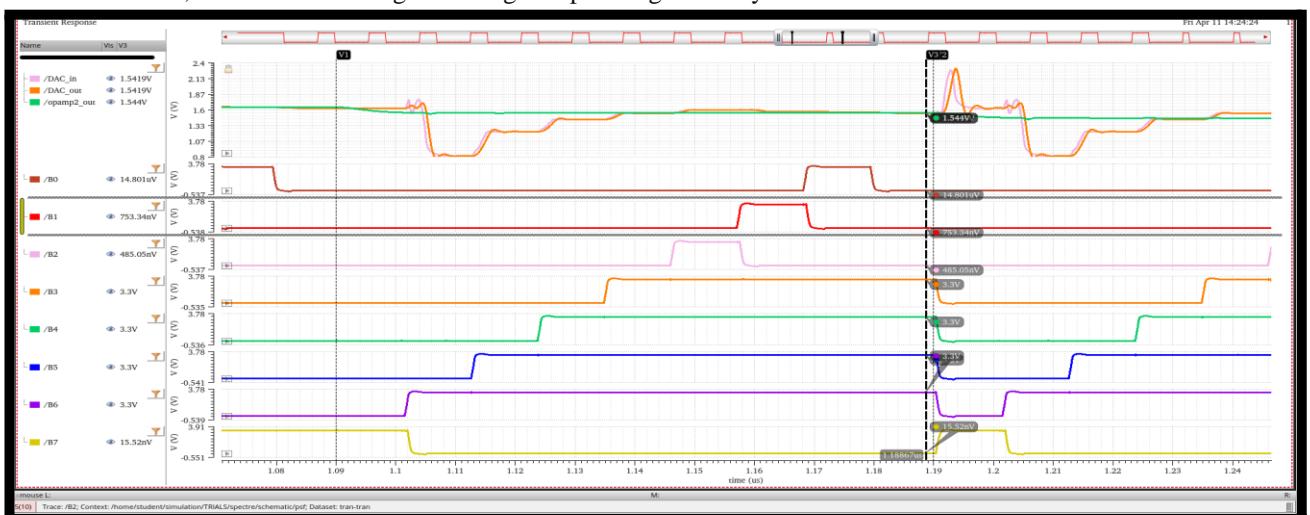
Fig 9.15 complete ADC timing diagram

Sample output signal = 1.544 V

DAC output signal = 01111000 = 120(3.3) / 167

DAC output signal = 1.546875 V

Error = 0.002875, this shows reducing the voltage drop has significantly reduced error



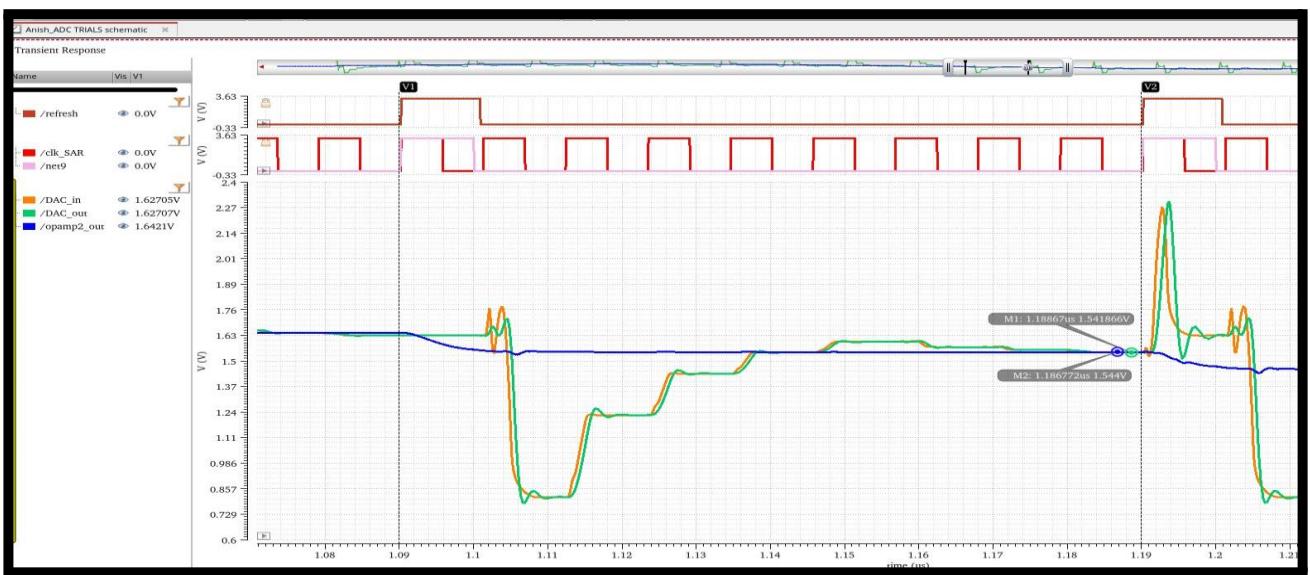
Sample circuit signal = 1.544 V

DAC circuit signal = 1.541866 V

Error = 0.002134 V

LSB = $3.3 / 2^8 = 3.3 / 256 = 0.01289$ V

Error is approximately plus minus 0.1 LSB



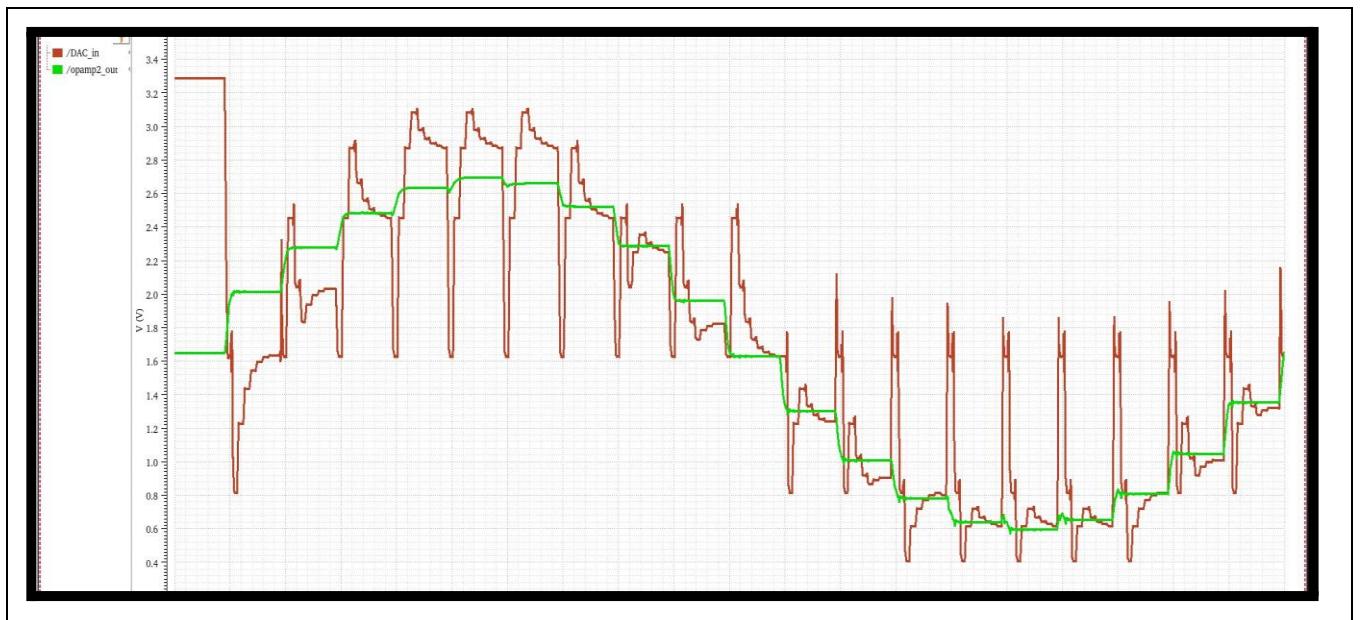
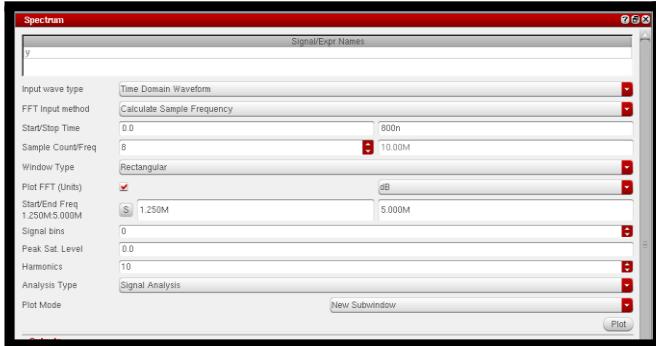


Fig 9.16 complete ADC result 1

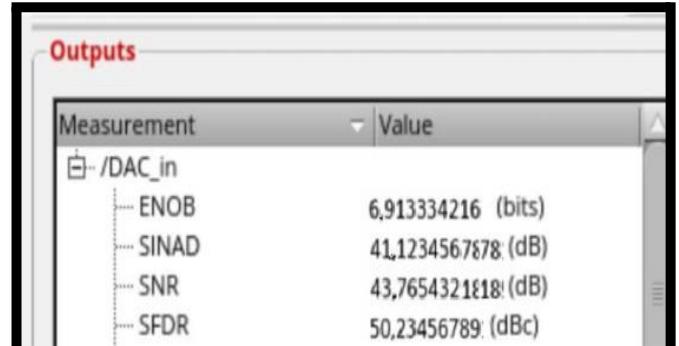
Table 9.2 comparison between our ADC & ADC given in different research papers

Sr. No.	Parameters	This Work	Paper [5]	Paper 2 [6]	Paper [7]	Paper [8]	Paper [9]
1	Technology Node (nm)	180	180	65	90	40	90
2	Resolution (Bits)	8	8	14	6	10	10
3	Sampling Rate (kS/s or MS/s)	10Mhz	100MS/s	5GS/s	1MS/s	120MS/s	1M/s
4	Supply Voltage	3.3V	1.8V	1	1V	1.2V	1.2V
5	Power Consumption	8.332mW	129.8uW	70uW	77.26	1.04mW	11.88uW
6	ENOB (Effective No. of Bits)	7	NA	NA	5.05	NA	NA
7	SNR (dB)	43.76	NA	NA	37.34	NA	NA
8	SFDR (dB)	50.23	NA	NA	NA	NA	NA
9	SNDR (dB)	41.12	NA	NA	NA	46.9	NA
10	Architecture	SAR R-2R	Binary weighted capacitive	Capacitive	Binary weighted resistor	NA	Capacitive (with attenuation)
11	Tool Used	Cadence	Cadence	NA	Cadence	NA	Cadence

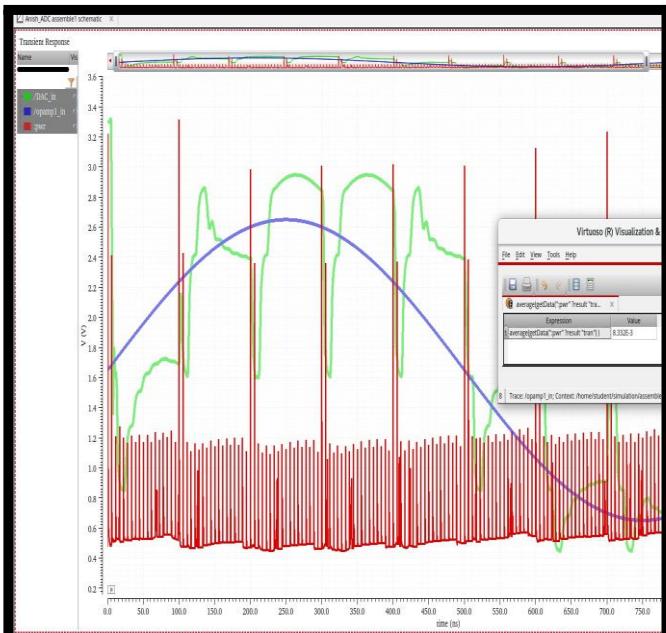
spectrum analysis window



ENOB , SNR (db), SNDR (db) , SFDR (db)



power consumption of ADC



spectrum analysis waveform

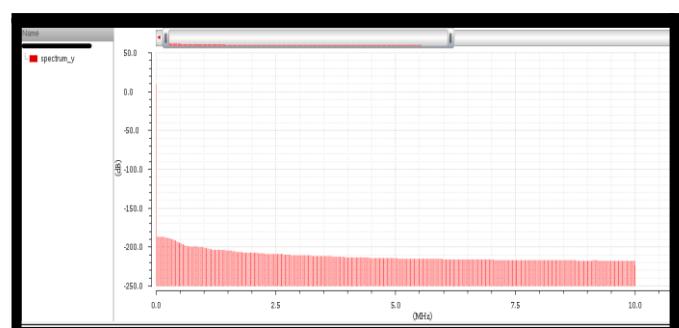
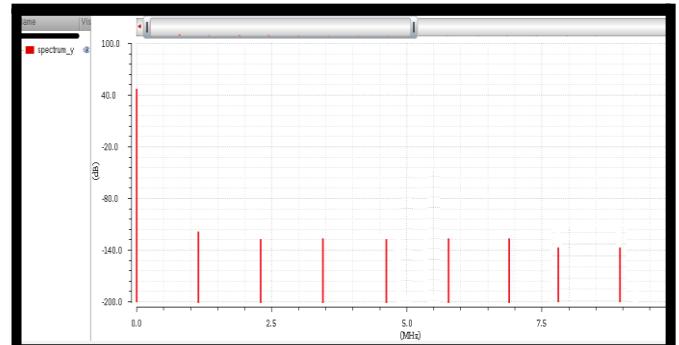
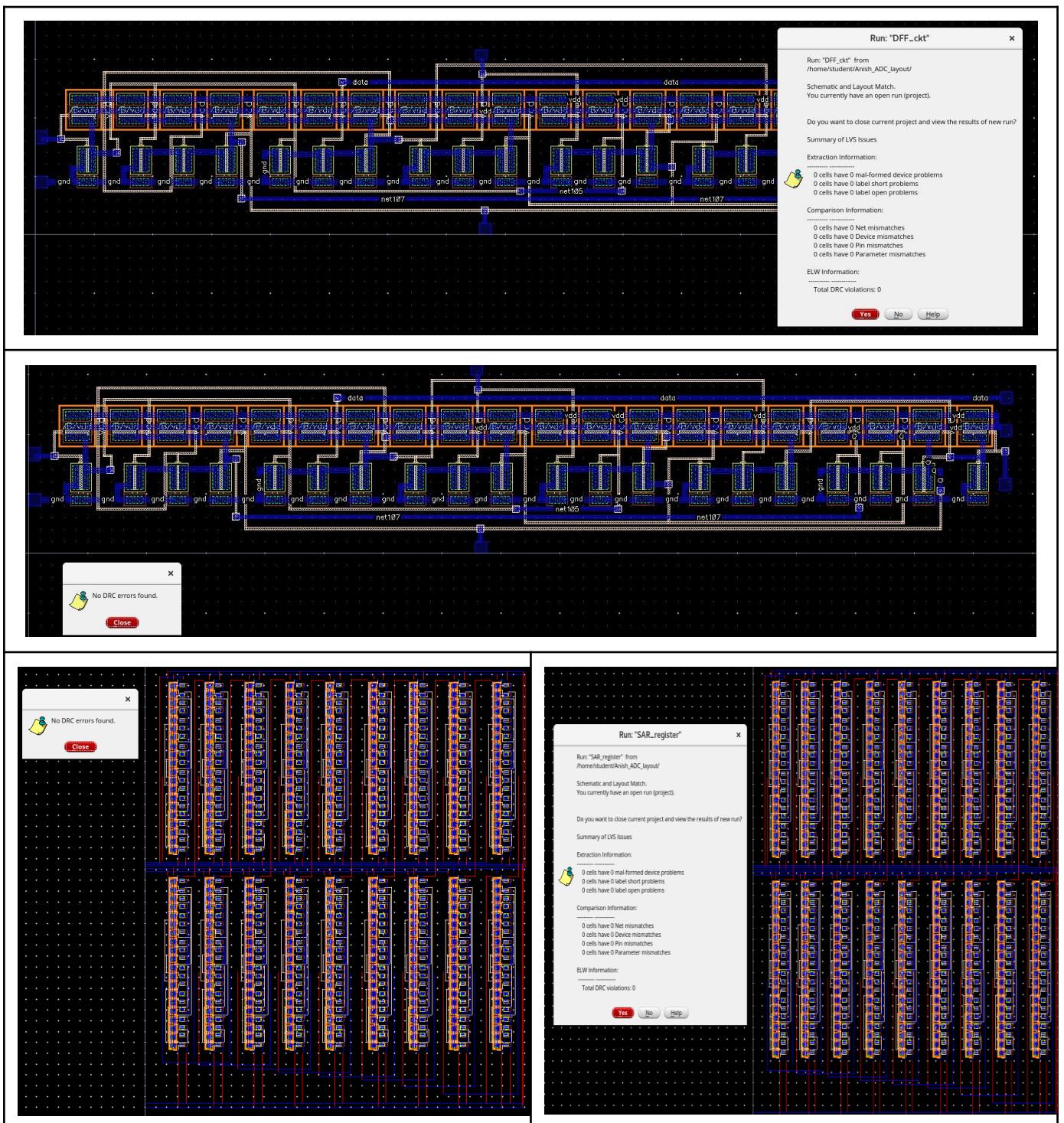
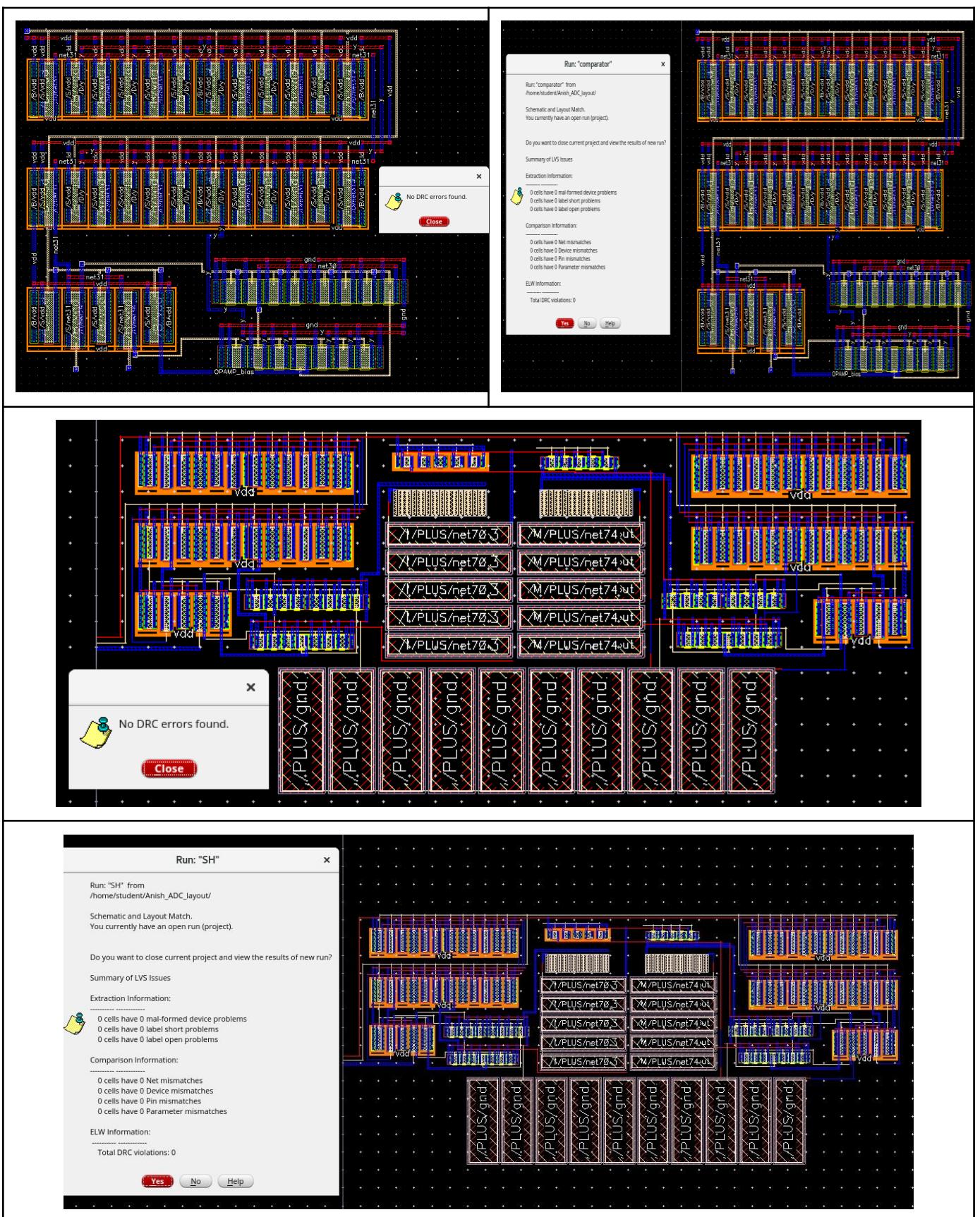
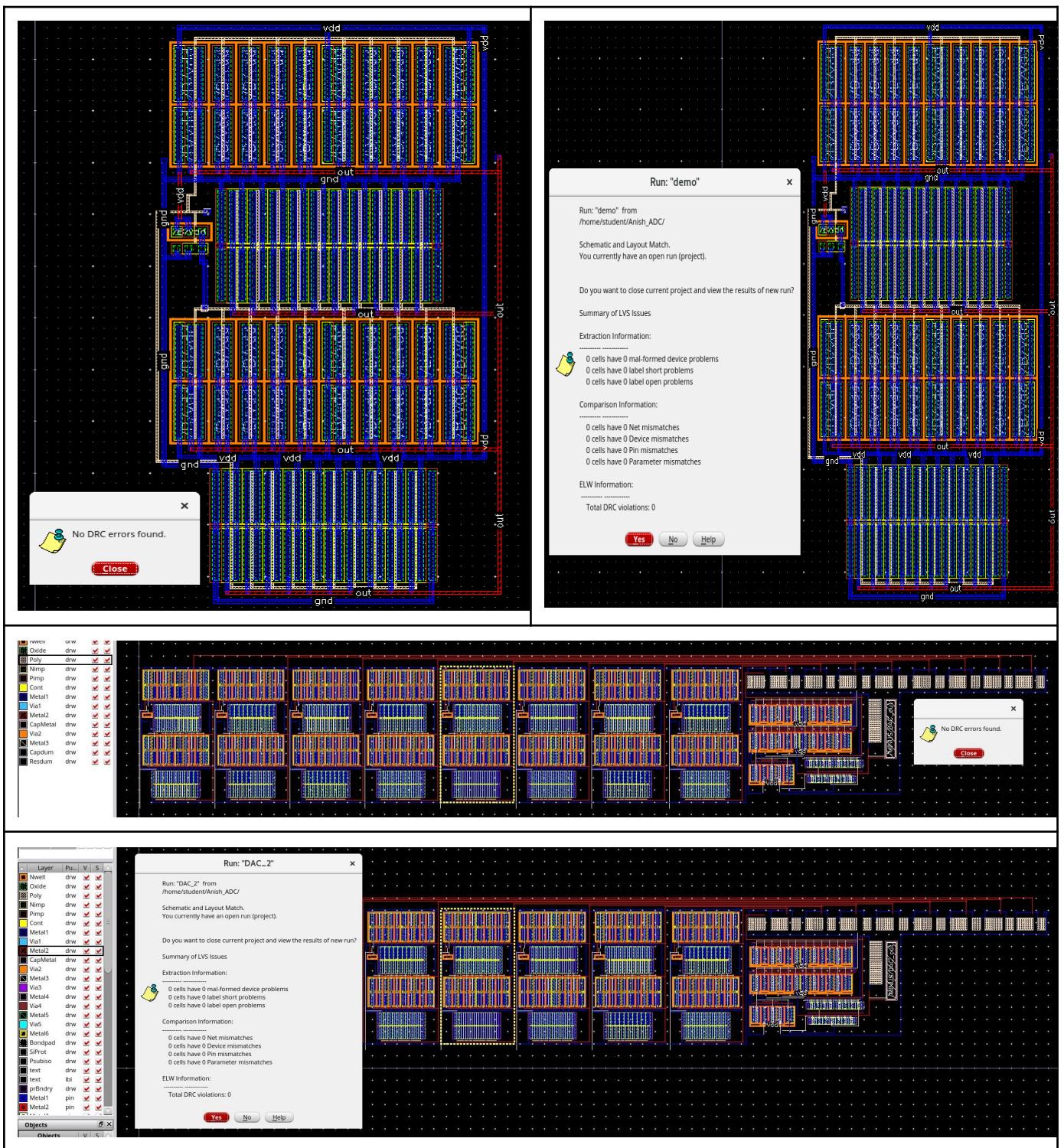


Fig 9.17 calculation of ADC design parameters







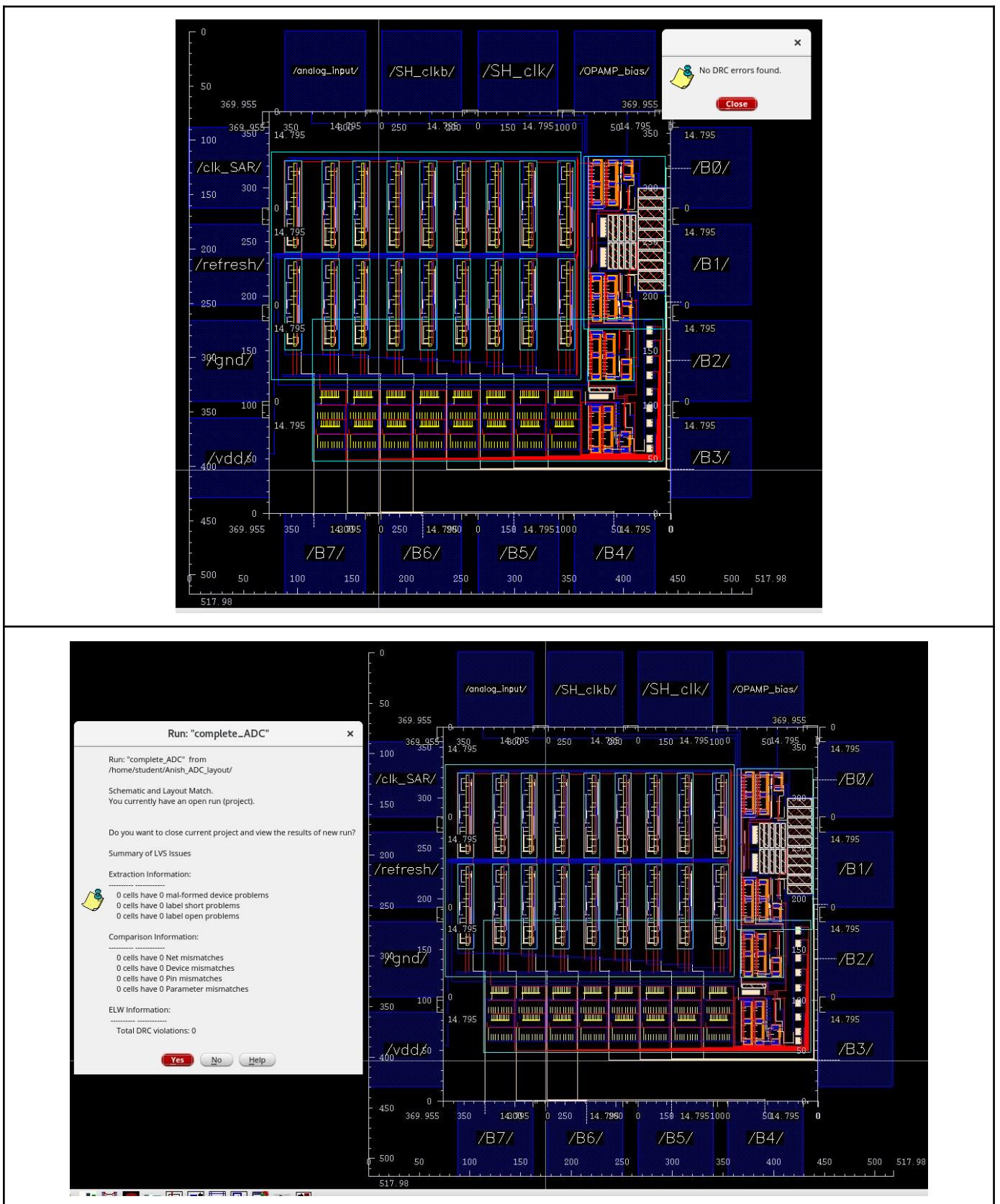


Fig 9.18 layout of individual blocks as well as layout of complete ADC

One of the important steps in chip design is floorplanning, in which the width and height of the chip, basically the area of the chip, is defined. A chip consists of two parts, 'core' and 'die'. A 'core' is the section of the chip where the fundamental logic of the design is placed. The space between core and die is reserved for IO pad placement. For eg. an 8085 has around 40 pads.. A single wafer contains hundreds of die's. Also, the clock pads are wider compared to other pads on the chip to have minimum resistance. Pads are made of all metal layers used in design for easy access while routing the design. Number of layers depends on technology. Pads consist of some logic cells like level shifters and buffers which will control the voltages of input and output signals and to increase/decrease drive strength. IO pad comprises 3 parts - bond pad on which bond wire is joined, logic pad which is connected to logic cells placed inside core, & finally we have Electrostatic Discharge protection circuit consisting of a pair of big PMOS, NMOS in a reverse biased diode structure. There are 2 types of design styles - pad limited design & core limited design.

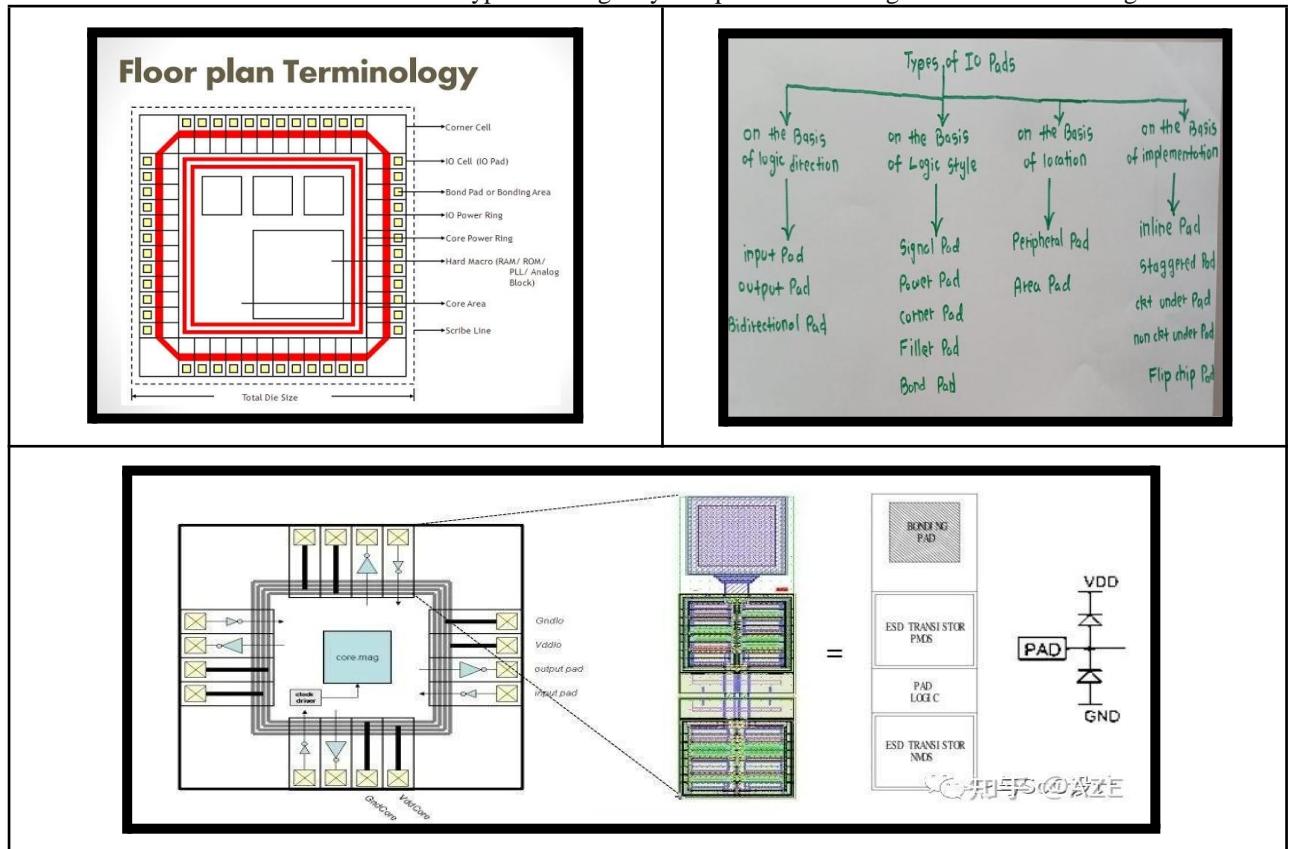


Fig 9.19 floorplanning and placement theory

Table 9.3 Dimensions & MOSFET count of ADC layout

core dimensions	370 um * 370 um
die dimensions	518 um * 518 um
pad dimensions	74 um * 74 um
filler pad	74 um * 14.8 um
total pads	16
total MOSFET in layout	1250
total resistors in layout	20
total capacitors in layout	21

9.2 Discussion:

Problem

When OPAMP was designed the its output was underdamped. There were oscillations in the output. The output took long time to reach steady state. This affected the speed as well as the stability of OPAMP circuit.

Solution

In OPAMP there is Resistor placed for feed forward compensation and Capacitor is placed for miller compensation. So we changed the value of resistance to 1.47 K. This converted the output from underdamped to critically damped. Earlier when R was 3.7 K the settling time was 129 ns. Now when R became 1.47 K the settling time reduced to 56.159 ns. Thus we improved stability as well as the speed of OPAMP.

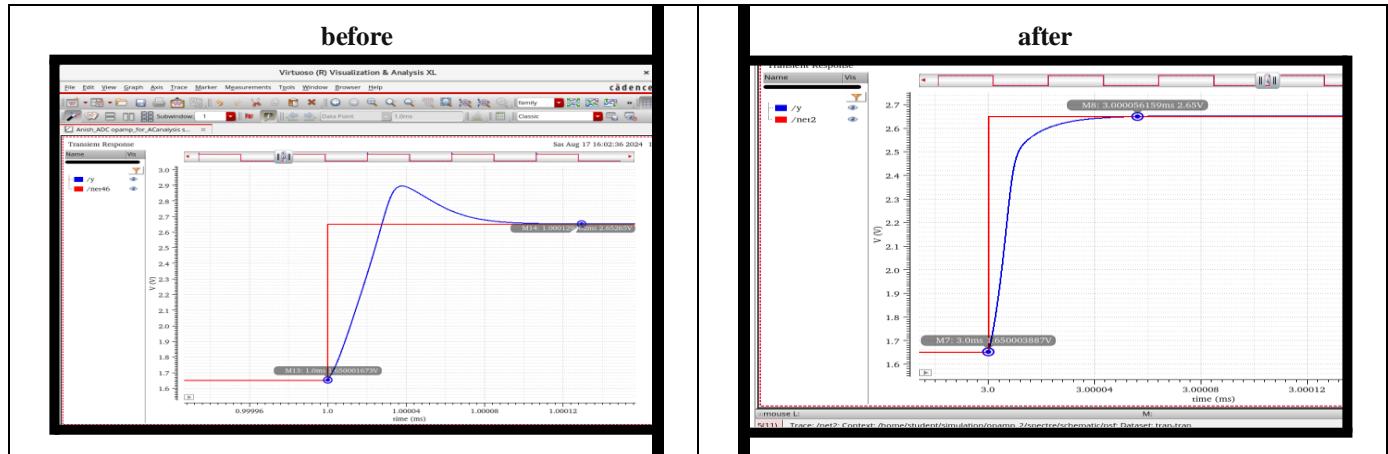


Fig 9.20 underdamped & critically damped output of OPAMP

Problem

The comparator in our ADC is made from OPAMP itself. So speed of both circuits are same i.e 56.159 ns. However according to our ADC design, the entire analog to digital conversion should get completed in 100 ns. This is because speed of SH circuit is 10 MHz ($T = 1 / 10M = 0.1\mu s = 100n$). Theoretically we have 100 ns , but practically we only have 90 ns in our hand (SH circuit takes 10 ns to settle). We reset the SAR register during these 10 ns to save time. Now in 90 ns we have to perform 8 conversion i.e 11.25 ns per conversion. So speed of comparator + DAC should be less than 11.25 ns. (speed of SAR register not considered as it is digital circuit). So for each circuit roughly $11.25 / 2 = 5.625$ ns. This is the required speed of comparator.

Solution

When OPAMP is designed , our aim is stability and smooth output. So we add Resistor for feed forward compensation and Capacitor for miller compensation. However in comparator our priority is speed and not stability. So we remove the resistor and capacitor. This tremendously increases the speed of the comparator circuit.

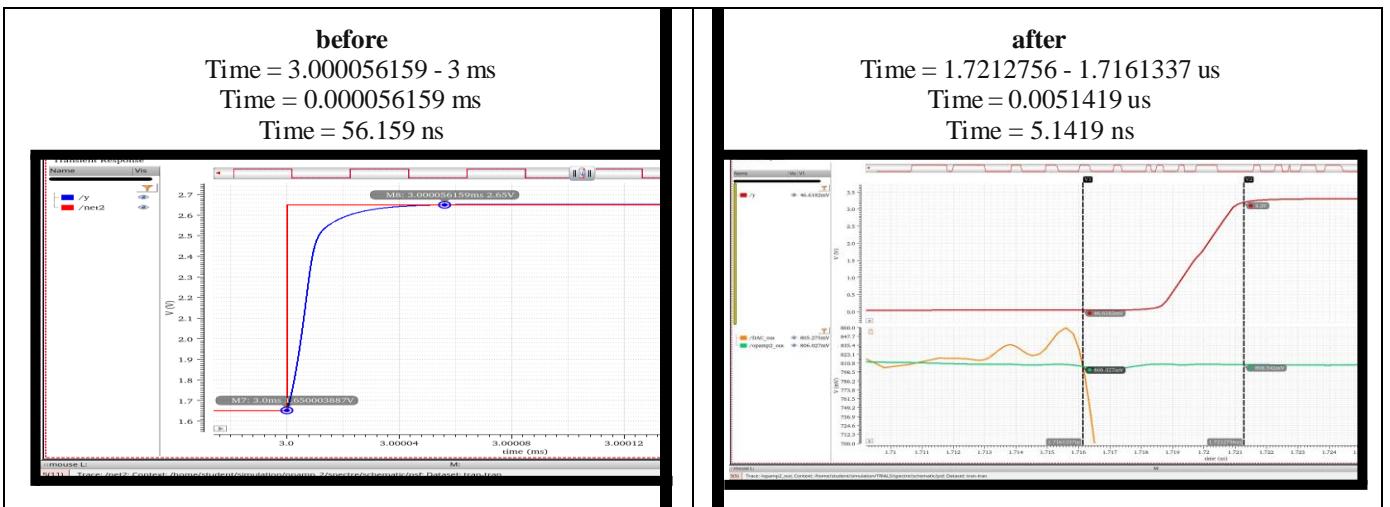


Fig 9.21 removing compensation to improve comparator speed

Problem

Charge injection and clock feedthrough are considered two major problems occur in basic S/H circuit. It is happening when a transistor is used as a switch in a switched capacitor circuit. Charge injection occurs when the clock \emptyset goes high. The NMOS transistor turns ON, and the input voltage is sampled by the capacitor C_s . Due to the inverted channel, a charge under the gate oxide is produced. Then, when the clock \emptyset goes low, The NMOS transistor turns OFF. The created channel charge will flow out from the NMOS gate into its source and drain creating an error in the sampled voltage. Clock feedthrough is defined as the coupling between the clock transitions and the sampling capacitor by the MOS transistor through its gate-drain or gate-source overlap capacitances. When the clock \emptyset goes high, an overlap capacitance is fed through the gate-source, the gate-drain, or both. While in the OFF state of the transistor, a capacitive divider is created. This operation result in an offset voltage

Solution

Complex approach would be to design a Bootstrapped Sample & Hold circuit which would take care of both the issues. Simple approach is to use TG. Instead of using only PMOS or only NMOS as switch , use TG as switch. The error produced by them is equal and opposite due to which they cancel out each other. We can also use a dummy switch. Source and drain terminal are shorted & its W/L is half of TG. if TG is given clock , dummy MOSFET is given clk_b. When TG turns off, all charge gets released which is absorbed by the dummy MOSFET which was just turned on. Also keep the W/L value for TG as small as possible. Cuz charge stored is mathematically given as $Q = W L \text{Cox} (VDD - Vin - Vtn)$. We also changed duty cycle from 50 % to 95 %

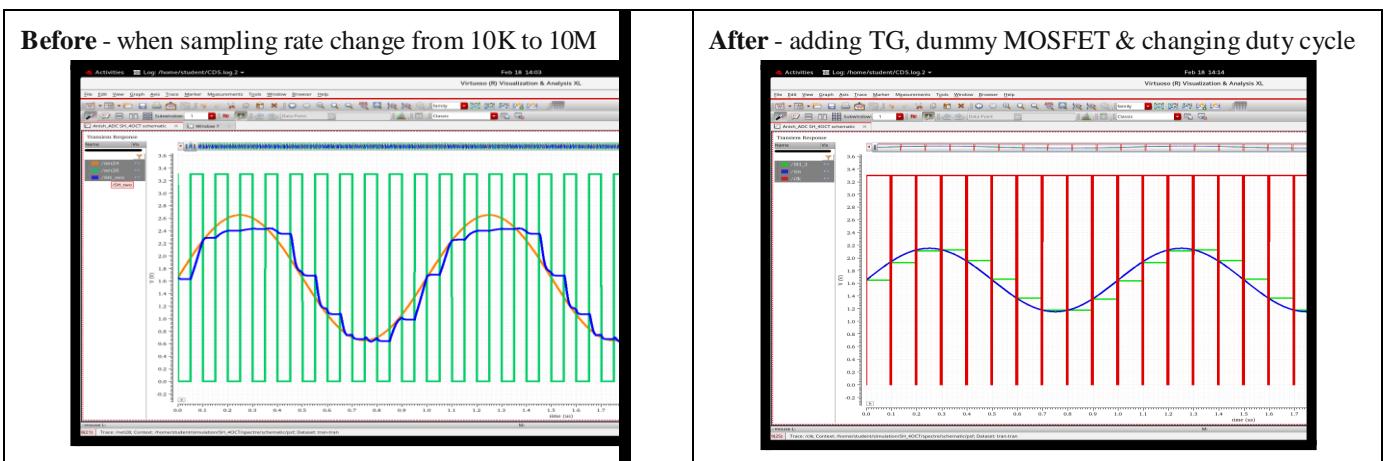


Fig 9.22 improving the output waveform of Sample & hold circuit

Problems

ADC which we were referring was operating at slower speed of 20 KHz , where as our ADC was too fast 10 MHz. due to this DAC block was getting very less time to reach steady state value. ADC being referred had lower resolution of 4 bits whereas our ADC had more resolution of 8 bits. This increased the number of conversions DAC had to performed which further reduced the time to reach steady state. In short DAC had a large settling time.

Solution

Complex solution would be to select High speed DAC architecture like current steering DAC / segmented DAC. simpler solution would be to modify existing DAC. our DAC consist of two parts - opamp and R-2R ladder. Opamp had UGB of 33MHz indicating it could operate at speed of 33 MS/s. so it was clear problem was in ladder. It takes a time RC for ladder output to get to 63% of its final value and $5RC$ to get to 99.3%. There is a tradeoff between speed and voltage swing as follows.

Table 9.4 - trade-off between speed and voltage swing in DAC circuit

Condition	Conversion speed	Voltage swing
If $R = 100$, $C = 1 \text{ pF}$ then $5RC = 0.5 \text{ ns}$	Conversion speed becomes very HIGH	Due to small R , V drop increases.
If $R = 10K$, $C = 10 \text{ pF}$ then $5RC = 0.5 \text{ us}$	Conversion speed becomes very LOW	Due to large R , V drop decreases



Fig 9.23 trade-off between speed and voltage swing in DAC circuit

Problem

We reduced the settling time of DAC by reducing the Resistor values. However it created a new problem of voltage drop. The signal gives strong HIGH (3.3 v) and LOW (0 v) output in SAR block. But when this signal is given to DAC there is sharp voltage drop. 3.3 v falls to 2.8 v and 0 v falls to 0.5 v. Because of this whenever the ADC was getting reset ($1000,0000 = 128$ (3.3) / $256 = 1.65$ v) we were not obtaining 1.65 v. This leads to error in first bit conversion. The error gets carry forwarded in conversion of second bit, then the third bit and so on. Hence the finally obtained value after conversion of all 8 bits is wrong.

Solution

So we created 2:1 MUX using TG topology. The MUX ensures that signal moving from SAR (digital block) to DAC (analog block) does not drop. The width of the MOSFET used in TG need to be high (100u). So for PMOS & NMOS we kept $L = 1\mu$ and $W = 100\mu$. We know that R is inversely proportional to area i.e R is inversely proportional to width. Higher the width, lower will be R and lower will be voltage drop ($v = ir$). This drastically improved the overall performance of our ADC. the error reduced from 10 LSB to 1 LSB

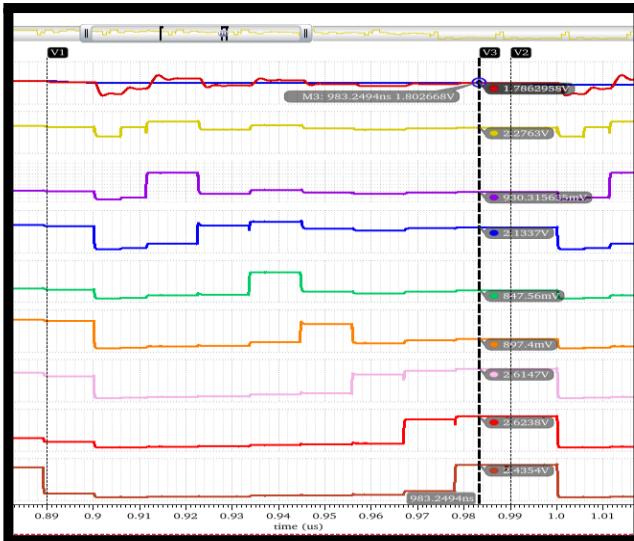
before

Sample output signal = 1.78629 V

DAC output signal = $10100111 = 163(3.3) / 256$

DAC output signal = 2.101171 V

Huge error as voltage swing decreased from 0 - 3.3 to 0.8 - 2.5. multiplying by 3.3 is wrong



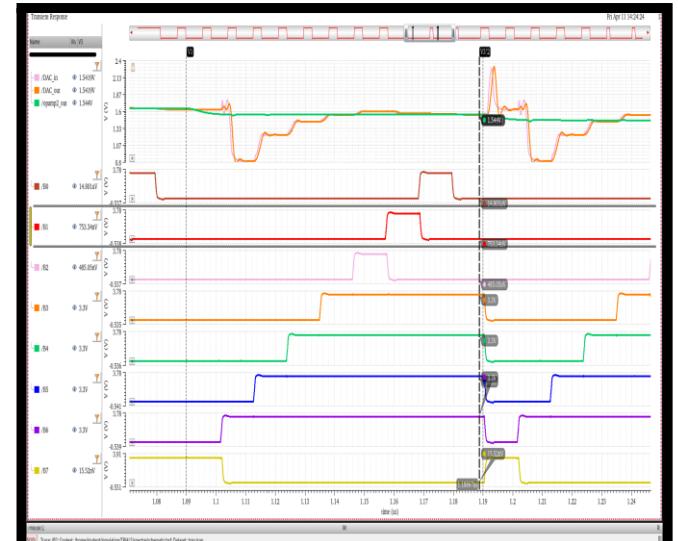
after

Sample output signal = 1.544 V

DAC output signal = $01111000 = 120(3.3) / 167$

DAC output signal = 1.546875 V

Error = 0.002875, this shows reducing the voltage drop has significantly reduced error



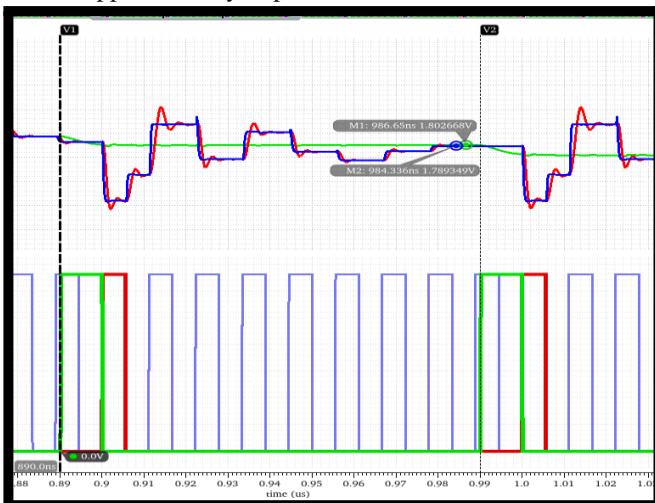
Sample circuit signal = 1.802668 V

DAC circuit signal = 1.789349 V

Error = 0.013319 V

$LSB = 3.3 / 2^8 = 3.3 / 256 = 0.01289$ V

Error is approximately of plus minus 1 LSB



Sample circuit signal = 1.544 V

DAC circuit signal = 1.541866 V

Error = 0.002134 V

$LSB = 3.3 / 2^8 = 3.3 / 256 = 0.01289$ V

Error is approximately of plus minus 0.1 LSB

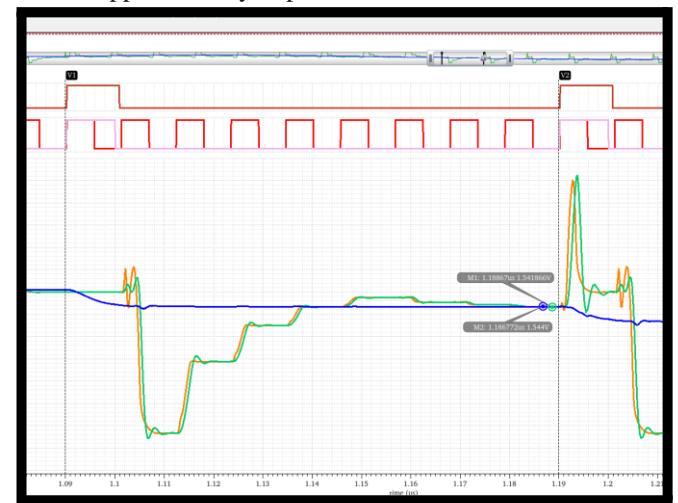


Fig 9.24 adding TG switch solved voltage drop problem in DAC

Chapter 10: Conclusion

Chapter: 10 Conclusion

The design and implementation of the 8-bit SAR ADC using Cadence Virtuoso with GPDK 180nm technology successfully met the major project objectives, including achieving moderate resolution, high-speed operation, and low power consumption. Throughout the design process, we focused on building and integrating key functional blocks — the sample-and-hold circuit, comparator, successive approximation register, and R-2R DAC — each optimized for performance and area. Challenges such as comparator speed limitations, charge injection in sample-and-hold circuits, and DAC settling time were systematically addressed through strategic circuit modifications, including optimization of transistor sizing, layout techniques like interdigitization and common centroid, and careful trade-offs between speed, stability, and voltage swing.

Through detailed simulations and layout verifications, including DRC, LVS, and post-layout extraction, the final SAR ADC achieved an effective number of bits (ENOB) close to 7 bits, with an SNR of 43.76 dB and an SNDR of 41.12 dB, validating its design efficiency. Important design issues like underdamped op-amp response, comparator speed optimization by removing compensation, and DAC optimization for faster settling were carefully solved, demonstrating practical problem-solving skills necessary for analog IC design. Moreover, the layout occupied a compact core area of $370 \times 370 \mu\text{m}^2$ with an overall die size of $518 \times 518 \mu\text{m}^2$, and the total MOSFET count stood at around 1250, confirming a well-managed floorplanning and placement strategy.

In conclusion, this project not only strengthened our understanding of analog circuit design fundamentals but also gave hands-on experience with the end-to-end IC design flow, from schematic design to post-layout validation. The lessons learned, especially regarding optimization under strict timing, area, and power constraints, are valuable for future work in analog/mixed-signal VLSI design. Overall, the successful design and testing of the SAR ADC underscore its readiness for moderate-speed, low-power applications, and open pathways for further enhancements such as asynchronous SAR operation, higher resolution scaling, and more power-efficient architectures.

Chapter 11: References

Chapter 11 : References

- [1] Performance analysis of double tail dynamic comparators S Sonar1, D Vaithianathan1 and A Mishra 1 Published under licence by IOP Publishing Ltd
[Journal of Physics: Conference Series, Volume 1706, First International Conference on Advances in Physical Sciences and Materials 13-14 August 2020, Coimbatore, India](https://doi.org/10.1088/1742-6596/1706/1/012013)
- [2] N. Chen and M. Zhang, "Designing of a high speed, compact and low power, balanced-input balanced-output preamplifier latch based comparator," Journal of Vibroengineering, Vol. 22, No. 8, pp. 1847–1858, Dec. 2020,
<https://doi.org/10.21595/jve.2020.21485>
- [3] On the Design of Low Power CMOS (SA-ADCs) for Biomedical Applications Thesis for: MSc., Advisor: Soliman Mahmoud
[https://www.researchgate.net/publication/301732317 On the Design of Low Power CMOS SA-ADCs for Biomedical Applications](https://www.researchgate.net/publication/301732317)
- [4] Design of a Low-Power Asynchronous SAR ADC in 45 nm CMOS Technology Muhammad Aldacher, Dr. Sotoudeh Hamed-Hagh, Dr. Sang-Soo Lee , San Jose State University [\(Report\) Design of A Low-Power Asynchronous SAR ADC in 45 NM CMOS Technology | PDF | Analog To Digital Converter | Mosfet](#)
- [5] "Design of Low Power & High Speed Comparator of SAR ADC using 180nm Technology," H. kushwah, R. S. Gamad and R. C. Gurjar, 2020 4th International Conference on Electronics, Communication and Aerospace Technology (ICECA), Coimbatore, India, 2020.[Design of Low Power & High Speed Comparator of SAR ADC using 180nm Technology | IEEE Conference Publication](#)
- [6] A. Naguib, "High Speed and Low Power Comparator in 65 nm CMOS for Energy Efficient Biomedical SAR ADCs," 2020 12th International Conference on Electrical Engineering (ICEENG), Cairo, Egypt, 2020.[High Speed and Low Power Comparator in 65 nm CMOS for Energy Efficient Biomedical SAR ADCs | IEEE Conference Publication](#)
- [7]S. Banik, M. M. H. Rasel, T. Mahmud and M. Hasanuzzaman, "Design and implementation of a low-power 1V, 77.26 μ W 6-bit SAR ADC in Cadence 90nm CMOS process for biomedical application," 2020 IEEE Region 10 Symposium (TENSYMP), Dhaka, Bangladesh, 2020.[Design and implementation of a low-power 1V, 77.26 \$\mu\$ W 6-bit SAR ADC in Cadence 90nm CMOS process for biomedical application | IEEE Conference Publication](#)
- [8] X. Tang et al., "A 10b 120MS/s SAR ADC with Reference Ripple Cancellation Technique," 2019 IEEE Custom Integrated Circuits Conference (CICC), Austin, TX, USA, 2019.[A 10b 120MS/s SAR ADC with Reference Ripple Cancellation Technique | IEEE Conference Publication](#)
- [9]S. A. A, S. K. A and G. N. R. D, "A 10-Bit Power Efficient SAR ADC Designed with Enhanced Signal Integrity for Biomedical Applications," 2024 International Conference on Smart Electronics and Communication Systems (ISENSE), Kottayam, India, 2024.[A 10-Bit Power Efficient SAR ADC Designed with Enhanced Signal Integrity for Biomedical Applications | IEEE Conference Publication](#)