

Design of 8 bit SAR ADC

Submitted as Final Year Major Project-I by

Group Number: BE-02	
Group Member Names	Roll No.
Vansh Dhoka	41
Atharva Godkar	42
Anish Godse	43
Anushri Kadam	45

Supervisor: Dr. Jaymala Adsul

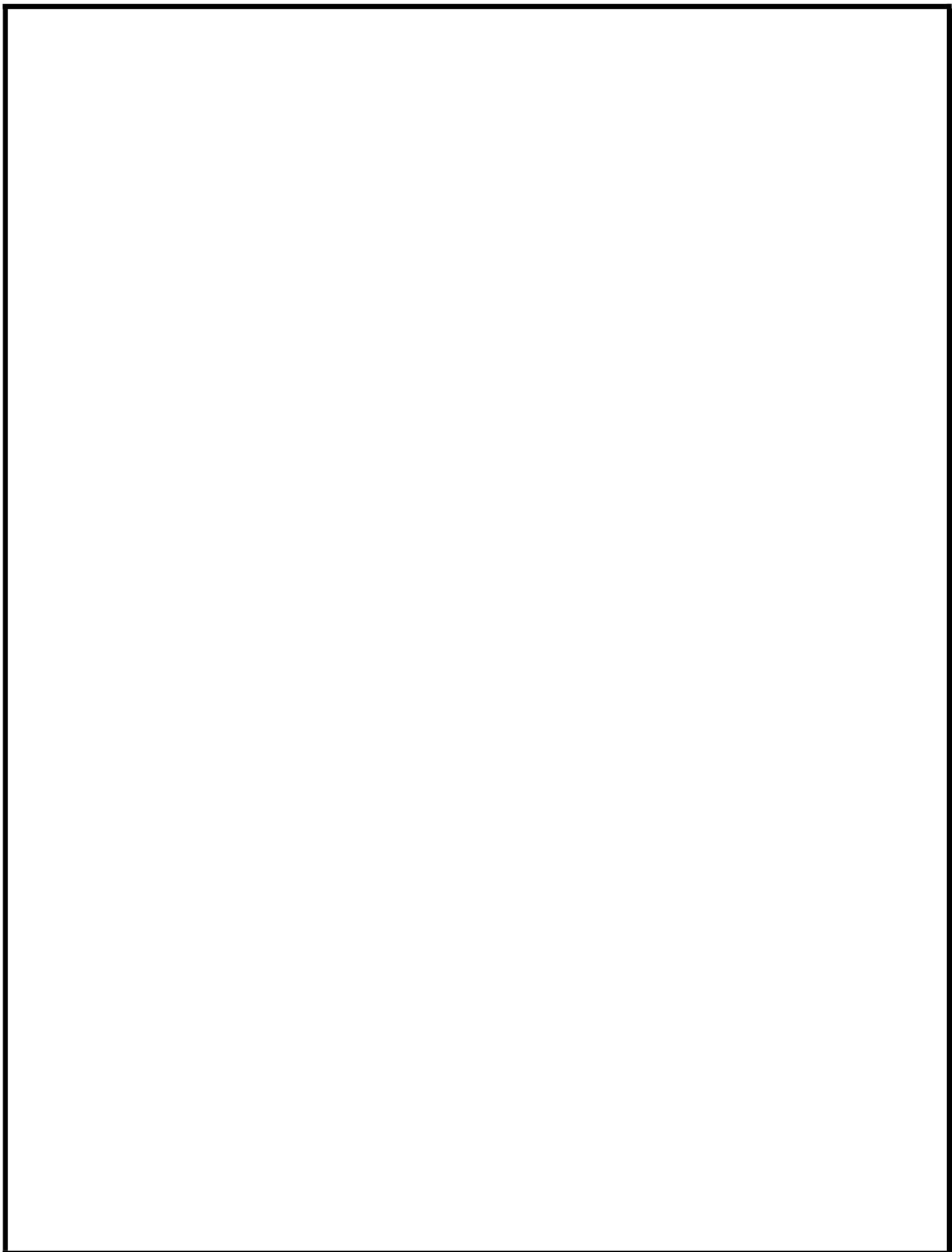


Department of Electronics Engineering

V.E.S. Institute of Technology

(An Autonomous Institute affiliated to University of Mumbai, Approved by AICTE & Recognized by Govt.of Maharashtra)

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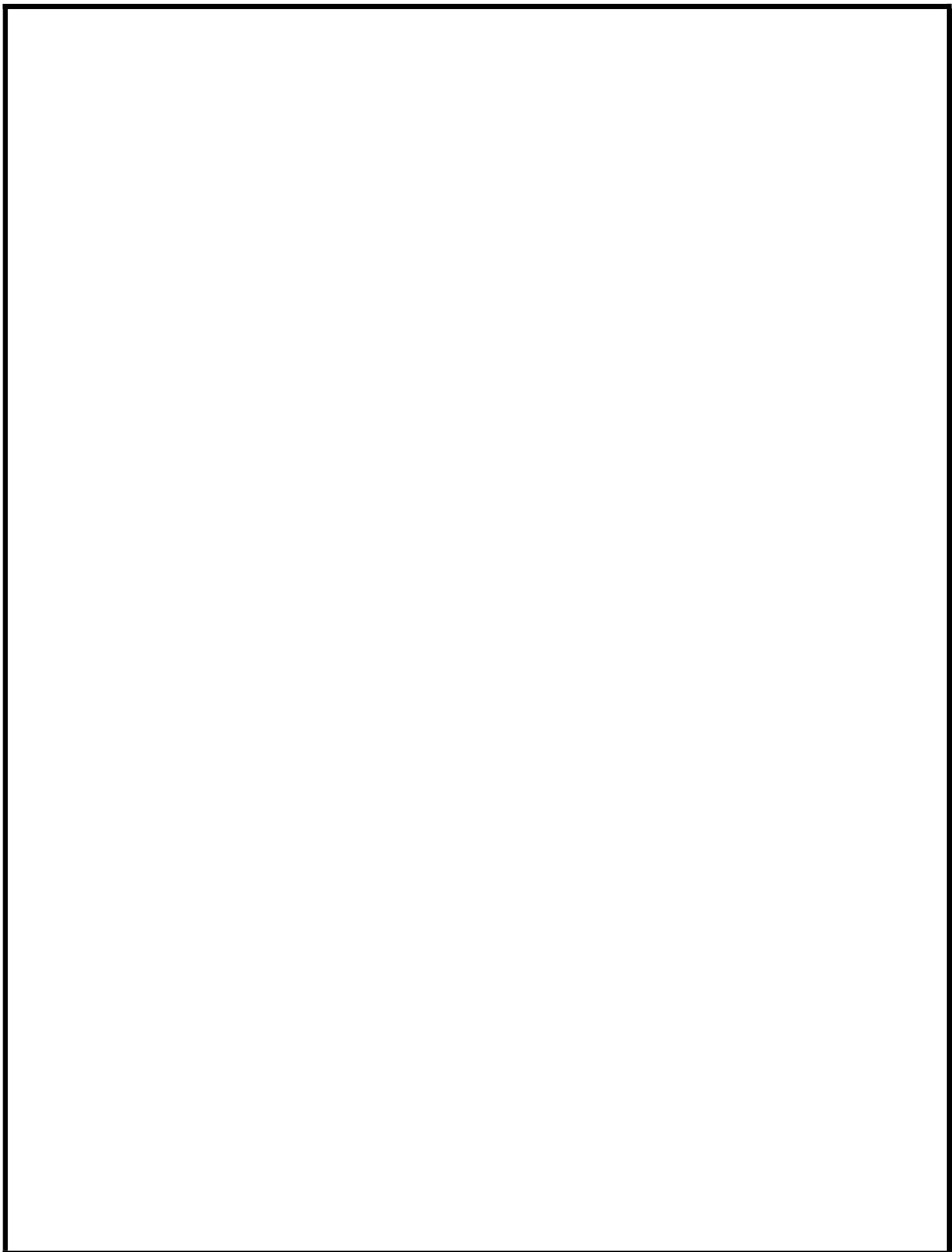
CERTIFICATE

This is to certify that the project entitled "**Design of 8 bit SAR ADC**" is a bonafide work of **Vansh Dhoka (41)**, **Atharva Godkar (42)**, **Anish Godse (43)**, **Anushri Kadam (45)** submitted to the V.E.S. Institute of Technology as a Final Year Major Project 1 during the academic 2024-25.

Dr. (Mrs.) Jayamala Adsul
Supervisor/Guide

Dr. (Mrs.) Kavita Tewari
Head of Department

Dr. (Mrs.) J.M. Nair
Principal



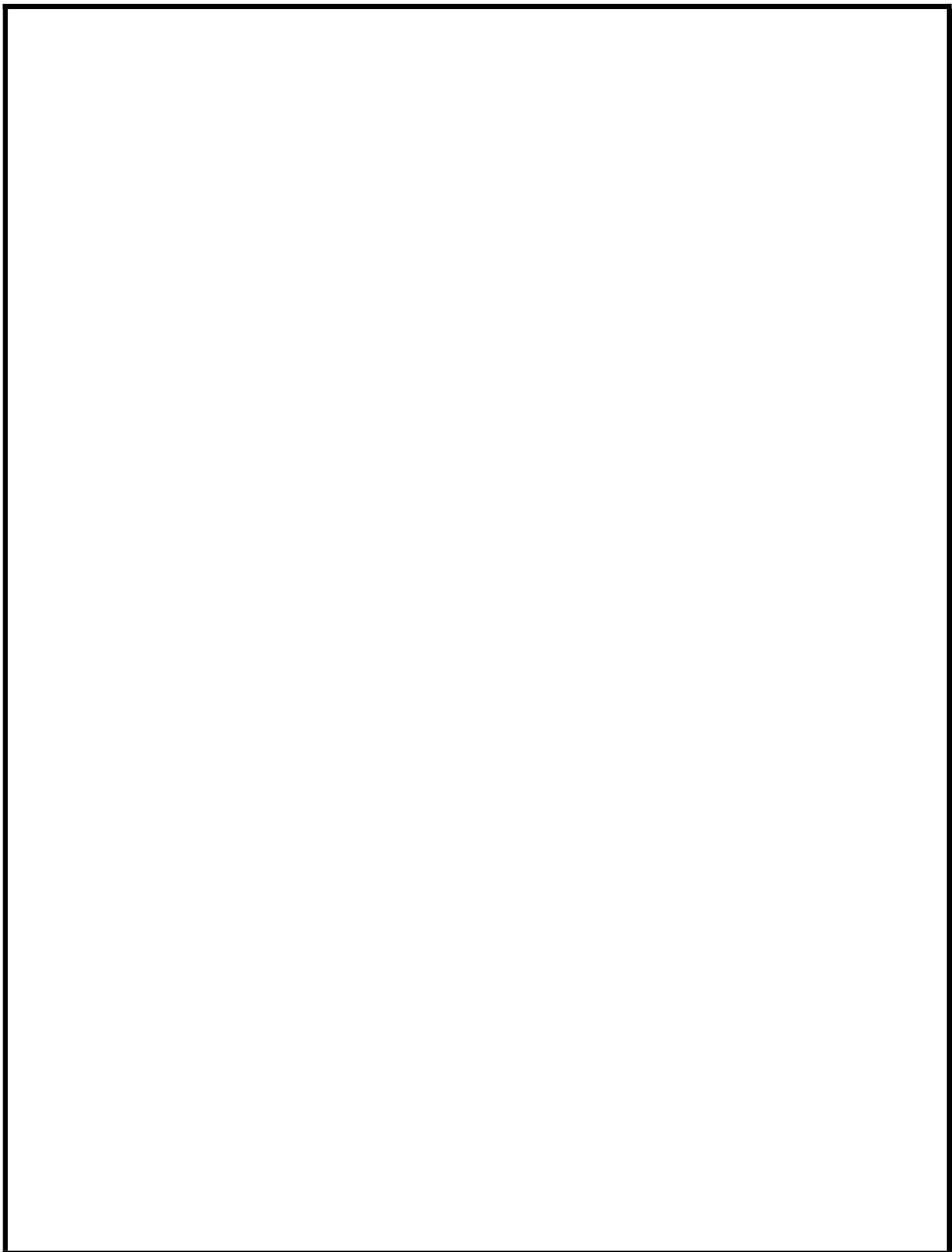
PROJECT REPORT APPROVAL

This project report entitled "**Design of 8 bit SAR ADC**" by **Vansh Dhoka (41), Atharva Godkar (42), Anish Godse (43), Anushri Kadam (45)** is approved as **Final Year Major project 1** during Academic year 2024-25.

Examiner

1.-----

2.-----



DECLARATION

We declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, we have adequately cited and referenced the original sources. We also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. We understand that any violation of the above will be cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

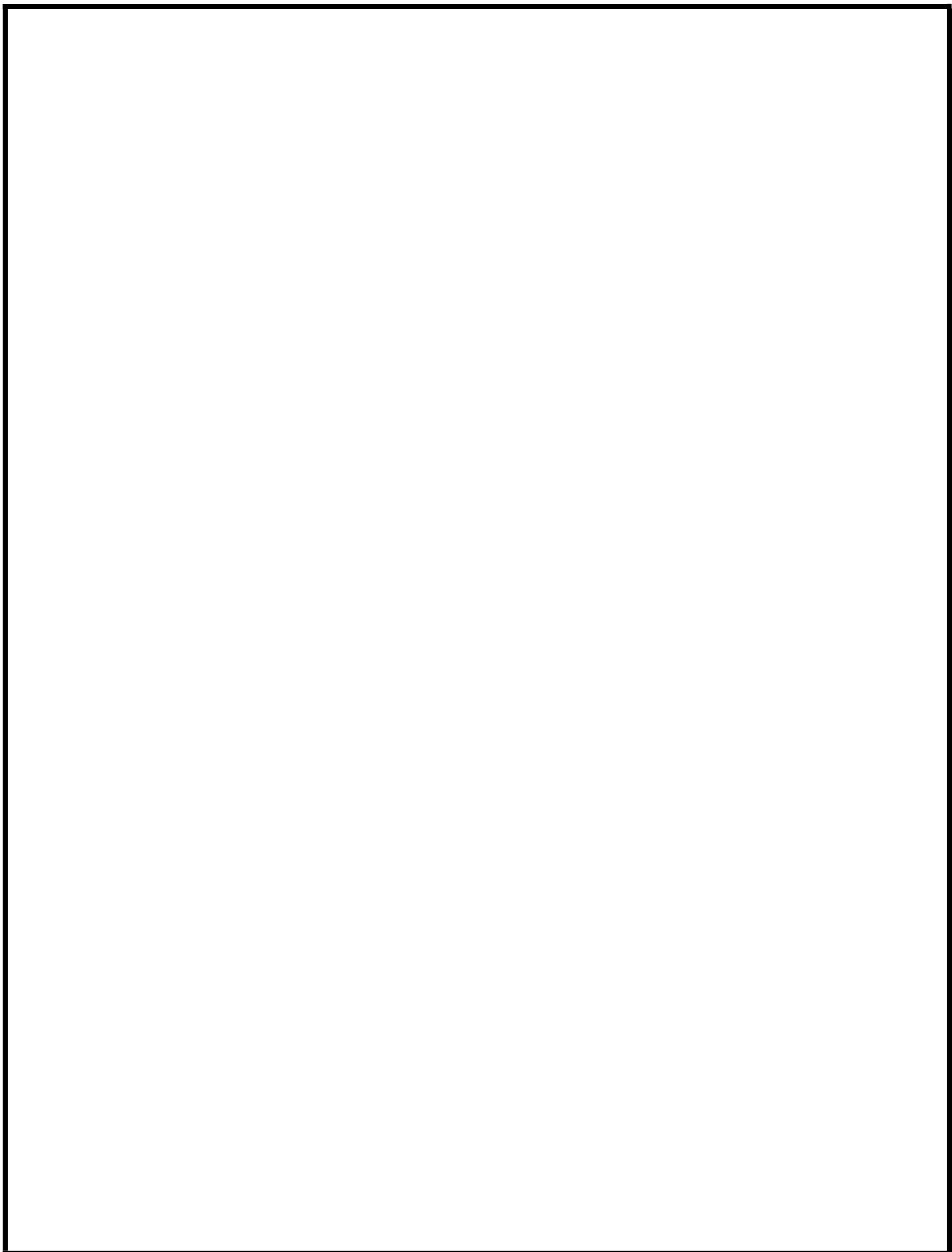
Vansh Dhoka (41)

Atharva Godkar (42)

Anish Godse (43)

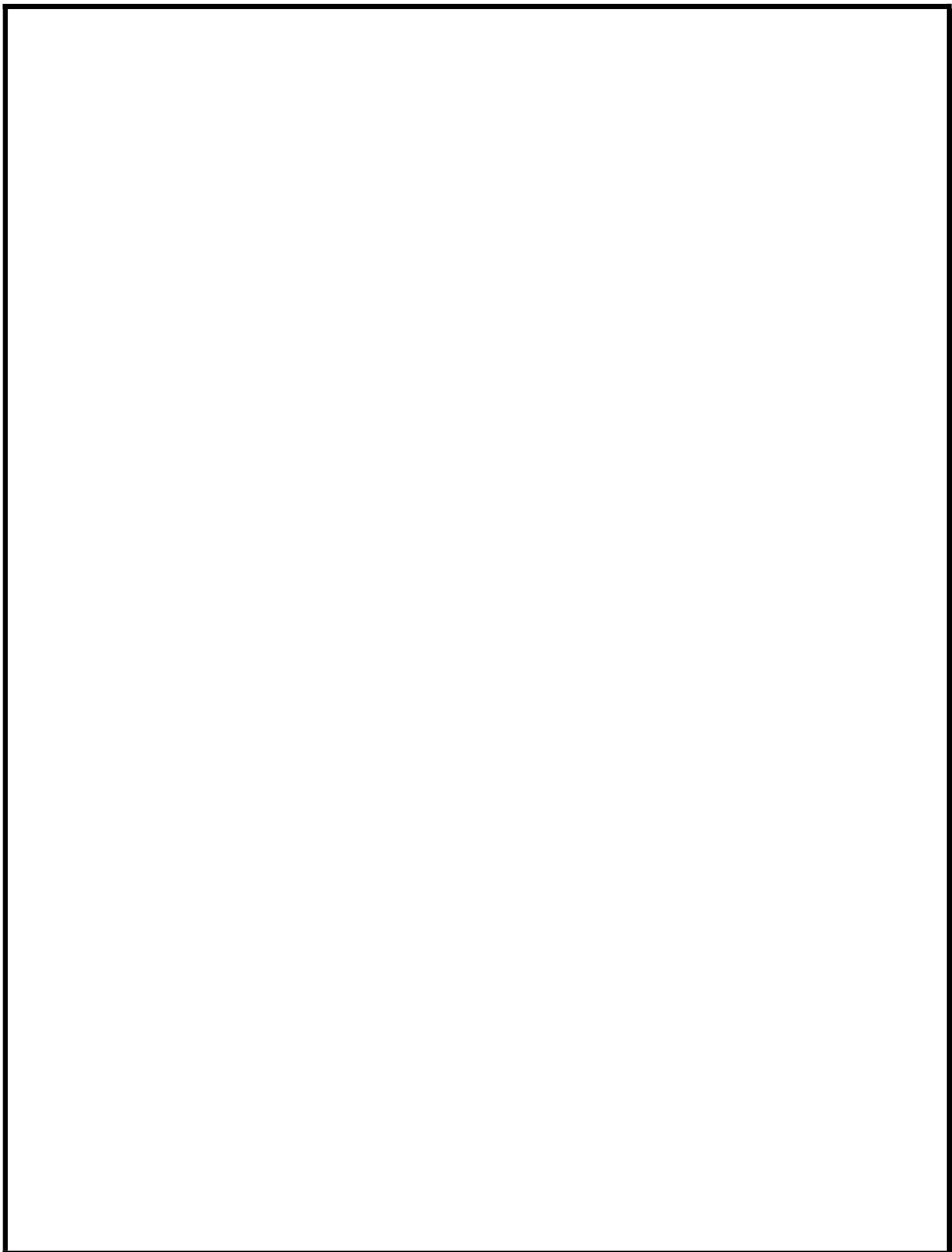
Anushri Kadam (45)

Date:



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CHAPTER 1

INTRODUCTION

CHAPTER 1 INTRODUCTION

Analog and digital converters (ADCs) are essential components in modern high-speed interactive devices. Significant efforts are continually made to enhance their performance. Alongside improving overall ADC functionality, there is considerable focus on enhancing individual sub-modules, such as comparators. These components play a crucial role in ADC operation. In this study, we propose a design for a Successive Approximation Register (SAR) ADC. Dynamic comparators are preferred in industrial applications due to their attributes like high input impedance, rail-to-rail swing, and minimal static power consumption. Depending on specific application needs, circuits can be selected based on criteria such as lower delay, smaller footprint, or higher operational frequency. Designing a comparator with precise characteristics including low voltage operation, high dynamic range, minimal power consumption, high speed, robustness, and low offset voltage presents a significant challenge for current and future applications.^[1]

1.2 Objectives:

To design a SAR ADC circuit. The circuit will comprise of 4 sub blocks - Sample and Hold Circuit, Comparator, Successive Approximation Register, Digital to Analog Converter. We will take an analog IC design approach for completing this circuit. We will make a schematic and layout of ADC on Cadence tool.

Specifications of ADC -

1. Type = SAR ADC
2. Resolution = 8 bits
3. clock speed = 0.1us (10Mhz)
4. Conversion time = 0.9us
5. Supply voltage = 3.3v
6. Technology used = 180nm

CHAPTER 2

LITERATURE

REVIEW

CHAPTER 2 LITERATURE REVIEW

Performance analysis of double tail dynamic comparators

[1] Analog and digital converters (ADCs) are the most inevitable part of today's high-speed human interacted devices. Continuous efforts are being made to improve their performance. Despite working for the improvement of the whole ADC, efforts to improve sub-modules are also significant. Comparators are also a vital part of ADC. In this work, we have proposed a design of an Asynchronous Successive Approximation Register (SAR) ADC.

Dynamic comparators have a high input impedance, rail to rail swing, and almost zero static power consumption; they are widely used in industrial applications over static comparators. Depending on the application requirements, the circuit can be chosen which provides less delay, area or higher operating frequency. Designing the comparator with high precision, low voltage, high dynamic range, lower power dissipation, high speed, robust and less offset voltage is a critical challenge for present and future applications.

The Circuit behavior was observed over a large supply voltage range. When the input voltage becomes lesser than the resolution of the comparator, the wrong output gets latched at the output. This method helps in determining the offset voltage.

The specifications of the same are as follows:

Common Mode Voltage - VDD/2

Technology used - 180 nm

Large supply voltage range of 2-0.6V

VDD - 1.8 V

Operating Freq - 500 MHz

Offset Voltage - 5.7 mV

Power Consumption - 480 μ W

Delay - 310 ps

Designing of a high speed, compact and low power, balanced-input balanced-output preamplifier latch based comparator

[2] The conventional SAR ADC which is known to be the most energy-efficient ADC amongst various types of other ADCs, has medium speed, medium resolution, less power dissipation and lesser hardware complexity. The speed of such ADCs is known to be limited mainly by the time taken by comparator to resolve the applied inputs and is of the order of few MHz. Designing the SAR ADC using a comparator with high precision, low voltage, high dynamic range, lower power dissipation, high speed, robust and less offset voltage is a critical challenge for present and future applications.

In this work, the author has proposed a novel high-speed Balanced-Input Balanced-Output (BIBO) preamplifier latch based comparator design, to be used for the designing of an Asynchronous Successive Approximation Register (SAR) ADC.

The key point that makes this design different from other designs is that it uses latch made using two back to back connected inverters. These inverters are farming a positive feedback arrangement that prohibits the comparator from bursting into the oscillation. The Latch circuit uses three non-overlapping phases and dissipates less power when operated on a single 1V supply voltage. All these features collectively made this comparator expedient and obtained results confirm that it can be used effectively for the designing of SAR ADC.

The only major drawback of dynamic latch comparator is the offset error that may appear due to transistor mismatch. This is overcomed by using a preamplifier circuit. Preamplifiers basically amplify the difference between two applied input signals and feed it to a dynamic latch.

The specifications of the same are as follows:

Technology - 500 nm

Supply voltage -1V

Power consumption - 65 μ W

Speed - 2100 KSP (Kilo Samples per Second) = 2KHz

On The Design of Low Power CMOS (SA-ADCs) for Biomedical Applications

[3] Charge injection and clock feedthrough are considered two major problems that occur in basic S/H circuits. Charge injection occurs when the clock \emptyset goes high. The NMOS transistor turns ON, and the input voltage is sampled by the capacitor C_s . Due to the inverted channel, a charge under the gate oxide is produced. Then, when the clock \emptyset goes low, The NMOS transistor turns OFF. The charge will flow out from the NMOS gate into its source and drain creating an error in the sampled voltage.

They aim to provide a small on-resistance of the sampling transistor which results in improving the switch linearity, reliability and bandwidth with high signal-to-noise and distortions ratio (SNDR). As a result of using bootstrapped technique, the gate-to-source voltage of the sampling transistor will have a constant voltage and it is relatively independent of the input signal. This will improve the switch linearity and the input bandwidth.

From this Thesis paper we understood that sample and hold circuit faces 2 problems i.e fluctuation in V_{gs} due changing V_{in} & charge injection. We use 2 additional circuits to solve these problems. Bootstrapped circuit to ensure that constant V_{gs} voltage is maintained. boosted driver circuit to shift supply voltage from $0-V_{dd}$ to $V_{dd} - 2V_{dd}$. This solves the Charge injection problem.

The specifications of the same are as follows:

technology = 90nm

resolution = 8 bit

power consumption 200nW

power supply = 1v

signal to noise ratio = 53.8 dB

DNL = +0.34/-0.3 LSB

INL = +0.79/-0.58 LSB

Design of a Low-Power Asynchronous SAR ADC in 45 nm CMOS Technology

[4] The asynchronous SAR ADC is called “asynchronous” because the blocks in this SAR system don’t operate with the same uniform clock signal. Each block produces a signal that signals another block to change state. The external clock only triggers the internal-clock generator to begin the conversion process. The generator produces 2 internal signals, “Clk_Sample”, which is a pulse used for the sampling phase by the sample-and-hold (S/H) block, and “Clk_SAR”, which controls the comparator and the SAR code that changes the DAC voltage. The conversion process starts with the S/H block sampling the input, then “Clk_SAR” goes high which prompts the SAR logic to apply the DAC code. After a certain delay (must be enough for the DAC to settle), “Clk_SAR” goes low to cause the comparator to compare and generate the output. When the comparator finishes the comparison and its output is stable, a “Ready” pulse is sent to the internal-clock generator to cause the “Clk_SAR” to toggle and repeat the cycle for the next iteration. After N cycles of “Clk_SAR”, an end-of-code (EOC) pulse is sent to an output register to send out the final DAC code of the conversion.

From this paper we learned that ADCs are basically of 4 types - flash , SAR, Counting, Dual slope, pipeline, sigma delta etc. Amongst these sigma delta is used for applications requiring high resolution whereas Flash is used for applications requiring high BW. SAR adc has moderate BW & resolution. It is further classified into 2 types. Synchronous sar adc the sampling clock is given externally. Whereas in asynchronous sar adc sampling clock is generated internally.

The specifications of the same are as follows:

technology = 45nm

resolution = 8 bit

input signal = 1.2v

power consumption 49uW

power supply = 1v

signal to noise ratio = 46 dB

CHAPTER 3

METHODOLOGY

CHAPTER 3 METHODOLOGY

3.1 Methodology:

This design comprises 4 blocks. Out of them 3 are analog circuits - comparator, R-2R DAC, Sample & hold circuit. The last block is a digital circuit - Successive approximation register. We will start by making the SAR block as it is comparatively easy. the rest of the three analog circuits have a common component inside them that is OPAMP. Hence completing OP AMP will be our fundamental target. Once OPAMP gets designed, the rest of 3 blocks can be easily derived.

In digital circuits we go with the default W/L ratio. However for analog circuits we calculate W/L ratio for each and every individual MOSFET. There are various techniques to do this. for MOSFETS having $L > 5\text{um}$ we use conventional technique i.e mathematical formulas. however for MOFETS having $L < 5\text{um}$ we have to go with - Gm/Id method, root force method, AI/ML models. This is because as the MOSFET length decreases 2nd order effects come into picture like - subthreshold conduction, body biasvoltage, channel length modulation. Considering all these effects makes calculation very complex, & hence we take the help of EDA tools like cadence.

We will design the individual blocks - comparator, DAC, SAR, SH & then check whether they meet the specified design parameters. We will perform DC, AC, Trans, Noise analysis of the above 4 circuits. after this we will start joining the blocks one by one to complete the entire SAR ADC. the input is first applied at SAR from there it goes to the comparator. so we will connect the first comparator to SH. Then we will connect SAR to both of them. finally we will connect DAC to three of them. Joining the circuits involves taking care of voltage & current level, noise, stability, poles & zeros, settling time, & speed of different blocks such that there is proper sync between them. it is time consuming work which involves fine tuning the circuits for achieving desire output. We will again perform a simulation for one last time to measure the overall performance. ADC must satisfy the following design parameters - 8 bit resolution ,10MHz conversion speed, 3.3 volt supply voltage, INL, DNL, power consumption, SNR. with this we complete the first half of the project. the second half of the project involves make a layout of the SAR ADC circuit. We will verify the layout using DRC check, LVS check, noise check , RC check etc. final a report will be generated which will tell how much the design parameters have varied in layout compared to the original schematic. with this we complete the entire project.

CHAPTER 4

BLOCK

DIAGRAM &

WORKING

CHAPTER 4 BLOCK DIAGRAM & WORKING

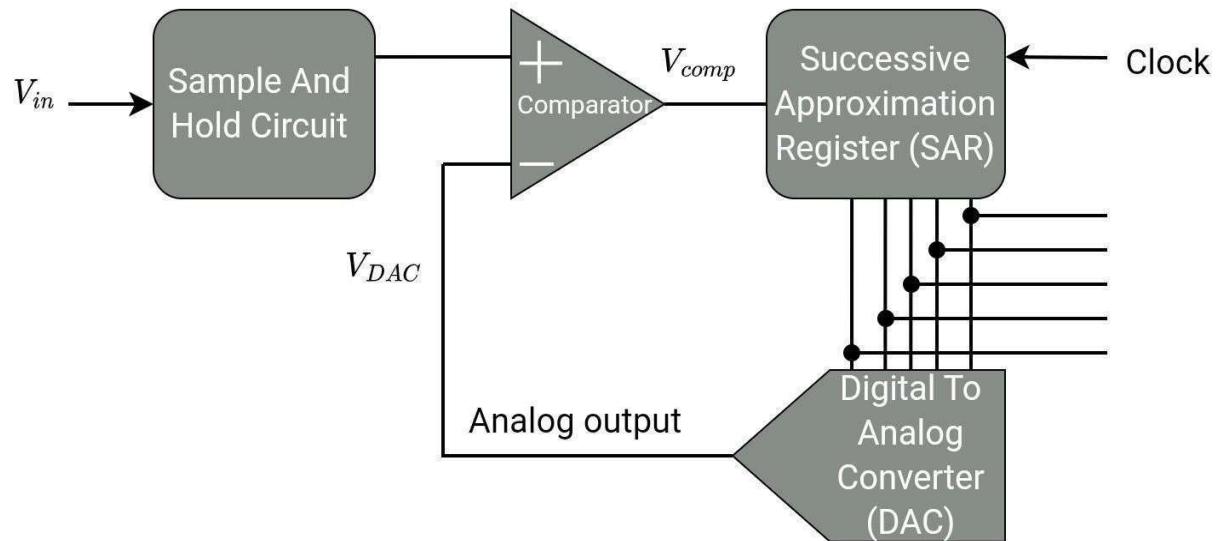


Fig. 4.1: Block diagram of the proposed system

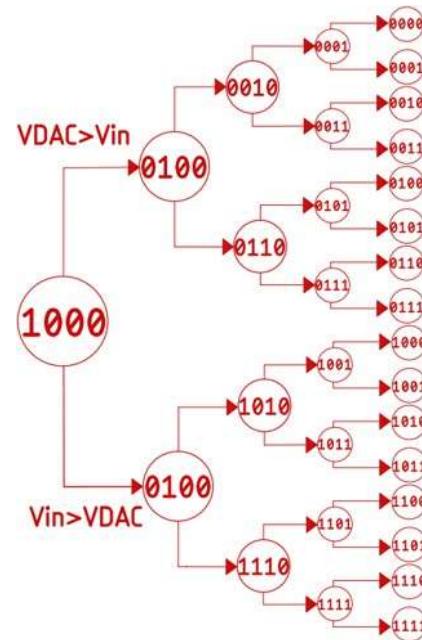


Fig. 4.2- Possible combinations for a 4-bit SAR ADC

Working of the SAR ADC:

An ADC (analog-to-digital converter) has three main parts: a comparator, a digital to analog converter (DAC), and a successive approximation register with a control circuit. Whenever a new cycle starts, the sample and hold circuit samples the input signal which is compared with the specific output signal of the DAC. Also, the sampled signal is held for a specific time period so that the subsequent circuit can compute the result. When the conversion starts, the successive approximation register sets the most significant bit to 1 and all other bits to zero. For example, for a 4-bit ADC, the value becomes 1000. Now let's say, the sampled input signal is 5.8V. For a 10V reference voltage, the DAC will produce a value of 5V which is half of the reference voltage. (The value will toggle between both extreme values.) Now this voltage will be compared to the input voltage and based on the comparator output, the output of the successive approximation register will be changed.

- This means if V_{IN} is greater than the output of the DAC, the most significant bit will stay as it is, and the next bit will be set for a new comparison.
- Otherwise, if the input voltage is less than the DAC value, the most significant bit will be set to zero, and the next bit will be set to 1 for a new comparison.

This is how the successive approximation ADC changes 1 bit at a time to determine the input voltage and produce the output value. And whatever the value might be, in four iterations/cycles, we will get the output digital code from the input value. A n-bit SAR ADC will take n-iterations to convert the analog signal to digital value.

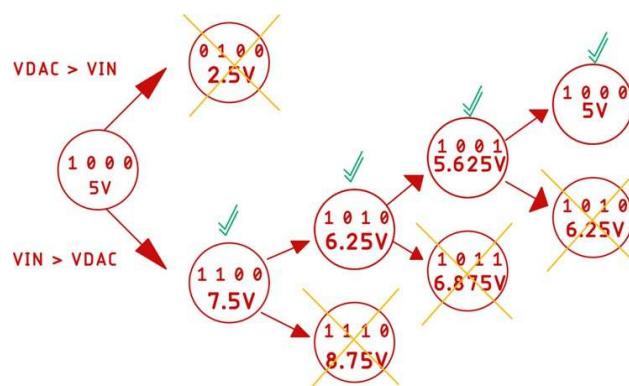
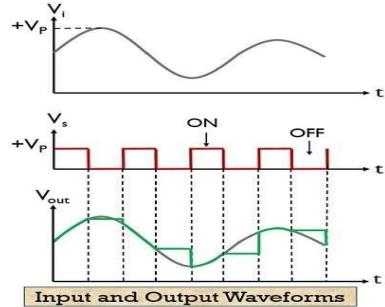
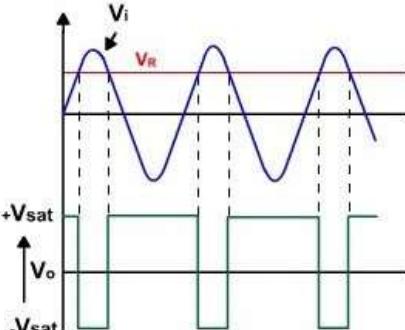
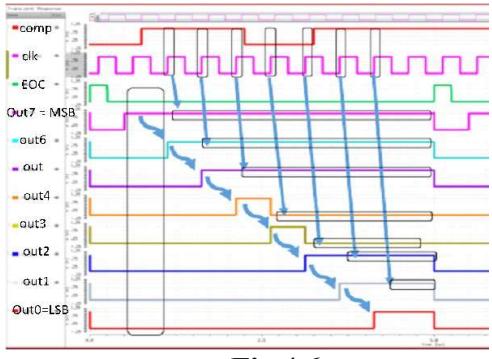
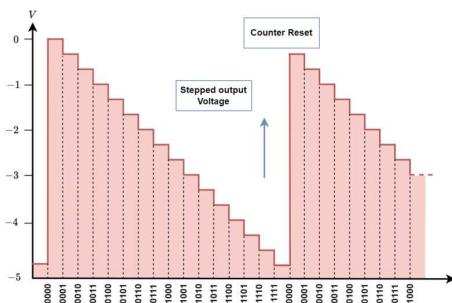


Fig. 4.3- n-iterations of a n-bit SAR ADC

The SAR ADC is collectively made up of four blocks, which are described as below:

COMPONENT	EXPECTED OUTPUT
Sample and Hold Circuit: It takes samples from the analog input signal and holds them for a particular period of time and then outputs the sampled part of the input signal. Capacitor holds the sampled input signal and provides it at output according to command input.	 <p>Fig 4.4</p>
Comparator: The comparator determines whether the SHA output is greater or less than the DAC output. There are two signals input to the comparator, V_{in} is the analog input voltage that needs to be converted into a digital format and V_{ref} is the reference voltage against which Vin is compared. If Vin > Vref, the comparator outputs a logic HIGH and if Vin < Vref, the comparator outputs a logic LOW.	 <p>Fig 4.5</p>
Successive Approximation Register (SAR): The SAR ADC uses a SAR to determine the digital output that represents the analog input voltage. It sequentially approximates the input analog voltage by setting and clearing bits in a shift register based on comparisons with the DAC output. This iterative process results in a digital output that accurately represents the analog input voltage.	 <p>Fig 4.6</p>
Digital to Analog Converter (DAC): A R-2R DAC is used here to convert digital signals back into analog form for comparison with the input signal. In an R-2R DAC, resistors are arranged in a ladder network where the values follow a binary weighting scheme.	 <p>Fig 4.7</p>

ADC design parameters

analog signal is continuous and infinite valued, whereas the digital signal is discrete with respect to time and quantized. A signal is said to be continuous if its value can be estimated at any point of time. A signal is said to be discrete if it is defined for only particular period of time. A signal that is quantized can only have certain values for each discrete period. Accuracy of digitized signal is dependent on two things: the number of samples taken and the resolution, or number of quantization levels. Nyquist criteria states that the sampling rate should be greater than twice the highest frequency of analog signal. This ensures that analog signal can be converted into digital signal & can be reconstructed back to analog accurately. For sampling we use a circuit called sample & hold . There is difference between sample & hold ckt & track & hold ckt.

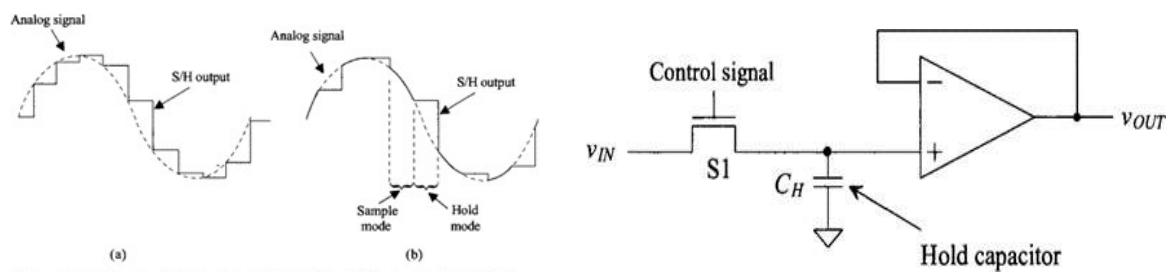


Figure 28.5 The output of (a) an ideal S/H circuit and (b) a track-and-hold (T/H).

Fig 4.8

Once the sampling command has been issued, the time required for the S/H to track the analog signal to within a specified tolerance is known as the acquisition time. Once the hold command is issued, the S/H faces Pedestal error which occurs as a result of charge injection and clock feedthrough. Parasitic capacitances of MOSFET get distributed onto the capacitor, which slightly changes its voltage. Droop error is related to the leakage of current from the capacitor. Solution is increasing the value of the sampling capacitor. The trade-off, however, is increased time will be required to charge the capacitor to the value of the input signal. The error that is introduced due to transient effect between the sample and the hold modes is called aperture error. A finite amount of time, referred to as aperture time, is required to disconnect the capacitor from the analog input source. if a periodic signal were being sampled repeatedly at the same points, slight variations in the hold value would result, thus creating sampling error. Aperture error depends on frequency of signal.

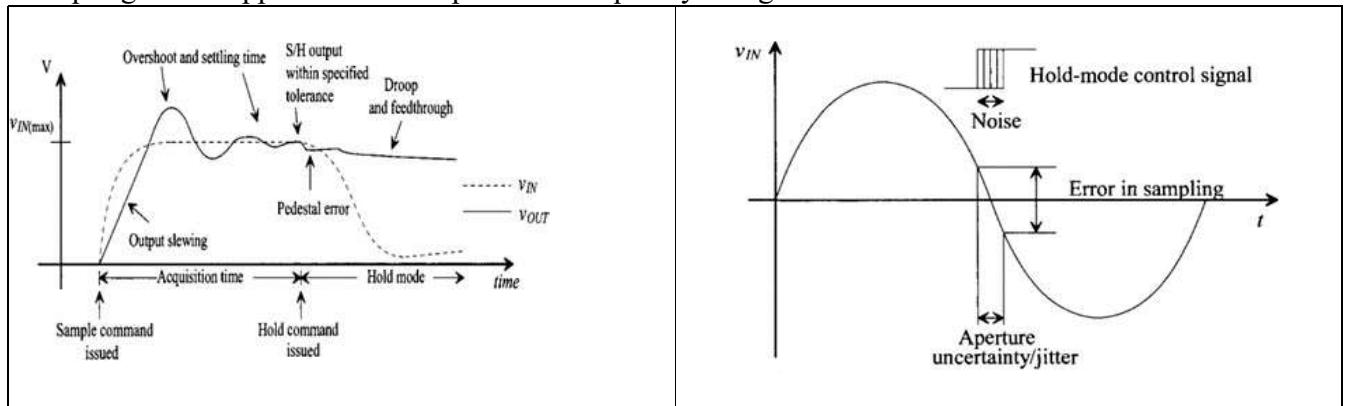


Fig 4.9

This maximum analog output voltage that can be generated is known as full-scale voltage, V_{fs} , and can be generalized to any N-bit DAC as $V_{fs} = (2^N - 1) V_{ref} / 2^N$. The least significant bit (LSB) refers to the rightmost bit in the digital input word. The LSB defines the smallest possible change in the analog output voltage. $LSB = V_{ref} / 2^N$. LSB bit is denoted by D_0 and MSB bit is denoted by D_{N-1} , where N is resolution of DAC / ADC. MSB causes the output to change by $V_{ref} / 2$. Resolution and LSB are almost same. To be very specific resolution (N) refers to the number bits that ADC / DAC can convert. Accuracy refers to how close the actual value is from the expected value. Increasing the resolution by 1 bit increases the accuracy by a factor of 2. $A = (V_{ref} - V_{fs})100 / V_{ref}$. The higher accuracy results in a higher linearity. A typically accuracy must lie in the range of $\pm 1/2$ LSB. Whenever the digital input increases by 1 bit there should be a corresponding increase of 1 LSB (0.635 V) in the output voltoge. However due to Nonideal components the actual analog increments tends to differ from their ideal values. The difference between the ideal and nonideal values is known as differential nonlinearity (DNL). $DNL = \text{actual height} - \text{ideal height}$. DNL is not one single value for entitre DAC / ADC. Instead DNL is calculated for every digital input. For eg for 3 bit DAC we find 8 DNL values fro DNL0 to DNL7. If dot lies above ideal curve DNL error is positive, if dot lies below ideal curve DNL error is negative. Always do DNL calculations in LSB instead of volts for simplicity. The DNL of entire DAC / ADC is equal to its largest value. Ideally a good DNL should lie between $\pm 1/2$ LSB. integral nonlinearity (INL) is defined as the difference between the actual output value and the ideal value. $INL = \text{actual pt.} - \text{ideal pt.}$ all points mentioned above for DNL apply to INL as well.

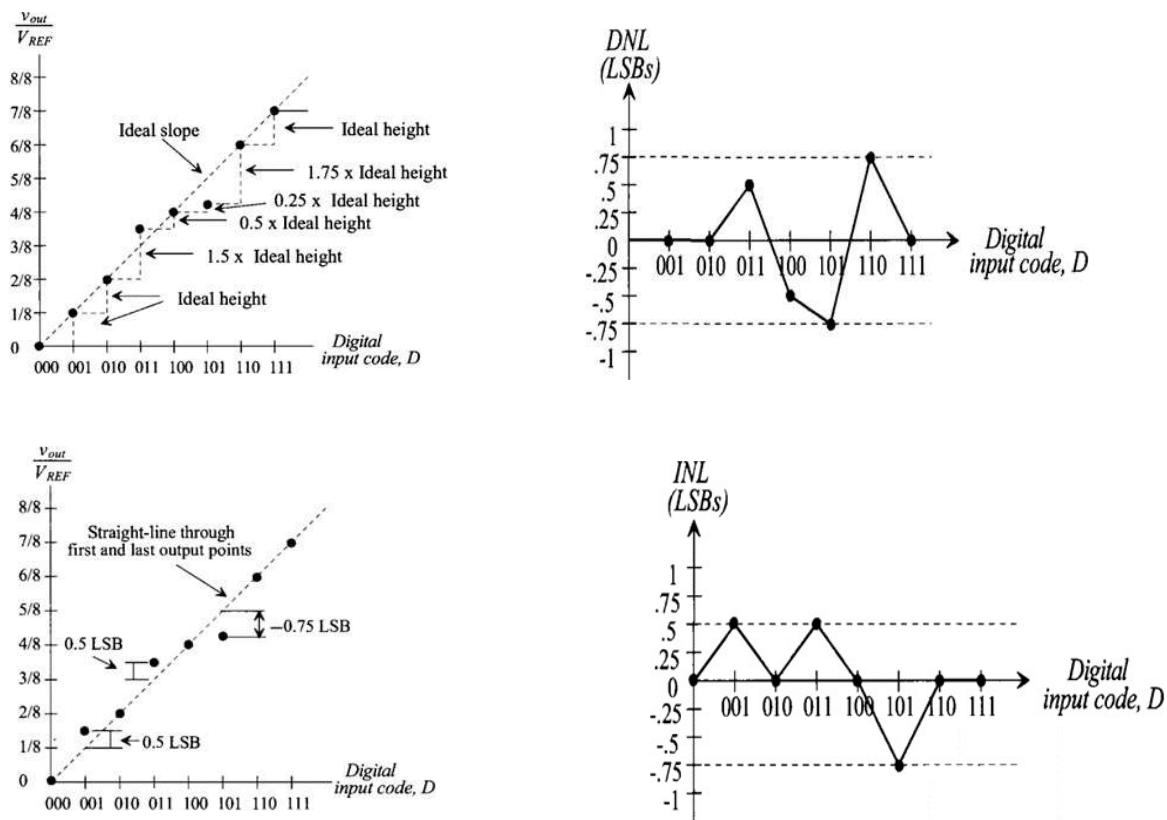


Fig 4.10

The analog output should be 0 V for $D = 0$. However, an offset exists if the analog output voltage is not equal to zero. This can be seen as a shift in the transfer curve. Gain error exist if ideal transfer curve and actual transfer curve are not equal. Gain error = Ideal slope - Actual slope. Another design specification is Latency which defines the total time from the moment that the input digital word changes to the time the analog output value has settled to within a specified tolerance. Latency = conversion time + settling time. Signal to noise ratio (SNR) is defined as ratio of power of signal to power of noise. Dynamic range is defined as the ratio of the largest output signal over the smallest output signal. dynamic range is related to the resolution of the converter. N-bit DAC can produce a maximum output of $(2^N - 1)$ LSBs and a minimum value of (1) LSB. $DR = 20\log [(2^N - 1)/1]$

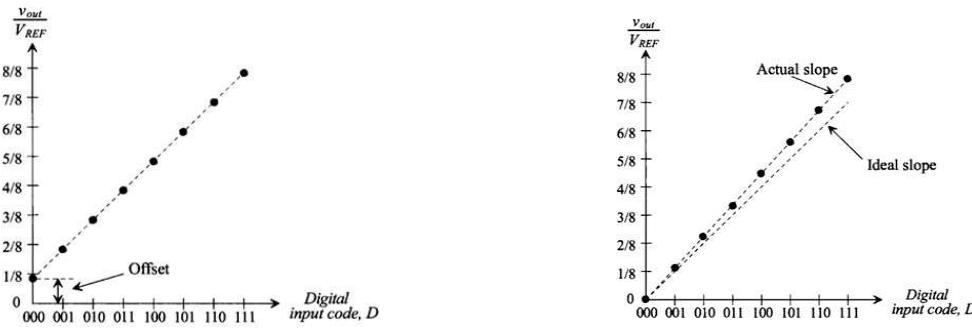


Fig 4.11

Since the analog input is an infinite valued quantity and the output is a discrete value, an error will be produced as a result of the quantization. This error, known as quantization error, Q_e , is defined as the difference between the actual analog output and the ideal analog output. $Q_e = \text{ideal} - \text{actual}$

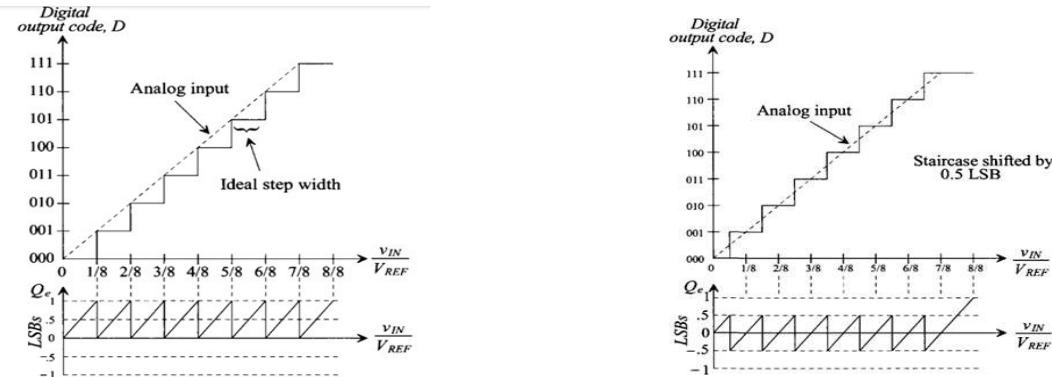
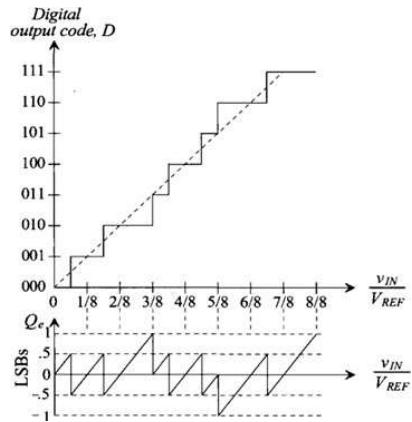


Fig 4.12

DNL of ADC is slightly different to that of DAC. Here we do not check step height, instead we check step width. DNL is the difference between the actual code width & ideal code width. $DNL = \text{actual width} - \text{ideal width}$. quantization error is directly related to the DNL. The total width of the step corresponding to 101 is completely missing; thus, the value of DNL_5 is -1 LSB. Any ADC possessing a DNL that is equal to -1 LSB is guaranteed to have a missing code. To calculate INL we measure distance between actual point and point on ideal curve. $INL = \text{actual pt.} - \text{ideal pt.}$ For INL of ADC we measure this distance horizontally , while for INL of DAC we measure this distance vertically. From fig it can be seen that $INL_3 = +0.5\text{LSB}$ & $INL_6 = -0.5\text{LSB}$ & rest all $INL = 0$. Offset error & gain error is same for both ADC/ DAC.



$$DNL_2 = 1.5 \text{ LSB} - 1 \text{ LSB} = 0.5 \text{ LSB}$$

$$DNL_3 = 0.5 \text{ LSB} - 1 \text{ LSB} = -0.5 \text{ LSB}$$

$$DNL_5 = -0.5 \text{ LSB}$$

$$DNL_6 = 0.5 \text{ LSB}$$

$DNL_7 = 0 \text{ LSB}$ (since the ideal step width at this code transition)

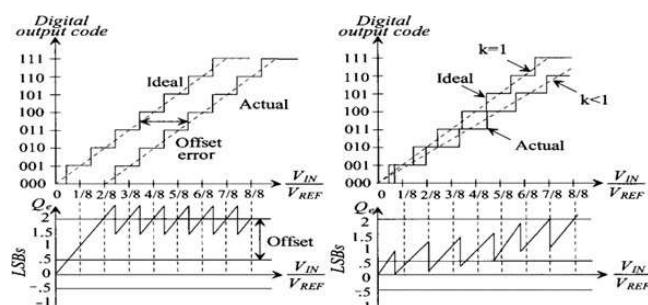
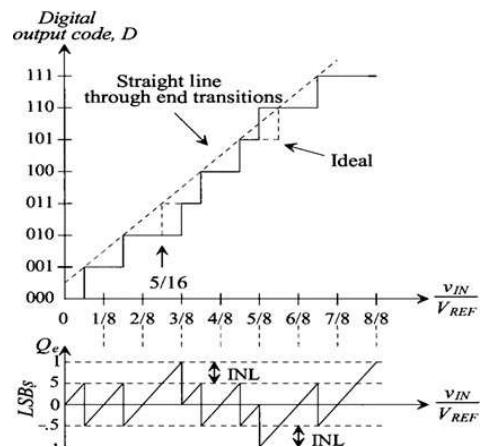
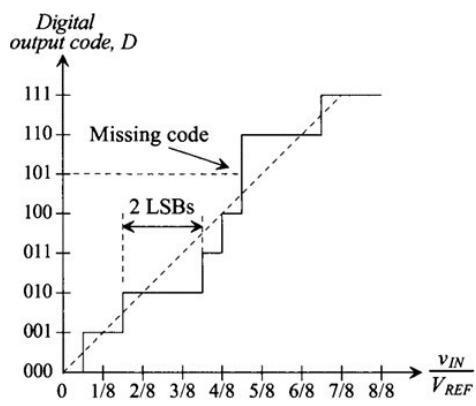


Figure 28.24 Transfer curve illustrating (a) offset error and (b) gain error.

Fig 4.13

Aliasing error occurs if Nyquist criteria is not followed for sampling the input analog signal in an ADC. Aliasing can be eliminated by both sampling at higher frequencies and by filtering the analog signal before sampling and removing any frequencies that are greater than one-half the sampling frequency. It is good practice to filter the analog signal before sampling to eliminate any unknown higher order frequency components or noise that could result in aliasing. Aperture error present in SH circuit also affects the overall performance of ADC. SNR for both ADC & DAC remains same.

SAR - Binary Search Algorithm

Working of the SAR Block :

SAR block uses a binary search algorithm to successively approximate the analog input signal to produce equivalent Binary output. It performs a series of steps to determine the digital code that represents the input signal by setting each bit of the digital output starting from the most significant bit (MSB) to the least significant bit (LSB). The SAR logic controls the Digital-to-Analog Converter (DAC) and Comparator. The SAR logic updates the approximation register depending upon the comparator's result (whether the DAC output is higher/lower than the input voltage). Once all bits are processed, the final binary equivalent value in the approximation register represents the digital equivalent of the analog input voltage.

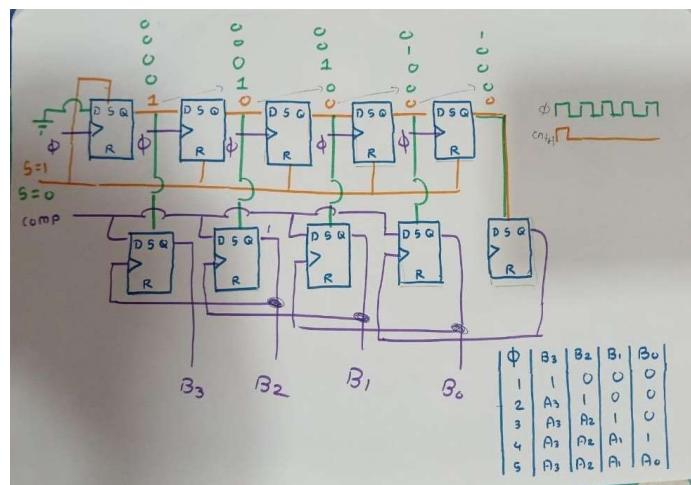


Fig 4.14

Conventional D flip flop

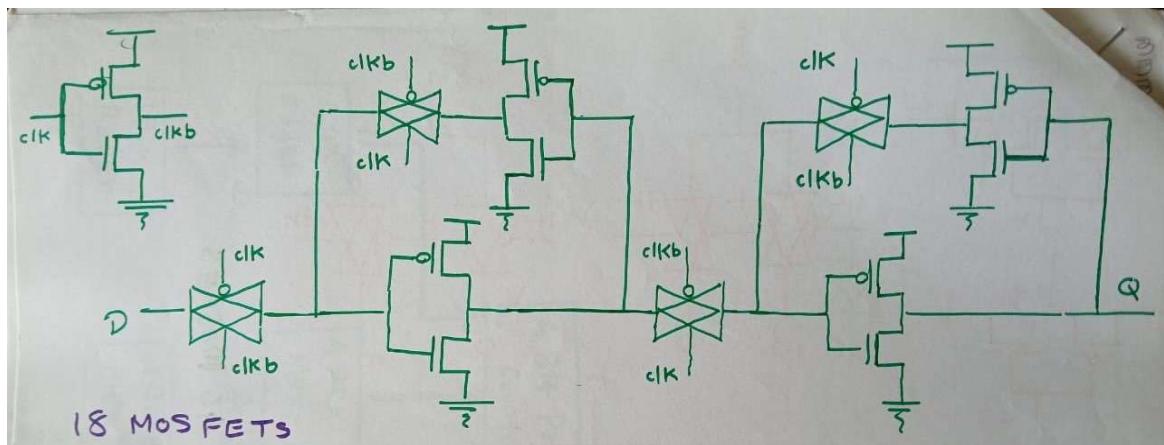


Fig 4.14

Upgraded D flip flop

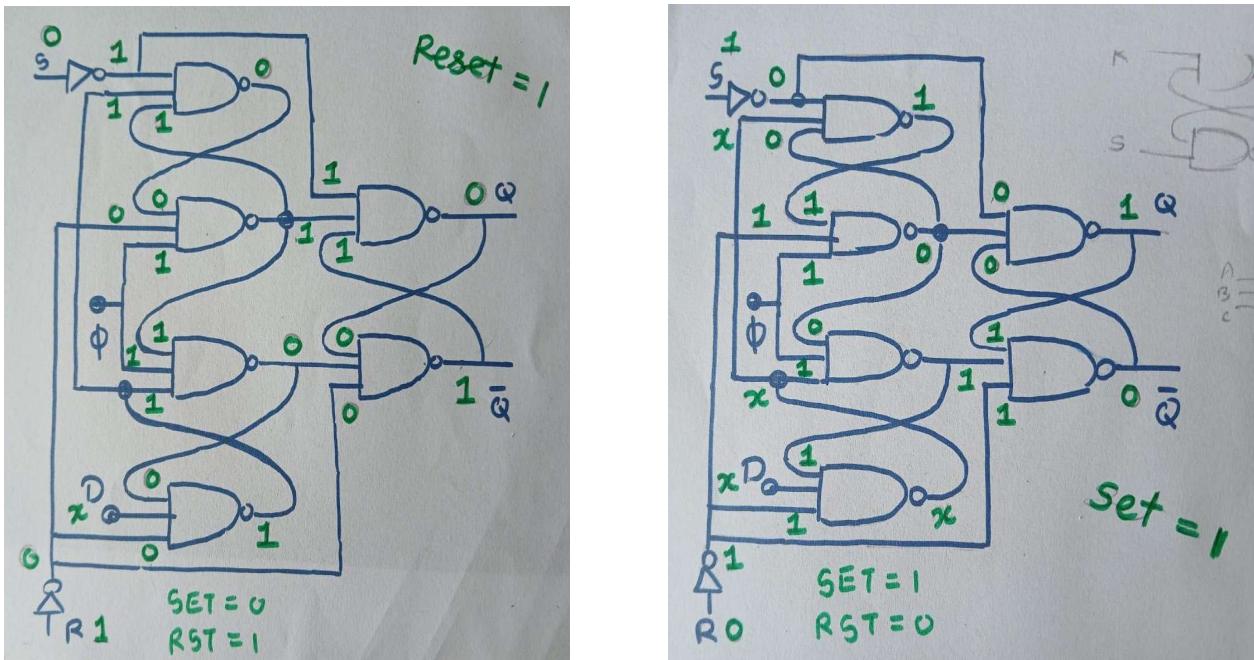


Fig 4.15

SAR block construction

SAR circuit is made up of 18 D flip flops. It is basically a combination of SISO shift register and PIPO shift register. SAR circuit takes input from comparator and gives output to R-2R DAC. SAR works on principle of Binary Search Algorithm. It generates output from LHS to RHS i.e from MSB to LSB. We are designing 8 bit SAR. so we will require total 9 clock cycles to generate output. At the start of conversion we reset SAR circuit i.e we store 1000,0000 inside the circuit. For next 8 clock cycles we keep this reset signal low. During these 8 clock cycles the input given by comparator is pushed into shift register. Some SAR circuits use additional signals like SOC (start of conversion) & EOC (end of conversion).

D flip flop - Working

The D flip flop used in the SAR circuit is positive edge triggered. It has active high SET & reset pins. It is Synchronous FF - set / reset action takes place only at a positive edge of clk. Both set and reset pins should not become HIGH simultaneously. It is invalid . This FF is made using 3 input NAND gates and 1 input NOT gates. At the positive edge of clk, output of FF = input to the FF. provided S = R = 0. Rest in all other cases the output of FF is retained, it does not change. When the set is HIGH output goes 1, irrespective of input given to FF. When reset is HIGH output goes 0 , irrespective of input given to FF. Outputs Q and $\sim Q$ are complementary to each other. Bottom - Up design approach is used to make the SAR circuit. SAR circuit is made using Semi Custom Design methodology

OPAMP construction

OP AMP circuits can be of 2 stage, 3 stage, or even 4 stage. The circuit given above is a 2 stage OP-AMP circuit. The first stage comprises an PMOS differential amplifier. The second stage comprises a common source NMOS amplifier. MOSFET M2 & M3 act as PMOS constant current sources. They are given external biasing (Vbias). 2 capacitors are used i.e Cc compensation capacitor & Cl load capacitor. MOSFET M4 & M5 form a differential pair circuit. Differential pair circuits can have passive load like resistor or active loads like current source & current mirror. In this circuit we have taken the current mirror as load. MOSFET M6 & M7 form NMOS current mirror circuit. Some OP-AMP circuits have a buffer stage on LHS while some do not have a buffer stage on LHS. For the buffer we use a common drain amplifier circuit. Our circuit is an buffered OPAMP circuit. MOSFET M1 & M8 make buffer.

OPAMP Working

Working of OP-AMP circuit The op-amp uses a single supply configuration, meaning it operates between voltages: VDD (positive) and GND (negative). for single supply OPAMP we cannot use NMOS differential pair, otherwise output will get clipped, hence we use PMOS differential pair. This allows the op-amp to amplify both positive and negative input signals, resulting in an output that can swing both above and below ground. Compensation Capacitor (Cc) To ensure stability, a compensation capacitor is placed between the output of the first and second stages. This provides frequency compensation, which helps maintain the phase margin and prevent oscillations in the op-amp. MOSFET M2, M3 act as PMOS current source. They ensure constant current flows through both the stages of OPAMP. MOSFET M4, M5 act as PMOS differential pair circuits. This circuit amplifies the difference between inputs Vin1 & Vin2. The common-mode rejection ratio (CMRR) is high due to the current mirror and the fact that any common-mode signal results in minimal change in output. differential amplifier & current mirror together make the 1st stage of OP-AMP. It offers high gain but low output current due to high output impedance provided by active load. MOSFET M6, M7 act as PMOS current mirror circuit. This circuit copies the current flowing through M4 into the current flowing through M5. it ensures that current coming from M2 gets equally distributed in both branches. MOSFET M6 is in diode configuration (because its gate and drain terminal are tied together). M9 is a single stage CS amplifier with PMOS current source as load (M3). this 2nd stage of OP-AMP. It provides high output current due to low output impedance, however gain decreases.

OPAMP circuit diagram

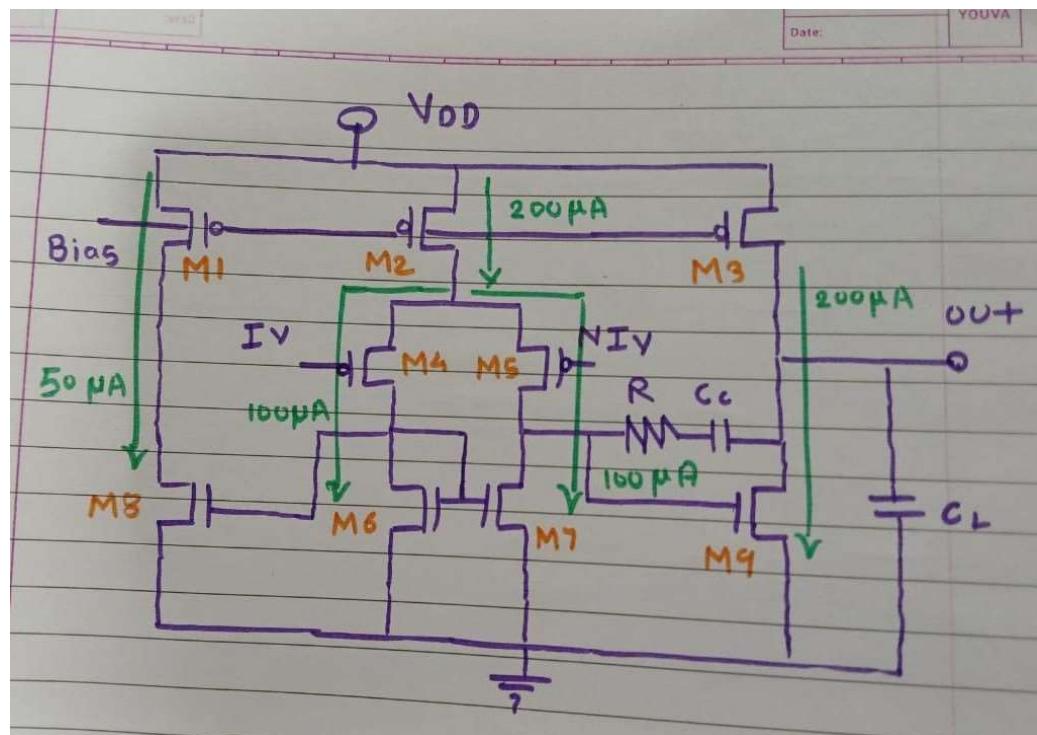


Fig 4.16

OPAMP - MOSFET sizing table

MOSFET	length	width
M2	1u	76.39u
M4 M5	1u	6.65u
M6 M7	1u	10u
M9	1u	14.55u
M1	1u	18.14u
M8	1u	2.46u
M3	1u	71.82u

MOSFET Sizing Procedure

Let the open loop gain > 60 dB

Phase margin has to be > 60 degree for stability

Conversion time < 60ns

Assuming comparator (20 ns) + DAC (60 ns) + SAR (10 ns) = 90 ns < 100 ns

Where 100 ns = 0.1 us is time required to convert one bit.

For 8 bits total 0.8 us required. Hence SH circuit holds input for 0.8 us.

Let us fix power dissipation < 2 mW

P < 2 mw

VI < 2 mW

(3.3 V) I < 2 mW

I < 606 mA

Let us fix the total current to be 450 mA

The distribution of current flowing via different MOSFETS is as follows

Current via M1 M8 is 50 uA

Current via M2 is 200 uA

Current via M4 M6 M5 M7 is 100 uA

Current via M3 M9 is 200 uA

MOSFET M2 (PMOS)

$V_{gs} < V_{th}$	$V_{ds} < V_{gs} - V_{th}$	V_g	W
$V_{sg} > V_{th}$	$-V_{sd} > -V_{sg} - V_{th}$	2.6	+ 100 μ
$V_s - V_g > V_{th}$	$-V_d > -V_g - V_{th}$	2.50	58.53 μ
$3.3 - V_g > 0.5$	$-3 > -V_g - 0.5$	2.55	76.39 μ
$V_g < 2.8$	$V_g > 2.5$		

MOSFET M4 M5 (PMOS)

$V_{sg} > V_{th}$	$-V_d > -V_g - V_{th}$	V_s	V_d	W
$V_s - V_g > V_{th}$	$-V_d > -1.65 - 0.5$	3	0.6	6.65 μ
$V_s - 1.65 > 0.5$	1.65 is mid value of 3.3	3	0.65	6.65 μ
1.65 is mid value of 3.3	$-V_d > -2.15$	3	0.7	6.66 μ
$V_s > 2.15$	$V_d < 2.15$			
Form above table $V_s = 3$ which satisfy the condition				

MOSFET M6 M7 (NMOS)

$V_{gs} > V_{th}$	$V_{ds} > V_{gs} - V_{th}$	V_g	W
$V_g - V_s > V_{th}$	$V_d > V_g - V_{th}$	0.6	12.97 μ
$V_g - 0 > 0.5$	However $V_g = V_d$	0.65	10.43 μ
$V_g > 0.5$	$V_g > V_g - 0.5$	0.7	18.51 μ
		0.75	21.37 μ

MOSFET M9 (NMOS)

$V_{gs} > V_{th}$	$V_{ds} > V_{gs} - V_{th}$	V_g	W
$V_g - V_s > V_{th}$	$V_d > V_g - V_{th}$	0.72	14.52 μ
$V_g - 0 > 0.5$	1.65 is mid value of 3.3		
$V_g > 0.5$	$1.65 > V_g - 0.5$		
	$V_g < 2.15$		

MOSFET M3 (PMOS)

V _{sg} > V _{th}	-V _{sd} > -V _{sg} - V _{th}	V _g	W
V _s - V _g > V _{th}	-V _d > -V _g - V _{th}	2.55	71.13 u
3.3 - V _g > 0.5	-1.65 > -V _g - 0.5		
V _g < 2.8	1.65 is mid value of 3.3		
	-V _g < -1.15		
	V _g > 1.15		

MOSFET M1 (PMOS)

V _{sg} > V _{th}	-V _{sd} > -V _{sg} - V _{th}	V _g	W
V _s - V _g > V _{th}	-V _d > -V _g - V _{th}	2.50	13.63 u
3.3 - V _g > 0.5	However V _d = V _g	2.55	18.14 u
V _g < 2.8	-V _g > -V _g - 0.5		
	V _g < V _g + 0.5		

MOSFET M8 (NMOS)

V _{gs} > V _{th}	V _{ds} > V _{gs} - V _{th}	V _g	V _d	W
V _g - V _s > V _{th}	V _d > V _g - V _{th}	0.6	2.5	2.46 u
V _g - 0 > 0.5	V _d > V _g - 0.5	0.6	2.55	2.42 u
V _g > 0.5		0.65	2.5	1.19 u
		0.65	2.55	1.17 u

$$R = (C_l + C_c) / G_m * C_c$$

$$R = (1p + 1p) / 1.36533 * 1p$$

$$R = 1.47 K$$

OPAMP design Parameters

PARAMETER	SI UNIT	FORMULA
Open-Loop Gain (AOL) - The gain of the op-amp without feedback.	Dimensionless (or in decibels (dB))	$AOL = V_{out} / V_{in}$ $AOL(dB) = 20\log_{10}(V_{out} / V_{in})$
Slew Rate (SR) - The maximum rate at which the output voltage can change.	V/ μ s (Volts per microsecond)	$SR = \Delta V_{out} / \Delta t$
Common-Mode Rejection Ratio (CMRR) - The ability of an op-amp to reject common-mode signals (signals present at both inputs).	Dimensionless (or in decibels (dB))	$CMRR = A_v / A_{cm}$ $CMRR(dB) = 20\log_{10}(A_v / A_{cm})$
Power Supply Rejection Ratio (PSRR) - The ability of the op-amp to reject variations in the power supply voltage.	Dimensionless (or in decibels (dB))	$PSRR = V_{supply} / V_{out}$ $PSRR(dB) = 20\log_{10}(V_{supply} / V_{out})$
Bandwidth (BW) - The frequency range over which the op-amp can amplify signals without significant attenuation.	Hertz (Hz)	$BW = UGBW / AOL$
Unity-Gain Bandwidth (UGBW) - The frequency at which the open-loop gain of the op-amp becomes unity	Hertz (Hz)	$UGBW = BW * AOL$

Gain Bandwidth Product (GBP) - It is the frequency range over which the op-amp maintains a given gain.	Hertz (Hz)	$\text{GBP} = \text{BW} * \text{Av}$
Input Offset Voltage (V_{os}) - The differential DC voltage required between the inputs to make the output zero.	Volts (V)	No direct formula, typically measured.
Input Bias Current (I_b) - The average of the DC currents entering the inverting and non-inverting terminals of the op-amp.	Amperes (A)	$I_b = [(I+) + (I-)] / 2$
Input Offset Current (I_{os}) - The difference between the DC bias currents entering the inverting and non-inverting terminals.	Amperes (A)	$I_{os} = (I+) - (I-)$
Output Voltage Swing - The maximum voltage swing the op-amp can output relative to its power supply voltage.	Volts (V)	$V_{out(\max \text{ swing})} = V_{DD} - V_{sat}$ $V_{out(\min \text{ swing})} = V_{SS} + V_{sat}$
Input Impedance (Z_{in}) - The impedance seen looking into the input terminals of the op-amp.	Ohms (Ω)	$Z_{in} = V_{in} / I_{in}$
Output Impedance (Z_{out}) - The impedance seen looking into the output terminal of the op-amp.	Ohms (Ω)	$Z_{out} = V_{out} / I_{out}$

Settling Time - The time taken for the output to settle within a specified error band after a step input.	Seconds (s)	Typically specified for different error bands (e.g., 0.1%, 1%).
Phase Margin - The phase difference between the output and the input of the amplifier at the frequency where the gain is unity.	Degrees ($^{\circ}$)	Typically measured from a Bode plot, no specific formula.
Noise (Voltage or Current Noise) - The random fluctuation of the output voltage or current due to inherent circuit noise.	Volts / $\text{Hz}^{0.5}$ Amp / $\text{Hz}^{0.5}$	Noise is found out by measuring noise spectral density
Total Harmonic Distortion (THD) - The measure of harmonic distortion present in the output signal of the op-amp.	Percent (%)	$\text{THD} = (\text{Power of Harmonics} * 100) / \text{Power of Fundamental}$
Input Voltage Range (IVR) - The range of input voltages over which the op-amp operates correctly.	Volts (V)	$V_{in(\text{max swing})} = V_{DD} - V_{sat}$ $V_{in(\text{min swing})} = V_{SS} + V_{sat}$

Sample and Hold Circuit Working:

In a SAR ADC, the S/H circuit is responsible for capturing the input analog signal at a specific moment in time and holding that value steady during the conversion process. It operates by successively narrowing down the value of the input signal through a series of comparisons with reference voltages. Before this process begins, the S/H circuit samples the analog input voltage when a control signal, usually a clock pulse, is triggered. This allows the S/H circuit to take a snapshot of the input signal, ensuring that the voltage remains constant throughout the subsequent conversion steps.

During the sample phase, the S/H circuit's switch (often a transistor or FET) is closed, connecting the input signal to a capacitor. This capacitor temporarily stores the sampled voltage. The timing of this sampling is critical; it must occur just before the ADC's conversion process to ensure that the input voltage accurately reflects the value that needs to be converted. The switch remains closed for a short duration, allowing the capacitor to charge to the input voltage level.

Once the sampling is complete and the control signal is removed, the switch opens, and the S/H circuit enters the hold phase. In this phase, the capacitor holds the voltage steady, isolating it from the input signal. This stability is crucial because the SAR ADC now begins the conversion process, comparing the held voltage against a series of reference levels to determine the corresponding digital output. The integrity of the voltage held by the capacitor must be maintained during this phase to avoid errors in the digital conversion.

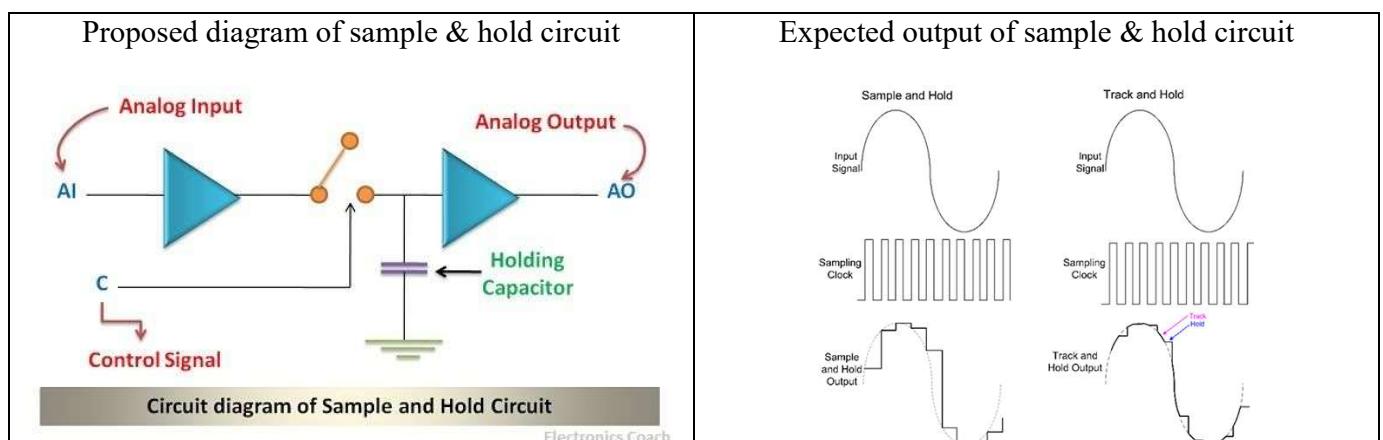


Fig 4.17

The effectiveness of the S/H circuit directly influences the performance of the SAR ADC. Key factors include the accuracy and speed of the S/H circuit, as well as the time it takes for the capacitor to charge and hold the voltage. A high-speed S/H circuit ensures that the ADC can operate at faster sampling rates, while a high-accuracy circuit minimizes quantization errors and improves the overall resolution of the ADC.

Additionally, after the hold phase, it's important that the capacitor discharges slowly enough to prevent voltage droop, which can occur if the load on the output is too large. To mitigate this, output buffers are often used to stabilize the output voltage and isolate it from load variations.

Working of DAC:

Digital-to-Analog Converters (DACs) are crucial components in various electronic systems, responsible for converting digital signals, typically represented in binary form, into corresponding analog voltages or currents. This conversion is essential in applications ranging from audio playback to video rendering and control systems. At its core, a DAC takes a binary input—such as a series of 1s and 0s—and produces an analog output that reflects the magnitude of that digital signal. The primary function of a DAC is to create a continuous analog representation from discrete digital values, allowing for smooth transitions and outputs.

The R-2R ladder DAC consists of only two resistor values: R and $2R$. This simplicity reduces the complexity of the design and makes it easier to create precise resistor values, which is crucial for accurate operation. The structure consists of a series of resistors connected in a ladder-like formation, with switches that connect to the digital input bits.

The output voltage is determined by the weighted contributions of each active bit, with the most significant bit (MSB) contributing the most to the output. This design allows the DAC to produce a continuous analog voltage that corresponds to the digital input, facilitating its use in various applications such as audio and control systems.

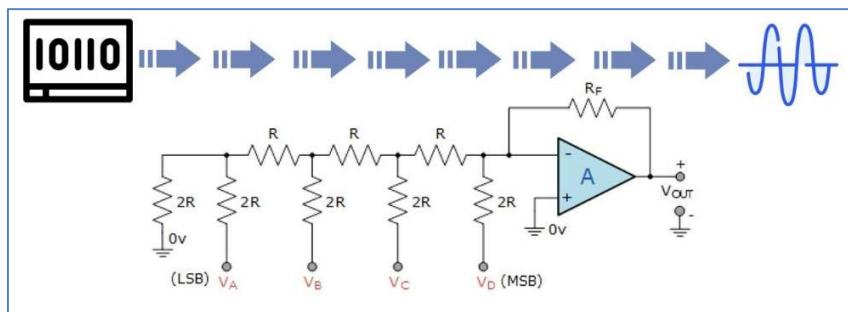


Fig 4.18

Working of Comparator:

The comparator has two input terminals, often referred to as the inverting input ($-$) and the non-inverting input ($+$). When a voltage is applied to these inputs, the comparator continuously monitors the two levels. If the voltage at the non-inverting input ($+$) exceeds the voltage at the inverting input ($-$), the output of the comparator switches to a high state (often close to the supply voltage). Conversely, if the voltage at the inverting input exceeds that at the non-inverting input, the output switches to a low state (near ground).

This output is typically a digital signal, which makes comparators useful in various applications such as analog-to-digital conversion, zero-crossing detection, and threshold detection. Comparators can be implemented using operational amplifiers (op-amps) configured in open-loop mode, allowing them to provide fast response times and high sensitivity. Some comparators also feature hysteresis to prevent rapid switching of the output due to noise or small fluctuations in input voltages, enhancing stability and reliability in practical applications.

CHAPTER 5

HARDWARE &

SOFTWARE

OVERVIEW

CHAPTER 5 HARDWARE & SOFTWARE

Software used: Cadence Virtuoso, version-

Cadence Virtuoso is a leading electronic design automation (EDA) tool suite widely used in the field of VLSI (Very Large Scale Integration) design. It provides a comprehensive environment for designing, simulating, and verifying integrated circuits (ICs), catering to both analog and mixed-signal designs. The platform supports a variety of design methodologies and is renowned for its user-friendly interface, robust features, and seamless integration with other Cadence tools.

Simulation is another vital component of the Virtuoso suite, with tools like Spectre and SpectreRF providing powerful simulation capabilities for both transient and frequency-domain analysis. These simulators enable engineers to validate the functionality and performance of their designs under various conditions, ensuring that they meet specified requirements. Additionally, the inclusion of modeling support for various semiconductor processes enhances the reliability of simulations, allowing for more accurate predictions of real-world performance.

The integration of Virtuoso with Cadence's other tools, such as the Encounter Digital Implementation and the Allegro PCB design tools, further extends its functionality. This interoperability facilitates a seamless design flow from concept to fabrication, enabling efficient collaboration across different stages of the design process. Furthermore, Virtuoso's extensive library of components and models aids in accelerating the design process by providing ready-to-use elements tailored to specific design needs.

In summary, Cadence Virtuoso is an essential tool for VLSI designers, offering a robust platform for the entire design lifecycle. Its combination of schematic capture, layout, and simulation capabilities, along with strong integration with other EDA tools, positions it as a cornerstone in modern semiconductor design workflows. As technology continues to evolve, Virtuoso remains at the forefront, helping engineers tackle the challenges of designing increasingly complex integrated circuits.

CHAPTER 6

RESULT &

DISCUSSION

CHAPTER 6 RESULT & DISCUSSION

SAR - Circuit Diagram

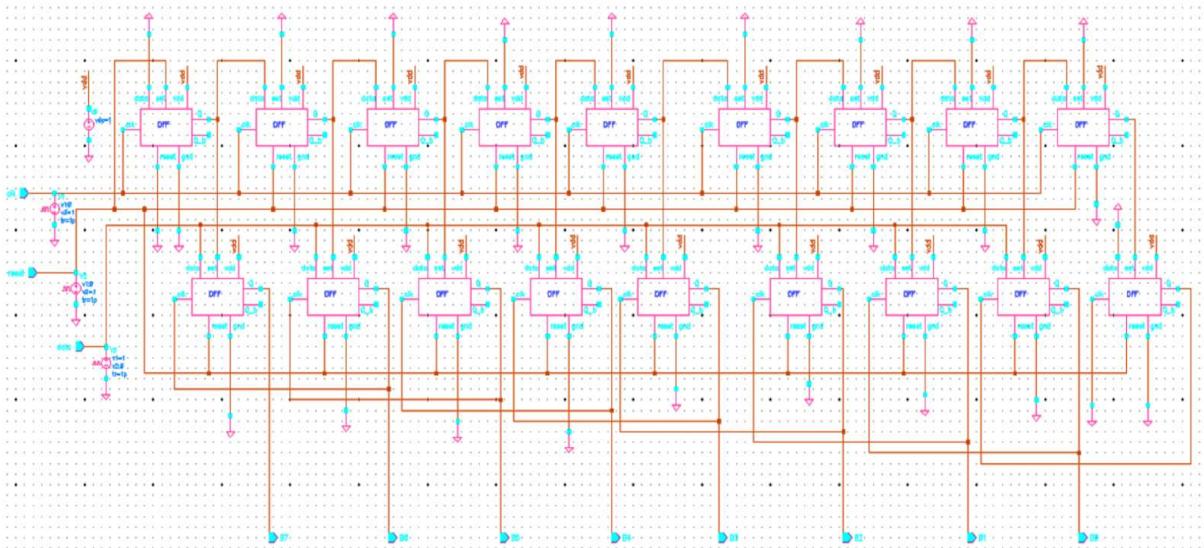


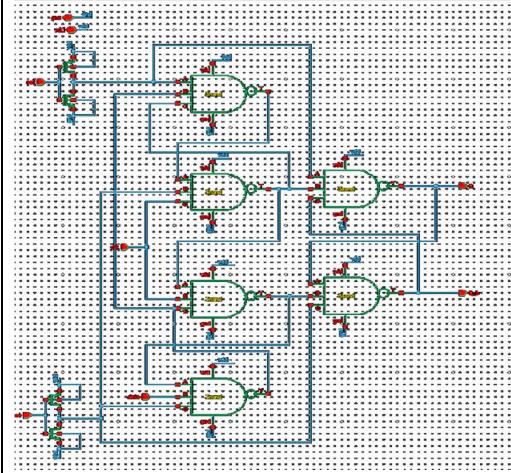
Fig 6.1

SAR - Output Waveform



Fig 6.2

D flip flop circuit



D flip flop output waveform

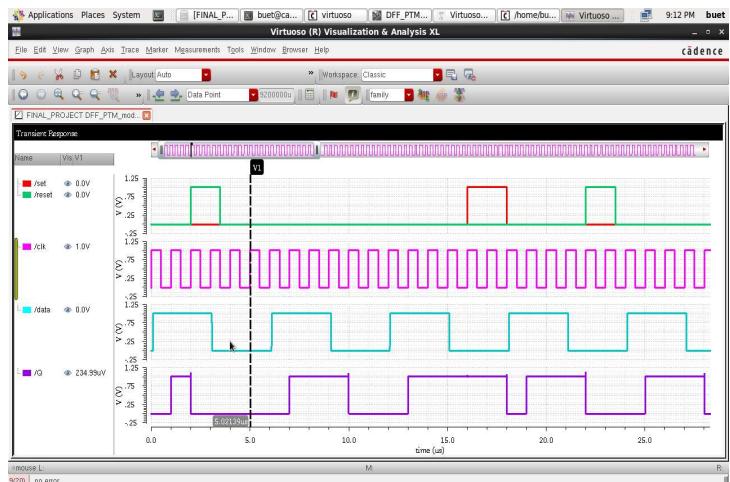
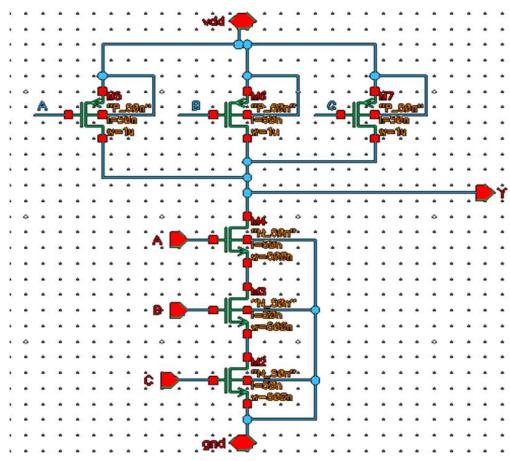


Fig 6.3

NAND gate circuit



Output waveform

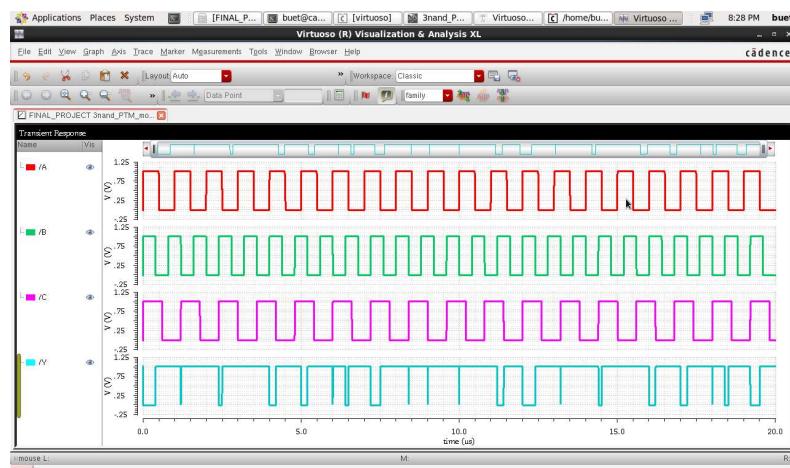


Fig 6.4

PMOS differential pair OP AMP circuit

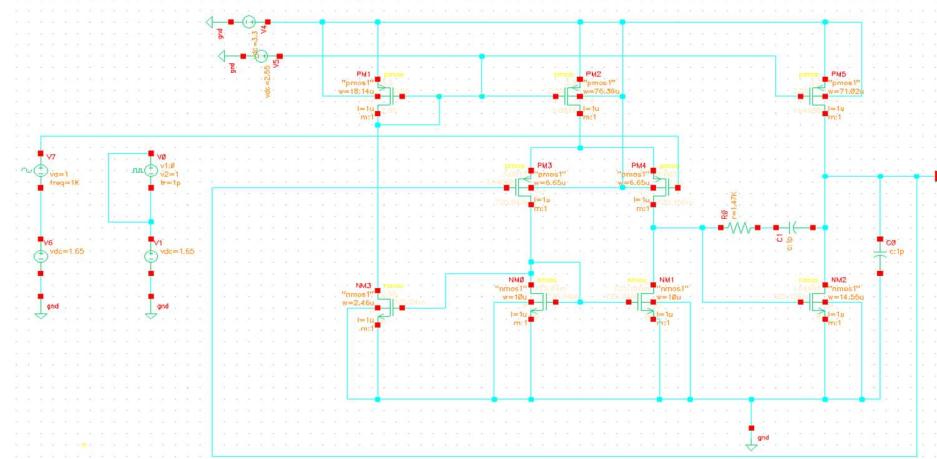


Fig 6.5

OPAMP circuit results

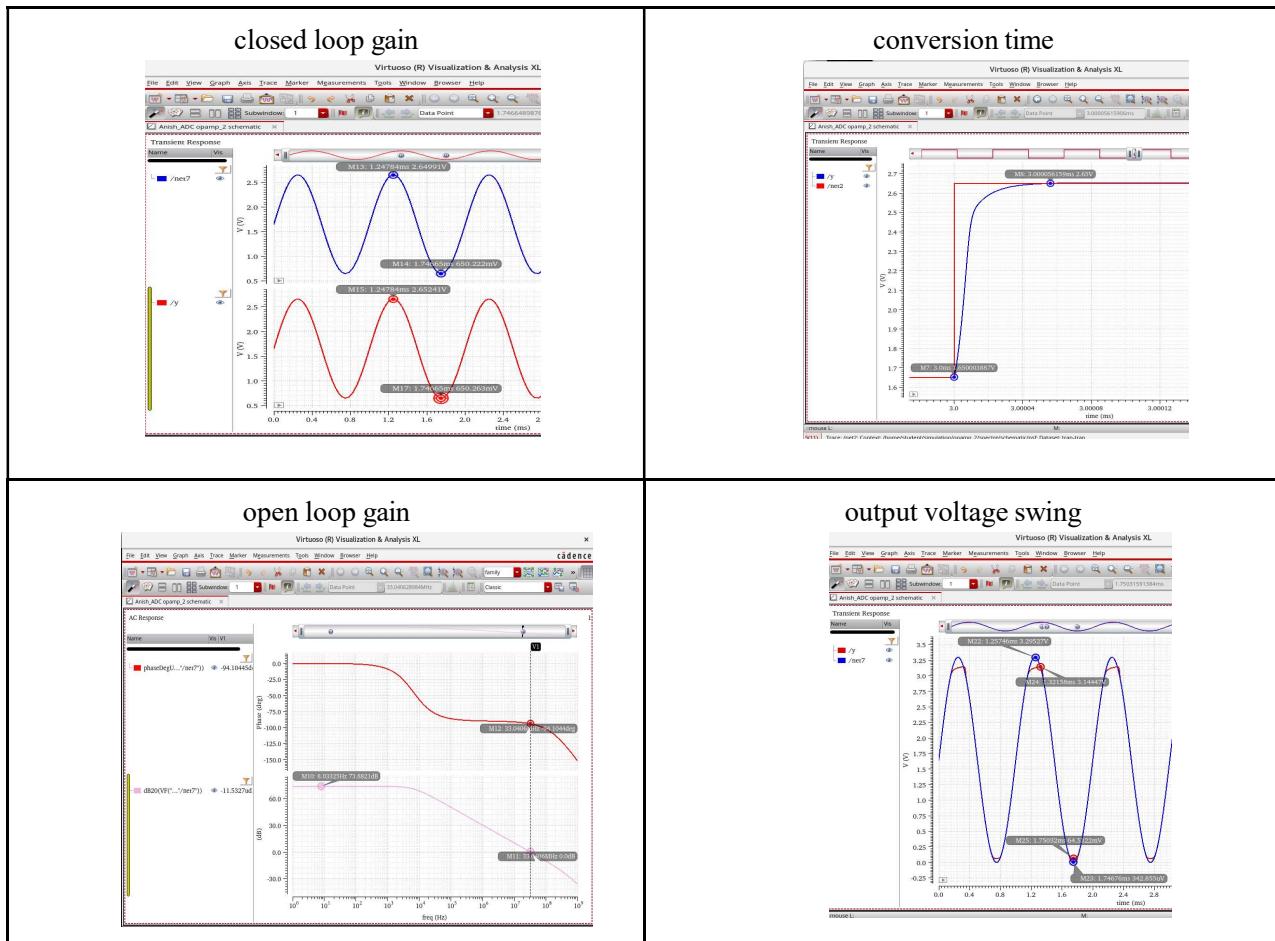


Fig 6.6

R-2R DAC circuit

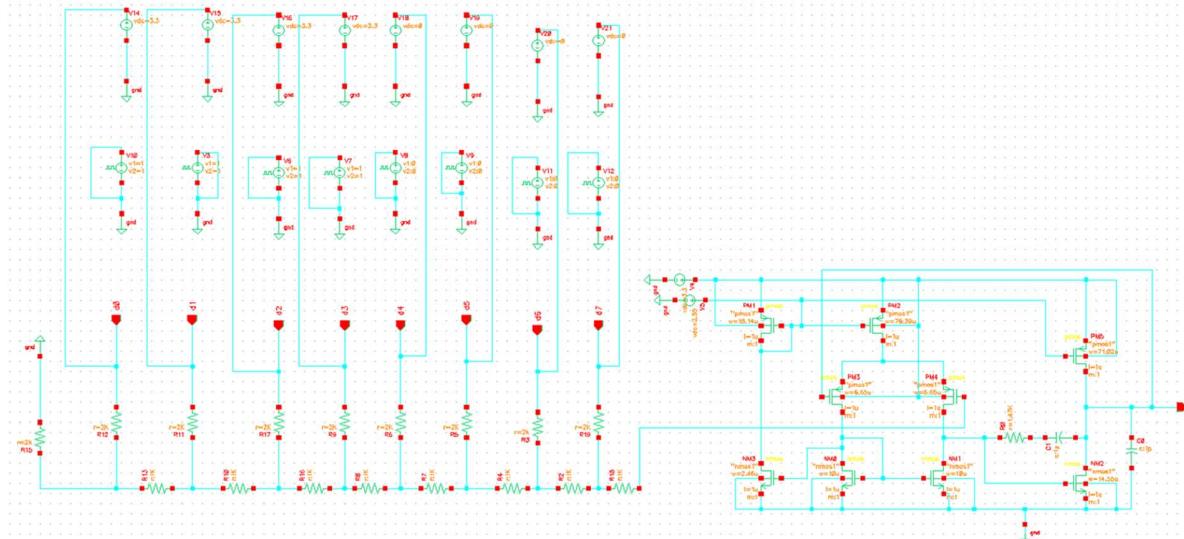


Fig 6.7

R-2R DAC circuit results

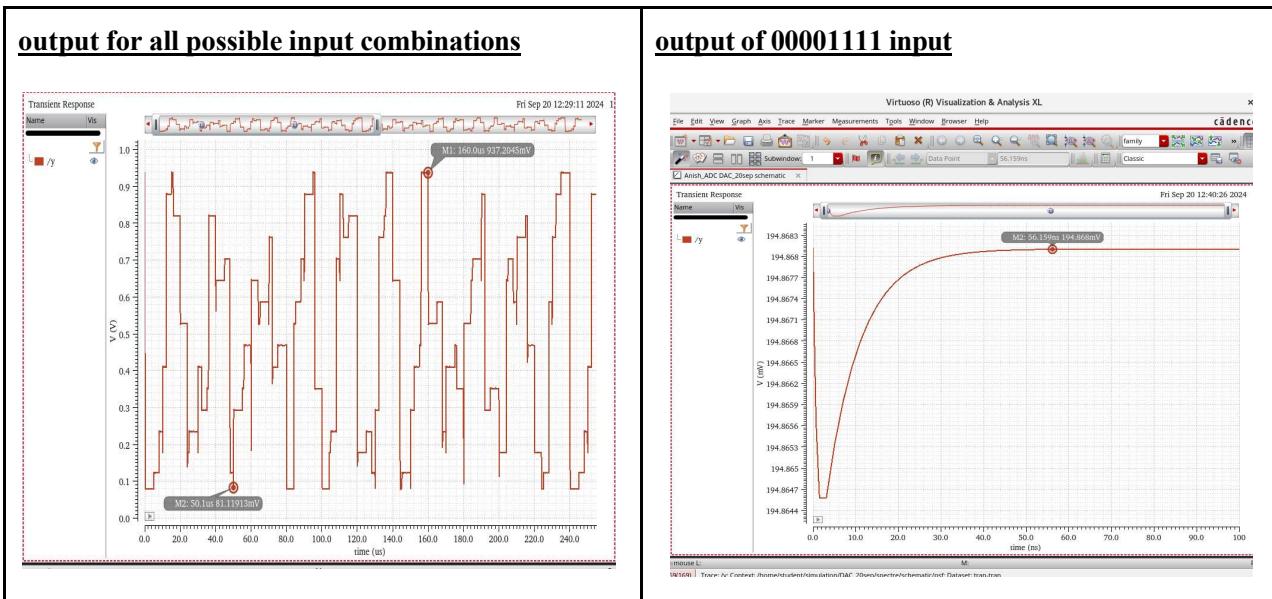


Fig 6.8

Sample & Hold Circuit

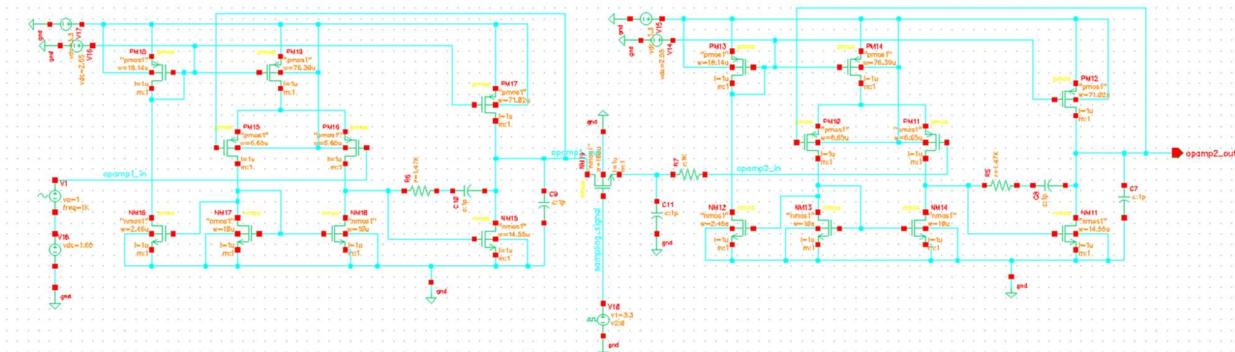


Fig 6.9

Sample & Hold Circuit Output

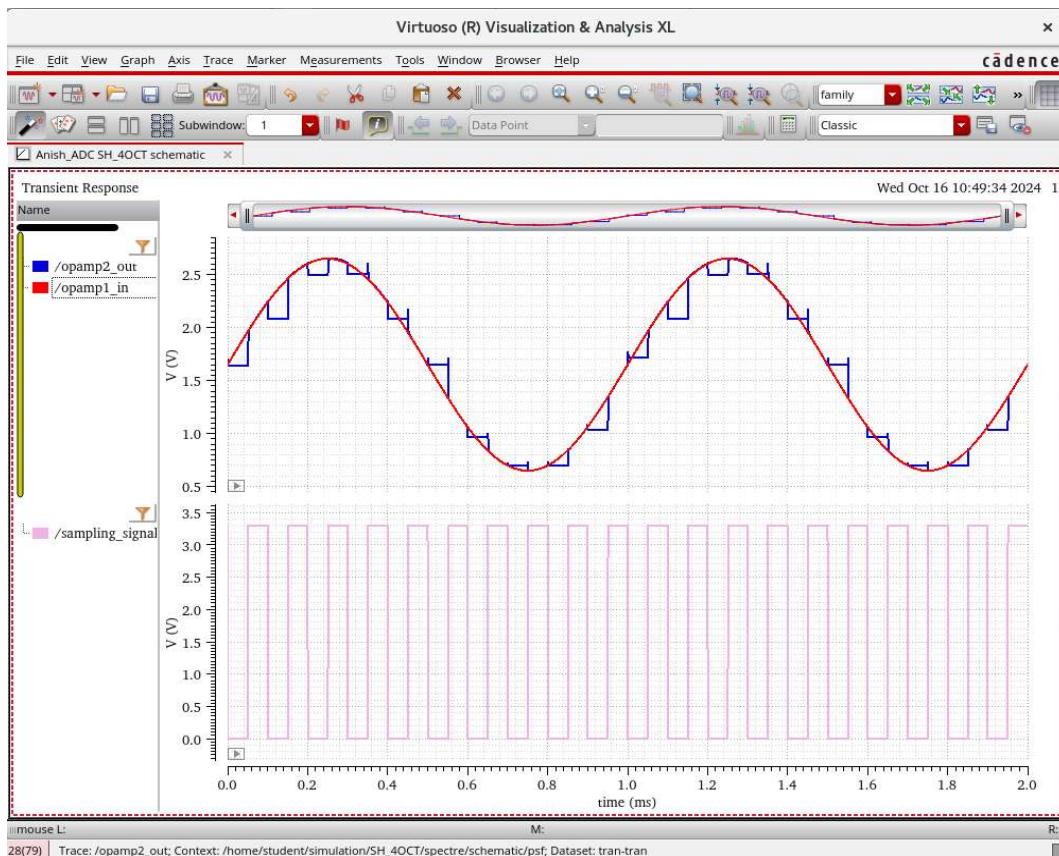


Fig 6.10

Trans analysis of Comparator circuit with input applied to non inverting terminal

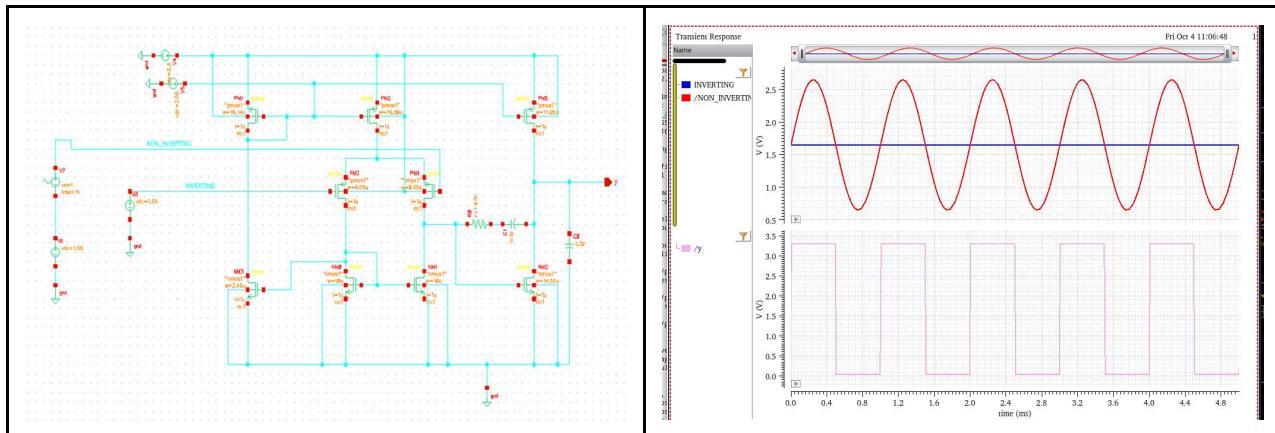


Fig 6.11

Trans analysis of Comparator circuit with input applied to non inverting terminal & inverting terminal

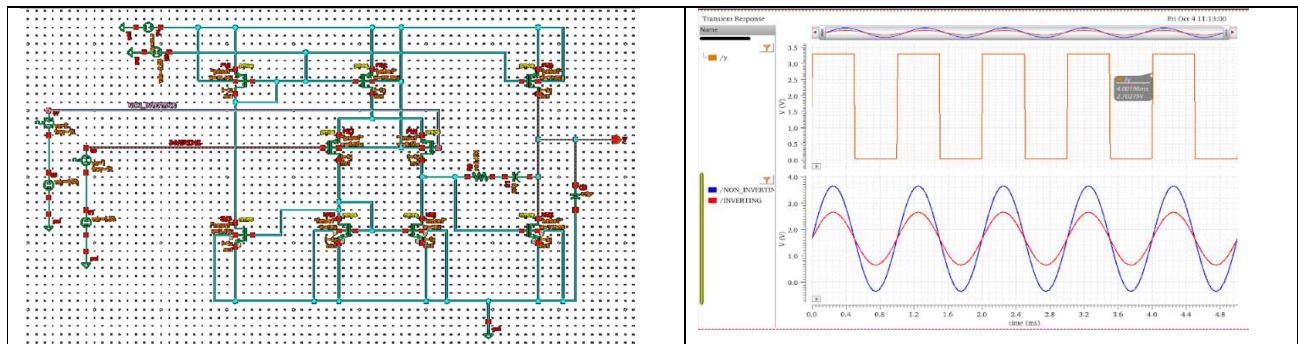


Fig 6.12

Conversion Time of Comparator

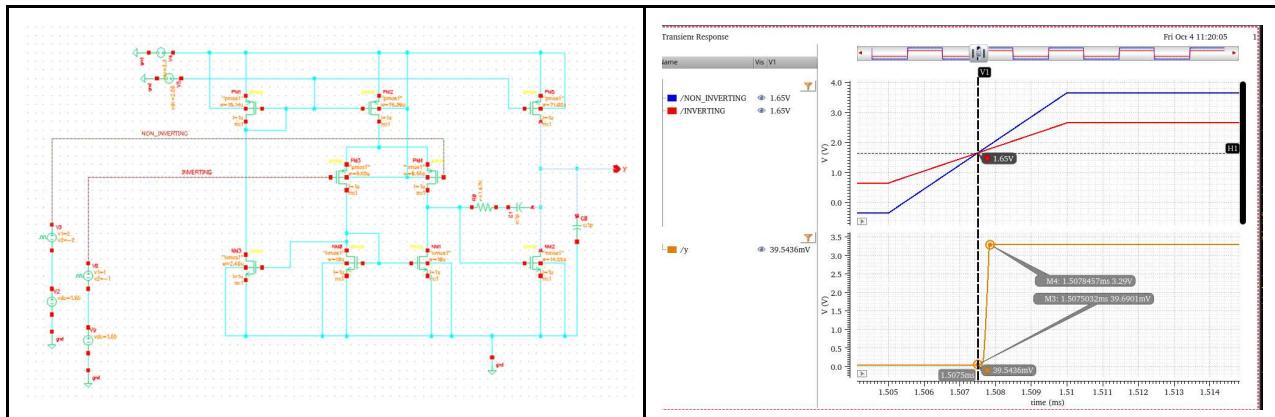
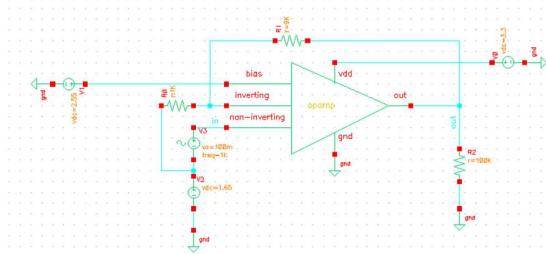
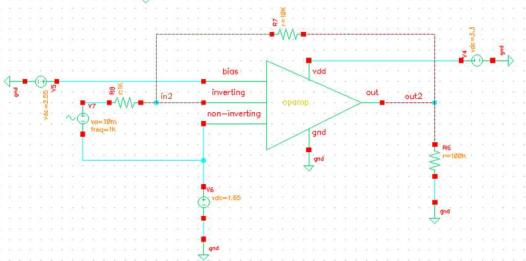


Fig 6.13

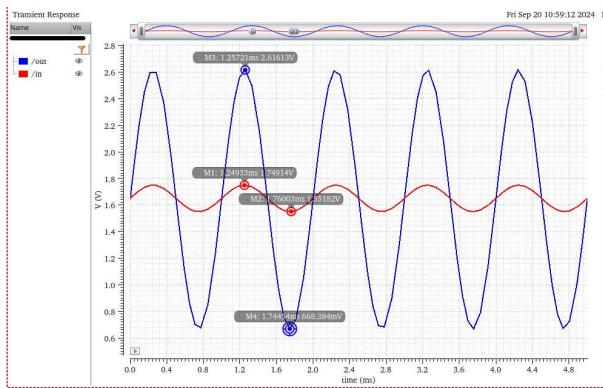
non inverting amplifier



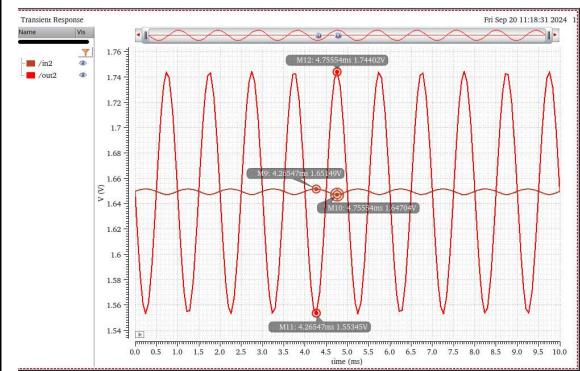
inverting amplifier



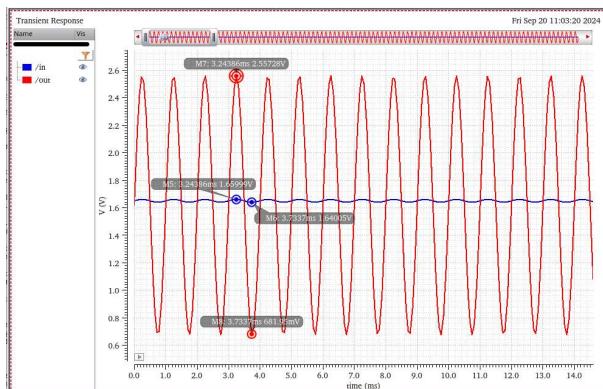
gain 10 output



gain 10 output



gain 100 output



gain 100 output

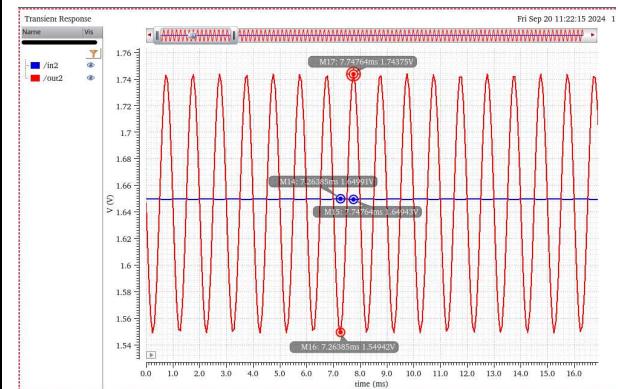


Fig 6.14

comparator calculations

$$\begin{aligned}\text{conversion time} &= 1.5078457 \text{ ms} - 1.5075032 \text{ ms} \\ &= 0.0003425 \text{ ms} \\ &= 342.5 \text{ ns}\end{aligned}$$

OPAMP calculations

output voltage swing = 64.5322 mV to 3.14447 V
input voltage swing = 100 mV to 3.2 mV

$$\begin{aligned}\text{conversion time} &= 3.000056159 \text{ ms} - 3 \text{ ms} \\ &= 0.000056159 \text{ ms} \\ &= 56 \text{ ns}\end{aligned}$$

open loop gain = 73.8 dB

Gain BW Product = 33 MHz

Phase margin = 180 - 94 degree
= 86 > 60 degree

$$\begin{aligned}\text{closed loop Gain} &= [2.65241 - 0.650263] / [2.64991 - 0.650222] \\ &= 2.002147 / 1.999688 \\ &= 1.00122\end{aligned}$$

R-2R DAC calculations

for 00001111 input
expected output = $15 * (3.3) / 256$
= 0.1933 V
= 193.3 mV
actual output = 194.868 mV

conversion time = 56.159 ns

CHAPTER 7

CONCLUSION &

FUTURE SCOPE

CHAPTER 7 CONCLUSION & FUTURE SCOPE

Summary of Work

The project involved the design and implementation of a data acquisition system utilizing key components: a Sample and Hold (SHA) circuit, a Comparator, a Successive Approximation Register (SAR) ADC, and a Digital to Analog Converter (DAC). Each component plays a crucial role in converting an analog signal into a digital format and vice versa, enabling effective signal processing.

Conclusions

1. Sample and Hold Circuit: The SHA circuit successfully captures and maintains the input analog signal, demonstrating reliable performance in sampling and holding operations. This component ensures that the signal remains stable during the conversion process.
2. Comparator Functionality: The comparator effectively distinguishes between the SHA output and the reference voltage. Its accurate logic level output allows for precise decision-making in the ADC process, confirming its essential role in ensuring signal integrity.
3. Successive Approximation Register (SAR): The SAR ADC efficiently determines the digital representation of the analog input. The iterative process employed results in a high-resolution output, demonstrating the SAR's effectiveness in fast and accurate analog-to-digital conversion.
4. Digital to Analog Converter (DAC): The R-2R DAC performed well in converting digital signals back to analog form. The binary-weighted resistor network provided precise voltage levels, facilitating accurate comparisons with the analog input signal.

Future Scope

Implementation of Layout Design: The next phase will involve the detailed layout design of the entire system, which is crucial for achieving optimal performance and manufacturability. This will include precise placement of components, routing of interconnections, and consideration of signal integrity to minimize noise and ensure efficient operation. steps involved in layout are as follows -

1. Design Import: This is the first step of layout. In this step we generate the layout of all components from our schematic design. These are called standard cells. These standard cells are later on joined by routing, depending on their connections in the circuit diagram. Along with standard cells even I/O pins also get generated.
2. IO Planning: It Identifies the input and output requirements of design, including signal types (analog, digital, high-speed), voltage levels, and signal integrity considerations. It forms a group of I/O pins based on their functions and connectivity requirements. It determines the location of connectors, headers, and other external interfaces on PCB layout. It ensures proper signal routing and signal integrity by minimizing signal reflections, crosstalk, and impedance mismatches.
3. Floor Planning: Floor Planning involves determining the location, shape, and size of modules in a way that one can avoid congestion. Floorplanning provides early feedback that evaluates architectural decisions, estimates chip areas, and estimates delay and congestion caused by wiring. In addition to chip area minimization, modern

VLSI floorplanning also needs to handle some important issues such as soft modules and fixed-outline constraints. Unlike a hard module that has a fixed dimension (width and height), the shape of a soft module is to be decided during floorplanning, although its area is fixed.

4. Power Planning: Power planning ensures proper power distribution across the chip, minimizing voltage drop and noise. It involves strategically placing power supplies, power stripes, and decoupling capacitors to ensure stable power delivery. The levels of power distribution are: Power Pads→Power Rings→Power Stripes→Power Rails→Standard Cells Power rings provide clean and stable power to sensitive or high-performance circuitry, as they help reduce noise and voltage fluctuations. Power stripes ensure that power can be efficiently distributed to all areas of the chip, minimizing voltage drop and power distribution network (PDN) resistance.
5. Placement: Placement is the process of placing the standard cells inside the core boundary in an optimal location. The tool tries to place the standard cell in such a way that the design should have minimal congestions and the best timing. For example 2 standard cells having max number of connections will be placed very close to each other to reduce routing cost. If cells are placed too close to each other there is a possibility of short circuit during routing.
6. Routing: Routing involves creating physical connections (metal traces) between the placed logic cells, power pads, and I/O pads. It aims to minimize wire length, congestion, and parasitic effects while meeting timing and signal integrity requirements. Ensure proper shielding and spacing to reduce noise and signal interference. It includes Defining routing constraints, such as minimum trace width, spacing, and maximum length.
7. Verification: Once all the above steps are completed it's time to check our design. There are 2 important methods - DRC & LVS. DRC (Design Rule Check): Ensures that the physical layout of a chip adheres to the fabrication process's rules. These rules are set by the foundry to ensure the layout can be correctly manufactured. Checks include minimum spacing, width of metal layers, overlaps, and layer density. LVS (Layout Versus Schematic): Verifies that the layout design matches the schematic design in terms of connectivity. It ensures that the netlist extracted from the layout corresponds to the intended circuit functionality defined in the schematic. Detects any errors like missing or extra components, incorrect connections, or wrong transistor types.
8. Export Layout: The final step of chip layout involves exporting the layout design in a standard format like GDSII (Graphic Data System II) or OASIS (Open Artwork System Interchange Standard) to ensure it can be sent to the foundry for fabrication. These formats store geometric shapes, layer information, and other metadata of the design in a compact and standardized way. GDSII: The traditional and widely used format, but it has limitations in terms of file size and efficiency for modern large-scale designs. OASIS: A newer format that is more efficient in terms of file size, especially for designs with many repeated structures. After completing the physical layout (and passing DRC and LVS checks), the design is ready to be handed off to the foundry

CHAPTER 8

REFERENCES

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Research Papers

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